DATA SHEET

t8566(7)
Multi-window graphic On-Screen-Display

Preliminary specification
Video Display Product Series

April 1999

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CONTENTS

1 FEATURE

ϒ Screen Attributes:

- Very wide OSD menu moving range for high resolution chassis: maximum up to **2048 dots**, **2048 scan lines** for horizontal and vertical position respectively; **OSD menu can penetrate the border of the screen**

- **Programmable horizontal and vertical positioning step: 2 dots (2 scan lines), 4 dots (4 scan lines), 6 dots (6 scan lines), 8 dots(8 scan lines) per step respectively.**

- Wipe-In / Wipe-out effect can be optionally enabled with **2 selectable directions (from top left corner to bottom right corner or vice verse)**

- **Programmable wipeing rate: maximum wiping time: 0.5 sec. or 0.25 sec.**

- The **built-in SP code** associated with boxing background color can produce multiple windows and **relieve software load** for creating background color underneath foreground character; up to **16 background color** supported

- **Built-in dynamic transparent effect for background color defined by SP code without the external color blending circuit**

- Up to **6 deticated hardware windows** with window shadow effect

- Programmable window shadow height and width, individully controllable

- **Selectable window shadow color out of 4 colors; each window can select different shadow color**

- 16 color selection, including intensity attribute, for each window

- **The display outside the windows and be masked: the wipe in/out effect from the center can be achieved through this feature**

- Built-in Half Tone effect for each window without the external color blending circuit

- Character basis background color change with 8 color selections; 16 color selections by row basis

- Software flag to clear the screen display

ϒ Multi-sync application supports:

- Wide Horizontal sync range from 15 KHz to **200 KHz**

- An internal PLL which generates pixel clock ranged from 6.25 to 96 MHz

- Programmable character height, not only for scaling up (18 to 66 lines) but also **scaling down (5, 9, 10, 13 lines)**

- Double Character Height and Double Character Width, programmable individually by row based control

- **Hardware Row to Row spacing by row based control**

ϒ Number of Character fonts

- Total 255 character fonts plus one dedicated Space code

- Flexible memory partitioning to allocate desired number of Normal Character Fonts (NCF) and Graphic Character Fonts (GCF); **the number of NCF and GCF can be customized and dependent of the application needs**.

ϒ Display dimension:

- **16 (rows) by 31 (columns)**

- Fixed display format for easy screen arrangement

- **On Screen Display can start from any row**, which will facilitate the arrangement of preloaded multiple menu segments in different Display RAM area and then displayed by the pointer

- **Scrolling effect** can be emulated through this flexible architecture

- The Display RAM and internal registers are readable through SPI or I2C interface so that huge

memory resource can be used as buffer and shared for other purposes

- Character attributes:
  - 12 X 18 dot matrix
  - No clearance between characters; higher resolution character fonts or some special graphic pattern/icon can be designed by combining two, three or more characters
  - **16 color selection**, including intensity attribute, per display **character basis**
  - **16 color selection**, including intensity attribute, for character background, per word basis
  - 8 color selection, for individual character background, **16 color selection per row basis**
  - **Row based character Bordering or Shadowing from 8 programmable directions**
  - Character based blinking function with **2** different rates
- **Proprietary adaptive approach to handle H, V sync collision automatically by internal hardware**
- Industrial standard SPI or I2C interface with default slave address, F4H (SPI, I2C and slave address can be selected by mask option)
- 8 X 8 bits PWM DAC outputs (applicable only for t8567)
- 24 pins (for t8567) or 16 pins PDIP package or 16 pins SO package

2 GENERAL DESCRIPTION

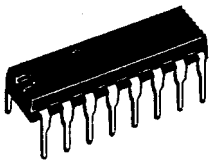
The t8566(7) stand alone OSD is designed to interface with microcontroller to display colored patterns, icons or characters onto display devices like TV, CRT monitor or LCD monitor. Since 256 character fonts (including one space code) are provided internally, it can cover the application of Multi-language TV/Monitor. The Graphic Character Fonts can produce the effect of the pixel based graphic display, which allows the impressive display of the customized pattern. symbols or logos. The large display RAM with fixed columns, rows, will relieve CPU from the overhead of screen refreshing.

The internal PLL system associated with the versatile programmable character height is particularly suitable for multi-scan application. Through those features, the desired aspect ratio can be achieved during mode change.

Meanwhile, t8566(7) also provides plentiful features to enhance the appearance of the displayed character fonts. Each character can have its own colors (up to 16 colors) and blinking option. Up to 10 shadowing modes (including bordering, boxing etc.) are provided together with 16 background colors. Multiple overlapping windows, and wipe-in or wipe-out from two directions can create more flexible user interface. The internal built-in half tone function can create the see-through effect without the intervention of the external circuit.

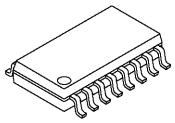
Some handy hardware design tackling some common application issues like the detection and automatic adjustment of Hsync and Vsync collision, the special handling while Hsync or Vsync coming before display finished, can minimizes the efforts of the application supports.

For t8567, 8 X 8 bits PWM DAC are available to provide DC voltage control for other peripherals like R, G, B bias, gain etc.



PDIP16

ORDER INFORMATION
T8566A PLASTIC PACKAGE



SO16

ORDER INFORMATION

T8566B PLASTIC PACKAGE

3 ORDERING INFORMATION

TYPE NO.	PACKAGE			TEMP. (T_A ,C)	FREQ. (MHZ)
	PINS	PKG TYPE	MATE RIAL		
t8566A	16	PDIP	plastic	0 to +70	6.25 to 96
t8566B	16	SOP	plastic	0 to +70	6.25 to 96
t8567	24	PDIP	plastic	0 to +70	6.25 to 96

4 PIN CONFIGURATION

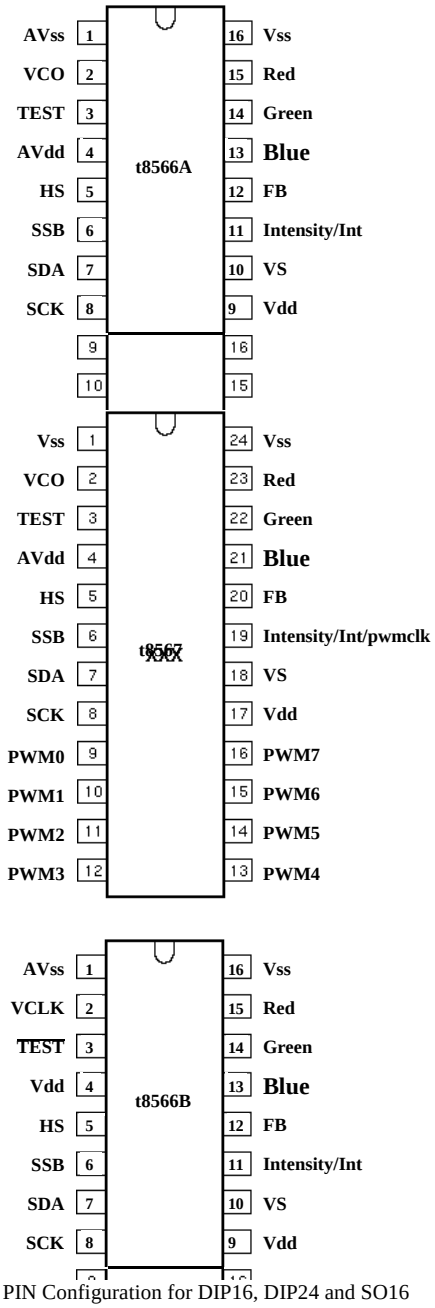


Fig.1 PIN Configuration for DIP16, DIP24 and SO16

5 PIN DESCRIPTION

SYMBOL	I/O	PDIP 16	PDIP 24	SOP 16	DESCRIPTION
AVss/Vss	S	1	1	1	**Analog Vss for t8566A and t8567.** **Digital Vss for t8566B.**
VCO/VCLK	IO/I	2	2	2	**Loop Filter connected to the internal Voltage Controlled Oscillator for t8566A and t8567.** **Driving Clock from the external side for t8566B.**
TEST/$\overline{\text{TEST}}$	I	3	3	3	**TEST pin; Active High for t8566A and t8567, pulled down internally.** **TEST pin; Active Low for t8566B; must be tied to High for normal operation.**
AVdd/Vdd	S	4	4	4	**Analog 5 Volt DC supply for t8566A and t8567.** **Digital 5 Volt DC supply for t8566B**
HS	I	5	5	5	**Horizontal Sync input; TTL level with Schmitt leading edge triggered**
SSB	I	6	6	6	**SPI interface enable pin; Active low, pulled up internally. For I^2C interface, just keep it floating or tied to high.**
SDA	IO	7	7	7	**Serial data input/output pin.**
SCK	IO	8	8	8	**Serial transfer clock pin.**
Vdd	S	9	9	9	**Digital 5 Volt DC supply**.
VS	I	10	10	10	**Vertical Sync input; TTL level with Schmitt leading edge triggered.**
Intensity(Int)/ PWMCLK	O	11	11	11	**Intensity color output; it can be switched as the interrupt pin for the ending of each displayed row or the leading edge of Vertical Sync. It can selected as the output of the PWM clock.**
FB	O	12	12	12	**Fast Blanking Output.**
Blue	O	13	13	13	**Blue color output.**
Green	O	14	14	14	**Green color output.**
Red	O	15	15	15	**Red color output.**
Vss	O	16	16	16	**Digital ground pin.**
PWM0	O	-	17	-	**PWM DAC Output 0**
PWM1	O	-	18	-	**PWM DAC Output 1**
PWM2	O	-	19	-	**PWM DAC Output 2**
PWM3	O	-	20	-	**PWM DAC Output 3**
PWM4	O	-	21	-	**PWM DAC Output 4**
PWM5	O	-	22	-	**PWM DAC Output 5**
PWM6	O	-	23	-	**PWM DAC Output 6**
PWM7	O	-	24	-	**PWM DAC Output 7**

6 BLOCK DIAGRAM

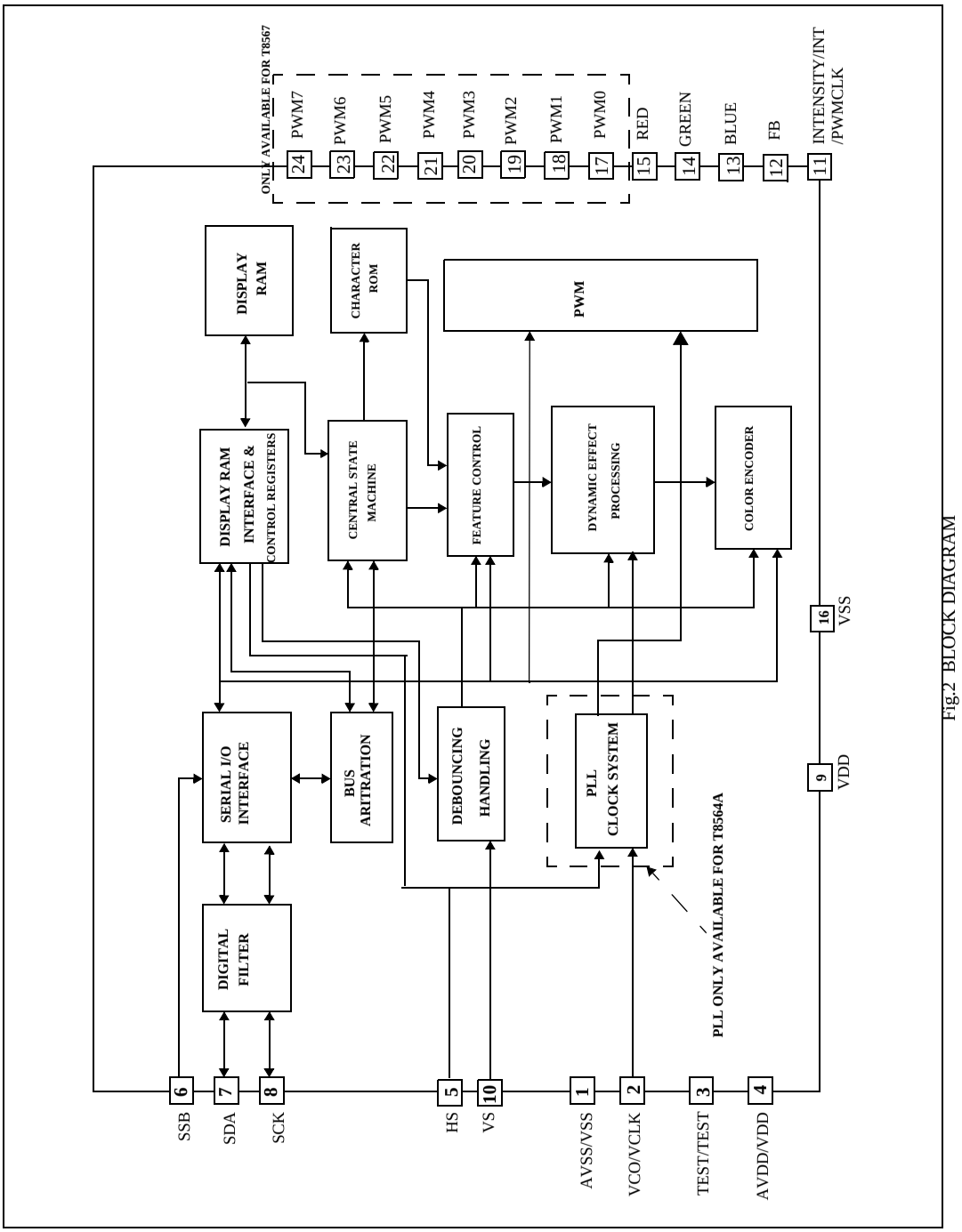


Fig.2 BLOCK DIAGRAM

7 ABSOLUTE MAXIMUM RATINGS

Voltage referenced to Vss

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	–0.3	+7.0	V
V_{in}	all input voltages	–0.3	V_{DD} +0.3	V
P_{tot}	total power dissipation	–	0.7	W
T_{stg}	storage temperature range	–65	+150	′C
T_{amb}	operating ambient temperature range:	0	+70	′C

8 DC CHARACTERISTICS

V_{DD} = 5 V Ÿ10%; V_{SS} = 0 V; AV_{DD} = 5 V Ÿ5%; AV_{SS} = 0 V;T_{amb} = 0 to +70′C. All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
AV_{DD}	Analog supply voltage range	(Applicable only for t8564A)	4.75	5.25	V
I_{DD}	supply current	V_{DD} = 5 V; f_{OSDCLK} = 90 MHz note (1)	TBD	TBD	mA
Inputs					
V_{IL1}	LOW level input voltage (for TEST/$\overline{TEST}$ pin, SSB, SDA, SCK)		–0.5	0.3V_{DD}	V
V_{IH1}	HIGH level input voltage (for TEST/$\overline{TEST}$ pin, SSB, SDA, SCK)		0.7 V_{DD}	V_{DD} +10%	V
V_{IL2}	LOW level input voltage (HS, VS)		–0.5	0.8	V
V_{IH2}	HIGH level input voltage (HS, VS)		2.0	V_{DD} +10%	V
I_{IH}	input current logic 1 (for TEST/$\overline{TEST}$ pin)	V_I = 5 V	TBD	TBD	µA
I_{IL}	input current logic 0 (for SSB pin)	V_I = 0 V	TBD	TBD	µA
I_{LI1}	input leakage current (for SDA, SCK, HS, VS)	0.45 < V_I < V_{DD}	–10	Ÿ10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Outputs					
V_{OL1}	LOW level output voltage (for Red, Green, Blue, Intensity, FB pins and PWM open drain outputs)	I_{OL} = 2 mA;	–	Vss + 0.4	V
V_{OL2}	LOW level output voltage (for SDA, SCK pins)	I_{OL} = 4 mA	–	Vss + 0.4V	V
V_{OH}	HIGH level output voltage (for Red, Green, Blue, Intensity, FB pins)	I_{OH} = 2 mA;	V_{DD} - 0.8	–	V
I_{HZ}	High-Z current (for Red, Green, Blue, Intensity, FB pins)		TBD	TBD	µA

Note

1. The operating supply current is measured with all output pins disconnected;
   a) $V_{IL} = V_{SS}$ +0.5 V;
   b) $V_{IH} = V_{DD}$ –0.5 V;
   c) TEST/$\overline{\text{TEST}}$= SSB = Not connected;
   d) SDA = SCK = Vdd (through 4,7 K ohm pullup resistor)
   e) HS = 48.5 KHz
   f) VS = 60 Hz
   g) VCO is connected to loop filter (C1=22 pf, R1 = 40 K ohm, C2 = 0.1 uF)

9 AC CHARACTERISTICS

V_{DD} = 5 V Ÿ10%; V_{SS} = 0 V; AV_{DD} = 5 V Ÿ5%; AV_{SS} = 0 V;T_{amb} = 0 to +70′C. All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Red, Green, Blue, FB, Intensity (C_{LOAD} = 30 pF)					
t_R	Rise TIme (see note (1))	–	4.7	–	ns
t_F	Fall TIme (see note (1))	–	4.8	–	ns
t_{SKEW}	Skew between those signals	–	5	–	ns
HS					
f_{HS}	Horizontal sync input frequency	15	–	120	KHz
t_R	Rise TIme (see note (1))	–	–	1	ns
t_F	Fall TIme (see note (1))	–	–	1	ns
SPI and I^2C interface: SSB, SDA and SCK (refer to Fig.3 and Fig.4)					
t_{SPISU}	SSB to SCK setup time	200	–	–	ns
t_{SPIH}	SSB to SCK hold time	100	–	–	ns

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{SCK1}	SPI baud rate	–	–	1000	K bps
t_{DATSU}	SDA data setup time	0	–	–	ns
t_{DATH}	SDA data hold time	500	–	–	ns
t_{SCKL1}	SCK Low period for SPI interface	400	–	–	ns
t_{SCKH1}	SCK High period for SPI interface	400	–	–	ns
f_{SCK2}	**I^2C** baud rate	–	–	400	K bps
t_{SUP}	Setup time for Stop condition	500	–	–	ns
t_{HDS}	Hold time for Start condition	500	–	–	ns
t_{SCKL2}	SCK Low period for **I^2C** interface	1000	–	–	ns
t_{SCKH2}	SCK High period for **I^2C** interface	1000	–	–	ns
t_R	Rise time for SDA and SCK	Depend on the pull-up resistor and the capacitive loading			
t_F	Fall time for SDA	–	–	20	ns

Note

1. Those parameters are guaranteed by internal qualification, including design characterization, process split lots analysis and temperature characterization.
2. For the falling edge, the time interval between 90% of (V_{DD} - V_{SS}) and 10% of (V_{DD} - V_{SS}) is defined as t_F. For the rising edge, the time interval between 10% of (V_{DD} - V_{SS}) and 90% of (V_{DD} - V_{SS}) is defined as t_R.

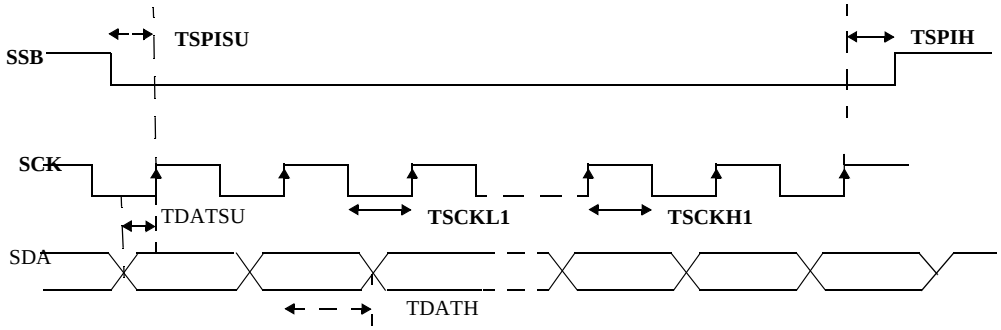


Fig.3 The AC timing definition for SPI interface

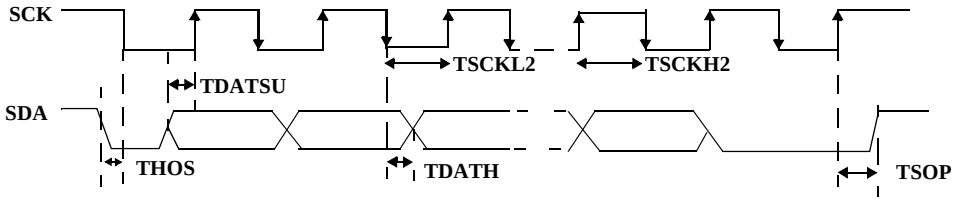


Fig.4 The AC timing definition for I^2C interface