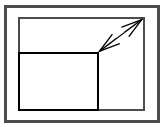
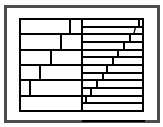
trumpion

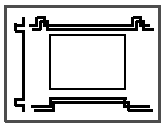
# ZiPRO

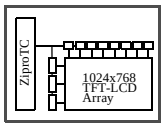
trumpion

# ZiPRO TC


Zoom up/down

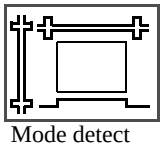

De-interlacing

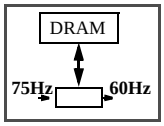

Accurate PHS



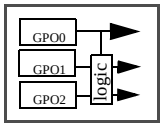
TCON for XGA

Faster adjust

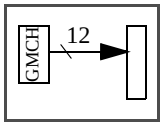

Mode detect



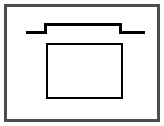
Optional DRAM

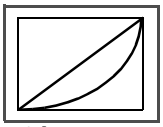


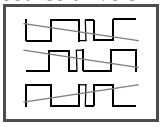
Support all gate/ source drivers

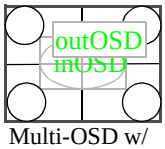


12/24-bit input

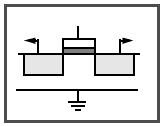

DE only for DVI

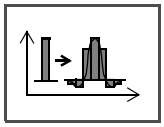

10-bit gamma

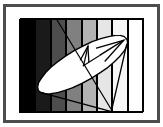

3 separate PWM



Multi-OSD w/ color blending


0.25um CMOS


Improved interpolation


256 steps each Hue/Satuation

**Specification** **May 30, 2001**

T-0944/0946

trumpion
microelectronics, Inc.

**TABLE 1.**

| Version | Date | Author | Description |
|---|---|---|---|
| 0.1 | Jun. 2000 | GC | preliminary release 1 |
| 0.2 | Jul. 2000 | GC | preliminary release 2 |
| 0.5 | Jul.29, 2000 | GC | preliminary release 5 |
| 0.6 | Aug. 31, 2000 | GC | preliminary release 6 |
| 0.7 | Oct. 20, 2000 | GC | 1) preliminary release for the 1st silicon of Zipro |
| 0.8 | Jan. 16, 2001 | GC | 1) preliminary release for the MP developing of Zipro |
| 0.9 | Feb. 13, 2001 | GC | 1) preliminary release for the MP of Zipro/ZiproTC.<br>Venus_D\documentation\t0944_09.fm |
| 0.95 | Feb. 28, 2001 | GC | 1) preliminary release for the MP of Zipro/ZiproTC. |
| 0.98 | Apr. 23,2001 | SY | 1) preliminary release for the MP of Zipro/ZiproTC. |
| 1.0 | May 30,2001 | GC | 1) Release for the MP of Zipro/ZiproTC. |

# 1.0 Introduction

Zipro (Zoom engine for Interlaced to PROgressive scan) or t0944 chip is targeted for XGA color display and ZiproTC (Zipro with Timing Control) or t0946 is designed for smart-panel system of SVGA/XGA TFT-LCD.

Zipro and ZiproTC chips convert PC/Mac and ATSC video signals for flat panel display (e.g. TFT-LCD monitor or Plasma Display Panel.) It performs image scaling on true color RGB or YUV data stream and feeds the scaled pixels to LCD/PDP panel. It includes a SDRAM controller for frame rate conversion and interlace to progessive video processing. Besides, the chip contains an OSD (On Screen Display) logic with an overlay port for external OSD signals interface. An auto adjustment function provides automatic frequency, phase, H&V position, and white balance tuning at any screen condition. With no user intervention, the auto adjustment feature offeres the jitter-free and best display quality while users display modes changed. To meet the market requirements of low cost, low power, and high level of integration, Zipro and ZiproTC also contain display mode auto detection circuitry which provides the best performance/cost solution for flat panel displays.

ZiproTC includes timing control circuit for handling gate and source driver ICs for SVGA/XGA TFT-LCD panel directly. This solution, so called smart-panel system, can save the cost of connectors and cable between interface-board and LCD panel module. It also helps to reduce the EMI issue.

Zipro (t0944) comes with 128 and 160-pin LQFPs while ZiproTC (t0946) is packed in a 160-pin LQFP.

# 2.0 General Features

- Embedded DRAM controller for interlaced to progressive video processing and frame-rate conversion for computer graphics.
- On chip programmable OSD for LCD/PDP user interface.
- Embedded hardware for display mode detection.
- Auto adjustment for frequency, phase, H/V position, and white balance.
- On chip hue, saturation, brightness, contrast, and gamma correction.
- Max pixel rate up to 108 MHz.
- Embedded timing control circuit for source/gate drivers of SVGA/XGA TFT-LCD panel.
- Three PWMs (Pulse Width Modulators) for general purpose control.
- Noise reduction by sin(x)/x filter.
- 0.25 um CMOS technology with 5V tolerance input pads.

## 2.1 Input for Zipro series (except ZiproSO)

- 12-bit GMCH interface with level-shifters.
- 24-bit RGB input up to 108MHz.
- 8-bit YUV 4:2:2 (CCIR 656), 16-bit YUV 4:2:2, and 24-bit YUV 4:4:4 video input. Glueless connection to video sources from ADC, MPEGII decoder or video decoder.
- Build-in YUV to RGB color space converter.
- 5V tolerance input pads support 5V/3.3V interface.

## 2.2 Scaler, and de-interlacer

- Auto cinema mode detection.
- Scaling up and down with filters for different sharpness.

## 2.3 Gamma correction and OSD

- 10-bit Gamma table.
- Downloadable 64-font RAM for user programmable and graphics fonts.
- Overlay port interface and color look-up table with 4 color indices (for anti-aliasing font and palette) from external OSD.
- Support the pixel-based pattern filling with a graphic port.

## 2.4 Output

- Single pixel/clock (24 bit) or double pixels/clock (48 bit) digital RGB output.
- Maximum resolution color display is 1280*1024 (SXGA).
- Single and dual pixel/clock for R/G/B or Y/Pb/Pr digital output.
- Free-run synchronization mode if sync signal disappeared.
- Compliant with proposed VESA FPDI-2 standard via direct connect to LVDS transceivers.

## 2.5 System software and support

- Windows based OSD font and GUI design software.
- HDTV display and LCD multi-sync monitor system software.
- Scaler programming timing table for all VESA/MAC/Workstation and ATSC to all size of LCD/PDP.

## 2.6 Applications

- High resolution TFT-LCD or smart panel LCD monitors.
- Set-top box and DVD player to LCD/PDP display devices.
- NTSC/PAL projection systems for office presentation and home theater.
- Line doubler for DVD player.
- LCOS or OLED displays for HMD applications.
- Image scaling for video format conversions.

**FIGURE 1. Typical application of Zipro/ZiproTC chip**

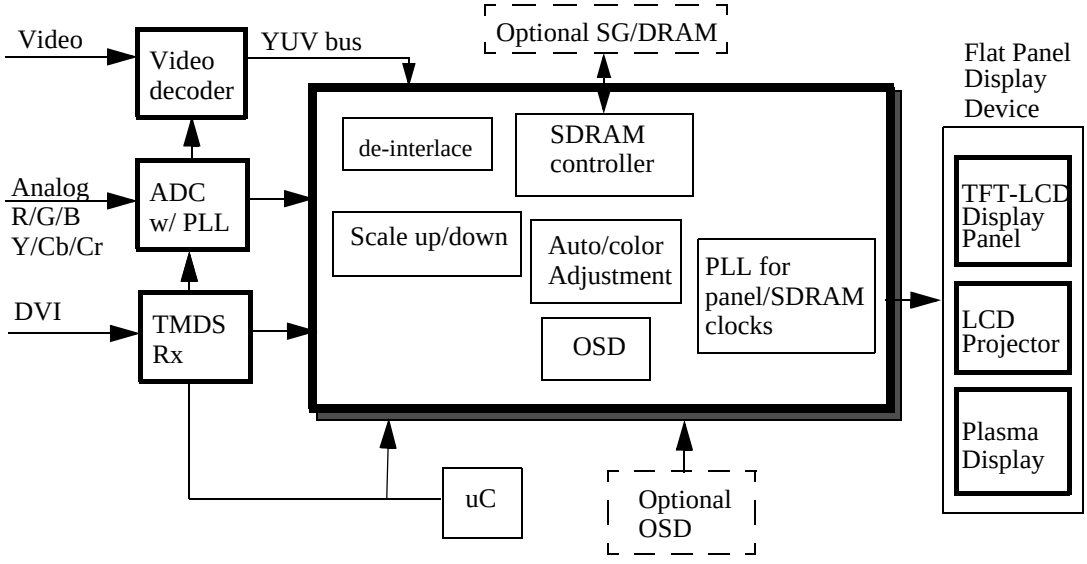
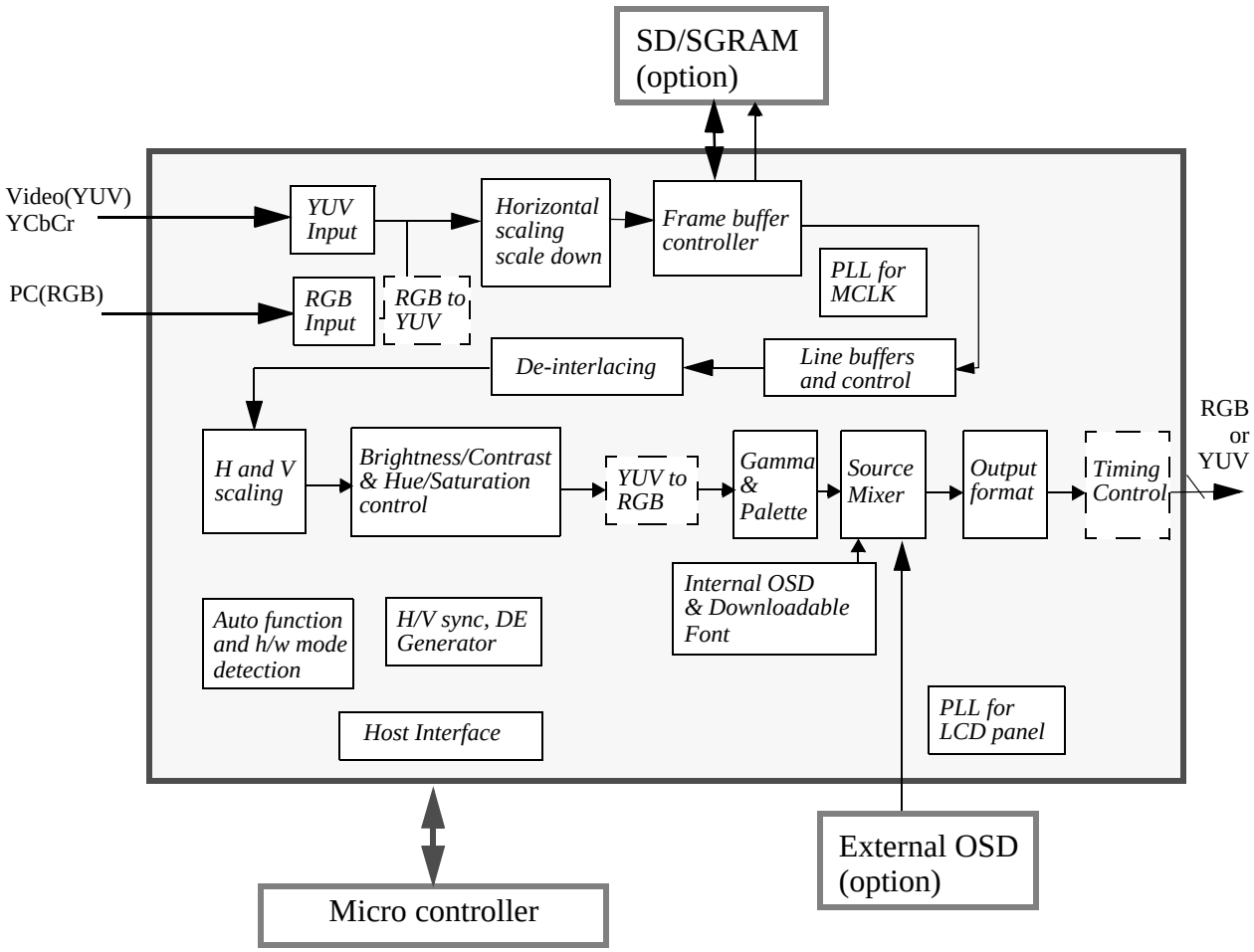


**FIGURE 2. Block diagram of Zipro chips**



## 2.7 Pinning of Zipro 160 pins

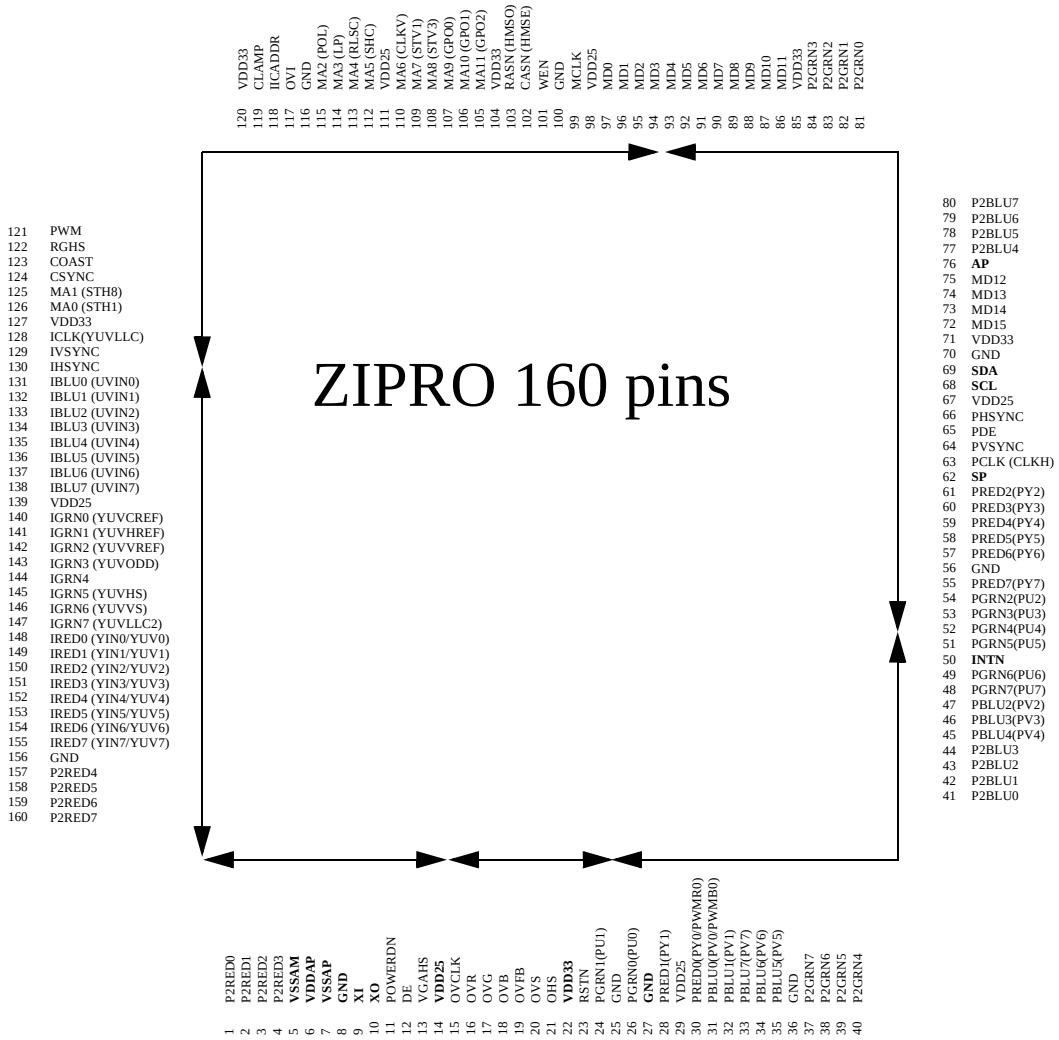



**TABLE 1. Input Ports (RGB and YUV Data, 34 pins)**

| Pin # | I/O (drive) | Name | Description |
|---|---|---|---|
| 128 | I | ICLK(YUVLLC) | Clock for A port input (single/double pixel per clock). |
| 129 | I | IVSYNC | Vertical Sync of video A port. |
| 130 | I | IHSYNC | Horizontal Sync of video A port |
| 155-148 | I | IRED[7:0] /YIN[7:0]/YUV[7:0]/RGB12[11:4] | Red input data of video A port. The pin numbers are listed from MSB to LSB. The RGB12bit uses this port and the MSB 4 bits of IGRN port. |

| Pin # | I/O (drive) | Name | Description |
|---|---|---|---|
| 147-140 | I | IGRN[7:0]/RGB12[3:0] | Green input data of video A port.<br>bit 7: YUVLLC2<br>bit 6: YUVVS<br>bit 5: YUVHS<br>bit 3: YUVODD (ODD or EVEN field)<br>bit 2: YUVVREF<br>bit 1: YUVHREF<br>bit 0: YUVCREF |
| 138-131 | I | IBLU[7:0]/UV[7:0] | Blue input data of video A port. |
| 123 | O | COAST | COAST signal to ADC (regenerated VS). |
| 122 | O | RGHS | Regenerated HS |
| 13 | I | VGAHS | VGA input HS |
| 12 | I | DE | Display enable signal from digital flat panel interface<br>This signal should be tied to high if DE function is not used |
| 124 | I | CSYNC | Composite sync signal that includes HS and VS |
| 119 | O | CLAMP | Clamp pulse to ADC. This pin can also be programmed to output FID, Cinema mode, or PWMR0. |
| 121 | O | PWM | Pulse width modulation output (NOTE: pin 23 is the VDD3 in Zurac) |

**TABLE 2. Panel interface (or Display Port) (RGB Data, 54 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 63 | O | PCLK (or PHCLK) | Display port A clock for panel (This clock is generated from internal PLL) |
| 65 | O | PDE | Display enable (active area of display) |
| 64 | O | PVSYNC | Display Vertical Sync |
| 66 | O | PHSYNC | Display Horizontal Sync |
| 55,57-61,28,30 | O | PRED[7:0] /PY[7:0]/ODRED[7:0] | Display A port or Odd port of red data. The pin numbers are listed from MSB to LSB |
| 48-49,51-54,24 ,26 | O | PGRN[7:0] /PU[7:0]/ODGRN[7:0] | Display A port or Odd port of green data. |
| 33-35,45-47,32 -31 | O | PBLU[7:0] /PV[7:0]/ODBLU[7:0] | Display A port or Odd port of blue data |
| 160-157,4-1 | O | P2RED[7:0]/EVRED[7:0] | Display B port or Even port for red data. |
| 37-40,84-81 | O | P2GRN[7:0]/EVGRN[7:0] | Display B port or Even port green data |
| 80-77,44-41 | O | P2BLU[7:0]/EVBLU[7:0] | Display B port or Even port blue data |
| **10** | O | XO | Reference frequency output for internal oscillator |
| **9** | I | XI | Reference frequency input for internal oscillator (should be connected to a 14.31818MHz crystal) |

**TABLE 3. Host Interface Signals (6 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 118 | I | IICADDR | Serial I/F sub-address setting. |
| **50** | O | INTN | Interrupt to host (active low) |
| 23 | I | RSTN | Device reset (active low) |
| **69** | I/O | SDA | Serial I/F data in/out |
| **68** | I | SCL | Serial I/F clock |
| 11 | I | POWERDN | Power Down, 0: normal, 1:Powerdown |

**TABLE 4. Memory Control Port (Frame buffer) (32 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 99 | O | MCLK | Memory clock output |
| 101 | I | WEN | Memory write enable |
| 102 | I | CASN | Memory column address strobe |
| 103 | I | RASN | Memory row address strobe |
| 72-75,86-97 | I | MD[15:0] | Memory data bus |
| 105-110,112-115,125,126 | I | MA[11:0] | Memory address bus |

**TABLE 5. Overlay Port (External OSD) (8 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 15 | O | OVCLK | Clock for external overlay circuit. |
| 16 | I | OVR | Overlay color select R |
| 17 | I | OVG | Overlay color select G |
| 18 | I | OVB | Overlay color select B |
| 117 | I | OVI | Overlay intensity select |
| 19 | I | OVFB | Overlay color enable |
| 20 | O | OVS | Overlay V sync signal |
| 21 | O | OHS | Overlay H sync signal |

**TABLE 6. Testing (2 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| **76** | I | AP | Action pin for testing (should be grounded) |
| **62** | I | SP | Shift pin for testing (should be grounded) |

FIGURE 3. Timing Control (48+18 shared pins)

| Pin # | I/O | Dr (mA) | Pin name of t0944 (Zipro) | Pin name of t0946 (ZiproTC) | Description |
|---|---|---|---|---|---|
| - | O | 4 | PRED[7:0], PGRN[7:0], PBLU[7:0] | ODRED[7:0], ODGRN[7:0], ODBLU[7:0] | Odd RGB pixel data (24 pins)<br>Note: The 1st pixel is at the ODD bus in ZiproTC. |
| - | O | 4 | P2RED[7:0], P2GRN[7:0], P2BLU[7:0] | EVRED[7:0], EVGRN[7:0], EVBLU[7:0] | Even RGB pixel data (24 pins)<br>Note: The 2nd pixel is at the EVEN bus in ZiproTC. |
| 63 | O | 16 | PCLK | CLKH | Clock for source driver IC |
| 126 | O | 4 | MA0 | STH1 | Start pulse for source driver IC (S1 to S8) |
| 125 | O | 4 | MA1 | STH8 | Start pulse for source driver IC (S8 to S1) |
| 115 | O | 4 | MA2 | POL | Polarity for source driver IC |
| 114 | O | 4 | MA3 | LP | Latch pulse for source driver IC |
| 103 | O | 4 | RASN | HMSO | Data inversion control for odd pixel bus<br>(if more than half signals in the bus change state, this signal wll be set.) |
| 102 | O | 4 | CASN | HMSE | Data inversion control for even pixel bus |
| 113 | O | 4 | MA4 | RLSC | R/L indication for source driver IC |
| 112 | O | 4 | MA5 | SHC | decode control for TI driver IC |
| 110 | O | 4 | MA6 | CLKV | Clock for gate driver IC |
| 109 | O | 4 | MA7 | STV1 | Start pulse for gate driver IC (G1 to G3) |
| 108 | O | 4 | MA8 | STV3 | Start pulse for gate driver IC (G3 to G1) |
| 107 | O | 4 | MA9 | GPO0 | Programmable general purpose output 0 |
| 106 | O | 4 | MA10 | GPO1 | Programmable general purpose output 1 |
| 105 | O | 4 | MA11 | GPO2 | Programmable general purpose output 2 |
| 66 | O | 4 | PHS | PHS | Panel H sync output signal |
| 64 | O | 4 | PVS | PVS | Panel V sync output signal |
| 65 | O | 4 | PDE | PDE | Panel display enable output signal |

**TABLE 7. Power and Ground Signals (24 pins include 14 VDD and 10 GND pins)**

| Pin # | V | Name | Description |
|---|---|---|---|
| **14**,29,67,98,111,139 | 2.5 | VDD25 | Digital power supply (for core cells) |
| **22**,71,85,104,120,127 | 3.3 | VDD33 | Digital power supply (for I/O cells) |
| **8**,25,**27**,36,56,70,100,116,156 | 0 | GND | Ground |
| **5** | 0 | VSSAM | Ground pin for MCLK PLL |
| **6** | 2.5 | VDDAP | Power pin for PCLK and MCLK PLL |
| **7** | 0 | VSSAP | Ground pin for PCLK PLL |
| | | | |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 1 | P2RED0 **(EVRED0)** | 41 | P2BLU0 **(EVBLU0)** |
| 2 | P2RED1 **(EVRED1)** | 42 | P2BLU1 **(EVBLU1)** |
| 3 | P2RED2 **(EVRED2)** | 43 | P2BLU2 **(EVBLU2)** |
| 4 | P2RED3 **(EVRED3)** | 44 | P2BLU3 **(EVBLU3)** |
| 5 | **VSSAM** | 45 | PBLU4(PV4) **(ODBLU4)** |
| 6 | **VDDAP** | 46 | PBLU3(PV3) **(ODBLU3)** |
| 7 | **VSSAP** | 47 | PBLU2(PV2) **(ODBLU2)** |
| 8 | **GND** | 48 | PGRN1(PU1) **(ODGRN1)** |
| 9 | **XI** | 49 | PGRN0(PU0) **(ODGRN0)** |
| 10 | **XO** | 50 | **INTN** |
| 11 | POWERDN | 51 | PGRN5(PU5) **(ODGRN5)** |
| 12 | DE | 52 | PGRN4(PU4) **(ODGRN4)** |
| 13 | VGAHS | 53 | PGRN3(PU3) **(ODGRN3)** |
| 14 | **VDD25** | 54 | PGRN2(PU2) **(ODGRN2)** |
| 15 | OVCLK | 55 | PRED7(PY7) **(ODRED7)** |
| 16 | OVR | 56 | GND |
| 17 | OVG | 57 | PRED6(PY6) **(ODRED6)** |
| 18 | OVB | 58 | PRED5(PY5) **(ODRED5)** |
| 19 | OVFB | 59 | PRED4(PY4) **(ODRED4)** |
| 20 | OVS | 60 | PRED3(PY3) **(ODRED3)** |
| 21 | OHS | 61 | PRED2(PY2) **(ODRED2)** |
| 22 | **VDD33** | 62 | **SP** |
| 23 | RSTN | 63 | PCLK **(CLKH)** |
| 24 | PGRN1 **(PU1/ODGRN1)** | 64 | PVSYNC **(PVS)** |
| 25 | GND | 65 | PDE **(PDE)** |
| 26 | PGRN0 **(PU0/ODGRN0)** | 66 | PHSYNC **(PHS)** |
| 27 | **GND** | 67 | VDD25 |
| 28 | PRED1 **(PY1/ODRED1)** | 68 | **SCL** |
| 29 | VDD25 | 69 | **SDA** |
| 30 | PRED0(PY0/PWMR0) **(ODRED0)** | 70 | GND |
| 31 | PBLU0(PV0/PWMB0) **(ODBLU0)** | 71 | VDD33 |
| 32 | PBLU1 **(PV1/ODBLU1)** | 72 | MD15 |
| 33 | PBLU7(PV7) **(ODBLU7)** | 73 | MD14 |
| 34 | PBLU6(PV6) **(ODBLU6)** | 74 | MD13 |
| 35 | PBLU5(PV5) **(ODBLU5)** | 75 | MD12 |
| 36 | GND | 76 | **AP** |
| 37 | P2GRN7 **(EVGRN7)** | 77 | P2BLU4 **(EVBLU4)** |
| 38 | P2GEN6 | 78 | P2BLU5 **(EVBLU5)** |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 39 | P2GRN5 **(EVGRN5)** | 79 | P2BLU6 **(EVBLU6** |
| 40 | P2GEN4 | 80 | P2BLU7 **(EVBLU7)** |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 81 | P2GRN0 **(EVGRN0)** | 121 | PWM |
| 82 | P2GRN1 **(EVGRN1)** | 122 | RGHS |
| 83 | P2GRN2 **(EVGRN2)** | 123 | COAST |
| 84 | P2GRN3 **(EVGRN3)** | 124 | CSYNC |
| 85 | VDD33 | 125 | MA1 **(STH8)** |
| 86 | MD11 | 126 | MA0 **(STH1)** |
| 87 | MD10 | 127 | VDD33 |
| 88 | MD9 | 128 | ICLK(YUVLLC) |
| 89 | MD8 | 129 | IVSYNC |
| 90 | MD7 | 130 | IHSYNC |
| 91 | MD6 | 131 | IBLU0(UVIN0) |
| 92 | MD5 | 132 | IBLU1(UVIN1) |
| 93 | MD4 | 133 | IBLU2(UVIN2) |
| 94 | MD3 | 134 | IBLU3(UVIN3) |
| 95 | MD2 | 135 | IBLU4(UVIN4) |
| 96 | MD1 | 136 | IBLU5(UVIN5) |
| 97 | MD0 | 137 | IBLU6(UVIN6) |
| 98 | VDD25 | 138 | IBLU7(UVIN7) |
| 99 | MCLK | 139 | VDD25 |
| 100 | GND | 140 | IGRN0(YUVCREF) |
| 101 | WEN | 141 | IGRN1(YUVVREF) |
| 102 | CASN **(HMSE)** | 142 | IGRN2(YUVVREF) |
| 103 | RASN **(HMSO)** | 143 | IGRN3(YUVODD) |
| 104 | VDD33 | 144 | IGRN4 |
| 105 | MA11 **(GPO2)** | 145 | IGRN5(YUVHS) |
| 106 | MA10 **(GPO1)** | 146 | IGRN6(YUVVS) |
| 107 | MA9 **(GPO0)** | 147 | IGRN7(YUVLLC2) |
| 108 | MA8 **(STV3)** | 148 | IRED0(YIN0/YUV0) |
| 109 | MA7 **(STV1)** | 149 | IRED1(YIN1/YUV1) |
| 110 | MA6 **(CLKV)** | 150 | IRED2(YIN2/YUV2) |
| 111 | VDD25 | 151 | IRED3(YIN3/YUV3) |
| 112 | MA5 **(SHC)** | 152 | IRED4(YIN4/YUV4) |
| 113 | MA4 **(RLSC)** | 153 | IRED5(YIN5/YUV5) |
| 114 | MA3 **(LP)** | 154 | IRED6(YIN6/YUV6) |
| 115 | MA2 **(POL)** | 155 | IRED7(YIN7/YUV7) |
| 116 | GND | 156 | GND |
| 117 | OVI | 157 | P2RED4 |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 118 | IICADDR | 158 | P2RED5 |
| 119 | CLAMP | 159 | P2RED6 |
| 120 | VDD33 | 160 | P2RED7 |

## 2.8 Pinning of Zipro 128 pins

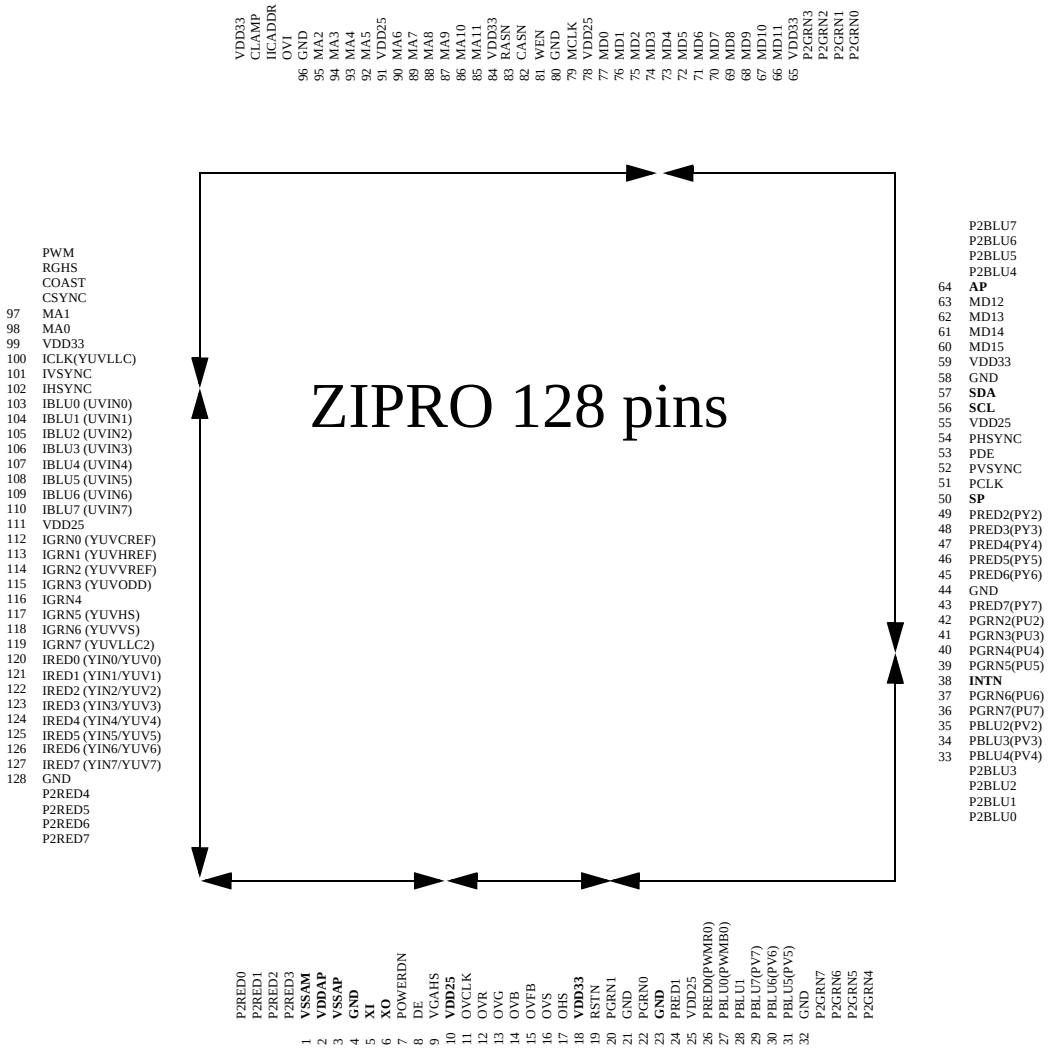


**TABLE 8. Input Ports (RGB and YUV Data, 34 pins)**

| Pin # | I/O (drive) | Name | Description |
|---|---|---|---|
| 100 | I | ICLK(YUVLLC) | Clock for A port input (single/double pixel per clock). |
| 101 | I | IVSYNC | Vertical Sync of video A port. |
| 102 | I | IHSYNC | Horizontal Sync of video A port |
| 127-120 | I | IRED[7:0] /YIN[7:]/YUV[7:0]/RGB12[11:4] | Red input data of video A port. The pin numbers are listed from MSB to LSB. The RGB12bit uses this port and the MSB 4 bits of IGRN port. |
| 119-112 | I | IGRN[7:0]/RGB12[3:0] | Green input data of video A port.<br>bit 7: YUVLLC2<br>bit 6: YUVVS<br>bit 5: YUVHS<br>bit 3: YUVODD (ODD or EVEN field)<br>bit 2: YUVVREF<br>bit 1: YUVHREF<br>bit 0: YUVCREF |
| 110-103 | I | IBLU[7:0]/UV[7:0] | Blue input data of video A port |
| 9 | I | VGAHS | VGA input HS |
| 8 | I | DE | Display enable signal from digital flat panel interface<br>This signal should be tied to high if DE function is not used |

**TABLE 9. Panel interface (or Display Port) (RGB Data, 54 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 51 | O | PCLK | Display port A clock for panel (capability is 8 mA) (This clock is generated from internal PLL) |
| 53 | O | PDE | Display enable (active area of display) |
| 52 | O | PVSYNC | Display Vertical Sync |
| 54 | O | PHSYNC | Display Horizontal Sync |
| 43,45-49,24,26 | O | PRED[7:0] /PY[7:0] | Display A port red data. |
| 36-37,39-42,20,22 | O | PGRN[7:0]/PU[7:0] | Display A port green data. The pin numbers are listed from MSB to LSB |
| 29-31,33-35,28-27 | O | PBLU[7:0]/PV[7:0] | Display A port blue data |
| **6** | O | XO | Reference frequency output for internal oscillator |
| **5** | I | XI | Reference frequency input for internal oscillator (should be connected to a 14.31818MHz crystal) |

**TABLE 10. Host Interface Signals (6 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| **38** | O | INTN | Interrupt to host (active low) |
| 19 | I | RSTN | Device reset (active low) |
| **57** | I/O | SDA | Serial I/F data in/out |
| **56** | I | SCL | Serial I/F clock |
| 7 | I | POWERDN | Power Down, 0: normal, 1:Powerdown |

**TABLE 11. Memory Control Port (Frame buffer) (32 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 79 | O | MCLK | Memory clock output |
| 81 | I | WEN | Memory write enable |
| 82 | I | CASN | Memory column address strobe |
| 83 | I | RASN | Memory row address strobe |
| 60-63,66-77 | I | MD[15:0] | Memory data bus |
| 85-90,92-95,97-98 | I | MA[11:0] | Memory address bus |

**TABLE 12. Overlay Port (External OSD) (8 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 11 | O | OVCLK | Clock for external overlay circuit. |
| 12 | I | OVR | Overlay color select R |
| 13 | I | OVG | Overlay color select G |
| 14 | I | OVB | Overlay color select B |
| 15 | I | OVFB | Overlay color enable |
| 16 | O | OVS | Overlay V sync signal |
| 17 | O | OHS | Overlay H sync signal |

**TABLE 13. Testing (2 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| **64** | I | AP | Action pin for testing (should be grounded) |
| **50** | I | SP | Shift pin for testing (should be grounded) |

**TABLE 14. Power and Ground Signals (23 pins include 13 VDD and 10 GND pins)**

| Pin # | V | Name | Description |
|---|---|---|---|
| **10**,25,55,78,91,111 | 2.5 | VDD25 | Digital power supply (for core cells) |
| **18**,59,65,84,99 | 3.3 | VDD33 | Digital power supply (for I/O cells) |
| **4**,21,**23**,32,44,58,80,96,128 | 0 | GND | Ground |
| **1** | 0 | VSSAM | Ground pin for MCLK PLL |
| **2** | 2.5 | VDDAP | Power pin for PCLK and MCLK PLL |
| **3** | 0 | VSSAP | Ground pin for PCLK PLL |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 1 | **VSSAM** | 33 | PBLU4(PV4) |
| 2 | **VDDAP** | 34 | PBLU3(PV3) |
| 3 | **VSSAP** | 35 | PBLU2(PV2) |
| 4 | **GND** | 36 | PGRN7(PU7) |
| 5 | **XI** | 37 | PGRN6(PU6) |
| 6 | **XO** | 38 | **INTN** |
| 7 | POWERDN | 39 | PGRN5(PU5) |
| 8 | DE | 40 | PGRN4(PU4) |
| 9 | VGAHS | 41 | PGRN3(PU3) |
| 10 | **VDD25** | 42 | PGRN2(PU2) |
| 11 | OVCLK | 43 | PRED7(PY7) |
| 12 | OVR | 44 | GND |
| 13 | OVG | 45 | PRED6(PY6) |
| 14 | OVB | 46 | PRED5(PY5) |
| 15 | OVFB | 47 | PRED4(PY4) |
| 16 | OVS | 48 | PRED3(PY3) |
| 17 | OHS | 49 | PRED2(PY2) |
| 18 | **VDD33** | 50 | **SP** |
| 19 | RSTN | 51 | PCLK |
| 20 | PGRN1 | 52 | PVSYNC |
| 21 | GND | 53 | PDE |
| 22 | PGRN0 | 54 | PHSYNC |
| 23 | **GDN** | 55 | VDD25 |
| 24 | PRED1 | 56 | **SCL** |
| 25 | VDD25 | 57 | **SDA** |
| 26 | PRED0(PWMR0) | 58 | GND |
| 27 | PBLU0(PWMB0) | 59 | VDD33 |
| 28 | PBLU1 | 60 | MD15 |
| 29 | PBLU7(PV7) | 61 | MD14 |
| 30 | PBLU6(PV6) | 62 | MD13 |
| 31 | PBLU5(PV5) | 63 | MD12 |
| 32 | GND | 64 | **AP** |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 65 | VDD33 | 97 | MA1 |
| 66 | MD11 | 98 | MA0 |
| 67 | MD10 | 99 | VDD33 |
| 68 | MD9 | 100 | ICLK |
| 69 | MD8 | 101 | IVSYNC |
| 70 | MD7 | 102 | IHSYNC |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 71 | MD6 | 103 | IBLU0(UVIN0) |
| 72 | MD5 | 104 | IBLU1(UVIN1) |
| 73 | MD4 | 105 | IBLU2(UVIN2) |
| 74 | MD3 | 106 | IBLU3(UVIN3) |
| 75 | MD2 | 107 | IBLU4(UVIN4) |
| 76 | MD1 | 108 | IBLU5(UVIN5) |
| 77 | MD0 | 109 | IBLU6(UVIN6) |
| 78 | VDD25 | 110 | IBLU7(UVIN7) |
| 79 | MCLK | 111 | VDD25 |
| 80 | GND | 112 | IGRN0(YUVCREF) |
| 81 | WEN | 113 | IGRN1(YUVVREF) |
| 82 | CASN | 114 | IGRN2(YUVVREF) |
| 83 | RASN | 115 | IGRN3(YUVODD) |
| 84 | VDD33 | 116 | IGRN4 |
| 85 | MA11 | 117 | IGRN5(YUVHS) |
| 86 | MA10 | 118 | IGRN6(YUVVS) |
| 87 | MA9 | 119 | IGRN7(YUVLLC2) |
| 88 | MA8 | 120 | IRED0(YIN0/YUV0) |
| 89 | MA7 | 121 | IRED1(YIN1/YUV1) |
| 90 | MA6 | 122 | IRED2(YIN2/YUV2) |
| 91 | VDD25 | 123 | IRED3(YIN3/YUV3) |
| 92 | MA5 | 124 | IRED4(YIN4/YUV4) |
| 93 | MA4 | 125 | IRED5(YIN5/YUV5) |
| 94 | MA3 | 126 | IRED6(YIN6/YUV6) |
| 95 | MA2 | 127 | IRED7(YIN7/YUV7) |
| 96 | GND | 128 | GND |

# 3.0 CHARACTERISTICS

## 3.1 Recommended Operating Conditions

| Item | Value |
|---|---|
| Operating voltage | 2.5V and 3.3V plus/minus 10% |
| Operating chassis temperature | $0^oC$ to $80^oC$ |
| Total power dissipation | Max. 0.64 W (XGA LCD panel @ 85Hz) |

## 3.2 DC CHARACTERISTICS

VDD3 = 3.0 to 3.6V; VDD2 = 2.25 to 2.75V; VDDAP = 2.4 to 2.6V; $T_{amb}$= 25 C; unless otherwise specified.

| SYMBOL | PARAMETER | Remark | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Powers | | | | | | |
| VDD3 | I/O digital supply voltage | | 3.0 | 3.3 | 3.6 | V |
| VDD2 | core digital supply voltage | | 2.25 | 2.5 | 2.75 | V |
| VDDAP | PLL A+D supply voltage | | 2.4 | 2.5 | 2.6 | V |
| $I_{DD3}$ | I/O digital supply current | | - | - | 80 | mA |
| $I_{DD2}$ | core digital supply current | | - | - | 150 | mA |
| Digital inputs | | | | | | |
| $VIL_{(SDA, SCL)}$ | input low level of SDA, SCL | | -0.5 | - | 0.3*VDD3 | V |
| $VIH_{(SDA, SCL)}$ | input high level of SDA, SCL | | 0.7*VDD3 | - | 5.0+0.5 | V |
| $VIL_{(IA/BCLK)}$ | input low level of clock pins | | -0.5 | - | 0.6 | V |
| $VIH_{((IA/BCLK)}$ | input high level of clock pins | | 2.2 | - | 5.0+0.5 | V |
| $VIL_{(all\ other)}$ | input low level of other inputs | | -0.5 | - | 0.8 | V |
| $VIH_{(all\ other)}$ | input high level of other inputs | | 2.0 | - | 5.0+0.5 | V |
| $I_{LI}$ | input leakage current | | - | - | 10.0 | uA |
| Digital outputs | | | | | | |
| $VOL_{(SDA)}$ | output low level @ SDA | IOL=3mA | - | - | 0.4 | V |
| $VOL_{(all\ other)}$ | output low level of all other | | - | - | 0.4 | V |
| $VOH_{(all\ other)}$ | output high level of all other | | 2.4 | - | - | V |

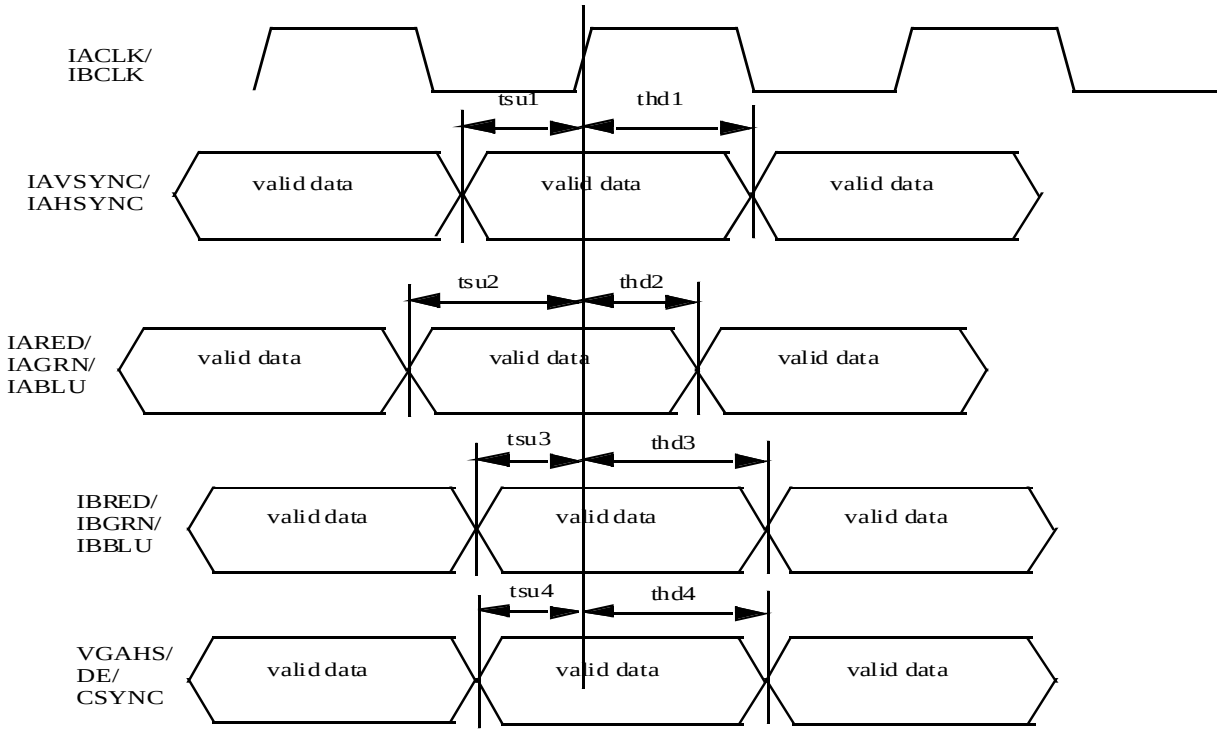
## 3.3 AC CHARACTERISTICS

All timing is measured at 1.5V logic switching threshold and VDD3 = 3.3V; VDD2 = 2.5V; VDDAP = 2.5V; $T_{amb}$= $25^o$ C; unless otherwise specified.

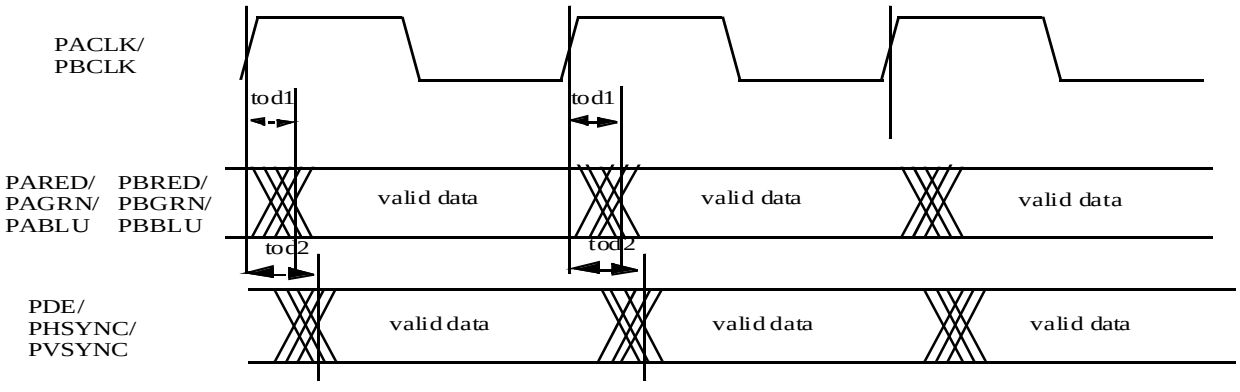
| SYMBOL | PARAMETER | min. setup time | min. hold time | UNIT |
|---|---|---|---|---|
| Input signals (RGB / YUV data and overlay ports) | | | | |
| tsu1/thd1 | IAVSYNC/IAHSYNC setup/hold time | 3.0 | 1.0 | ns |
| tsu2/thd2 | IAR/IAG/IAB input data setup/hold time | 3.0 | 1.0 | ns |
| tsu3/thd3 | IBR/IBG/IBB input data setup/hold time | 3.0 | 1.0 | ns |
| tsu4/thd4 | control signal (VGAHS/DE/CSYNC) setup/hold time | 3.0 | 1.0 | ns |

| SYMBOL | PARAMETER | min. setup time | min. hold time | UNIT |
|---|---|---|---|---|
| tsu5/thd5 | Overlay inputs (OVR/G/B/I/FB) setup/hold time | 1.0 | 3.4 | ns |
| Output signals | | max. delay time | | |
| tod1 | pixel data output delay (PAR/G/B, PBR/G/B) | 4.5 | | ns |
| tod2 | control signal (PDE, PHS/PVS) output delay | 5.0 | | ns |

INPUT TIMINGS




OUTPUT TIMINGS



trumpion microelectronics inc. reserves the right to change products or specifications without notice.


# trumpion microelectronics inc.

11F, No. 17 Sec. 1, Cheng-Teh Rd. Taipei, Taiwan, R.O.C.
Tel: 886-2-2558-7855
Fax: 886-2-2558-7850
www.trumpion.com


trumpion
microelectronics, Inc.