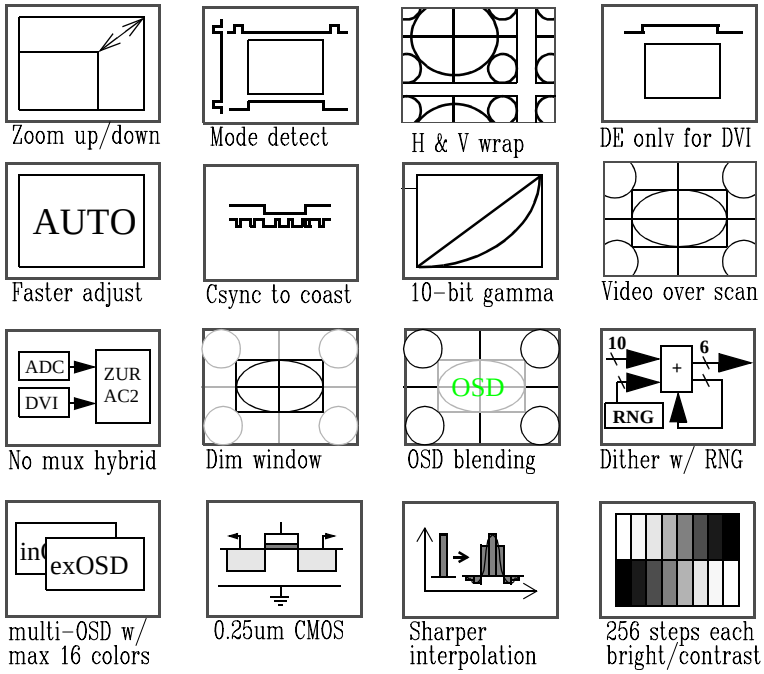
t r u m p i o n

# ZUR AC2 & 3

## Zoom Engine for TFT-LCD Monitor




Preliminary Spec.

**Preliminary specification** **Mar. 3, 2000**

T-0911/T-0912

trumpion
microelectronics, Inc.

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# ZURAC 2 & 3

**TABLE 1.**

| Version | Date | Author | Description |
|---|---|---|---|
| 0.1 | Oct. 1999 | Gene Chuang | preliminary release 1 |
| 0.2 | Dec. 1999 | Gene Chuang | preliminary release 2 for selected customers with NDA only |
| 0.3 | Jan. 2000 | Gene Chuang | preliminary release 3 of zuracII and III for selected customers with NDA only |
| 0.4 | Mar. 2000 | Gene Chuang | preliminary release 4 of zuracII and III for first-silicon promotion (selected customers with NDA only.) |
| | | | |

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# 1.0 Introduction

ZURACII/III (Zoom Up/down RAte Converter II and III) chip converts PC/Mac video signals for TFT-LCD monitor display. It performs image scaling on 24-bit RGB or YUV data stream and feeds the scaled pixels to LCD panel. The chip embeds line buffers so that the scaling needs no external memory ICs. An OSD (On Screen Display) logic is embedded for supporting the user interface, besides, there is an overlay port for external OSD signals interface. An auto adjustment function provides automatic frequency, phase, H&V position, and white balance tuning. The chip includes also the contrast/brightness circuit and gamma tables for color correction.

ZURACII and III chips are drop-in replacements for the trumpion Zurac scaler. The ZURACII is targeted for XGA/SVGA TFT-LCD panel, while ZURACIII is intended primarily for SXGA applications. The registers in Zurac and ZURACII/III are compatible unless high-lighted.

# 2.0 Additional ZURACII/III Features beyond ZURAC

- Scale up (same as Zurac) and down.
- Besides the Bresenham Linear as in Zurac, B-cubic and Bresenham Sinc scaling algorithms are also available.
- Improved auto function, full screen input format detection and best phase searching.
- DE input for digital FPD (e.g. DDWG or OpenLDI) interface.
- Hardware mode detection for both H/V sync or DE only mode.
- Composite sync (H+V) input and coast signal output for ADC.
- Programming viewing window for PC/TV, programmable Href/Vref delays for video overscan.
- Sync processing for H/V wrap effect.
- Improved resolution for Hsf (H scaling factor).
- Improved resolution for contrast adjusting for each R/G/B.
- Color (alpha) blending of OSD and video.
- Interlaced field detection for PC.
- Dim of programmable display area.
- The default state (immediately after system reset) is in free-run mode.
- 10-bit Gamma table.
- Max LCD panel support is SXGA@75Hz.

## 2.1 scaler

Scale down is available in ZuracII/ZuracIII.

Besides the Bresenham Linear as in Zurac, B-cubic and two Bresenham Sinc (sin x / x) scaling algorithms are also available.

Scale up algo can be programmed to use sharpness/smoothness for text and graphics display.

**TABLE 1. The scaling factor for each display mode**

| Input mode | Resolution | Zoom to 800*600 | | Zoom to 1024*768 | | Zoom to 1280*1024 | |
|---|---|---|---|---|---|---|---|
| | | H | V | H | V | H | V |
| SXGA | 1280*1024 | 5/8 | n/a | 0.8 | 0.75 | 1 | 1 |

| Input mode | Resolution | Zoom to 800*600 | | Zoom to 1024*768 | | Zoom to 1280*1024 | |
|---|---|---|---|---|---|---|---|
| | | H | V | H | V | H | V |
| WS | 1152*864 | 25/36 | 2/3 (576) | 8/9 | =0.8888 | 11/10 (1267) | 32/27 |
| XGA | 1024*768 | 25/32 | 3/4 (576) | 1 | 1 | 5/4 | 4/3 |
| All other display modes are the same as Zurac | | | | | | | |

# 3.0 .General Features

- Single-chip video scaling solution. No external memory required.
- Programmable independent horizontal and vertical **zoom up and down**.
- **DE input for digital FPD (e.g. DVI or OpenLDI) interface.**
- **Hardware display mode detection for both H/V sync or DE only mode.**
- **Composite sync (H+V) input and coast signal (synchronized with the rising or falling of Hsync, programmable delay) output for ADC.**
- On chip programmable OSD for LCD monitor user interface.
- **Enhanced** auto adjustment for frequency, phase, H/V position, and white balance.
- On chip brightness, contrast and gamma correction.
- **Enhanced** dithering with RNG and feedback for error diffusion
- 0.25 um CMOS technology with 5V tolerance input pads.
- 160-pin PQFP package.

## 3.1 Input

- Single RGB port mode: 24-bit RGB 1-pixel/transfer @ 100 MHz (max.)
- **Single-port input can be from either A or B input port.**
- Dual RGB port mode: 48-bit RGB 2-pixel/transfer @ 70 MHz (or pixel rate at 135MHz)
- 8-bit YUV 4:2:2 (CCIR 656), 16-bit YUV 4:2:2 video input. Glue-less connection to video sources from MPEGII decoder or video decoder, e.g. SAA7113.
- Build-in YUV to RGB color space converter.
- 5V tolerant input pads support 5V/3.3V interface.

## 3.2 Gamma correction and OSD

- **10-bit Gamma table.**
- Downloadable true-color gamma correction table.
- Downloadable font RAM for 64 fonts with 20x12 font size for internal OSD.
- Overlay port interface and color look-up table with 4 color indices from external OSD.
- Color blending of OSD and video.
- **Improved OSD range of location.**

## 3.3 Output

- Single pixel/clock (24 bit) or double pixel/clock (48 bit) digital RGB output.

- Maximum resolution up to 1280x1024x75Hz.
- Output size: 800*600, 1024*768, 1280*1024, 1400x1050 (if scale up).
- Compliant with proposed VESA FPDI-2 standard via direct connect to LVDS transceivers.

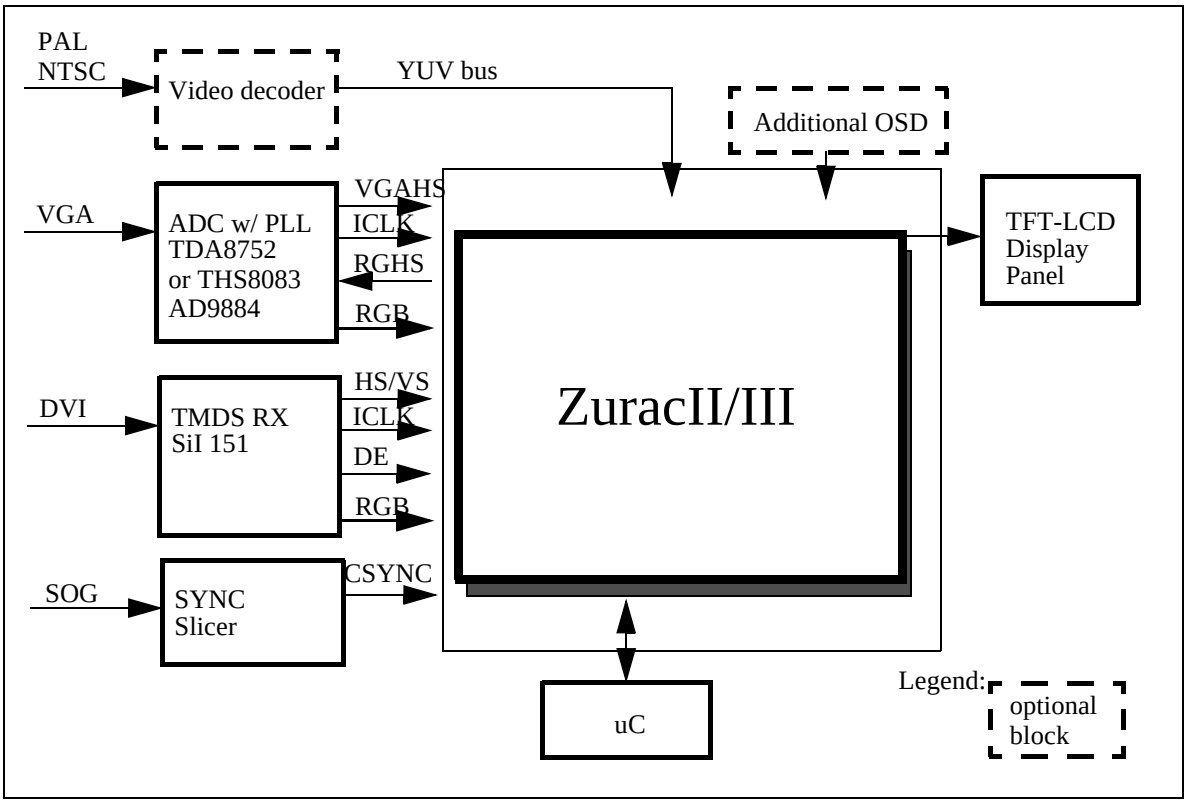
## 3.4 Display Synchronization Modes

- Input and output frames have the equal frame rate and the vertical active periods are synchronized.

## 3.5 Applications

- TFT-LCD monitors.
- NTSC/PAL projection systems for office presentation and home theater.
- Image scaling for video format conversions.

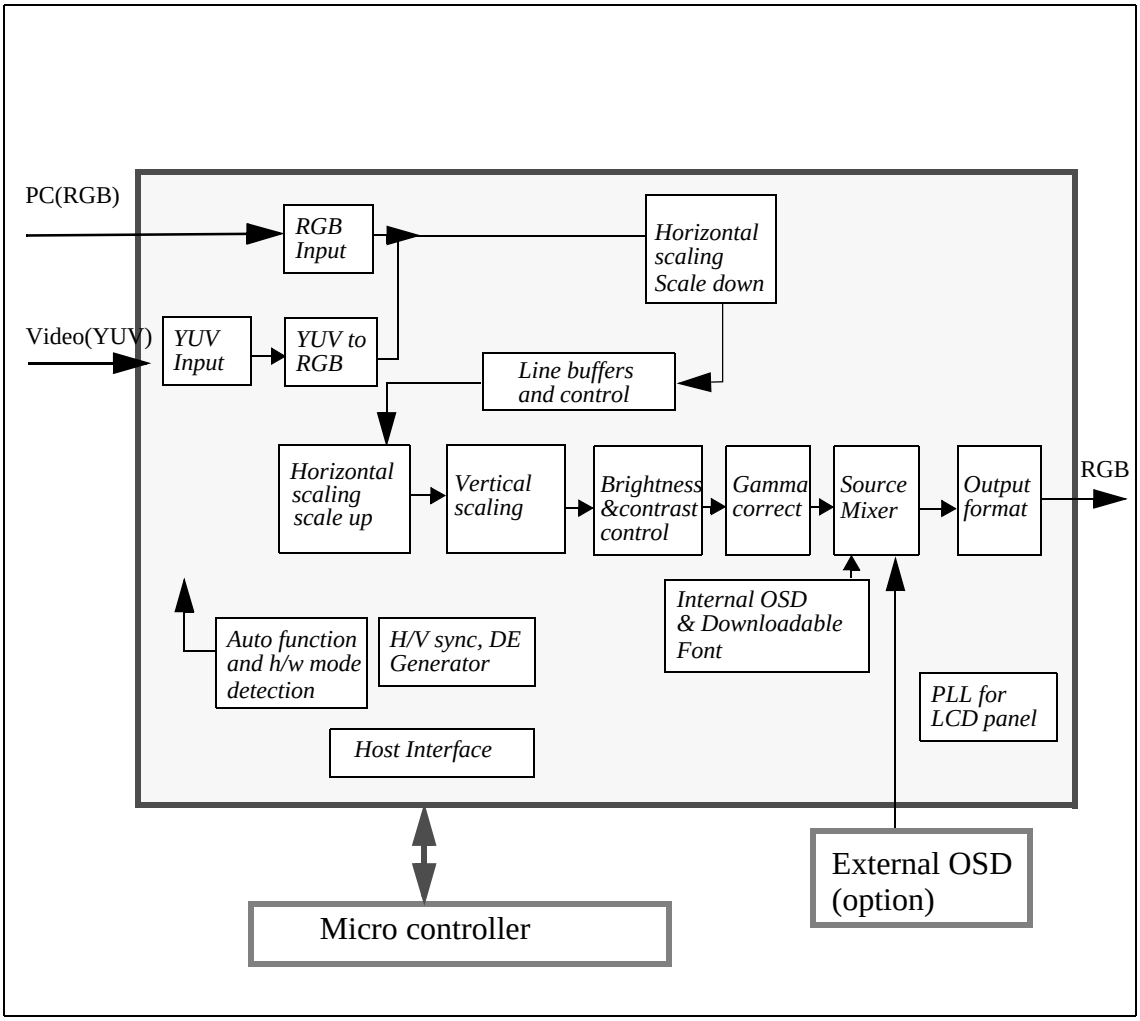
**FIGURE 1. Typical application in a LCD monitor**




## 3.6 Block Diagram

The hardware block diagram of the chip is the following:

**FIGURE 2. Block Diagram of ZURAC chip**




## 3.7 Supported Display Modes

**TABLE 2. The supported scaling for each display mode**

| Input mode | Resolution | Zoom to 800*600 | Zoom to 1024*768 | Zoom to 1280*1024 |
|---|---|---|---|---|
| SXGA | 1280*1024 | HQscaledown | HQscaledown | 1:1 |
| WS | 1152*864 | HQscaledown | HQscaledown | HQscaleup |
| XGA | 1024*768 | HQscaledown | 1:1 | HQscaleup |
| SVGA | 800*600 | 1:1 | HQscaleup | HQscaleup |
| VGA | 640*480 | HQscaleup | HQscaleup | HQscaleup |
| DOS(TEXT) | 640*400 | scaleup | scaleup | scaleup |
| DOS(EGA) | 640*350 | scaleup | scaleup | scaleup |
| TEXT | 720*400 | scaleup | scaleup | scaleup |

| Input mode | Resolution | Zoom to 800*600 | Zoom to 1024*768 | Zoom to 1280*1024 |
|---|---|---|---|---|
| Mac | 832*624 | scaledown | HQscaleup | HQscaleup |
| NTSC | 720*(240*2) | De-interlaced | De-interlaced | De-interlaced |
| PAL | 720*(288*2) | De-interlaced | De-interlaced | De-interlaced |

Without external frame buffers, the scaling up are performed under the condition that the output frame-rate is the same as the input frame-rate. For example, VGA with frame-rate 60Hz (640*480*60Hz) can be scaled to 800*600*60Hz or 1024*768*60Hz.

Legend: HQscaleup means High Quality scale up is supported, De-interlaced means interlaced video signal is scaled up to fit the panel resolution and the starting lines on the panel are different to compensate the offset for even and odd fields. N/A means not available.

# 4.0 Chip Characteristics

## 4.1 Recommended Operating Conditions

### 1 ABSOLUTE MAXIMUM RATINGS

| **Item** | **Value** |
|---|---|
| Operating voltage | 2.5V and 3.3V plus/minus 5% |
| Operating chassis temperature | $0^{o}$C to $80^{o}$C |
| Total power dissipation | 0.5W (estimated for XGA LCD panel) |

## 4.2 Pinning

**Pin 127 ADCCLKP (out) is now COAST (out), Pin 129 ADCCLKN (out) is now RGHS (out)**
**Pin 4 GND is now VGAHS (in)**
**Pin 8 SCSN (in) is now DE (in), Pin 9 SDAI (in) is now CSYNC (in), pin 10 SDAO is renamed to SDA**
**Pin 54 PCLK in now PACLK**
**Pin 53 is now PBCLK (it was VDDPP which are internally tied together now with pin 52 VDDAP)**
**Pin 23 VDD3 is now PWM (out), Pin 130 GND is now PCLKIN (in) (IN MP VERSION ONLY)**

**FIGURE 3. Pin assignment of ZuracII/ZuracIII**

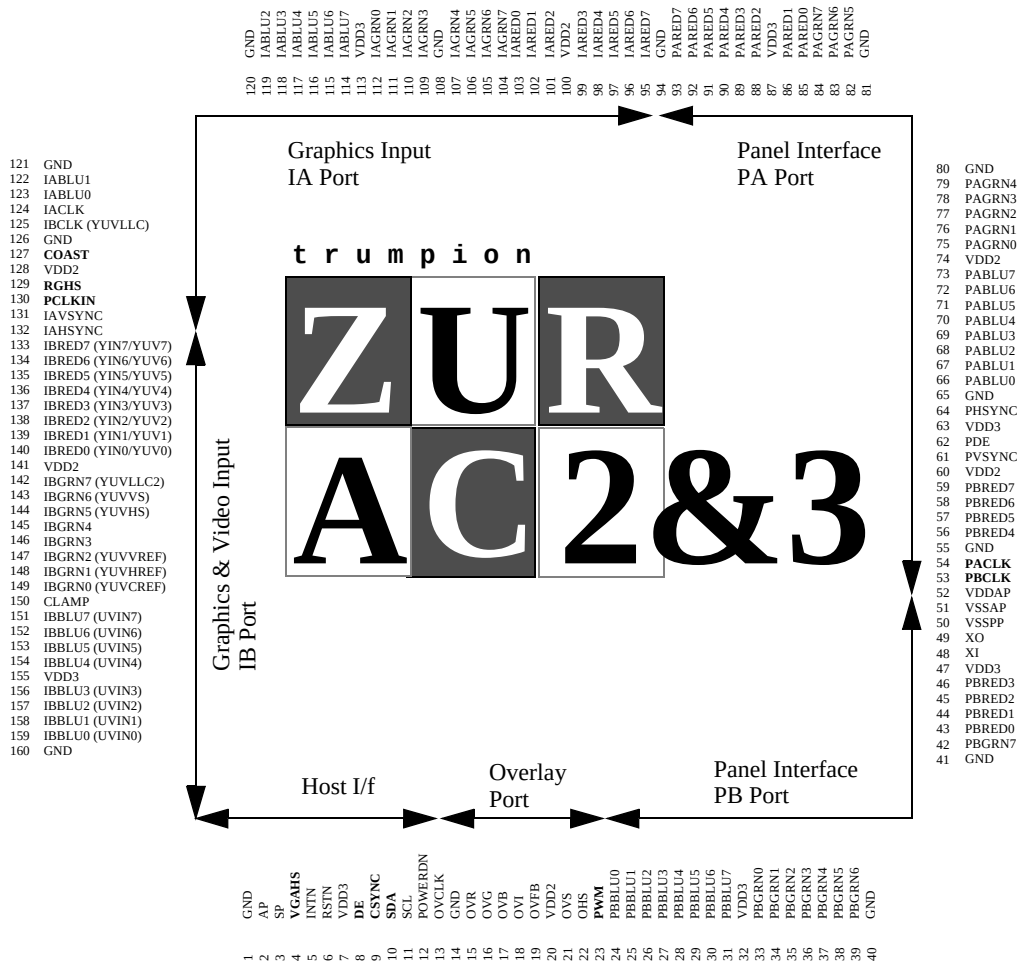


**TABLE 3. Input Ports (RGB and YUV Data, 59 pins)**

| Pin # | I/O (drive) | Name | Description |
|---|---|---|---|
| 124 | I | IACLK | Clock for A port input (single/double pixel per clock). |
| 131 | I | IAVSYNC | Vertical Sync of video A port. |
| 132 | I | IAHSYNC | Horizontal Sync of video A port |
| 95-99, 101-103 | I | IARED[7:0] | Red input data of video A port. The pin numbers are listed from MSB to LSB. |
| 104-107, 109-112 | I | IAGRN[7:0] | Green input data of video A port. |
| 114-119, 122-123 | I | IABLU[7:0] | Blue input data of video A port |
| 133 - 140 | I | IBRED[7:0] / YIN[7:0]/ YUV[7:0] | Red of video B port or Y input data for 16-bit YUV422 or YUV for 8-bit YUV422 |
| 125 | I | IBCLK/YUVLLC | Clock for B port input. Also used as LLC signal when YUV mode is selected. |
| 127 | O | **COAST** | COAST signal to ADC (regenerated VS). |
| 129 | O | **RGHS** | Regenerated HS |
| 4 | I | **VGAHS** | VGA input HS |
| 8 | I | **DE** | Display enable signal from digital flat panel interface<br>This signal should be tied to high if DE function is not used |
| 9 | I | **CSYNC** | Composite sync signal that includes HS and VS |
| 142 - 149 | I | IBGRN[7:0] | Green input data of video B port<br>bit 7: YUVLLC2<br>bit 6: YUVVS<br>bit 5: YUVHS<br>bit 2: YUVVREF<br>bit 1: YUVHREF<br>bit 0: YUVCREF |
| 151-154, 156 - 159 | I | IBBLU[7:0] / UVIN[7:0] | Blue of video B port or UV input data for 16-bit YUV422 |
| 150 | O | CLAMP | Clamp pulse to ADC |
| 23 | O | **PWM** | Pulse width modulation output (NOTE: pin 23 is the VDD3 in Zurac) |

**TABLE 4. Panel interface (or Display Port) (RGB Data, 56 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 54 | O | **PACLK** | Display port A clock for panel (capability is 8 mA) (This clock is generated from internal PLL) |
| 53 | O | **PBCLK** | Display port B clock for panel (capability is 16mA) This clock is generated from internal PLL) |
| 130 | I | **PCLKIN** | Display data and control signals will be synchronized by this external clock source. |
| 62 | O | PDE | Display enable (active area of display) |
| 61 | O | PVSYNC | Display Vertical Sync |
| 64 | O | PHSYNC | Display Horizontal Sync |
| 93-88, 86-85 | O | PARED[7:0] | Display A port red data. |
| 84-82, 79-75 | O | PAGRN[7:0] | Display A port green data. The pin numbers are listed from MSB to LSB |
| 73-66 | O | PABLU[7:0] | Display A port blue data |
| 59-56, 46-43, | O | PBRED[7:0] | Display B port red data. |
| 42, 39-33 | O | PBGRN[7:0] | Display B port green data |
| 31-24 | O | PBBLU[7:0] | Display B port blue data |
| 49 | O | XO | Reference frequency output for internal oscillator |
| 48 | I | XI | Reference frequency input for internal oscillator (should be connected to a 14.31818MHz crystal) |

**TABLE 5. Host Interface Signals (5 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 5 | O | INTN | Interrupt to host (active low) |
| 6 | I | RSTN | Device reset (active low) |
| 10 | I/O | **SDA** | Serial I/F data in/out |
| 11 | I | SCL | Serial I/F clock |
| 12 | I | POWERDN | Power Down, 0: normal, 1:Powerdown |

**TABLE 6. Overlay Port (External OSD) (8 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 13 | O | OVCLK | Clock for external overlay circuit |
| 15 | I | OVR | Overlay color select R |
| 16 | I | OVG | Overlay color select G |
| 17 | I | OVB | Overlay color select B |
| 18 | I | OVI | Overlay intensity select |
| 19 | I | OVFB | Overlay color enable |

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 21 | O | OVS | Overlay V sync signal |
| 22 | O | OHS | Overlay H sync signal |

**TABLE 7. Testing (2 pins)**

| Pin # | I/O | Name | Description |
|---|---|---|---|
| 2 | I | AP | Action pin for testing (should be grounded) |
| 3 | I | SP | Shift pin for testing (should be grounded) |

**TABLE 8. Power and Ground Signals (30 pins include 14 VDD and 16 GND pins)**

| Pin # | V | Name | Description |
|---|---|---|---|
| 20, 60, 74, 100, 128, 141 | 2.5 | VDD2 | Digital power supply (for core cells) |
| 7, ~~23,~~ 32, 47, 63, 87, 113, 155 | 3.3 | VDD3 | Digital power supply (for I/O cells) |
| 1, 41, 81, 121 | 0 | VSS2 (GND) | Digital ground (for core cells) |
| ~~4, 130,~~ | ~~0~~ | ~~VSS3 (GND)~~ | ~~Digital ground (for I/O cells)~~ |
| 14, 40, 55, 65, 80, 94, 108, 120, 126, 160 | 0 | VSS3 (GND) | Digital ground (for I/O cells) |
| ~~53~~ | ~~2.5~~ | ~~VDDPP~~ | ~~Digital power for PCLK PLL~~ |
| 52 | 2.5 | VDDAP | Analog **and digital** powers for PCLK PLL |
| 51 | 0 | VSSAP | Analog ground for PCLK PLL |
| 50 | 0 | VSSPP | Digital ground for PCLK PLL |
| Pin 53 is now PBLCK (it was VDDPP which are internally tied together now with pin 52 VDDAP)<br>Pin 4 is now VGAHS (it was GND) and Pin 23 is now PWM (it was VDD3)<br>Pin 130 is now PCLKIN (it was GND) | | | |

| **Pin no.** | **Pin name** | **Pin no.** | **Pin name** |
|---|---|---|---|
| 1 | GND | 41 | GND |
| 2 | AP | 42 | PBGRN7 |
| 3 | SP | 43 | PBRED0 |
| 4 | **VGAHS** | 44 | PBRED1 |
| 5 | INTN | 45 | PBRED2 |
| 6 | RSTN | 46 | PBRED3 |
| 7 | VDD3 | 47 | VDD3 |
| 8 | **DE** | 48 | XI |
| 9 | **CSYNC** | 49 | XO |
| 10 | **SDA** | 50 | VSSPP |
| 11 | SCL | 51 | VSSAP |
| 12 | POWERDN | 52 | VDDAP |
| 13 | OVCLK | 53 | **PBCLK** |
| 14 | GND | 54 | **PACLK** |
| 15 | OVR | 55 | GND |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 16 | OVG | 56 | PBRED4 |
| 17 | OVB | 57 | PBRED5 |
| 18 | OVI | 58 | PBRED6 |
| 19 | OVFB | 59 | PBRED7 |
| 20 | VDD2 | 60 | VDD2 |
| 21 | OVS | 61 | PVSYNC |
| 22 | OHS | 62 | PDE |
| 23 | **PWM** | 63 | VDD3 |
| 24 | PBBLU0 | 64 | PHSYNC |
| 25 | PBBLU1 | 65 | GND |
| 26 | PBBLU2 | 66 | PABLU0 |
| 27 | PBBLU3 | 67 | PABLU1 |
| 28 | PBBLU4 | 68 | PABLU2 |
| 29 | PBBLU5 | 69 | PABLU3 |
| 30 | PBBLU6 | 70 | PABLU4 |
| 31 | PBBLU7 | 71 | PABLU5 |
| 32 | VDD3 | 72 | PABLU6 |
| 33 | PBGRN0 | 73 | PABLU7 |
| 34 | PBGRN1 | 74 | VDD2 |
| 35 | PBGRN2 | 75 | PAGRN0 |
| 36 | PBGRN3 | 76 | PAGRN1 |
| 37 | PBGRN4 | 77 | PAGRN2 |
| 38 | PBGRN5 | 78 | PAGRN3 |
| 39 | PBGRN6 | 79 | PAGRN4 |
| 40 | GND | 80 | GND |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 81 | GND | 121 | GND |
| 82 | PAGRN5 | 122 | IABLU1 |
| 83 | PAGRN6 | 123 | IABLU0 |
| 84 | PAGRN7 | 124 | IACLK |
| 85 | PARED0 | 125 | IBCLK (YUVLLC) |
| 86 | PARED1 | 126 | GND |
| 87 | VDD3 | 127 | **COAST** |
| 88 | PARED2 | 128 | VDD2 |
| 89 | PARED3 | 129 | **RGHS** |
| 90 | PARED4 | 130 | **PCLKIN** |
| 91 | PARED5 | 131 | IAVSYNC |
| 92 | PARED6 | 132 | IAHSYNC |
| 93 | PARED7 | 133 | IBRED7 (YIN7/YUV7) |
| 94 | GND | 134 | IBRED6 (YIN6/YUV6) |

| Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|
| 95 | IARED7 | 135 | IBRED5 (YIN5/YUV5) |
| 96 | IARED6 | 136 | IBRED4 (YIN4/YUV4) |
| 97 | IARED5 | 137 | IBRED3 (YIN3/YUV3) |
| 98 | IARED4 | 138 | IBRED2 (YIN2/YUV2) |
| 99 | IARED3 | 139 | IBRED1 (YIN1/YUV1) |
| 100 | VDD2 | 140 | IBRED0 (YIN0/YUV0) |
| 101 | IARED2 | 141 | VDD2 |
| 102 | IARED1 | 142 | IBGRN7 (YUVLLC2) |
| 103 | IARED0 | 143 | IBGRN6 (YUVVS) |
| 104 | IAGRN7 | 144 | IBGRN5 (YUVHS) |
| 105 | IAGRN6 | 145 | IBGRN4 |
| 106 | IAGRN5 | 146 | IBGRN3 |
| 107 | IAGRN4 | 147 | IBGRN2 (YUVVREF) |
| 108 | GND | 148 | IBGRN1 (YUVHREF) |
| 109 | IAGRN3 | 149 | IBGRN0 (YUVCREF) |
| 110 | IAGRN2 | 150 | CLAMP |
| 111 | IAGRN1 | 151 | IBBLU7 (UVIN7) |
| 112 | IAGRN0 | 152 | IBBLU6 (UVIN6) |
| 113 | VDD3 | 153 | IBBLU5 (UVIN5) |
| 114 | IABLU7 | 154 | IBBLU4 (UVIN4) |
| 115 | IABLU6 | 155 | VDD3 |
| 116 | IABLU5 | 156 | IBBLU3 (UVIN3) |
| 117 | IABLU4 | 157 | IBBLU2 (UVIN2) |
| 118 | IABLU3 | 158 | IBBLU1 (UVIN1) |
| 119 | IABLU2 | 159 | IBBLU0 (UVIN0) |
| 120 | GND | 160 | GND |

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# 5.0 Functional description of Blocks

## 5.1 YUV input port

The YUV input port supports interlaced video streams and provides connection to most common decoder ICs.

This chip supports 8-bit YUV 4:2:2 (CCIR 656), 16-bit YUV 4:2:2 video input. Each input format can be binary offset or 2's complement.

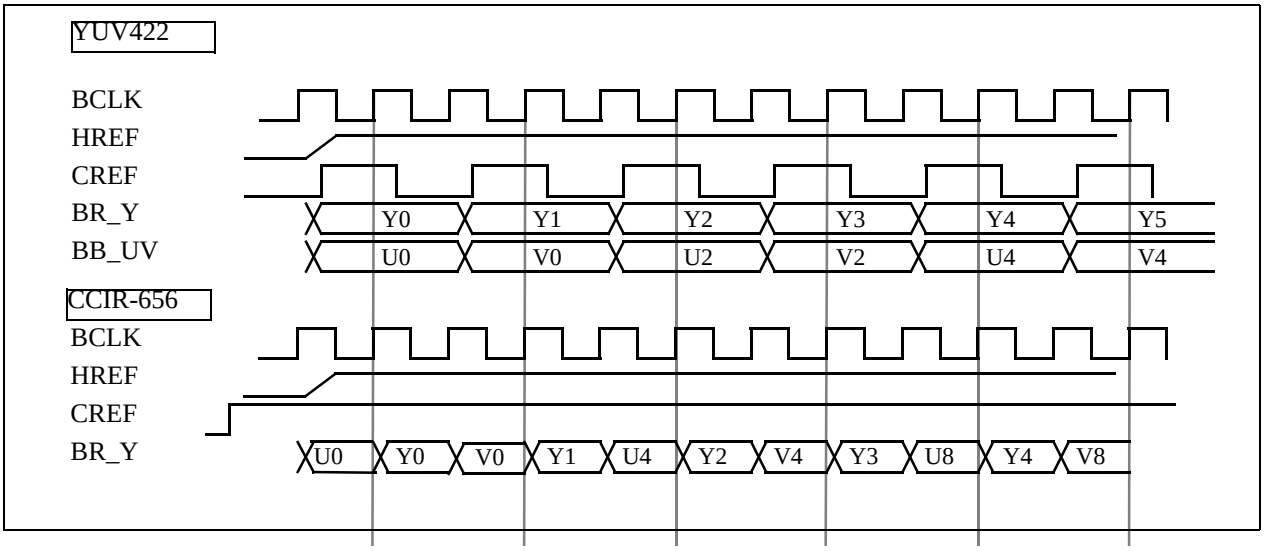
The YUV input formats are tabulated below. The selection of YUV or RGB inputs are activated by the setting of YUVF (bit 4 of INCTR1 or 02 hex) bit.

**TABLE 9.**

| **Signal** | **16-bit 4:2:2** | | **8-bit 4:2:2 (CCIR-656)** | | | |
|---|---|---|---|---|---|---|
| YIN7 | Y07 | Y17 | U07 | Y07 | V07 | Y17 |
| YIN6 | Y06 | Y16 | U06 | Y06 | V06 | Y16 |
| YIN5 | Y05 | Y15 | U05 | Y05 | V05 | Y15 |
| YIN4 | Y04 | Y14 | U04 | Y04 | V04 | Y14 |
| YIN3 | Y03 | Y13 | U03 | Y03 | V03 | Y13 |
| YIN2 | Y02 | Y12 | U02 | Y02 | V02 | Y12 |
| YIN1 | Y01 | Y11 | U01 | Y01 | V01 | Y11 |
| YIN0 | Y00 | Y10 | U00 | Y00 | V00 | Y10 |
| UVIN7 | U07 | V07 | | | | |
| UVIN6 | U06 | V06 | | | | |
| UVIN5 | U05 | V05 | | | | |
| UVIN4 | U04 | V04 | | | | |
| UVIN3 | U03 | V03 | | | | |
| UVIN2 | U02 | V02 | | | | |
| UVIN1 | U01 | V01 | | | | |
| UVIN0 | U00 | V00 | | | | |

The timing for YUV format is shown below:

**FIGURE 4. INPUT YUV format & timing.**

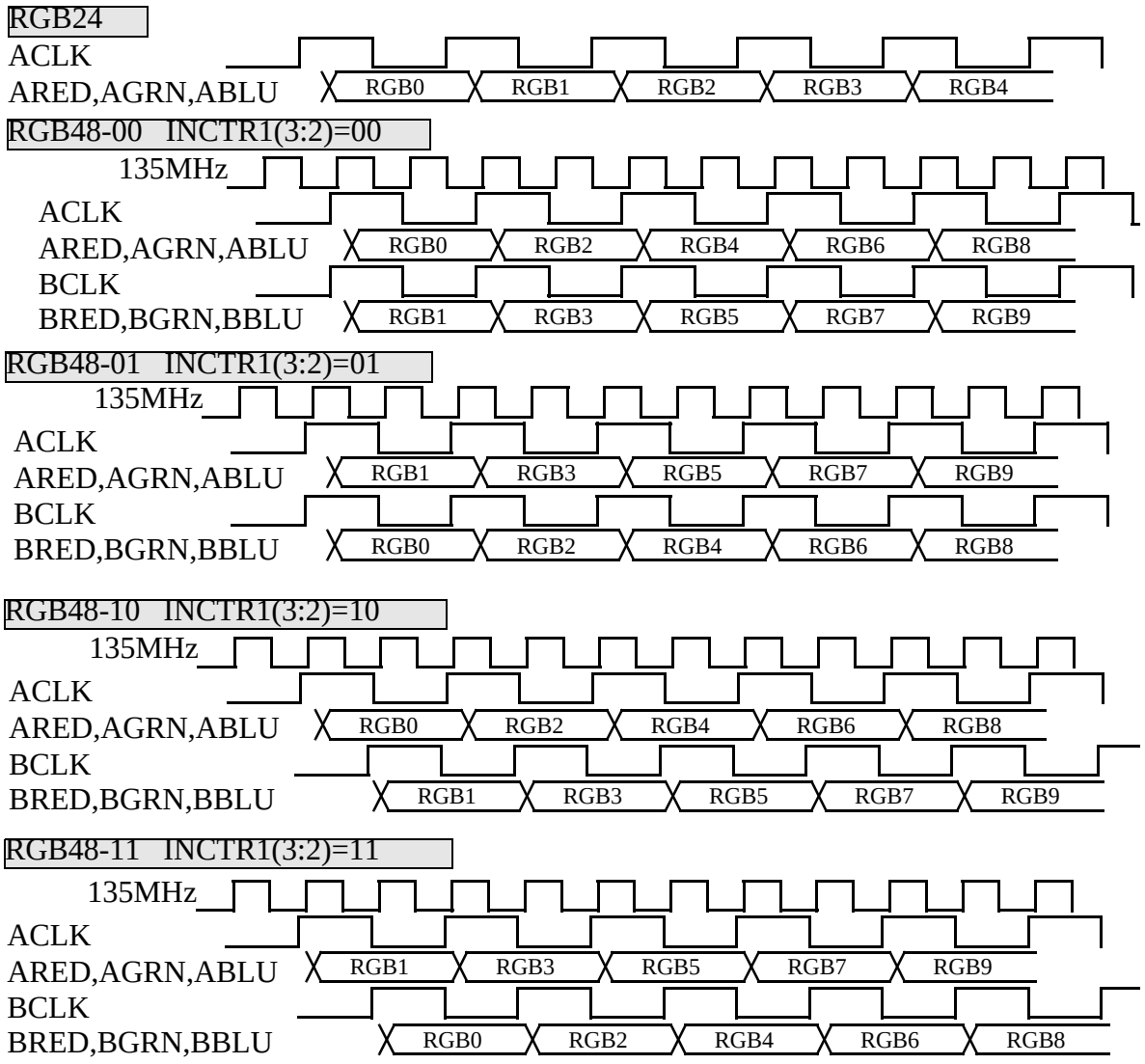


## 5.2 RGB input format and timing

The chip supports RGB 24 bits and 48 bits input. For RGB 48 bits input, there are four formats can be chosen by INCTR1(3:2) when IRGBEN=1, IRGB24=0. For RGB24 bits, set IREGBEN=1 and IRGB24=1. The single port input can be from either A or B port.

Here are the format and timing.

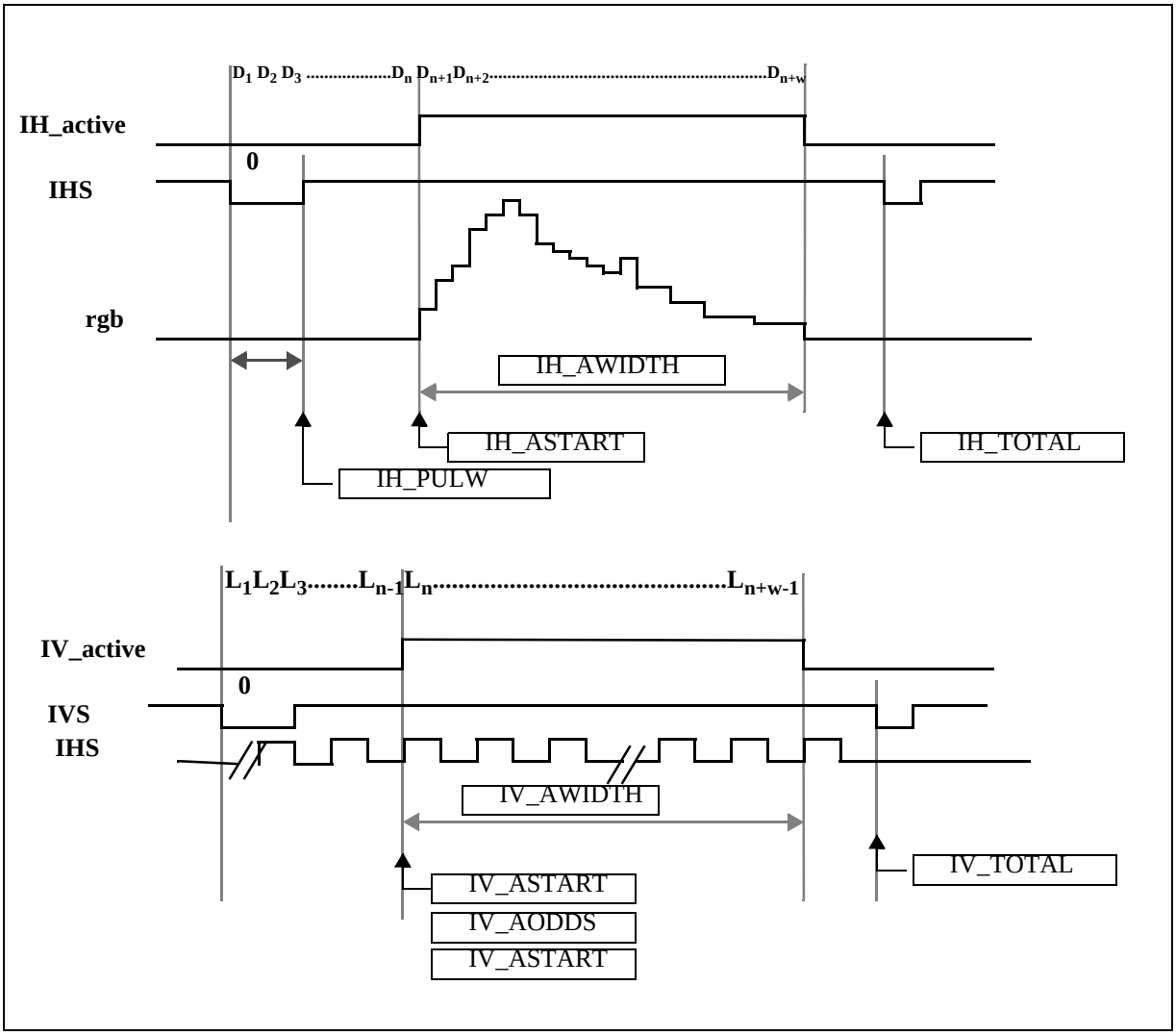
**FIGURE 5. INPUT RGB format & timing:**



## 5.3 Input/output window definition

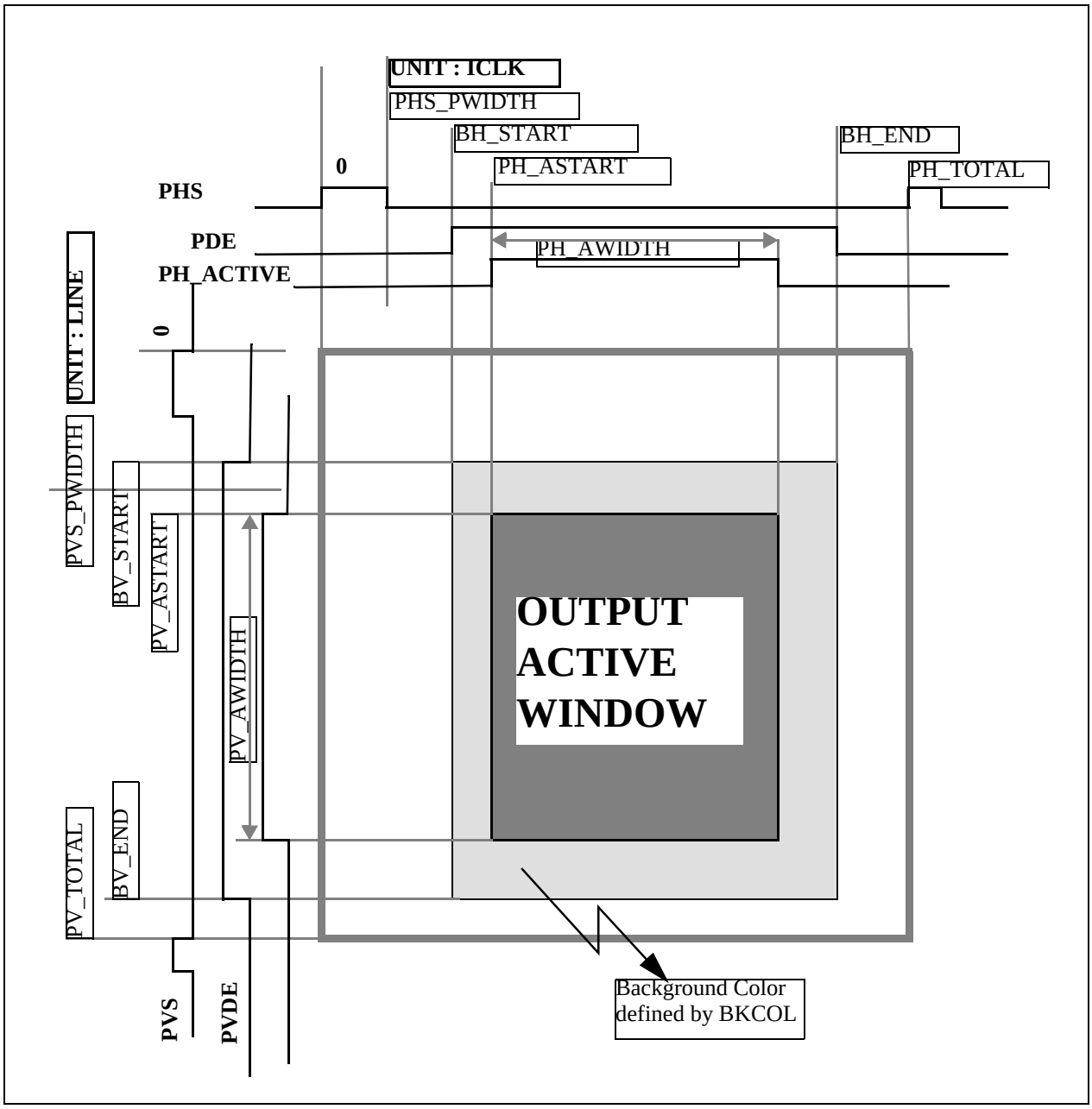
This section describes the input window. The signals IH_PULW, IH_ASTART and IH_TOTAL count from IHS falling edge. If IH_ASTART= n and IH_AWIDTH = w, then the first and the last active data are $D_{n+1}$ and $D_{n+w}$ respectively. If IV_ASTART=n and IV_ACTIVE = w, then the fist active line is $L_n$ and last active line is $L_{n+w-1}$

**FIGURE 6. INPUT WINDOW PARAMETER:**



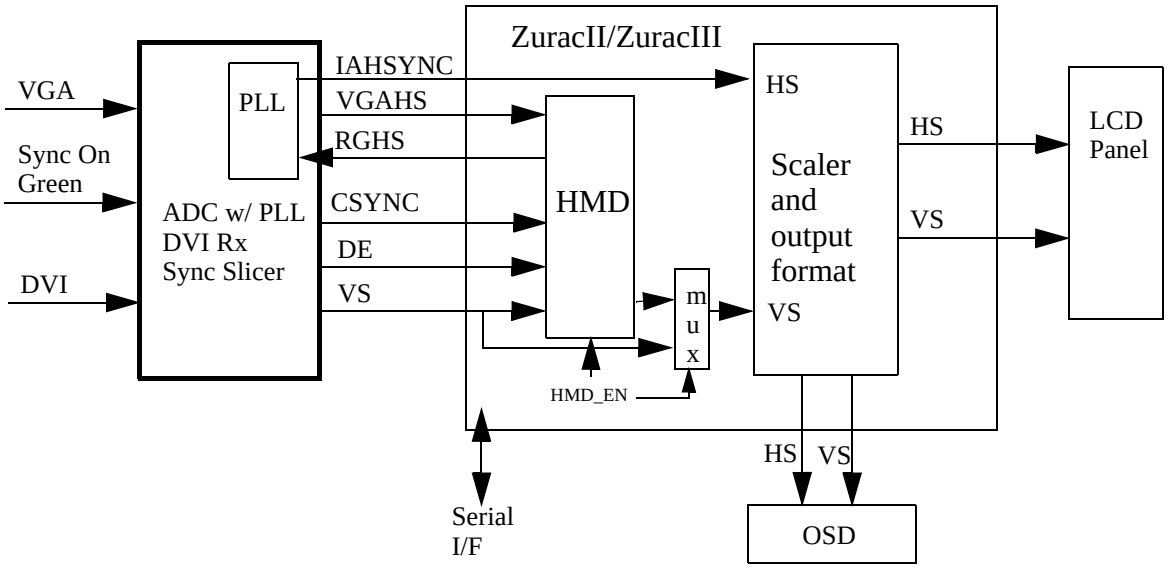
Output window parameter is shown in the following figure.

**FIGURE 7. Output Window parameters.**




## 5.4 Hardware Mode Detection (HMD)

Hardware mode detection detects the presences and frequencies of HS, VS, and DE.




Note: The IAHSYNC is the line-locked HS generated by PLL of ADC

## 5.5 Scaling

Zurac performs scaling function without any extra frame buffers. Based on a chosen scaling factor, in order to calculate the output panel Hsync from the input Hsync, we have to program some parameters such as SPH_EMU and SIH_EMU. The formula to set SPH_EMU[10:0] value is IH_TOTAL/VSf where VSf is the vertical scaling factor. A better understanding can be obtained by the following example: with VGA input that IH_TOTAL = 800 pixels and VSf = 1.6, the SPH_EMU = 800/1.6 = 500.

ZURAC also provides a free running mode (by setting BYPASS bit = 0). In this mode, without referring to input Hsync, the output panel Hsync can be generated via the setting of SIH_EMU. The formula to set SIH_EMU[11:0] value is (PH_TOTAL*VSf) where VSf is the vertical scaling factor. For example in XGA output mode, if the PH_TOTAL = 1344 pixels and the vertical scaling factor is 1.6, then the register SIH_EMU = 1344*1.6 = 2150. For detail description of scaler-related registers, please refer to registers 60 Hex to 70 Hex.

**TABLE 10. The scaling factor for each display mode**

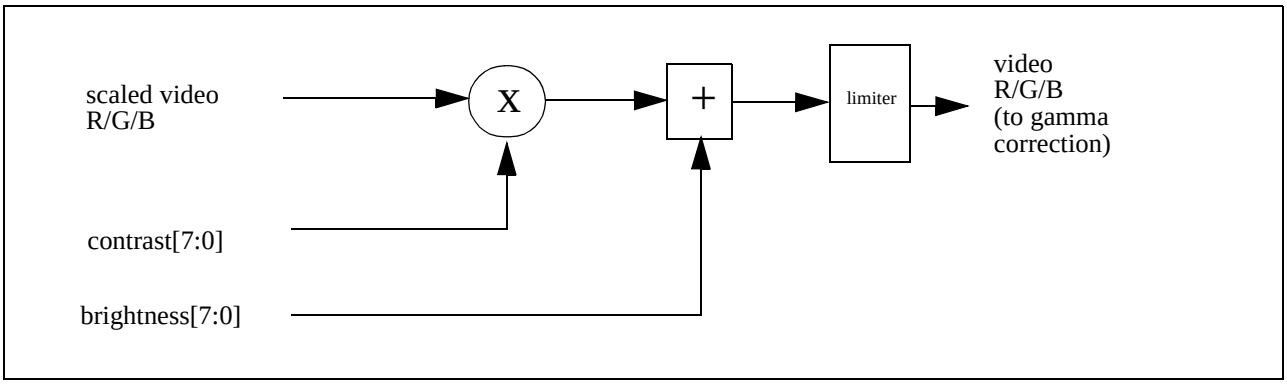
| Input mode | Resolution | Zoom to 800*600 | | Zoom to 1024*768 | | Zoom to 1280*1024 | |
|---|---|---|---|---|---|---|---|
| | | H | V | H | V | H | V |
| SXGA | 1280*1024 | 5/8 | n/a | 0.8 | 0.75 | 1 | 1 |
| WS | 1152*864 | 25/36 | 2/3 (576) | 8/9 | =0.8888 | 11/10 (1267) | 32/27 |
| XGA | 1024*768 | 25/32 | 3/4 (576) | 1 | 1 | 5/4 | 4/3 |
| SVGA | 800*600 | 1 | 1 | 32/25 | =1.28 | 8/5 | 17/10 (1020) |
| VGA | 640*480 | 5/4 | =1.25 | 8/5 | =1.6 | 2/1 | 32/15 |

| Input mode | Resolution | Zoom to 800*600 | | Zoom to 1024*768 | | Zoom to 1280*1024 | |
|---|---|---|---|---|---|---|---|
| | | H | V | H | V | H | V |
| DOS | 640*400 | 1.25 | 1.5 | 1.6 | 48/25 | 2.0 | 2.5 (1000) |
| DOS | 640*350 | 1.25 | 12/7 | 1.6 | 17/8 (743.75) | 2.0 | 29/10 (1015) |
| TEXT | 720*400 | 10/9 | 1.25 | 64/45 <-7/5 (1008) | 1.9 (760) | 16/9 | 64/25 <-2.5 (1000) |
| Mac | 832*624 | 25/26 | 25/26 | 16/13 | 16/13 | 20/13 | 64/39 <-1.6 (998.4) |
| NTSC | 720*(240*2) | 10/9 | 5/4 or 10/9 (533.3) | 36/25 (1036) | 1.6 | 16/9 | 32/15 |
| PAL | 720*(288*2) | 10/9 | 25/24 | 36/25 (1036) | 4/3 | 16/9 | 16/9 |

| **REGISTER FUNCTION** | **Addr (hex)** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
|---|---|---|---|---|---|---|---|---|---|
| **SDnAHhinc** | **6EH** | **SALGO[1:0]** | | **HSD_EN** | **VSD_EN** | **SAHhinc[3:0]** | | | |

## 5.6 Brightness and contract control

**FIGURE 8. Function of contrast followed by brightness control for each RGB.**




The H and V scaled signals are sent to a contrast followed by a brightness correction circuit for each R/G/B channel. The contrast control uses a 8-bit signal to set a multiply value from 2 to 0 (in fact, the 256 choices are 255/128, 254/128,

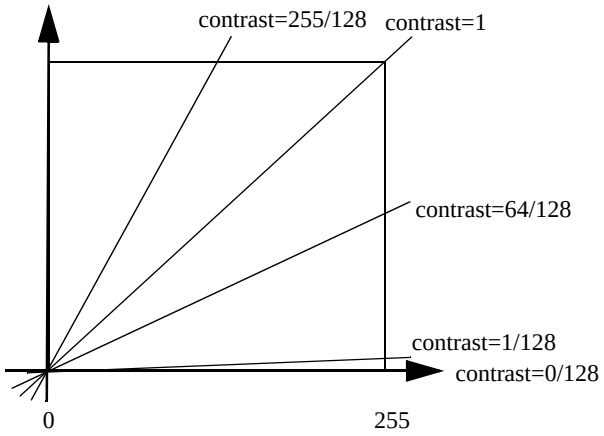
..., 128/128, .., 1/128, 0). The brightness correction uses a 8-bit signal to set an offset value from 127 to -128 (the 256 choices are 127, 126, ..., 1, 0, -1, ..., -127, -128). The control signals BRIGHTNESS[7:0] and CONTRAST[7:0] are programmable via serial interface.

The formula to set CONTRAST[7:0] value is ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0]. For brightness control, the signal BRIGHTNESS[7:0] is interpreted as a 2s complement value. These settings are tabulated as

**TABLE 11.**

| **Contrast correction for MSB=0** | | | | | | |
|---|---|---|---|---|---|---|
| contrast[7:0] | 7f(hex) | 7e | ..... | 02 | 01 | 00 |
| multiply value | 255/128 | 254/128 | ..... | 130/128 | 129/128 | 128/128 |
| **Contrast correction for MSB=1** | | | | | | |
| contrast[7:0] | ff(hex) | fe | ..... | 82 | 81 | 80 |
| multiply value | 127/128 | 126/128 | ..... | 2/128 | 1/128 | 0/128 |

| Brightness correction for MSB=0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| brightness[7:0] | 7f(hex) | 7e | 7d | ..... | 02 | 01 | 00 |
| offset value | 127 | 126 | 125 | ..... | 2 | 1 | 0 |
| Brightness correction for MSB=1 | | | | | | | |
| brightness[7:0] | ff(hex) | fe | fd | ..... | 82 | 81 | 80 |
| offset value | -1 | -2 | -3 | ..... | -126 | -127 | -128 |




## 5.7 Gamma Correction RAM Tables

Gamma correction RAM tables are implemented after the Brightness/Contrast block to provide the color-mapping of the RGB data. The tables can be activated by setting GAMMAUSE (MSB of MISCTR0 or 0A hex) bit = 1. We can also by-pass the gamma correction function by resetting the GAMMAUSE bit = 0. Through three gamma table registers (GRWADDR, GGWADDR and GBWADDR) the data representing gamma curves can be put into the RAMs sequentially. These 10-bit gamma tables can be programmed by writing first the two MSB bits to high byte and the eight LSB

bits to low byte for the first entity then the second and so on. And we can repeatedly program the register GRWADDR 512 times (high and low bytes for 256 entities). This will put the Red gamma curve into the Red RAM table (the first 10-bit data is written into RAM at address 0 and the 256th data is written into RAM at address 255). In a similar way, we can program the tables for Green and Blue channels.

## 5.8 OSD, CLUT, and Dithering

The chip t0911/0912 embeds an On Screen Display function for human interfacing. It is designed to display colored patterns, icons or characters onto the screen. A 64 character fonts (downloadable from MCU) are provided for the application of Multi-language TV/Monitor. The Graphic Character Fonts can produce the effect of the pixel based graphic display, which allows the impressive display of the customized pattern. symbols or logos.

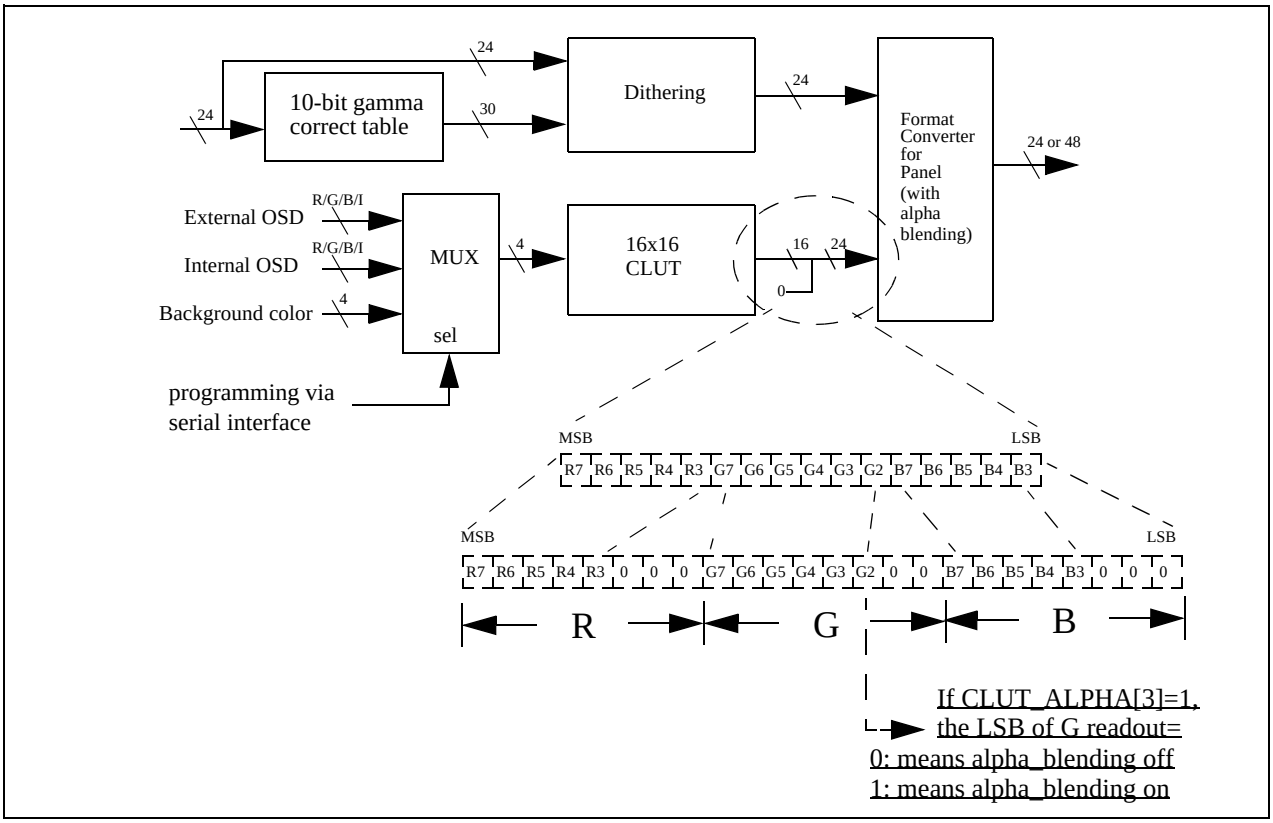
The OSD provides plentiful features to enhance the appearance of the displayed character fonts. Each character can have its own colors (up to 16 colors) and blinking option. Up to 10 shadowing modes (including bordering, boxing etc.) are provided together with 16 background colors. Multiple overlapping windows, and wipe-in or wipe-out from two directions can create more flexible user interface.

The versatile choice for display font color, background/shadow/window color, and shadow modes (including bordering and graphic character mode) leads to a unique OSD style. Some dynamic features, such as built-in see-through curtain effect, two-direction wipe in/out, character basis blinking, hardware overlapping windows etc. also enhance the image of OSD menu.

There is a 16x16 CLUT (color look-up table) which provides a programmable color palette for internal/external OSD and background color. The color index bus, namely R/G/B/I, is used as the address to the CLUT which defines the 16 colors for OSD and background color. The content and the index selection of CLUT are programming via serial interface. The mapping of the 16-bit RGB565 color to 24-bit true color is depicted as the following figure.

The format converter function for LCD panel also supports the dithering function that can be programmed via DITHER_ON (bit 6 and 5 of OUTCTR0, i.e. 03 Hex)

**FIGURE 9. Color look-up table for internal, external, and background color**



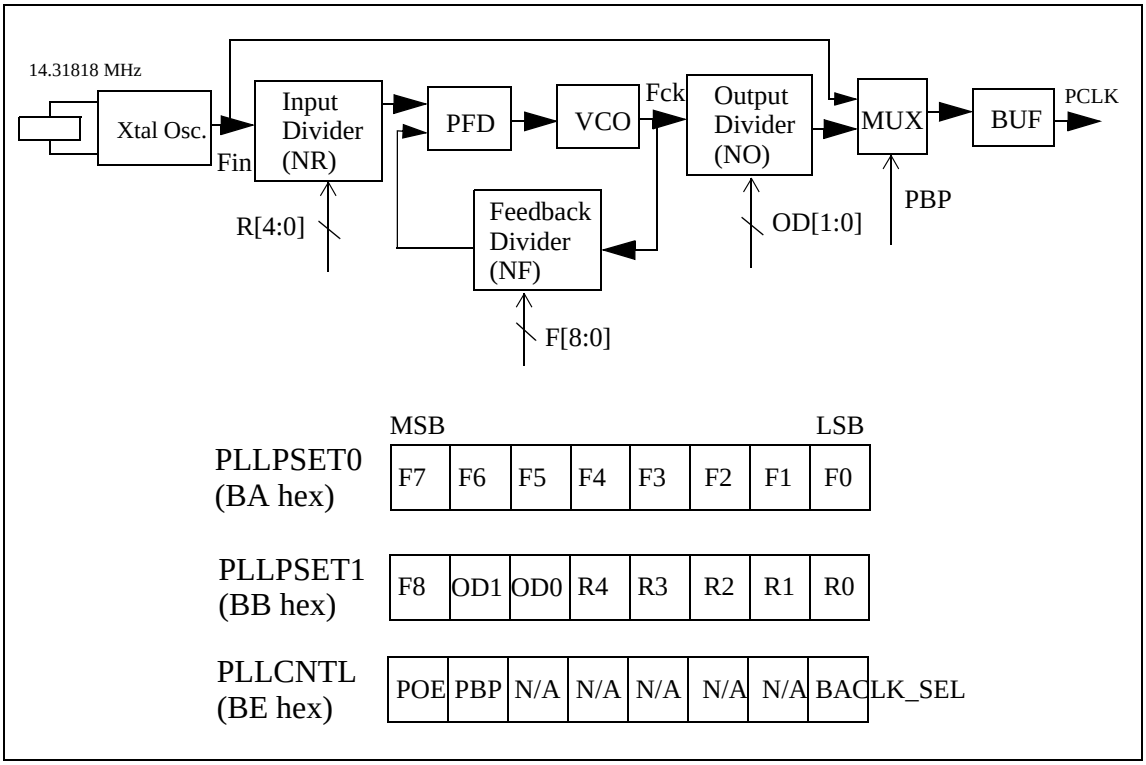
## 5.9 Clock system

t0911/0912 takes clocks from external ADCs or video decoder: namely IACLK/IBCLK. The default condition is that input video data will be latched by the rising edges of IACLK/IBCLK. There is one control bit INCTR1(7) which can invert the phase of IACLK/IBCLK. In a sense, when INCTR1(7) is high, input data are latched by the falling edge of IACLK/IBCLK.

The output of PACLK/PBCLK also has similar function. OUTCTR0(4) is used to control the phase of PACLK/PBCLK (or called PHCLK). In addition to this phase tuning, we can use OUTCTR0(3:2) to choose 4 different phases of PHCLK (the delays are around 0, 2, 4, and 6ns). LCD panel interface can choose either PACLK or PBCLK for different driving capabilities, namely 8mA or 16mA.

The pclk can be obtained either from an external source (from PCLKIN pin) or generated from an internal PLL. This PLL that synthesizes a clock for LCD panel can be programmed via the 2-wire serial bus. There are registers that can be programmed to generates clocks for different display modes. The registers and block diagram are depicted as follows:

**FIGURE 10. PLL Block diagram and its control registers that generates clock for LCD**




| PLL program parameter | | | | |
|---|---|---|---|---|
| PLLPSET0<br>FI(7 downto 0) | BA | 4F | W | F7(MSB), F6, F5, F4, F3, F2, F1, F0 (LSB)<br>The 8 LSB of feedback 9-bit divider<br>The default value will set the PCLK to 65MHz |

| | | | | |
|---|---|---|---|---|
| PLLPSET1<br>FI(8) & ODI(1 downto 0) & RI(4 downto 0) | BB | 47 | W | F8(MSB), OD1, OD0, R4, R3, R2, R1, R0 (LSB)<br>F8 is the MSB of feedback 9-bit divider, OD0 (MSB) and OD1 (LSB) are the control pins for output divider, and R4 to R0 are the pins for input 5-bit divider |
| PLLCNTL<br>Output enable and bypass control for Pclk ~~and Mclk~~ PLL.<br>~~LSB is for IBCLK or IACLK selection~~ | BE | 00 | W | POE(MSB), PBP, xx, xx, ~~MOE, MBP, xx, BACLK_SEL (LSB)~~<br>where POE is the freq Output Enable of Pclk PLL (default 0), PBP is the ByPass control of Pclk PLL (default 0), ~~and MOE/MBP are for Mclk PLL, xx is do not care.~~<br>PLL will go to power down mode as the external POWERDN pin activated.<br>~~bit 0: BACLK_SEL is for IBCLK or IACLK selection.~~<br>~~0: ICLK = IBCLK/2 (for LLC2)~~<br>~~1: ICLK = IACLK~~<br>The control of BACLK_SEL is now moved to Bit 1 of MISCTR1. |

**Note:**

1. The frequency derived from the PLL frequency synthesizer is formulated as follows:

   PCLK = Fin * NF/(NR*NO).

   Where Fck = Fin*NF/NR, the output freq of VCO, should be in the range of 80 MHz to 200 MHz.

   The freq of PCLK can be modified by programming the register of NF, NR, and OD. The values of the divider should be set by substrating the actual value by 2, i.e. if divided by 8 is what we want, then the binary values of the input control register should be set to 6 (e.g. NF is 000000110). The output divider (NO) control register is set by the following.

2. The bit BP (bypass) will be set to 1, if PLL is being tested, otherwise reset for normal PLL function.

**TABLE 12.**

| Output Divider | Divided by |
|---|---|
| OD1=0 OD0=0 | 1 |
| OD1=0 OD0=1 | 2 |
| OD1=1 OD0=0 | 2 |
| OD1=1 OD0=1 | 4 |

For example, if we want to get a 100 MHz output freq clock and Fin=14.31818 MHz, we need to set NF/NR = 140/10, and OD=2. In a sense, NF=010001010(bin), NR=01000, and OD=10.

Another example, if we want to get a 65 MHz output freq clock for XGA LCD panel and Fin=14.31818 MHz, we need to set NF/NR = 227/25, and OD=2. In a sense, NF=227-2=e1(hex), NR=25-2=17(hex), and OD=10(bin).Therefore, we need to program the register PLLPSET0 (BA) with a value e1(hex) and PLLPSET0 (BB) with 59.

## 5.10 Power down

The chip enters into power down status by setting POWERDN pins to high. The system returns to normal after POWERDN is set to low.

In power down status, all circuits are set to off except the **mode detection circuit** which is always working.

## 5.11 Communication Protocol

The control of t0911/0912 can be achieved through two kinds of serial transfer, namely, SPI and 2-wire serial bus interface. The selection between two kinds of interface can be done automatically by hardware. 2-wire serial bus interface also supports the read back of the some control registers.

The communication between t0911/0912 and MCU is performed by 2-wire serial bus interface or SPI interface. The industrial standard 2-wire serial bus interface supports bidirectional transfer (READ and WRITE) with baud rate up to 400 K bps. The 3-wire SPI interface can provide up to 1 M bps baud rate.

### 5.11.1 2-wire serial bus interface

t0911/0912 supports the industrial standard 2-wire serial bus interface, which consists of SDA bidirectional data line and SCL clock line. The 2-wire serial bus slave address of this chip is 1111000(binary). The definition of the basic 2-wire serial bus interface protocol is illustrated as follows. For detailed timing and operation protocol, please refer to the standard 2-wire serial bus specification.

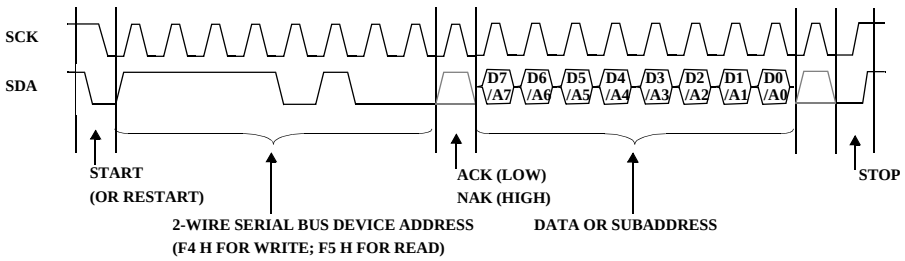
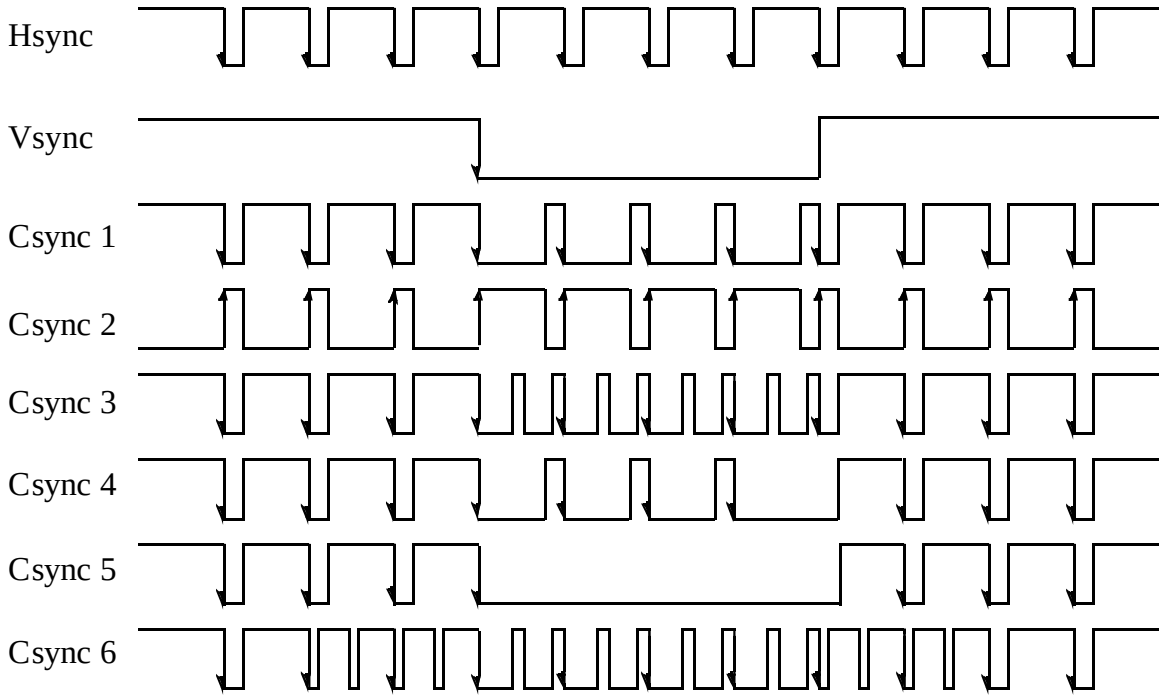



Fig.11 The definition of the basic 2-wire serial bus timing protocol

### 5.12 Mode detection

The hardware mode detection circuit has the functions as mode detection blocks of all CRT monitor micro-controllers. For example, it can detect the presences, polarities, and frequencies of HS, VS, and DE. It sends out interrupt at certain programmable events, etc. Besides, there is a Vsync separation that handles six types of Csync inputs (depicted as in the following figure) and generate the corresponding Vsync pulse which can be used as the COAST signal into ADC chips. Generally, these Csync signals come from Hsync plus Vsync or Hsync exclusively OR Vsync or added serration pulse. The Composite sync to coast signal generation is depicted as in the following figure.




## 5.13 Auto-Adjustment

These functions will be supported by Zurac:

Searching a line for H-start, and H-end (if the Mth line designation is 00, the entire screen is searched)

A segment (including the full-line) of line is frozen and the RGB values can be read by host.

Optimum phase searching is via the calculation of the *sum of difference* of pixels in a window (including the entire screen) which is defined by IIC (for each RGB, or for the sum of RGB, for a frame, or for some frames)

The *sum* of pixels on a window (including the entire screen) defined by IIC (for each RGB, or for the sum of RGB, for a frame, or for some frames) will be also performed.

While only *sum of difference* or *sum* operation (selected by IIC programming) is available for intra-frame operation, the *sum of difference* and *sum* operations are simultaneous available for inter-frame operations.

Besides, there are four functions supported by Zurac, namely, line frozen, line-edge (high-low-high or low-high-low), V start-end, and H start-end searching. The procedure are as follows:

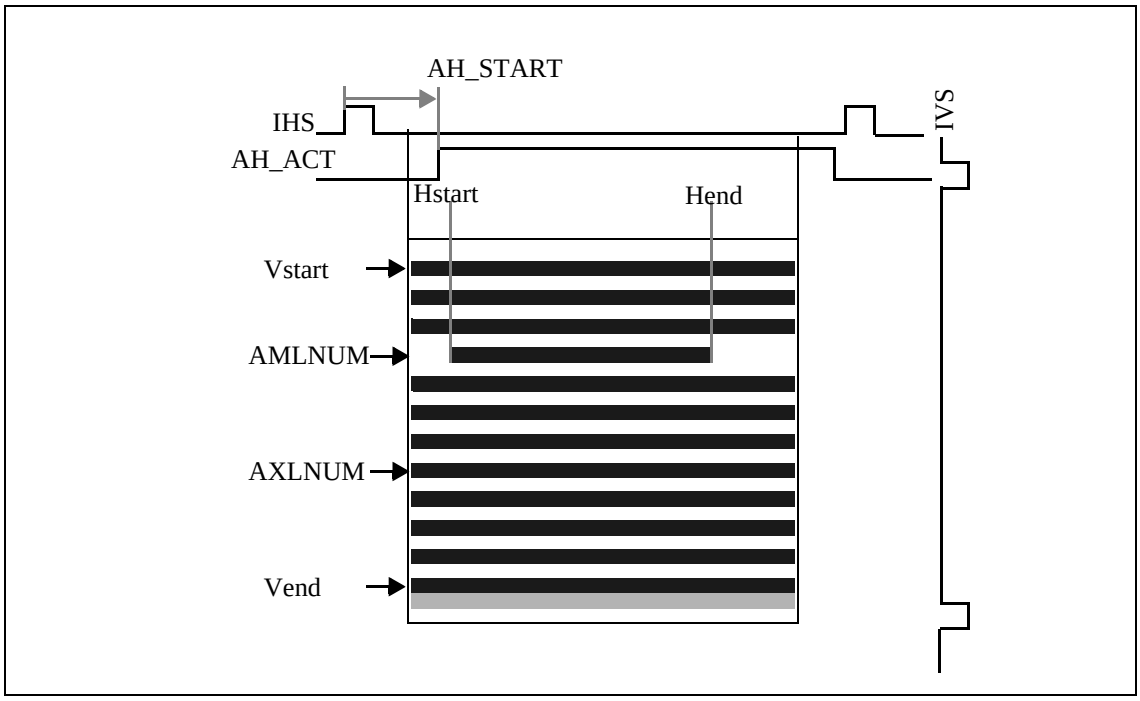
1) Define a compare window: When the value of color channel R or G or B (designated by AACMP[1:0]) is greater than ARGB_MIN, a valid data is found. We use the parameter AH_START to define the starting location of searching window in horizontal direction. For vertical searching, the start point is the first line counted from the rising edge

of IVS.

2) Check Vstart and Vend: When one line contain 8 (or greater then 8) valid data. The first valid line is named as Vstart and the last valid line is Vend.

3) Check Hstart and Hend: The parameter AMLNUM designates the line to perform the position searching of Hstart and Hend. Hstart is the first valid data and Hend is last valid data on the AMLNUM line. The RGB values of Hstart and Hend are also stored so that the value can be accessed by the host micro-controller

**FIGURE 12. Parameters definition for auto adjustment.**

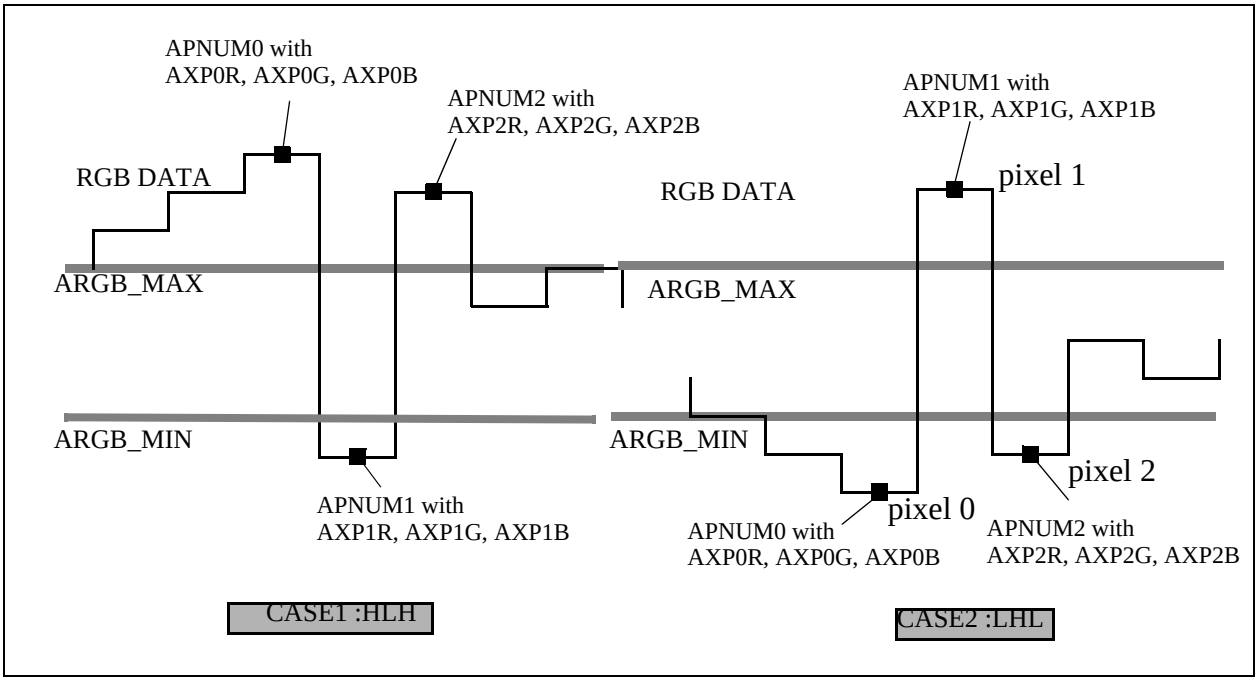



4) Check HLH or LHL: The pixel data -R or G or B chosen by AACMP(1:0) - greater than ARGB_MAX is called H-data, lower then ARGB_MIN is called L-data. AXLNUM define which line to check 3 sequential data is H-L-H or L-H-L, record the 3 pixels position and data.

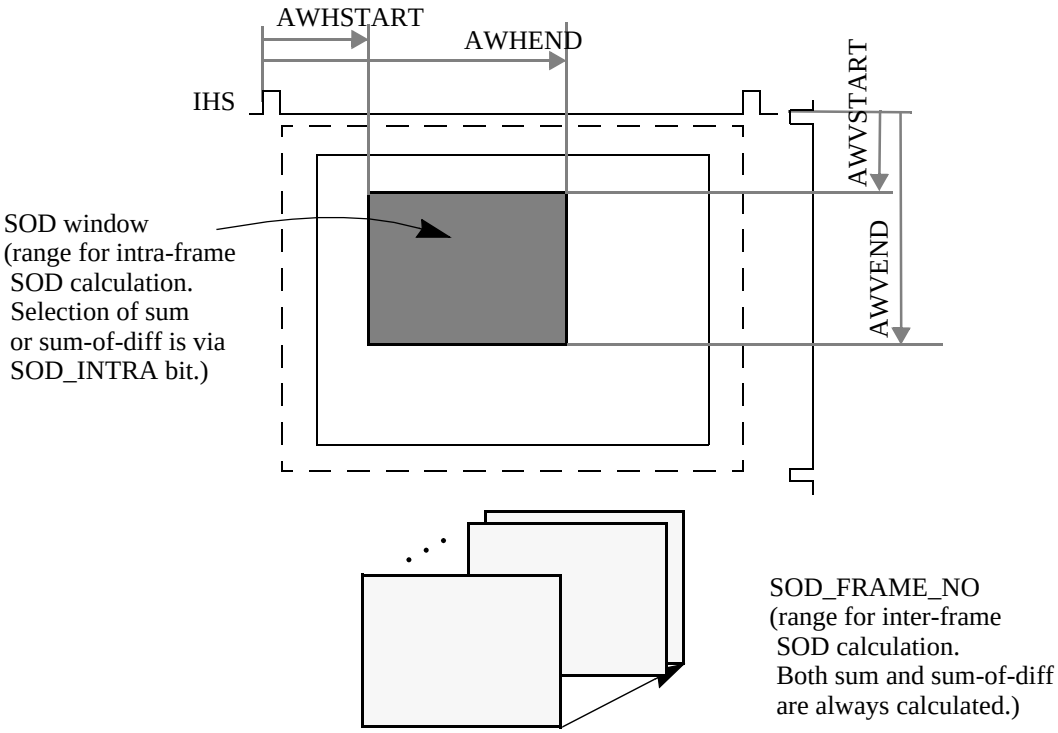
5) To freeze a line buffer and read the content, one should designate the line address (counted from the first active line) and the starting pixel (counted from the H active region) and then read the same address AFZREAD sequentially.

All data are updated per frame and check continuously.

**FIGURE 13. Auto adjustment circuits that search the high-low-high and low-high-low along the Xth line:**




Inter and intra-frame SOD (sum and sum of difference) calculations



# 6.0 Register Definition:

The 2-wire serial bus slave address of this chip is 1111000 (bin):

**TABLE 13.** PANORAMA OF SUB-ADDRESS REGISTER

| | | **LOW NIBBLE OF SUBADDRESS** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Addr (hex)** | X0 H | X1 H | X2 H | X3 H | X4 H | X5 H | X6 H | X7 H | X8 H | X9 H | XA H | XB H | XC H | XD H | XE H | XF H |
| **HIGH NIBBLE** | 0X H | ID_VER | IN_CTR | | | **OUT_CTR** | | | FB_CTR | | | MISCTR | | ~~STATUS0~~ | STATUS1 | ~~INTC TR~~ | ~~FBC_PAT~~ |
| | 1X H | INPUT WINDOW PARAMETERS | | | | | | | | | | | | | **IVH REF _DE LAY** | **IVS_ DEL AY** | |
| | 2X H | **AUTO ADJUST PARAMETERS** | | | | | | | | | | | | | | | |
| | 3X H | OUTPUT WINDOW PARAMETERS | | | | | | | | | | | | | | | |
| | 4X H | BACKGROUND WINDOW PARAMETERS | | | | | | | **DE DIM WINDOW PARAMETERS** | | | | | | | | |
| | 5X H | | | | | | | OSD PARAMETERS | | | | | | | | | |
| | 6X H | **SCALING PARAMETERS** | | | | | | | | | | | | | | | |
| | 7X H | **SCALING PARAME-TERS** | | | | **AUTO ADJUST PARAMETERS** | | | | | **PW M** | MISC (CLAMP) | | **IHV_DELAY4WRAP** | | | |
| | 8X H | AUTO ADJUST PARAMETERS | | | | | | | | | | | | | | | |
| | 9X H | AUTO ADJUST PARAMETERS | | | | | | | AUTO ADJUST PARAMETERS | | | | | | | | |
| | AX H | AUTO ADJUST PARAMETERS | | | | | | | | | **PX_ AS_ ALI NE** | AUTO ADJUST PARAMETERS | | | | **BRIGHT-NESS, CON-TRAST** | |
| | BX H | **BRIGHTNESS, CONTRAST, GAMMA, CLUT, and ALPHA BLENDING** | | | | | | | | | | PLL PARAMETERS | | | | | |
| | CX H | | | OSD freq | | | | | | | | OSD PARAMETERS | | | | | |
| | DX H | **HARDWARE MODE DETECTOR PARAMETERS** | | | | | | | | | | | | | | | |
| | EX H | | | | | | | | | | | | | | | | |
| | FX H | | | | | | | | | | | | | | | | |

**TABLE 14. I/O CONTROL REGISTER**

| REGISTER FUNCTION | Addr (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Chip ID and Version (ID_VER) | 00H | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| Input Control Register0 (INCTR0) | 01H | DIS_IHSPOL | IHS_POL | **IRGB24AB** | DEINTERLACE_ON | DE_ONLY | **DE_DELAY(2)** | **DE_DELAY(1)** | **DE_DELAY(0)** |
| Input Control Register1 (INCTR1) | 02H | ICLK_INV | ODD_POL | INCODE | YUVF | IRGB48(1) | IRGB48(0) | IRGB24 | IRGBEN |
| Output Control Register0 (OUTCTR0) | 03H | **RELD_FHADR** | DITHER_ON (1) | DITHER_ON (0) | PCLK_INV/ PHCLK_INV | PCLK_OP (1) | PCLK_OP (0) | PDE_POL | PRGB48 |
| Output Control Register1 (OUTCTR1) | 04H | PVS_POL | PHS_POL | POUT_OFF | BKFRC | BKCOL (3) | BKCOL (2) | BKCOL (1) | BKCOL (0) |
| **Output Control Register2 (OUTCTR2)** | 05H | | | | **PCLKIN_EXT** | **OVS_VACTIVE** | **DITHER_FDBK_ON** | | **PABCLK_EN** |
| OSD control register0 (OSDCTR0) | CEH | VITORENDL | VINT | TEST0 | ETF | R | G | B | I |
| OSD control register1 (OSDCTR1) | CFH | SPLIT | HTONE | MONITOR | HP | VP | BP | BF | IODS_EN |
| FBC control register0 (FBCTR0) | 07H | FILL_PAT | LMR_REQ | IFIFO_COF (1) | IFIFO_COF (0) | FBDB | RAMOD (2) | RAMOD (1) | RAMOD (0) |
| FBC control register1 (FBCTR1) | 08H | | REF_CYC (2) | REF_CYC (1) | REF_CYC (0) | REF_RASL (3) | REF_RASL (2) | REF_RASL (1) | REF_RASL (0) |
| FBC control register2 (FBCTR2) | 09H | | | MCLKPH (3) | MCLKPH (2) | MCLKPH (1) | MCLKPH (0) | ACKPH (1) | ACKPH (0) |
| Misc. Control Register 0 (MISCTR0) | 0AH | GAMMAUSE | CREF_INV | VHSYN_SEL | FREEZE | EOSD_EN | EOSDFR | BYPASS | **DE_DIM_EN** |
| Misc. Control Register 1 (MISCTR1) | 0BH | AACMP(1) | AACMP(0) | **DITHER_RNG(1)** | **DITHER_RNG(0)** | EOSD_SYNSEL | CLAMP_OFF | **BACLK_SEL** ~~ADCLKEN~~ | IIC_ACT_DIRECT |
| Status Register (STATUS0)/READ | 0CH | | | | ~~OFUDF~~ | ~~IFOVF~~ | ~~LBUDF~~ | ~~LBOVF~~ | ~~IRQ~~ |
| Status Register (STATUS1) | 0DH | | | | | **AXL_RDY** | **AFREEZE_RDY** | **ASOD_RDY** | **AML_RDY** |
| Interrupt Control Register (INTCTR) | 0EH | INTEN | | | ~~OFUDFEN~~ | ~~IFOVFEN~~ | ~~LBUDFEN~~ | ~~LBOVFEN~~ | ~~IRQEN~~ |
| ~~FBC test pattern (FBC_PAT)~~ | ~~0FH~~ | ~~MPAT_R2~~ | ~~MPAT_R1~~ | ~~MPAT_R0~~ | ~~MPAT_G2~~ | ~~MPAT_G1~~ | ~~MPAT_G0~~ | ~~MPAT_B1~~ | ~~MPAT_B0~~ |

| REGISTER FUNCTION | Addr (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| SOD Control Register (SODCTR) | 77H | SOD_FRAME_NO[3:0] | | | | | | | SOD_INTRA |
| SOD Mask Register (SODMASK) | 78H | SOD_MASK_BIT[2:0] | | | | | SOD_R_MASK | SOD_G_MASK | SOD_B_MASK |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| INPUT WINDOW PARAMETER | | hex | | |
| Input Horizontal Active Start(IH_ASTART[10:0]) | 11, 10 | 01,28 | W | This value should be at least larger than six. |
| Input Horizontal Active Width (IH_AWIDTH[10:0]) | 13, 12 | 04,00 | W | All default values are setting for 1024*768@60Hz |
| Input Hsync TOTAL (IH_TOTAL[10:0]) | 15,14 | 05,40 | W | |
| Input Vertical Active Start (IV_ASTART[10:0]) | 17,16 | 00,23 | W | |
| Input Vertical Active Width (IV_AWIDTH[10:0]) | 19,18 | 03,00 | W | |
| Input Vsync TOTAL (IV_TOTAL[10:0]) | 1B,1A | 03,26 | W | |
| Input Hsync Pulse Width (IH_PULW[7:0]) | 1C | 44 | W | This register specifies the pulse width of the input Hsync. Within this region the input video data are forced to zero by the internal circuit. The max. allowed value is 255 (in the unit of iclk). |
| **Input VREF and HREF Delay (IVHREF_DELAY[7:0])** | 1D | 00 | W | The H and V delay for YUV input.<br>The MSB 4-bit is defined as VREF_DELAY[3:0] and the LSB 4-bit is HREF_DELAY[3:0]. By programming this byte, the display of video YUV signals have VREF_DELAY*2 lines and HREF_DELAY*4 pixels offsets in V and H respectively. In a word, the unit of VREF delay is 2*H-line and the unit of HREF delay is 4 pixels (or 6.75MHz). For VREF delay, VREF_DELAY=00 (default) means no delay. For HREF delay, HREF_DELAY=00 (default) means no delay. |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| **Input VS Delay (IVS_DELAY[3:0])** | 1E | 00 | W | The input VS delay.<br>The LSB 4-bit is used. By programming these bits, the input VS signal will be delayed by IVS_DELAY*16 or IVS_DELAY*32 pixels (depends on IRGB24=1 or 0, see INCTR1 at register 02H). IVS_DELAY=00 (default) means no delay. |
| **Input Vsync Delay for Wrap Around (IV_DELAY4WRAP[10:0])** | 7D,7C | 00,02 | W | The V delay for VGA input.<br>The value 2 (default) means no delay and 3 means one H line delay, and so on (0 and 1 are not allowed.) |
| **Input Hsync Delay for Wrap Around (IH_DELAY4WRAP[10:0])** | 7F,7E | 00,01 | W | The H delay for VGA input.<br>The value 1 (default) means no delay and 2 means one pixel delay, and so on (0 is not allowed.) |
| OUTPUT WINDOW PARAMETER | | | | |
| Panel Horizontal Active Start (PH_ASTART[10:0]) | 31,30 | 01,28 | W | Please refer to the figure of Output Window |
| Panel Horizontal Active Width(PH_AWIDTH[10:0]) | 33,32 | 04,00 | W | |
| Panel Vertical Active EVEN Start (PV_ASTART_EVEN[10:0]) | 35,34 | 00,23 | W | This 10-bit register defines the Panel Vertical Active Start for non-interlaced video or the Even Field Active Start for interlaced video. |
| Panel Vertical Active Width (PV_AWIDTH[10:0]) | 37,36 | 03,00 | W | |
| Panel Vsync EVEN TOTAL (PV_TOTAL_EVEN[10:0]) | 39,38 | 03,26 | W | This 10-bit register defines the Panel Vertical Active Total Lines for non-interlaced video or the Even Field Active Total Lines for interlaced video. |
| Panel Hsync Pulse Width (PH_PULW[7:0]) | 3A | 88 | W | |
| Panel Vsync Pulse Width (PV_PULW[7:0]) | 3B | 06 | W | |
| Panel Vertical Active ODD Start (PV_ASTART_ODD[10:0]) | 3D,3C | | W | This register defines the Odd Field Active Start for interlaced video. |
| Panel Vsync ODD TOTAL (PV_TOTAL_ODD[10:0]) | 3F,3E | | W | This register defines the Odd Field Active Total Lines for interlaced video. |
| BACKGROUND AND DE DIM WINDOW PARAMETER | | | | |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| Background Horizontal Start (BH_START[10:0]) | 41,40 | 01,28 | W | Please refer to the figure of Output Window<br>ALL default values are setting for 1024*768@60Hz |
| Background Horizontal End (BH_END[10:0]) | 43,42 | 05,28 | W | |
| Background Vertical Start (BV_START[10:0]) | 45,44 | 00,23 | W | |
| Background Vertical END (BV_END[10:0]) | 47,46 | 03,23 | W | |
| **DE_DIM Horizontal Start (DMH_START[10:0])** | **49.48** | **00.00** | **W** | This parameter is used if DE_DIM_EN is on.<br>The start and end points are counted from the H or V display active region. Please refer to the figure of Output Window<br>ALL default values are setting for 1024*768<br>**The MSB 4-bit of 4F,4E register will be used for the lightness control of DE dim function under the condition that DE_DIM_EN (Bit 0 of MISCTR1) is on.**<br>**DE_LIGHT[15:12] is used to adjust the contrast of the dim area.** |
| **DE_DIM Horizontal End (DMH_END[10:0])** | **4B.4A** | **04.00** | **W** | |
| **DE_DIM Vertical Start (DMV_START[10:0])** | **4D.4C** | **00.00** | **W** | |
| **DE_DIM Vertical END (DMV_END[10:0])**<br>**DE_LIGHT[15:12]** | **4F.4E** | **03.00** | **W** | |
| OSC control register | | | | |
| OSD Font address [5:0] | 56 | 00 | W | Font RAM write address (auto increment). There are 51 address for the downloadable fonts |
| OSD FONT LSB [5:0] | 57 | 00 | W | Font LSB, each font is composed of 20x12 bits |
| OSD FONT MSB [11:6] | 58 | 00 | W | Font MSB |
| OSD attribute for FONT Code(OSD_AT[4:0]) | 59 | 00 | W | Attribute for Font code |
| OSD FONT code address(OSD_DT[7:0]) | 5A | 00 | W | Font code |
| OSD Display RAM address LSB(0~255) (OSD_ADL[7:0]) | 5B | 00 | W | Display RAM, low address range (0-255) |
| OSD Display RAM address MSB(256-511) (OSD_ADM[7:0]) | 5C | 00 | W | Display RAM, high address range (256-511) |
| OSD freq | C2 | 00 | W | 3 (LSB) bits for dot rate selection |
| OSD default setting for back-ground color (OSD_SPDEF[3:0]) | CA | 00 | W | |
| OSD first display ROW(OSD_SROW[3:0]) | CB | 00 | W | |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| OSD Horizontal Start in Window(OSD_HPOS[6:0]) | CC | 7F | W | |
| OSD Vertical Start in Window(OSD_VPOS[5:0]) | CD | 3F | W | |
| OSD control register2 (OSD_CTRL2) | CE | 01 | W | please refer to more detailed description of CE and CF registers |
| OSD control register (OSD_CTRL) | CF | 1C | W | |
| SCALING PARAMETER | | | | |
| Emulated PH period by ICLK (SPH_EMU[11:0]) | 61,60 | 05,40 | W | The period of panel HS counted by the input clock ICLK. This value can be calculated by input H_TOTAL/Vsf where VSf is the vertical scaling factor. |
| Emulated IH period by PCLK (SIH_EMU[11:0]) | 63,62 | 05,40 | W | The period of input HS counted by the panel clock PCLK. This value can be calculated by output H_TOTAL*Vsf where VSf is the vertical scaling factor.<br>Note that PCLK can be 2 time fast of PHCLK if PRGB48 = 1 (Please refer to OUTCTR0) |
| Course/Fine tune Delay between input data and display data in pixel number<br>SVdelay[1:0], SHdelay[10:0] | 65,64 | 18,f4 | W | The values 18 and F4 are recommended for all modes |
| SHdx[6:0],SHdy[6:0],SHhinc[4:0] | 66,67, 68 | 01,00, 10 | W | SHhinc= floor(16/Hsf), Hdy/Hdx= 16/Hsf - SHhinc. Note that we should set SHdx[6:0]=01, SHdy[6:0]=00, and SHhinc[3:0]=10 for scaling down operation.<br>NOTE: SHhinc= floor(8/Hsf), Hdy/Hdx= 8/Hsf - SHhinc[3:0]. (IN PROTOTYPE VERSION ONLY) |
| SVdx[5:0],SVdy[5:0],SVhinc[4:0] | 69,6A, 6B | 01,00, 10 | W | SVhinc= floor(16/Vsf), Vdy/Vdx= 16/Vsf - SVhinc. These parameters are used for both scaling up and down.<br>NOTE: SVhinc= floor(8/Vsf), Vdy/Vdx= 8/Vsf - SVhinc[3:0]. (IN PROTOTYPE VERSION ONLY) |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| SAHdx[6:0], SAHdy[6:0], **SDnAHhinc[7:0]** | 6C,6D ,6E | 01,00, 08 | W | AHhinc= floor(8*Hsf), AHdy/AHdx= 8*Hsf - AHhinc. **The MSB 2-bit of SDnAHhinc is defined as SALGO for scaling algorithm selection, where** **SALGO = 0 chooses BCubic (default).** **SALGO = 1 selects BH SINC.** **SALGO = 2 selects TC SINC.** **SALGO = 3 chooses BLinear interpolation.** **The algorithms in the order of sharpness to smoothness are TC SINC, BCubic, BH SINC, and BLinear.** **The 3rd and 4th MSB bits of SDnAHhinc, H_SD_ON and V_SD_ON, are used for enabling H and V scaledown operations, i.e.** **SD_ON=0 (default) for scaling up.** **SD_ON=1 for scaling down.** |
| Vertical Nume(SV_NUME[**5:0**]) | 6F | 01 | W | Vnume/Vdeno = Vsf (scaling factor in V direction) |
| Vertical Deno(SV_DENO[**5:0**]) | 70 | 01 | W | Vnume/Vdeno = Vsf (scaling factor in V direction) |
| **SDNHdx[6:0],SDNHdy[6:0],SDNHhinc[3:0]** | ~~71,72,~~ **73** | 01,00, 08 | W | For scaling down, SDNHhinc= floor(8/Hsf), SDNHdy/SDNHdx= 8/Hsf - SDNHhinc. Note that we should set SHdx[6:0]=01, SHdy[6:0]=00, and SHhinc[3:0]=10 for scaling down operation. Also note that SDNHdx[6:0]=01, SDNHdy[6:0]=00, and SDNHhinc[3:0]=08 should be set for scaling up operation. |
| MISC | | | | |
| **PWM[7:0]** | 79 | 00 | W | The PWM (pulse width modulated) signal is used for backlight control.The default value 00 means a low output while the value ff (hex) can be integrated by a capacitor for an almost high signal. |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| Clamp pulse starting setting register (CLAMP_STA) | 7A | 8A | W | The starting point of clamp pulse setting. Counted from the falling edge of sync pulse by IACLK. |
| Clamp pulse width setting register (CLAMP_WIDTH) | 7B | 80 | W | The width of clamp pulse by IACLK (1.2us is suggested) |
| AUTO Adjust Register | | | | Please refer to AACMP(1:0), which are bit 7 and 6 of MISCTR1, for functions apply to R or G or B |
| **The 1st line of the window for SOD calculation (AWVSTART[10:0])** | 21,20 | 00,00 | W | Define the range of intra-frame SOD operation. |
| **The last line of the window for SOD calculation (AWVEND[10:0])** | 23,22 | 00,00 | W | |
| **The 1st pixel of the window for SOD calculation (AWH-START[11:0])** | 25,24 | 00,00 | W | |
| **The last pixel of the window for SOD calculation (AWHEND[11:0])** | 27,26 | 00,00 | W | |
| **The resulting value of the sum of the SOD calculation (ASUM[31:0])** | 2B,2A ,29,28 | 00,00 | R | Check the status (ASOD_RDY of STATUS1, ready or not) before reading the results of inter-frame SOD operation.<br>Note that the results of both sum of difference and sum are simultaneously available. |
| **The resulting value of sum of difference of the SOD calculation (ASOD[31:0])** | 2F,2E ,2D,2C | 00,00 | R | |
| **The resulting value of the sum of the SOD calculation of boundaries (ABDSUM[23:0])** | 76,75, 74 | 00,00 | R | Check the status (AML_RDY of STATUS1, ready or not) before reading the results of this operation. |
| **SOD Control Register (SODCTR[7:0])** | 77 | 00 | W | The MSB 4 bit of SODCTR[7:0], SOD_FRAME_NO[3:0], is used to designate the number of frames involved in the inter-frame SOD operations. The actual number of frame is SOD_FRAME_NO + 1, e.g. SOD_FRAME_NO=0 means only one frame is involved. And SOD_FRAME_NO=0f (hex) means 16 frames are involved.<br>The LSB of SODCTR[7:0], SOD_INTRA, is used to select the intra-frame SOD operation as<br>0: sum,<br>1: SOD (sum of difference). |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| **SOD Mask Register(SOD-MASK[7:0])** | 78 | 00 | W | The MSB 3 bit of SODMASK[7:0], SOD_MASK_BIT[2:0], is used to select the number of MSB bits for SOD operation. There are five possibilities. If SOD_MASK_BIT=000, all bits are calculated. If SOD_MASK_BIT=001, the LSB 1 bit is not cared. While if SOD_MASK_BIT=1xx, the LSB 4 bits are not cared.<br>The LSB 3 bit of SODMASK[7:0], SOD_R_MASK, SOD_G_MASK, and SOD_B_MASK, are used to select the color channels for SOD operation, e.g. if SOD_R_MASK=1, the RED channel is not involved in the calculation. The default state is all channels are calculated. |
| Maximum Threshold (ARGB_MAX[7:0]) | 80 | 7F | W | Designate the threshold value for either R, G, or B |
| Minimum Threshold (ARGB_MIN[7:0]) | 81 | 00 | W | Designate the threshold value for either R, G, or B |
| Freeze line address(AFZLADDR[10:0]) | 83,82 | 00,00 | W | Designate the line to be frozen and read by host. The line number is counted from V active region. |
| Freeze line pixel start address(AFZHSTART[10:0]) | 85,84 | 00,00 | W | Designate the line to be frozen and read by host. The pixel number is counted from H active region.<br>Please refer to the MSB of OUTCTR0 register 03 Hex |
| Freeze line read address (AFZREAD[7:0]) | 86 | 00 | R | After the registers AFZLADDR and AFZHSTART are designated, this register can be read sequentially for the content of frozen line buffer. |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| The Mth line chosen to check the horizontal start & end (AML-NUM[10:0]) | 89,88 | 00,00 | R/W | Designated by host, the auto adjust function searches (horizontally) the starting and ending pixels along the Mth line. **If 00 are programmed, the entire screen is covered for H_start and H_end points searching. After the AMLNUM=00 searching, this address will be filled with the line number of the line of the maximum length. (If there are more than one, the 1st line will be recorded.) In a word, AMLNUM=00 searching will require the writing to this address for every operation.** |
| The 1st line exceeds ARGB_MIN (AVSTART[10:0]) | 8B,8A | 00,00 | R | |
| The last line exceeds ARGB_MIN (AVEND[10:0]) | 8D,8C | 00,00 | R | |
| The 1st pixel exceeds ARGB_MIN position at Mth line (AMLH-STA[10:0]) | 8F,8E | 00,00 | R | |
| The last pixel of the Mth line exceeds ARGB_MIN position (AML-HEND[10:0]) | 91,90 | 00,00 | R | If SOD_INTRA = 1 (SOD, sum of difference), the number read should minus one. |
| the RGB value of the 1st pixel of the Mth line that exceeds ARGB_MIN (AMLHSTAR[7:0],AMLH-STAG[7:0],AMLHSTAB[7:0]) | 92,93, 94 | 00,00, 00 | R | If SOD_INTRA = 1 (SOD, sum of difference), the values are not available. |
| the RGB value of the last pixel of the Mth line that exceeds ARGB_MIN (AMLHENDR[7:0],AML-HENDG[7:0],AMLHENDB[7:0]) | 95,96, 97 | 00,00, 00 | R | If SOD_INTRA = 1 (SOD, sum of difference), the values are not available. |
| Xth Line number (AXNUM[10:0]) for low-high-low or high-low-high searching | 99,98 | 00,00 | W | |
| pixel 0 position (AXPNUM0[10:0]) | 9B, 9A | 00,00 | R | The 1st pixel of low-high-low or high-low-high (please refer to figures of low-high-low or high-low-high search-ing) |
| pixel 1 position (AXPNUM1[10:0]) | 9D, 9C | 00,00 | R | The 2nd pixel of low-high-low or high-low-high |
| pixel 2 position (AXPNUM2[10:0]) | 9F,9E | 00,00 | R | The 3rd pixel of low-high-low or high-low-high |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| pixel 0 RGB value (AXP0R[7:0],AXP0G[7:0],AXP0B[7:0]) | A0,A1,A2 | 00,00,00 | R | If SOD_INTRA = 1 (SOD, sum of difference), the values are not available. |
| pixel 1 RGB value (AXP1R[7:0],AXP1G[7:0],AXP1B[7:0]) | A3,A4,A5 | 00,00,00 | R | If SOD_INTRA = 1 (SOD, sum of difference), the values are not available. |
| pixel 2 RGB value (AXP2R[7:0],AXP2G[7:0],AXP2B[7:0]) | A6,A7,A8 | 00,00,00 | R | If SOD_INTRA = 1 (SOD, sum of difference), the values are not available. |
| PX_AS_ALINE[3:0] | A9 | 06 | W | The threshold of number of pixels that will be treated as an active line. The LSB 4-bit will be used. The default number is at least 6 pixels will be treated as an active line. |
| H START point for AUTO ADJUST compare (AH_START[10:0]) | AB, AA | 00,10 | W | The leading edge of searching window (counted from the leading edge of sync pulse). The trailing edge is 2 pixels before the next sync pulse. The value AH_START should be at least larger than six. |
| An overflow had been detected on the Mth line (AML_OVERFLOW) (0: B channel, 1: G channel, 2: R channel, other bits are reserved) | AC | 00 | R | An overflow (ff in hex) of color value in R, G, or B has been detected on Mth line. |
| Brightness, Contrast, Gamma, CLUT, and ALPHA BLENDING | | | | |
| **RCONTRAST[7:0]** | AE | 00 | W | 256 level contrast control for R<br>The input signal is multiplied by a value ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0]. |
| **RBRIGHTNESS[7:0]** | AF | 00 | W | 256 level brightness control for R<br>7f ->127,..., 01 -> 1, 00 -> 0, ff -> -1,..., 80 -> -128<br>i.e. The input data is added by a 2's complement value. |
| **GCONTRAST[7:0]** | B0 | 00 | W | 256 level contrast control for G |
| **GBRIGHTNESS[7:0]** | B1 | 00 | W | 256 level brightness control for G |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| GAMMA table R write address(GRWADDR[7:0]) | B2 | 00 | W | Each gamma-correction table is a 256x10 LUT (look-up table) which can be updated by writing to these ports. Each entity is composed of high and low bytes which share the same write address. Low byte content is written followed by the high byte content.<br>Lower entity data are sent to a certain channel (e.g. R or G or B) followed by the next higher entity. In a word, R channel is updated by sending data for entity 0, 1, till the final one entity 255. Then channel G followed by channel B. |
| GAMMA table G write address(GGWADDR[7:0]) | B3 | 00 | W | |
| GAMMA table B write address(GBWADDR[7:0])<br>(The table write address will be auto increased upon each writing) | B4 | 00 | W | |
| CLUT write address (CLUT-WADDR[7:0]) | B5 | 00 | W | This 16x16 Color LUT can be written by host from this port. First the lower byte data are sent to an entity, then followed by the higher byte data, color index 0 is filled followed by color index 1 until color index 15, the final one.<br>The 16-bit output of this color LUT will be interpreted as the RGB565 format, i.e. the MSB 5 bits are for R, the middle 6 bits for G, and the LSB 5 bits for B. |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| CLUT alpha blending (CLUT_ALPHA[3:0]) | B6 | 00 | W | The MSB of CLUT_ALPHA is used indirectly for the interpretation of the I signal of OSD, while CLUT_ALPHA[2:0] is used to select the blending factor between the output of the CLUT and the output of the dithered video.<br>CLUT_ALPHA[3]=<br>0: The content of CLUT is RGB565.<br>1: The content of CLUT is RGB555. And the LSB of G will be interpreted as<br>LSB of G of CLUT read out<br>=0: means alpha_blending off.<br>=1: means alpha_blending on.<br>If alpha_blending is on and any one of the internal/external OSD/background color is activated, the final video of panel out will be equal to Video*CLUT_ALPHA[2:0]/8+CLUT*(1-CLUT_ALPHA[2:0]/8). For the case that CLUT_ALPHA[2:0]=0, the final video of panel is directly from the output of CLUT. And for CLUT_ALPHA[2:0]=7, the final video is Video*7/8+CLUT*1/8. |
| **BCONTRAST[7:0]** | B7 | 00 | W | 256 level contrast control for B<br>The input signal is multiplied by a value ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0]. |
| **BBRIGHTNESS[7:0]** | B8 | 00 | W | 256 level brightness control for B<br>7f ->127,..., 01 -> 1, 00 -> 0, ff -> -1,..., 80 -> -128<br>i.e. The input data is added by a 2's complement value. |
| PLL program parameter | | | | |
| PLLPSET0<br>FI(7 downto 0) | BA | F2 | W | F7(MSB), F6, F5, F4, F3, F2, F1, F0 (LSB)<br>The 8 LSB of feedback 9-bit divider<br>The default value will set the PCLK to 65/2 MHz |

**TABLE 15.**

| REGISTER FUNCTION | ADDR (HEX) MSB:ODD LSB:EVEN | RESET VALUE | R/W | Description |
|---|---|---|---|---|
| PLLPSET1<br>FI(8) & ODI(1 downto 0) & RI(4 downto 0) | BB | 57 | W | F8(MSB), OD1, OD0, R4, R3, R2, R1, R0 (LSB)<br>F8 is the MSB of feedback 9-bit divider, OD0 (MSB) and OD1 (LSB) are the control pins for output divider, and R4 to R0 are the pins for input 5-bit divider |
| PLLCNTL<br>Output enable and bypass control for Pclk ~~and Mclk~~ PLL.<br>~~LSB is for IBCLK or IACLK selection~~ | BE | 00 | W | POE(MSB), PBP, xx, xx, ~~MOE, MBP, xx, BACLK_SEL (LSB)~~<br>where POE is the freq Output Enable of Pclk PLL (default 0), PBP is the ByPass control of Pclk PLL (default 0), ~~and MOE/MBP are for Mclk PLL, xx is do not care.~~<br>PLL will go to power down mode as the external POWERDN pin activated.<br>~~bit 0: BACLK_SEL is for IBCLK or IACLK selection.~~<br>~~0: ICLK = IBCLK/2 (for LLC2)~~<br>~~1: ICLK = IACLK~~<br>The control of BACLK_SEL is now moved to Bit 1 of MISCTR1. |

| ID_VER (Chip ID and Version, 00H) | | | Default |
|---|---|---|---|
| 7-0 | ID_VER | 10110010 (bin) | B2 |

| INCTR0(INput ConTrol Register 0, 01H) | | | Default |
|---|---|---|---|
| 7 | DIS_IHSPOL | 0: Auto detecting function of the polarity of HS of input video will be checked automatically<br>1: Auto detecting function of the polarity of HS of input video will be disabled<br>Note: The polarity of VS of input video will be checked automatically | 0 |
| 6 | IHS_POL | 0: The rising edge of input HS will be used as the start of the sync pulse<br>1: The falling edge of input HS will be used as the start of the sync pulse | 0 |
| 5 | **~~IRGB24A~~ B** | 0: Input RGB 24-bit data use A port<br>1: Input RGB 24-bit data use B port | 0 |
| 4 | DEINTERLACE_ON | 0: Deinterlace function off<br>1: Deinterlace function on<br>Note: Panel Vertical Active EVEN Start, Panel Vertical Active ODD Start, Panel Vertical EVEN Total, and Panel Vertical ODD Total should be defined before Deinterlace function set to on | 0 |
| 3 | **DE_ON** | 0: The H and V sync signals are used for synchronizing the display data.<br>1: The DE (Display Enable) signal is used for synchronizing the display data. | 0 |

| INCTR0(INput ConTrol Register 0, 01H) | | | Default |
|---|---|---|---|
| 2-0 | **DE_DELAY[2:0]** | DE signal can be delayed or advanced for the matching of display data vs. enable signal. This signal is valid only if DE_ON=1.<br>0xx: No delay (x means do not care)<br>100: -2 clock delay.<br>101: -1 clock delay.<br>110: +1 clock delay.<br>111: +2 clock delay. | 000 |
| | | | |

**TABLE 16.**

| INCTR1(INput ConTrol Register 1, 02H) | | | Default |
|---|---|---|---|
| 7 | INCLK_INV | INCLK invert enable<br>0: normal input clock<br>1: invert input clock | 0 |
| 6 | ODD_POL | ODD indicate polarity (inside use only)<br>0: 1st field is ODD and ODD is ACTIVE HIGH<br>1: 1st field is ODD and ODD is ACTIVE LOW | 0 |
| 5 | INCODE | 0: input video code is binary offset<br>1: input video code is 2 complement | 0 |
| 4 | YUVF | 0: 16 bit YUV422<br>1: 8 bit YUV422 (CCIR 656) | 0 |
| 3:2 | IRGB48(1:0) | 00: RGB48 input no offset AB<br>01: RGB48 input no offset BA<br>10: RGB48 input offset AB<br>11: RGB48 input offset BA (See the attached graphic explanation) | 00 |
| 1 | IRGB24 | 0: RGB 48 bits input<br>1: RGB 24 bits input | 0 |
| 0 | IRGBEN | 0: YUV input<br>1: RGB input | 1 |
| | | | |

**TABLE 17.**

| OUTCTR0(Output ConTrol Register 0, 03H) | | | Default |
|---|---|---|---|
| 7 | RELD_FHADR | Reload Freeze Address<br>The starting address of frozen line which will be reloaded if a low to high transient detected. Please refer to the register 84 and 85 for more detail. | 0 |
| 6:5 | DITHER_ON(1:0) | 00: no dithering (for the panel with 8 bit color depth per R/G/B)<br>01: 1 bit dithering (for the panel with 7 bit color depth per R/G/B)<br>10: 2 bit dithering (for the panel with 6 bit color depth per R/G/B)<br>11: 4 bit dithering | 00 |
| 4 | PHCLK_INV | 0: Normal PHCLK clock output to panel<br>1: Inverted PHCLK clock output to panel<br>(The relationship of PHCLK and PCLK is also defined by PHCLK_OP(1:0) and PRGB48) | 1 |

**TABLE 17.**

| OUTCTR0(Output ConTrol Register 0, 03H) | | | Default |
|---|---|---|---|
| 3:2 | PHCLK_OP(1:0) | Phase deviation of PHCLK with respect to PCLK<br>00: No delay 10: Delay 2 unit<br>01: Delay 1 unit 11: Delay 3 unit<br>(The relationship of PHCLK and PCLK is also defined by PHCLK_INV and PRGB48. This control of delay and inversion applies to both PACLK and PBCLK.) | 00 |
| 1 | PDE_POL | 0: active High display data enable output to panel<br>1: active Low display data enable output to panel | 0 |
| 0 | PRGB48 | 0: Single pixel output per panel clock (the frequency of PHCLK is equal to PCLK, the phase is defined by PHCLK_INV and PHCLK_OP(1:0))<br>1: Double pixel output per panel clock (the frequency of PHCLK is equal to half of PCLK, the phase is defined by PHCLK_INV and PHCLK_OP(1:0)) | 1 |

**TABLE 18.**

| OUTCTR1 (OUTput ConTrol Register 1, 04H) | | | |
|---|---|---|---|
| 7 | PVS_POL | PVS output polarity (inside use active High)<br>0: Negative polarity (active Low)<br>1: Positive polarity (active High) | 0 |
| 6 | PHS_POL | PHS output polarity (inside use active High)<br>0: Negative polarity (active Low)<br>1: Positive polarity (active High) | 0 |
| 5 | POUT_OFF | Panel output control & data disable<br>0: PHS, PVS,DEN,DAR,DAG,DAB,DBR,DBG,DBB output are enabled<br>1: PHS, PVS,DEN,DAR,DAG,DAB,DBR,DBG,DBB output are set to zero | 0 |
| 4 | BKFRC | Panel output Force to Background color<br>0: Normal Panel output<br>1: Output Panel is forced to Background color, the color is selected by BKCOL[3:0] | 0 |
| 3:0 | BKCOL[3:0] | Panel output Background color select signals.<br>These signals share the look-up table with OSD to generate colors. | 00<br>0 |

**TABLE 19.**

| OUTCTR2 (OUTput ConTrol Register 1, 05H) | | | |
|---|---|---|---|
| 7-5 | reserved | | |
| 4 | **PCLKIN_EXT** | The way PCLK, panel clock, is generated.<br>0: PCLK is generated by internal PLL.<br>1: PCLK is fed from PCLKIN pin (by external source). | 0 |
| 3 | **OVS_VACTIVE** | The OSD VS output is generated using<br>0: Overlay VS as in Zurac1.<br>1: Vertical display active signal. | 0 |
| 2 | **DITHER_FDBK_ON** | The error due to resolution change is fed back for dithering<br>0: feedback path is disconnected.<br>1: feedback path is connected for dithering. | 0 |

**TABLE 19.**

| **OUTCTR2 (OUTput ConTrol Register 1, 05H)** | | | |
|---|---|---|---|
| 1 | reserved | | |
| 0 | **PABCLK_ EN** | PACLK or PBCLK output pad will be enabled<br>0: PACLK, which has the drive capability of 8mA, is enabled. (PBCLK is disabled)<br>1: PBCLK, which has the drive capability of 16mA, is enabled. (PACLK is disabled) | 0 |

**TABLE 20.**

| **MISCTR0(Misc. ConTrol Register 0, 0AH)** | | | **Default** |
|---|---|---|---|
| 7 | GAM-MAUSE | Use GAMMA correction table for each R,G, and B.<br>0: Bypass the GAMMA table<br>1: Use the GAMMA look-up table | 0 |
| 6 | CREF_INV | CREF invert enable<br>0: Normal logic polarity (clock enable CREF=1)<br>1: inverted CREF (clock enable CREF=0) | 0 |
| 5 | VHSYN_SEL | Port A VS & HS synchronization edge<br>0: Use ACLK rising edge<br>1: Use ACLK falling edge | 0 |
| 4 | FREEZE | 0: Normal function<br>1: Freeze function | 0 |
| 3 | EOSD_EN | 0: External OSD will be disabled<br>1: External OSD will be enabled<br>(The internal OSD can be enabled by IOSD_EN in bit 0 of OSDCTR1 register) | 0 |
| 2 | EOSDFR | In case of EOSD_EN (bit 3) = 1,<br>0: Internal OSD will be put in front of external OSD<br>1: External OSD will be put in front of internal OSD | 0 |
| 1 | BYPASS | 0: **(Default)** Panel VS and HS are free running and act as the sync master.<br>1: In this mode, the input and output frames are synchronized. In a sense, input VS and HS are the sync master that generate Panel VS and HS.<br><br>Note: In order to activate free-run mode, micro-controller should choose BYPASS = 0. To this, the input data can be ignored, if necessary, by setting BKFRC= 1 so background colors are sent to panel. | **0** |
| **0** | **DE_DIM_EN** | **Dim of an area (defined by DMH_START, DMH_END, DMV_START, and DMV_END) in the display is enabled if this bit is set** | **0** |

**TABLE 21.**

| MISCTR1(Misc. ConTrol Register 1, 0B hex) | | | Default |
|---|---|---|---|
| 7:6 | AACMP(1:0) | Choose R or G or B to compare. This setting is applicable to all Auto Adjust functions (please refer to AUTO Adjust registers for detail description).<br>00: reserved<br>01: compare R<br>10: compare G<br>11: compare B | 00 |
| **5:4** | **DITHER_RNG(1:0)** | **DITHER RNG ON and choices.**<br>**00: RNG off**<br>**01: RNG 10**<br>**10: RNG 12**<br>**11: RNG 16** | 00 |
| 3 | EOSD_SYNSEL | 0: EOSD data latch uses OVCLK<br>1: EOSD data latch uses the inverse of OVCLK | 0 |
| 2 | CLAMP_OFF | CLAMP pulse will be generated according to the register 7A and 7B (hex)<br>0: clamp pulse is sent out. 1: clamp pin is in tri-state | 0 |
| ~~1~~ | ~~ADCLKEN~~ | ~~0: Output clock ADCCLKP & ADCCLKN is disable. In this case, the input data are synchronized by IACLK and IBCLK input clocks~~<br>~~1: Output clock ADCCLKP & ADCCLKN is enable for the external double ADCs (ADCCLKP is IACLK divided by 2, while ADCCLKN is the inversed ADCCLKP)~~ | ~~0~~ |
| 1 | **BACLK_SEL** | BACLK_SEL is for IBCLK or IACLK selection.<br>0: ICLK = IBCLK/2 (for LLC2)<br>1: ICLK = IACLK | ~~1~~ |
| 0 | IIC_ACT_DIRECT | 0: 2-wire serial bus parameters are activated until next VS retrace period.<br>1: 2-wire serial bus parameters are activated upon data received | 1 |

**TABLE 22.**

| STATUS0 (Status Register 0, 0CH) | | | Default |
|---|---|---|---|
| ~~7-3~~ | ~~reserved~~ | | |
| ~~2~~ | ~~LBUDF~~ | ~~0: Normal~~<br>~~1: Line Buffer underflow.~~ | ~~0~~ |
| ~~1~~ | ~~LBOVF~~ | ~~0: Normal~~<br>~~1: Line Buffer overflow~~ | ~~0~~ |
| ~~0~~ | ~~IRQ~~ | ~~0: Normal~~<br>~~1: Internal Interrupt~~ | ~~0~~ |
| | | | |

| STATUS1 (Status Register 0, 0DH) | | | Default |
|---|---|---|---|
| 7-4 | reserved | | |
| 3 | AXL_RDY | For auto adjustment, by setting to 0, the Xth line function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit. | 1 |
| 2 | AFREEZE_RDY | For auto adjustment, this status bit will be set to 1 as the freeze function is completed.This is a RD only status bit. | ~~0~~ |

| STATUS1 (Status Register 0, 0DH) | | | Default |
|---|---|---|---|
| 1 | ASOD_RDY | For auto adjustment, by setting to 0, the SOD (sum or sum of difference) function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit. | 1 |
| 0 | AML_RDY | For auto adjustment, by setting to 0, the Mth line function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit. | 1 |

**TABLE 23.**

| INTCTR (Interrupt Control Register, 0EH) | | | Default |
|---|---|---|---|
| 7 | INTEN | 0: Disable all interrupt<br>1: Enable all interrupt | 1 |
| ~~6-3~~ | ~~reserved~~ | | |
| ~~2~~ | ~~LBUDFEN~~ | ~~0: Disable LBUDF interrupt~~<br>~~1: Enable LBUDF interrupt~~ | ~~0~~ |
| ~~1~~ | ~~LBOVFEN~~ | ~~0: Disable LBOVF interrupt~~<br>~~1: Enable LBOVF interrupt~~ | ~~0~~ |
| ~~0~~ | ~~IRQEN~~ | ~~0: Disable IRQ interrupt~~<br>~~1: Enable IRQ interrupt~~ | ~~0~~ |

Please refer to the register INTSRC (D1H, in the Section of Hardware Mode Detector) for the interrupt control and interrupt source identification.

# 7.0 Register Map Hardware Mode Detector

**TABLE 24. The register map of Hardware Mode Detector in Zurac II**

| Name: | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| HWDCNT (D0H) | Enhwd | SelDE | Hwd_inten | Vint_ren | Vint_fen | Vcnt-Sel | HVsep1 | HVsep0 |
| 83H | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| IntSrc (D1H) | - | - | Vint_R | Vint_F | VfChanged | Vpol-cha | HfChanged | Hpol-cha |
| 00H | - | - | R | R | R | R | R | R |
| SyncStatus (D2H) | - | Falt | FwHalf | Odd_Even | Vpres-ence | Hpres-ence | Vpolar-ity | Hpolar-ity |
| 00H | - | R | R | R | R | R | R | R |
| HperHigh (D3H) | Hper11 | Hper10 | Hper9 | Hper8 | Hper7 | Hper6 | Hper5 | Hper4 |
| 00H | R | R | R | R | R | R | R | R |
| VHperLow (D4H) | Vper3 | Vper2 | Vper1 | Vper0 | Hper3 | Hper2 | Hper1 | Hper0 |
| 00H | R | R | R | R | R | R | R | R |
| VperHigh (D5H) | Vper11 | Vper10 | Vper9 | Vper8 | Vper7 | Vper6 | Vper5 | Vper4 |

**TABLE 24. The register map of Hardware Mode Detector in Zurac II**

| Name: | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 00H | R | R | R | R | R | R | R | R |
| PulCnt (D6H) | EnVout | EnHout | VoutMode1 | VoutMode0 | HoutMode1 | HoutMode0 | Htolerance1 | Htolerance0 |
| C0H | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| HVPwth (D7H) | - | VPW3 | VPW2 | VPW1 | VPW0 | HPW2 | HPW1 | HPW0 |
| 43H | - | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| PoutPolPos (D8H) | **VCoast Delay1** | **VCoast Delay0** | Vshift3 | Vshift2 | Vshift1 | Vshift0 | Vout-Pol | Hout-Pol |
| 00H | -R/W | -R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| HfpHigh (D9H) | Hfp9 | Hfp8 | Hfp7 | Hfp6 | Hfp5 | Hfp4 | Hfp3 | Hfp2 |
| 4AH | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| HVfpLow (DAH) | - | - | Vfp3 | Vfp2 | Vfp1 | Vfp0 | Hfp1 | Hfp0 |
| 18H | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| VfpHigh (DBH) | Vfp11 | Vfp10 | Vfp9 | Vfp8 | Vfp7 | Vfp6 | Vfp5 | Vfp4 |
| 32H | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

## 7.1 HWDCNT (Hardware Mode Detector Control Register)

B1 - B0 (HVsep1 - HVsep0):

Multiplexer to select Vsync source:

00: Csync/DE + VsyncSep

01: Hsync + VsyncSep

10: Hsync + VsyncSep XOR Vsync

11: Hsync + Vsync

(if SelDE = 1, 00 is chosen, i.e. DE is treated as one kind of Csync)

B2 (VcntSel):

Select Vperiod count by time or by line number

0: By time; i.e. Vclk (Hclk/88)

1: By H line

B3 (Vint_fen):

Enable interrupt at Vsync trailing edge

0: Disabled

1: Enabled

B4 (Vint_ren):

Enable interrupt at Vsync leading edge

0: Disabled

1: Enabled

B5 (HWD_inten):

Enable interrupt from one of Sync signal changes: H/V frequency or Polarity change

0: Disabled

1: Enabled

B6 (SelDE):

Selection between DE and Csync input (DE and Csync are mutually exclusive)

(if SelDE = 1, HVsep is automatically set as 00)

0: Csync is selected

1: DE is selected

B7 (EnHWD):

Enable Hardware mode detector

0: Disabled; (clock is sleeping also to save power)

1: Enabled

## 7.2 IntSrc (Interrupt Source; NOTE: The flags in this register will be cleared automatically after read)

B0 (HpolCha):

Interrupt is caused by H polarity change

0: H polarity not changed

1: H polarity changed

B1 (HfChanged):

Interrupt is caused by H frequency change

0: H frequency not changed

1: H frequency changed

B2 (VpolCha):

Interrupt is caused by V polarity change

0: V polarity not changed

1: V polarity changed

B3 (VfChanged):

Interrupt is caused by V frequency change

0: V frequency not changed

1: V frequency changed

B4 (Vint_F):

Interrupt is caused by Vsync trailing edge

0: Vsync trailing edge not happened

1: Vsync trailing edge happened

B5 (Vint_R):

Interrupt is caused by Vsync leading edge

0: Vsync leading edge not happened

1: Vsync leading edge happened

## 7.3 SyncStatus (H/V sync signals status)

B0 (Hpolarity):

the polarity of Hsync

0: Positive polarity (Pulse width smaller than 1/4 of Hperiod)

1: Negative polarity (Pulse width larger than 3/4 of Hperiod)

B1 (Vpolarity):

the polarity of Vsync

0: Positive polarity (Pulse width smaller than 1/4 of Vperiod)

1: Negative polarity (Pulse width larger than 3/4 of Vperiod)

B2 (Hpresence):

the presence status of Hsync/Csync

0: Not present

1: Present

B3 (Vpresence):

the presence status of Vsync

0: Not present

1: Present

B4 (Odd_Even):

Indicate current field is Odd field or Even field

0: odd field/1st field; with earlier H sync

1: even field/2nd field; with lagged H sync

B5 (FwHalf):

Indicate whether Field contains n+1/2 lines (half line)

0: Not this format

1: Yes

B6 (Falt):

Indicate whether Field contains alternating n / n+1 lines

0: Not this format

1: Yes

## 7.4 HperHigh

B7 - B0 (Hperiod11 - Hperiod4):

The high nibble of Hperiod (11 - 0)

## 7.5 VHperLow

B3- B0 (Hperiod3 - Hperiod0):

The low nibble of Hperiod (11 - 0)

B7- B4 (Vperiod3 - Vperiod0):

The low nibble of Vperiod (11 - 0)

## 7.6 VperHigh

B7 - B0 (Vperiod11 - Vperiod4):

The high nibble of Vperiod (11 - 0); it is counted by clock (Hclk/88) or by H line, depending on VcntSel

## 7.7 PulCnt (H/V output pulse control register)

B1 - B0 (Htolerance1 - Htolerance0):

The definition of H/V frequency/count deviation is programmable:

00: +/- 4 counts

01: +/- 8 counts

10: +/- 16 counts

11: +/- 88 counts

B3 - B2 (HoutMode1 - HoutMode0):

00( FreeRun): the period of HsyncOut is programmed by 10-bit counter, Hfper. The pulse width is programmed by 3-bit register, HPW (0->0.28us, 1->0.59us, 2-> 1.12us, 3->1.40us, 4->1.68us, 5->1.96us, 6->2.23us, 7 ->2.51us)

01(Loopth_st): the HsyncOut will be snapped to the rising/falling edge of incoming Hsync; if the pulse of incoming Hsync is missing, an artificial pulse will be inserted with pulse width defined by HPW. The serration pulses are still kept as the incoming Hsync. The artificial pulse will be inserted after Hperiod/4 + 2 is counted (2 is the tolerance parameter)

10(R_aligned): the leading edge of the outputed Hsync is aligned with the incoming Hsync. However, the pulse width is defined by HPW. The pulse occurred in the midway of Hsync during serration period

is suppressed (Hperiod/8 - 8 is the threshold). An artificial pulse will be inserted while incoming pulse is missing

11(Loopth): completely copy the shape of the incoming Hsync

B5 - B4 (VoutMode1 - VoutMode0):

00(FreeRun): the period of VsyncOut is programmed by 12-bit counter, Vfper. The pulse width is programmed by 4 bit register, Vpw, extended to 6 bits (2, 4, 6, ... 28, 30, 32 lines; should be able to cover fly back period). The output waveform is certainly in phase with HsyncOut

01(Loopth_st): the leading edge of VsyncOut will be roughly close to the incoming Vsync, however, snapped to the leading edge of incoming HsyncOut; if the pulse of incoming Vsync is missing, an artificial pulse will be inserted with pulse width defined by VPW. The tailing edge of VsyncOut is also close to the tailing edge of the inputted Vsync but snapped to the leading edge of HsyncOut

10(R_aligned): the leading edge of VsyncOut will be shifted ahead or after the leading edge of Vsync based on the programmed value, however, snapped to the leading edge of incoming HsyncOut; if the pulse of incoming Vsync is missing, an artificial pulse will be inserted with pulse width defined by VPW. The pulse width in this mode is also programmable by VPW

11(Loopth): completely copy the shape of the incoming Vsync

B6 (EnHout):

Enable HsyncOut pulse

0: Disabled; HsyncOut is kept low

1: Enabled

B7 (EnVout):

Enable VsyncOut pulse

0: Disabled; VsyncOut is kept low

1: Enabled

## 7.8 HVPwth (The Pulse Width of H/V sync output)

B2 - B0 (Hpw2 - Hpw0):

The pulse width of Hsync Output:

000: 4(0.28us)

001: 8(0.59us)

010: 16(1.12us)

011: 20(1.40us)

100: 24(1.68us)

101: 28(1.96us)

110: 32(2.23us)

111: 36(2.51us)

B6 - B3 (Vpw3 - Vpw0):

There are 16 programmable values to set the pulse width of VsyncOut

2*(Vpw + 1) => 2, 4, 6, .... 30, 32 H lines

## 7.9 PoutPolPos (The polarity of H/V sync output and the position of VsyncOut)

B0 (HoutPol):

the polarity of HsyncOut

0: Positive polarity (Pulse width smaller than 1/4 of HsyncOut)

1: Negative polarity (Pulse width larger than 3/4 of HsyncOut)

B1 (VoutPol):

the polarity of VsyncOut

0: Positive polarity (Pulse width smaller than 1/4 of VsyncOut)

1: Negative polarity (Pulse width larger than 3/4 of VsyncOut)

B5 - B2 (Vshift3 - Vshift0):

Vshift(3) = 1 (Leading edge of VsyncOut ahead the incoming Vsync):

000: Ahead 1 H line

001: Ahead 2 H lines

010: Ahead 3 H lines

011: Ahead 4 H lines

100: Ahead 5 H lines

101: Ahead 6 H lines

110: Ahead 7 H lines

111: Ahead 8 H lines

Vshift(3) = 0 (Leading edge of VsyncOut after the incoming Vsync):

000: Kept at the same position as incoming Vsync

001: After 1 H line

010: After 2 H lines

011: After 3 H lines

100: After 4 H lines

101: After 5 H lines

110: After 6 H lines

111: After 7 H lines

**B7 - B6 ( VCoastDelay1 - VCoastDelay0)**

**When VsyncOut signal is going to scaler as a V sync signal internally, this signal is called VCoast. This control register will generate VCoastDelay by delaying the designated numbers of Hsync at the rising edge of the VsyncOut. The falling edge is almost the same as VsyncOut.**

**00 : VCoast is the same as VsyncOut**

**01 : VCoast rising edge is delayed by 1 Hsync from VsyncOut**

**10 : VCoast rising edge is delayed by 2 Hsync from VsyncOut**

**11 : VCoast rising edge is delayed by 3 Hsync from VsyncOut**

**Make sure the VsyncOut width is larger the number of Hsync delay, otherwise VCoast can not have a correct falling edge.**

## 7.10 HfpHigh

B7 - B0 (Hfperiod9 - Hfperiod2):

The high nibble of H free run period (9 - 0)

## 7.11 HVfpLow

B1- B0 (Hfperiod1 - Hfperiod0):

The low nibble of H free run period (9 - 0)

B5- B2 (Vfperiod3 - Vfperiod0):

The low nibble of V free run period (11 - 0)

## 7.12 VfpHigh

B7 - B0 (Vfperiod11 - Vfperiod4):

The high nibble of V free run period (11 - 0)

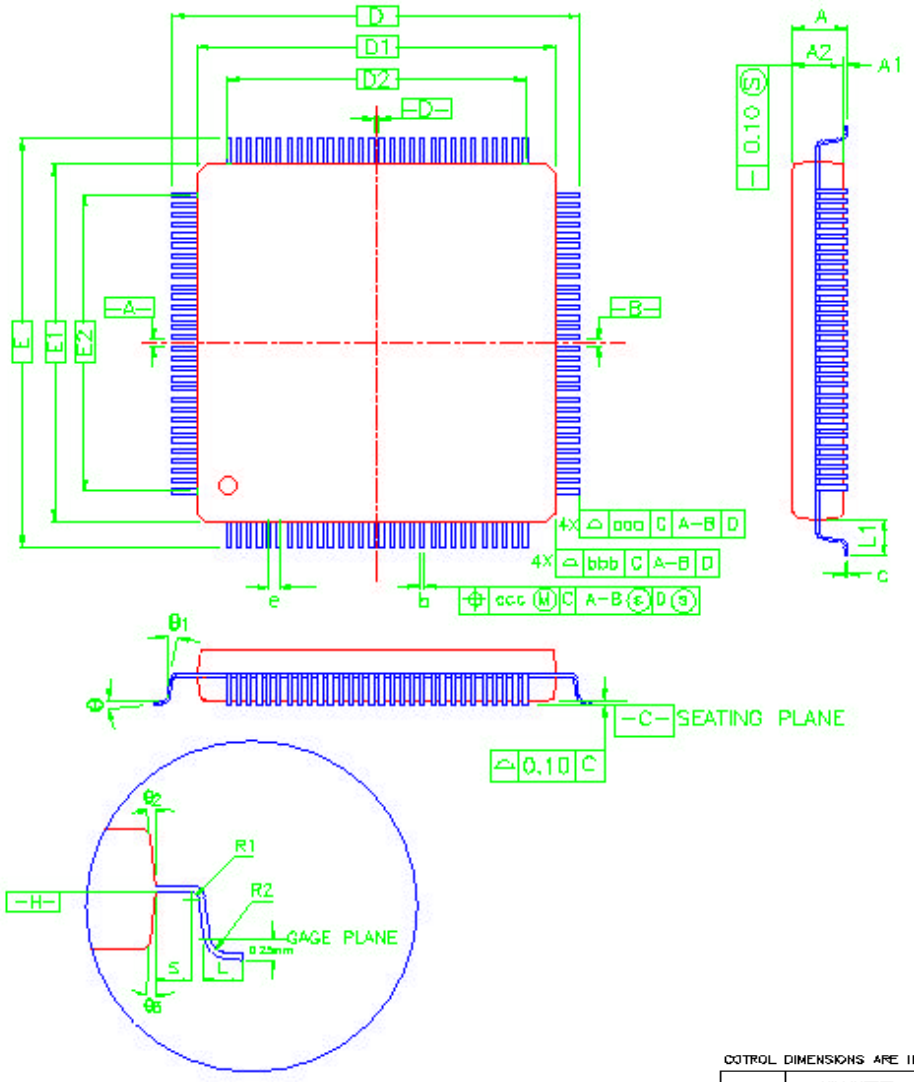
| **OSDCTR0(OSD control0, CEH)** | | | **Default** |
|---|---|---|---|
| 7 | VINTORENDL | if VINT = 1 then<br>0: pin I will send out a pulse upon vertical leading edge<br>1: pin I will send out a (active low) pulse when OSD is activated vertically | 0 |
| 6 | VINT | 0: normal mode pin I is color I,<br>1: pin I will be defined by VINTORENDL | 0 |
| 5 | TEST0 | test bit | 0 |
| 4 | ETF | 0: disable test font<br>1: enable test font | 0 |
| 3 | CLUT_R | Color index R for OSD or background color look-up table | 0 |
| 2 | CLUT_G | Color index G for OSD or background color look-up table | 0 |
| 1 | CLUT_B | Color index B for OSD or background color look-up table | 0 |
| 0 | CLUT_I | Color index I for OSD or background color look-up table | 1 |

**Note that the external OSD selection can be set by the bit 3 and 2 in the MISCTR0 (Misc. ConTrol Register 0, 0AH) register.**

**TABLE 25.**

| OSDCTR1(OSD control1, CFH) | | | Default |
|---|---|---|---|
| 7 | SPLIT | 0: SP (Space code) not spite<br>1: SP (Space code) spite | 0 |
| 6 | HTONE | 0: Half Tone effect not enable in BOXING mode<br>1: Half Tone effect enable in BOXING mode | 0 |
| 5 | MONITOR | 0: TV mode (Video background not overlaid)<br>1: Monitor mode (Non-OSD part overlaid by preset background color) | 0 |
| 4 | OSD_H_NEG | 0: positive polarity for HS<br>1: negative polarity for HS | 0 |
| 3 | OSD_V_NEG | 0: positive polarity for VS<br>1: negative polarity for VS | 0 |
| 2 | OSD_RGBI_NEG | 0: positive polarity for RGBI<br>1: negative polarity for RGBI | 1 |
| 1 | OSD_BLINK | 0: Blinking rate, displaying or not displaying toggled per 32 Vsync pulse<br>1: Blinking rate, displaying or not displaying toggled per 64 Vsync pulse | 0 |
| 0 | IOSD_EN | 0: Internal OSD is disabled<br>1: Internal OSD is enabled<br>(The external OSD can be enabled by EOSD_EN in bit 3 of MISCTR0 register, the priorities of both OSDs are defined by EOSDFR in bit 2 of MISCTR0) | 0 |

**FIGURE 14. PQFP160 package range and dimensions**




| SYMBOL | 160L | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETER | | | INCH | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| b | 0.22 | 0.30 | 0.38 | 0.009 | 0.012 | 0.015 |
| e | 0.65 BSC. | | | 0.026 BSC. | | |
| D2 | 25.35 | | | 0.998 | | |
| E2 | 25 35 | | | 0.998 | | |
| | | | | | | |
| aaa | 0.25 | | | 0.010 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.13 | | | 0.005 | | |

CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 4.10 | — | — | 0.161 |
| A1 | 0.25 | — | — | 0.010 | — | — |
| A2 | 3.20 | 3.32 | 3.60 | 0.126 | 0.131 | 0.142 |
| D | 31.20 BASIC | | | 1.228 BASIC | | |
| D1 | 28.00 BASIC | | | 1.102 BASIC | | |
| E | 31.20 BASIC | | | 1.228 BASIC | | |
| E1 | 28.00 BASIC | | | 1.102 BASIC | | |
| R2 | 0.13 | — | 0.38 | 0.005 | — | 0.012 |
| R1 | 0.13 | — | — | 0.005 | — | — |
| θ | 0° | — | 7° | 0° | — | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 8° REF | | | 8° REF | | |
| θ3 | 8° REF | | | 8° REF | | |
| c | 0.11 | 0.15 | 0.23 | 0.004 | 0.006 | 0.009 |
| L | 0.73 | 0.88 | 1.03 | 0.029 | 0.035 | 0.041 |
| L1 | 1.60 REF | | | 0.063 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H- .

For more information

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trumpion microelectronics inc. reserves the right to change products or specifications without notice.

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