8 D Vcc

7 NOUT-

6 NOUT+

5 GND

OUT+

D, JG, P, OR PW PACKAGE (TOP VIEW)

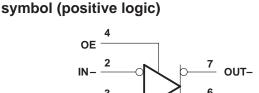
- Operates From a Single 5-V Supply
- 0 to 5 V Common-Mode Input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- Enable Capability
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

# NC-No internal connection

NC [

OΕΓ

IN- **1** 2

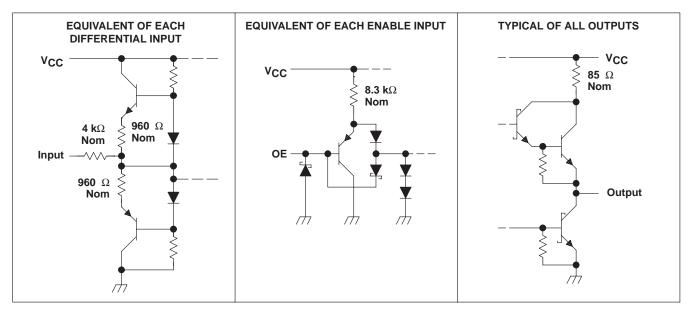


#### description

The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable, (OE), is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

The TL712 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## schematics of inputs and outputs



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage, V<sub>I</sub>, any differential input .....±25 V Differential input voltage, V<sub>ID</sub> (see Note 2) .....±25 V Low-level output current, I<sub>OL</sub> ...... 50 mA Operating free-air temperature range, T<sub>A</sub> ...... 0°C to 70°C Storage temperature range ...... – 65°C to 150°C 

#### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.75	5	5.25	V
Common-mode input voltage, V <sub>IC</sub>	0		5	V
High-level output current, IOH			-1	mA
Low-level output current, IOL			16	mA
Operating free-air temperature, T <sub>A</sub>	0		70	°C

### electrical characteristics at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VT	Threshold voltage (V <sub>T+</sub> and V <sub>T-</sub> )	V <sub>ICR</sub> = 0 to 5 V		-100‡		100	mV
V <sub>hys</sub>	Hysteresis $(V_{T+} - V_{T-})$				5		mV
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV}, \qquad I$	I <sub>OH</sub> = -1 mA	2.7	3.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV}, I$	I <sub>OL</sub> = 16 mA		0.4	0.5	V
loz	Off-state output current	V <sub>O</sub> = 2.4 V				-20	μΑ
lį	Enable current	V <sub>I</sub> = 5.5 V				100	μΑ
IIH	High-level enable current	V <sub>IH</sub> = 2.7 V				20	μΑ
IĮL	Low-level enable current	V <sub>IL</sub> = 0.4 V				-360	μΑ
rį	DIfferential input resistance			4			kΩ
r <sub>O</sub>	Output resistance					100	W
los	Short-circuit output current			-15		-85	mA
ICC	Supply current	V <sub>ID</sub> = 0, No load			17	20	mA

<sup>‡</sup> The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	TTI load Con Figure 4 Co	ee Note 3		25		ns
tPHL	Propagation delay time, high-to-low-level output	TTL load, See Figure 1, See	ee Note 3		25		ns

The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total), and is the interval between the input step function and the instant when the output crosses 2.5 V.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.

<sup>2.</sup> Differential voltage values are at IN+ with respect to IN-.

#### PARAMETER MEASUREMENT INFORMATION

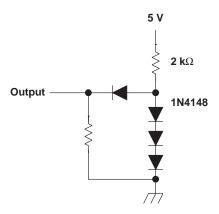
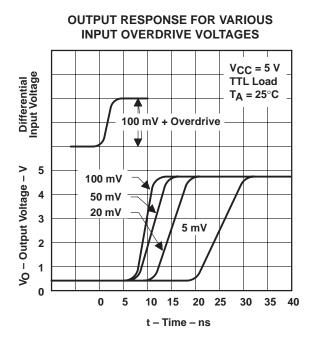


Figure 1. TTL Output Load Circuit

### **TYPICAL CHARACTERISTICS**





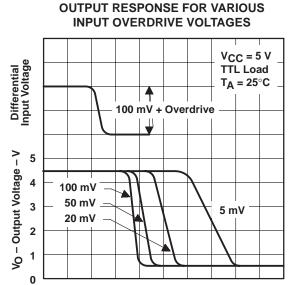


Figure 3

10 15

t - Time - ns

20 25

30 35

0

5

### TYPICAL CHARACTERISTICS

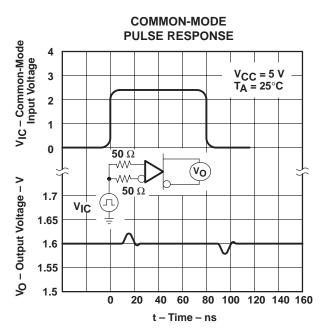


Figure 4

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