

DATA SHEET

TDA3605Q Multiple voltage regulator with switch

Preliminary specification
Supersedes data of 1995 Nov 20
File under Integrated Circuits, IC01

1997 Jul 09

Multiple voltage regulator with switch

TDA3605Q

FEATURES

- Two V_P -state controlled regulators (regulator 1 and regulator 3) and a power switch
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and the power switch
- Supply voltage range of -18 to $+50$ V (operating from 11 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3, and power switch are switched off)
- Hold output (only valid when regulator 1 is switched on)
- Reset and hold outputs (open collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Back-up capacitor for regulator 2.

PROTECTIONS

- Reverse polarity safe (down to -18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protected on all pins
- Thermal protection
- Local thermal protection for power switch
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- Delayed second current limit protection for the power switch (at short-circuit)
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P .

GENERAL DESCRIPTION

The TDA3605Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. It contains:

1. Two fixed voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.
2. A power switch with protections, operated by an enable input.
3. Reset and hold outputs can be used to interface by the microcontroller. The reset signal can be used to call up the microcontroller and the hold output indicates regulator 1 voltage available and within range.
4. A supply pin which can withstand load dump pulses and negative supply voltage.
5. Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.
6. Also there is a provision for use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3605Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		11	14.4	18	V
	operating		–	–	–	V
	reverse battery		–18	–	–	V
	regulator 2 on		2.4	14.4	18	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during ≤ 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	500	600	μ A
T_j	junction temperature		–	–	150	$^{\circ}$ C
Voltage regulators						
V_{REG1}	output voltage regulator 1	$0.5 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$	9.5	10.0	10.5	V
V_{REG2}	output voltage regulator 2	$0.5 \text{ mA} \leq I_{REG2} \leq 300 \text{ mA}$; $V_P = 14.4 \text{ V}$	4.75	5.0	5.25	V
V_{REG3}	output voltage regulator 3	$0.5 \text{ mA} \leq I_{REG3} \leq 400 \text{ mA}$	4.75	5.0	5.25	V
Power switch						
$V_{sw(d)}$	drop-out voltage	$I_{sw} = 1 \text{ A}$	–	0.45	0.7	V
		$I_{sw} = 1.8 \text{ A}$	–	1	1.8	V
I_{swM}	peak current		3	–	–	A

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BLOCK DIAGRAM

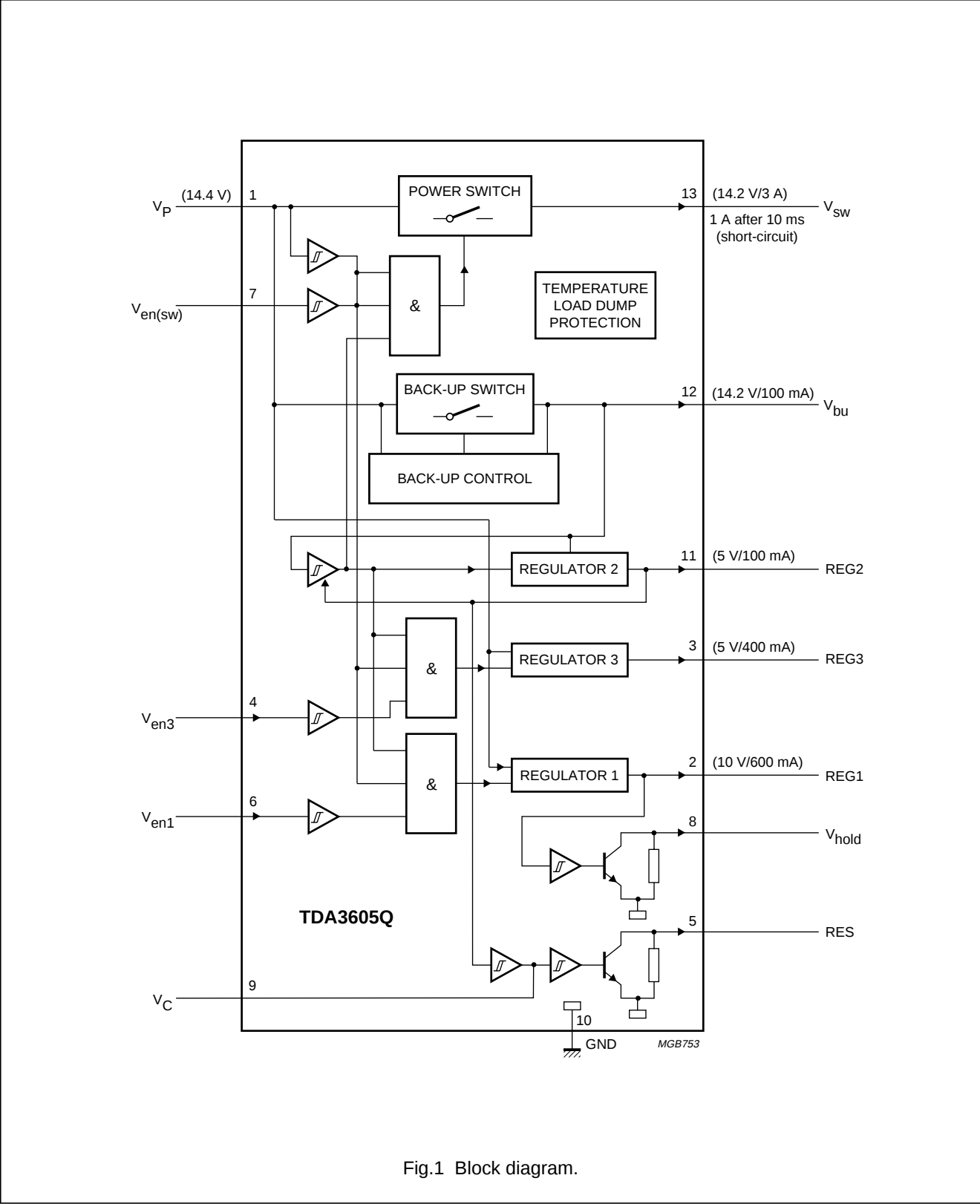


Fig.1 Block diagram.

Multiple voltage regulator with switch

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PINNING

SYMBOL	PIN	DESCRIPTION
V _P	1	supply voltage
REG1	2	regulator 1 output
REG3	3	regulator 3 output
V _{en3}	4	enable input regulator 3
RES	5	reset output voltage
V _{en1}	6	enable input regulator 1
V _{en(sw)}	7	enable input power switch
V _{hold}	8	hold output
V _C	9	reset delay capacitor
GND	10	ground (0 V)
REG2	11	regulator 2 output
V _{bu}	12	back-up
V _{sw}	13	power switch output voltage

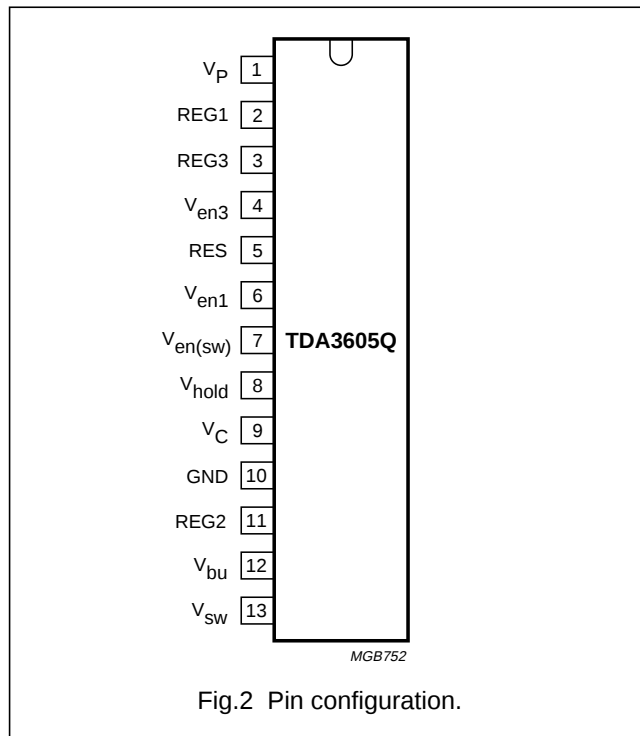


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3605Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used in the TDA3605Q.

Regulator 2 will switch-on when the back-up voltage exceeds 6.5 V for the first time and will switch-off again when the output voltage of regulator 2 is below 1.9 V (this is far below an engine start). When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output will be enabled (reset will go HIGH via a pull-up resistor) to generate a reset to the microcontroller. The reset cycles can be extended by an external capacitor at pin 9. The above mentioned start-up feature is built-in to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

The charge of the back-up capacitor can be used to supply regulator 2 for a short period when the supply falls to 0 V (time depends on value of storage capacitor). When both regulator 2 and the supply voltage ($V_P > 4.5$ V) are available, regulators 1 and 3 can be operated by means of enable inputs (pins 6 and 4 respectively).

Regulator 1 has a hold output (open collector) indicating that the output voltage of this regulator is settled (held HIGH by external pull-up resistor) and when the output voltage of this regulator drops out of regulation (because of supply voltage drop or high load) the hold output will go LOW. The hold output signal is only valid when regulator 1 is enabled by its enable input (pin 6).

The power switch can also be controlled by means of a separate enable input (pin 7).

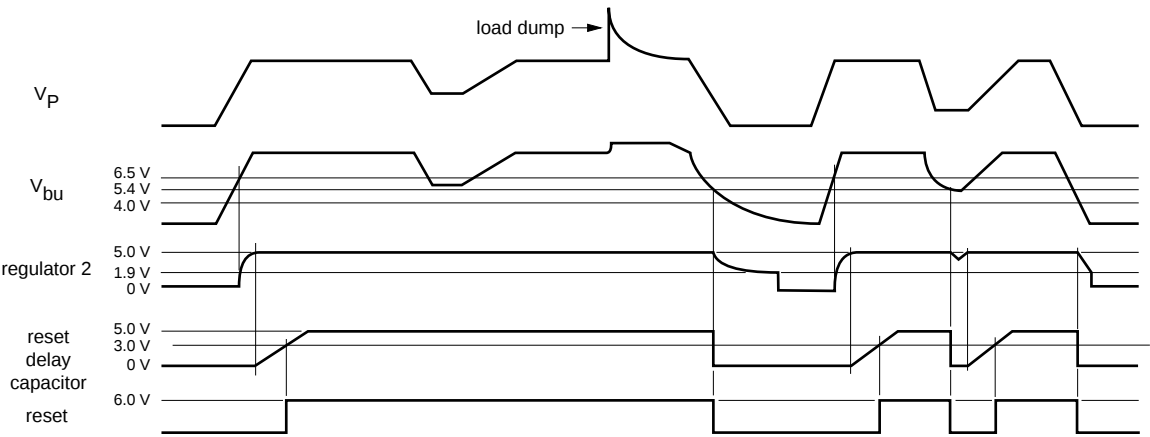
All output pins are fully protected. The regulators are protected against load dump (regulator 1 and 3 will switch off at supply voltages >18 V) and short-circuit (foldback current protection).

The switch contains a current protection, but this protection is delayed at short-circuit condition for at least 10 ms. During this time the output current is limited to a peak value of at least 3 A and 2 A (DC) ($V_P \leq 18$ V). At supply voltages >17 V the switch is clamped at maximum 16 V (to avoid external connected circuitry being damaged by an overvoltage) and the switch will switch-off at load dump.

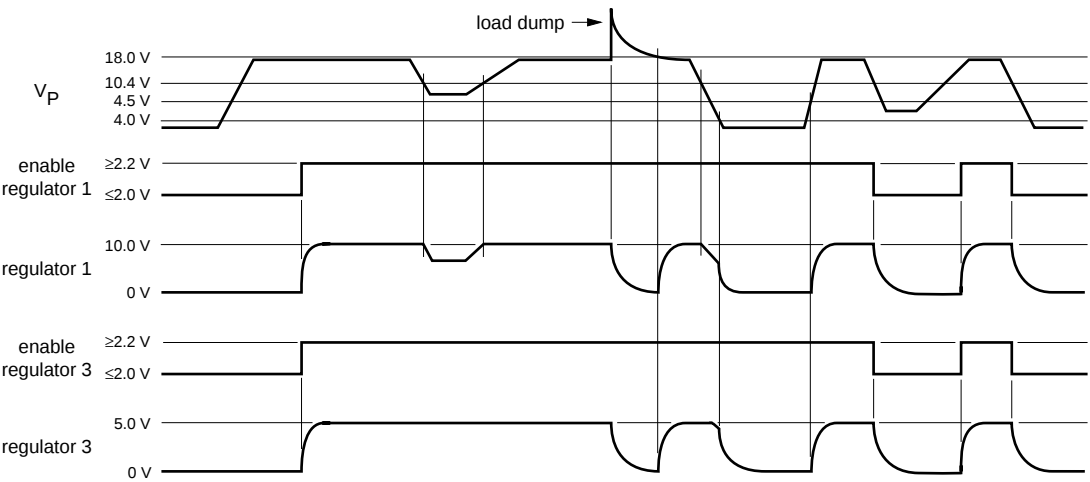
The total timing of a semi on/off logic set is shown in Fig.3.

Multiple voltage regulator with switch

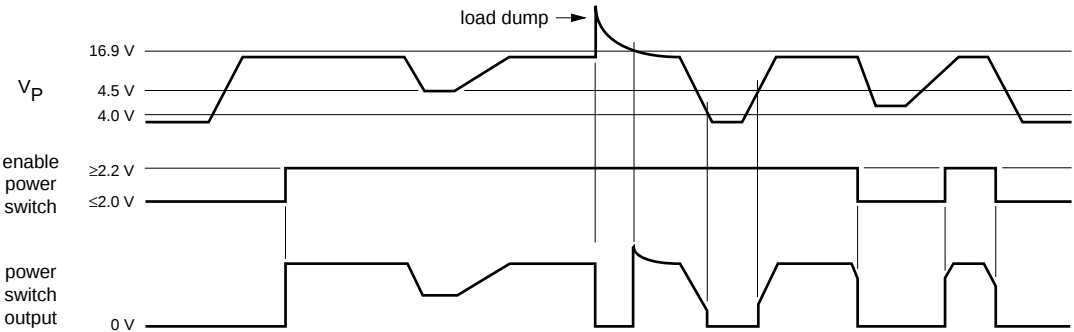
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Back-up Schmitt-trigger and reset behaviour



V_P and enable Schmitt-trigger



Switch behaviour

MGB759

Fig.3 Timing diagram.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	jump start	$t \leq 10$ minutes	–	30	V
	load dump protection	during ≤ 50 ms; $t_r \geq 2.5$ ms	–	50	V
V_P	reverse battery voltage	non-operating	–	–18	V
P_{tot}	total power dissipation		–	62	W
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	2	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	50	K/W

CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; see Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V _P	supply voltage		11	14.4	18	V
	operating					
	regulator 2 on	note 1	2.4	14.4	18	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	during ≤50 ms; t _r ≥ 2.5 ms	–	–	50	V
I _q	quiescent current	V _P = 12.4 V; note 2; I _{R2} = 0.1 mA	–	500	600	μA
		V _P = 14.4 V; note 2; I _{R2} = 0.1 mA	–	520	–	μA
Schmitt-trigger power supply for switch, regulator 1 and regulator 3						
V _{thr}	rising voltage threshold		4.0	4.5	5.0	V
V _{thf}	falling voltage threshold		3.5	4.0	4.5	V
V _{hys}	hysteresis		–	0.5	–	V
Schmitt-trigger power supply for regulator 2						
V _{thr}	rising voltage threshold		6.0	6.5	7.1	V
V _{thf}	falling voltage threshold		1.7	1.9	2.2	V
V _{hys}	hysteresis		–	4.6	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Schmitt-trigger for enable input (regulator 1, regulator 3 and switch)						
V_{thr}	rising voltage threshold		1.7	2.2	2.7	V
V_{thf}	falling voltage threshold		1.5	2.0	2.5	V
V_{hys}	hysteresis	$I_{REG} = I_{SW} = 1 \text{ mA}$	0.1	0.2	0.5	V
I_{LI}	input leakage current	$V_{en} = 5 \text{ V}$	1	5	10	μA
Schmitt-trigger for reset buffer						
V_{thr}	rising voltage threshold of regulator 2	V_P rising; $I_{REG1} = 50 \text{ mA}$; note 3	–	$V_{REG2} - 0.15$	$V_{REG2} - 0.075$	V
V_{thf}	falling voltage threshold of regulator 2	V_P rising; $I_{REG1} = 50 \text{ mA}$; note 3	4.3	$V_{REG2} - 0.35$	–	V
V_{hys}	hysteresis		0.1	0.2	0.3	V
Schmitt-trigger for hold						
V_{thr}	rising voltage threshold of regulator 1	V_P rising; note 3	–	$V_{REG1} - 0.15$	$V_{REG1} - 0.075$	V
V_{thf}	falling voltage threshold of regulator 1	V_P rising; note 3	9.2	$V_{REG1} - 0.35$	–	V
V_{hys}	hysteresis		0.1	0.2	0.3	V
Reset and hold buffer						
I_{Lsink}	LOW level sink current	$V_{RES/hold} \leq 0.8 \text{ V}$	2	–	–	mA
I_{LO}	output leakage current	$V_P = 14.4 \text{ V}$; $V_{RES/hold} = 5 \text{ V}$	–	16	32	μA
t_r	rise time	note 4	–	7	50	μs
t_f	fall time	note 4	–	1	50	μs
Reset delay						
I_{ch}	charge current		2	4	8	μA
I_{dch}	discharge current		500	800	–	μA
V_{thr}	rising voltage threshold		2.5	3.0	3.5	V
t_d	delay time	$C = 47 \text{ nF}$; note 5	20	35	70	ms
Regulator 1 ($I_{REG1} = 5 \text{ mA}$)						
$V_{REG1(off)}$	output voltage off		–	1	400	mV
V_{REG1}	output voltage	$1 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$	9.5	10.0	10.5	V
		$11 \text{ V} \leq V_P \leq 18 \text{ V}$	9.5	10.0	10.5	V
ΔV_{REG1}	line regulation	$11 \text{ V} \leq V_P \leq 18 \text{ V}$	–	2	75	mV
ΔV_{REGL1}	load regulation	$1 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$	–	20	50	mV
I_q	quiescent current	$I_{R1} = 600 \text{ mA}$	–	25	60	mA
SVRR1	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$; $V_{i(p-p)} = 2 \text{ V}$	60	70	–	dB
V_{REGd1}	drop-out voltage	$I_{REG1} = 550 \text{ mA}$; $V_P = 9.5 \text{ V}$; note 6	–	0.4	0.7	V
I_{REGm1}	current limit	$V_{REG1} > 8.5 \text{ V}$; note 7	0.65	1.2	–	A

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{REGsc1}	short-circuit current	$R_L \leq 0.5 \Omega$; note 8	250	800	–	mA
Regulator 2 ($I_{REG2} = 5 \text{ mA}$)						
V_{REG2}	output voltage	$0.5 \text{ mA} \leq I_{REG2} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
		$0.5 \text{ mA} \leq I_{REG2} \leq 300 \text{ mA}$	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_P \leq 18 \text{ V}$	4.75	5.0	5.25	V
		$18 \text{ V} \leq V_P \leq 50 \text{ V}$; $I_{REG2} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
ΔV_{REG2}	line regulation	$6 \text{ V} \leq V_P \leq 18 \text{ V}$	–	2	50	mV
		$6 \text{ V} \leq V_P \leq 50 \text{ V}$	–	15	75	mV
ΔV_{REGL2}	load regulation	$1 \text{ mA} \leq I_{REG2} \leq 150 \text{ mA}$	–	20	50	mV
		$1 \text{ mA} \leq I_{REG2} \leq 300 \text{ mA}$	–	–	100	mV
SVRR2	supply voltage ripple rejection	$f = 3 \text{ kHz}$; $V_{i(p-p)} = 2 \text{ V}$	60	70	–	dB
V_{REGd2}	drop-out voltage	$I_{REG2} = 100 \text{ mA}$; $V_P = 4.75 \text{ V}$; note 6	–	0.4	0.6	V
		$I_{REG2} = 200 \text{ mA}$; $V_P = 5.75 \text{ V}$; note 6	–	0.8	1.2	V
		$I_{REG2} = 100 \text{ mA}$; $V_{bu} = 4.75 \text{ V}$; note 7	–	0.2	0.5	V
		$I_{REG2} = 200 \text{ mA}$; $V_{bu} = 5.75 \text{ V}$; note 7	–	0.8	1.0	V
I_{REGm2}	current limit	$V_{REG2} > 4.5 \text{ V}$; note 7	0.32	0.37	–	A
I_{REGsc2}	short-circuit current	$R_L \leq 0.5 \Omega$; note 8	20	100	–	mA
Regulator 3 ($I_{REG3} = 5 \text{ mA}$)						
$V_{REG3(off)}$	output voltage off		–	1	400	mV
V_{REG3}	output voltage	$1 \text{ mA} \leq I_{REG3} \leq 400 \text{ mA}$	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_P \leq 18 \text{ V}$	4.75	5.0	5.25	V
ΔV_{REG3}	line regulation	$7 \text{ V} \leq V_P \leq 18 \text{ V}$	–	2	50	mV
ΔV_{REGL3}	load regulation	$1 \text{ mA} \leq I_{REG3} \leq 400 \text{ mA}$	–	20	50	mV
I_q	quiescent current	$I_{R3} = 400 \text{ mA}$	–	15	40	mA
SVRR3	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$; $V_{i(p-p)} = 2 \text{ V}$	60	70	–	dB
V_{REGd3}	drop-out voltage	$I_{REG3} = 400 \text{ mA}$; $V_P = 5.75 \text{ V}$; note 6	–	1	1.5	V
I_{REGm3}	current limit	$V_{REG3} > 4.5 \text{ V}$; note 7	0.45	0.70	–	A
I_{REGsc3}	short-circuit current	$R_L \leq 0.5 \Omega$; note 8	100	400		mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power switch						
V_{swd}	drop-out voltage	$I_{sw} = 1 \text{ A}$; note 10	–	0.45	0.7	V
		$I_{sw} = 1.8 \text{ A}$; note 10	–	1.0	1.8	V
$I_{sw(dc)}$	continuous current	$V_P = 16 \text{ V}$; $V_{sw} = 13.5 \text{ V}$	1.8	2.0	–	A
V_{swcl}	clamping voltage	$V_P \geq 17 \text{ V}$	13.5	15.0	16.0	V
I_{swM}	peak current	$V_P = 17 \text{ V}$; notes 11 and 12	3	–	–	A
V_{swfb}	fly back voltage behaviour	$I_{sw} = -100 \text{ mA}$	–	$V_P + 3$	22	V
$I_{sw(sc)}$	short-circuit current	$V_P = 14.4 \text{ V}$; $V_{sw} \leq 1.2 \text{ V}$; note 12	–	0.8	–	A
Back-up switch						
$I_{bu(DC)}$	continuous current		0.3	0.35	–	A
V_{bucl}	clamping voltage	$V_P \geq 16.7 \text{ V}$	–	–	16	V
V_r	reverse current	$V_P = 0 \text{ V}$; $V_{bu} = 12.4 \text{ V}$	–	–	900	ms

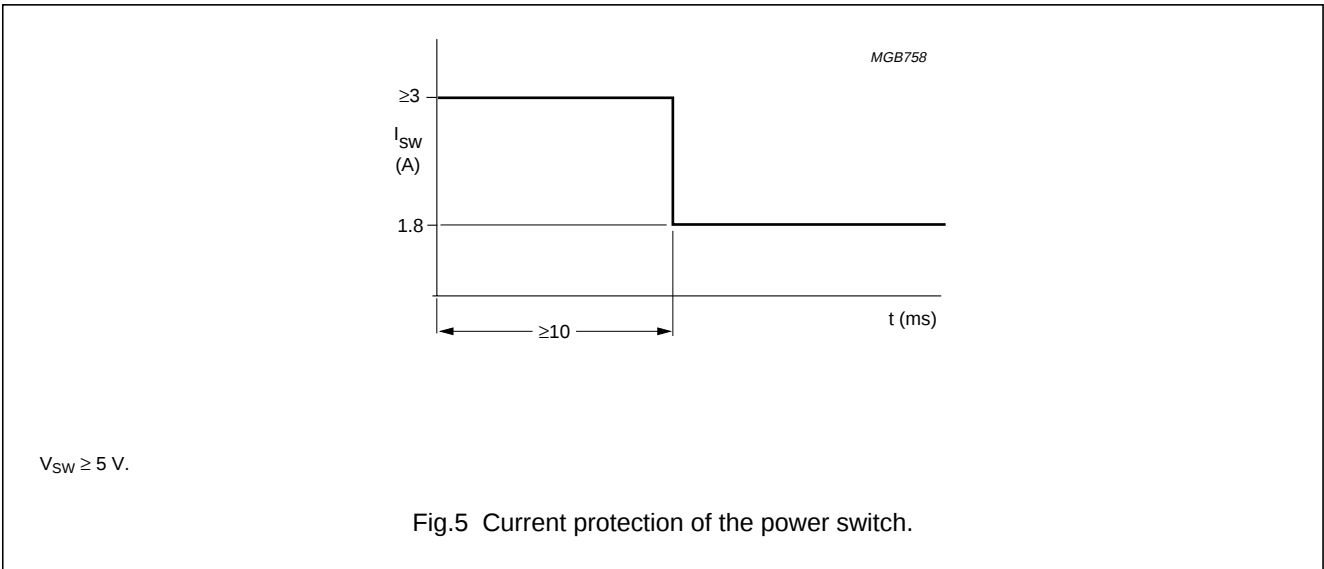
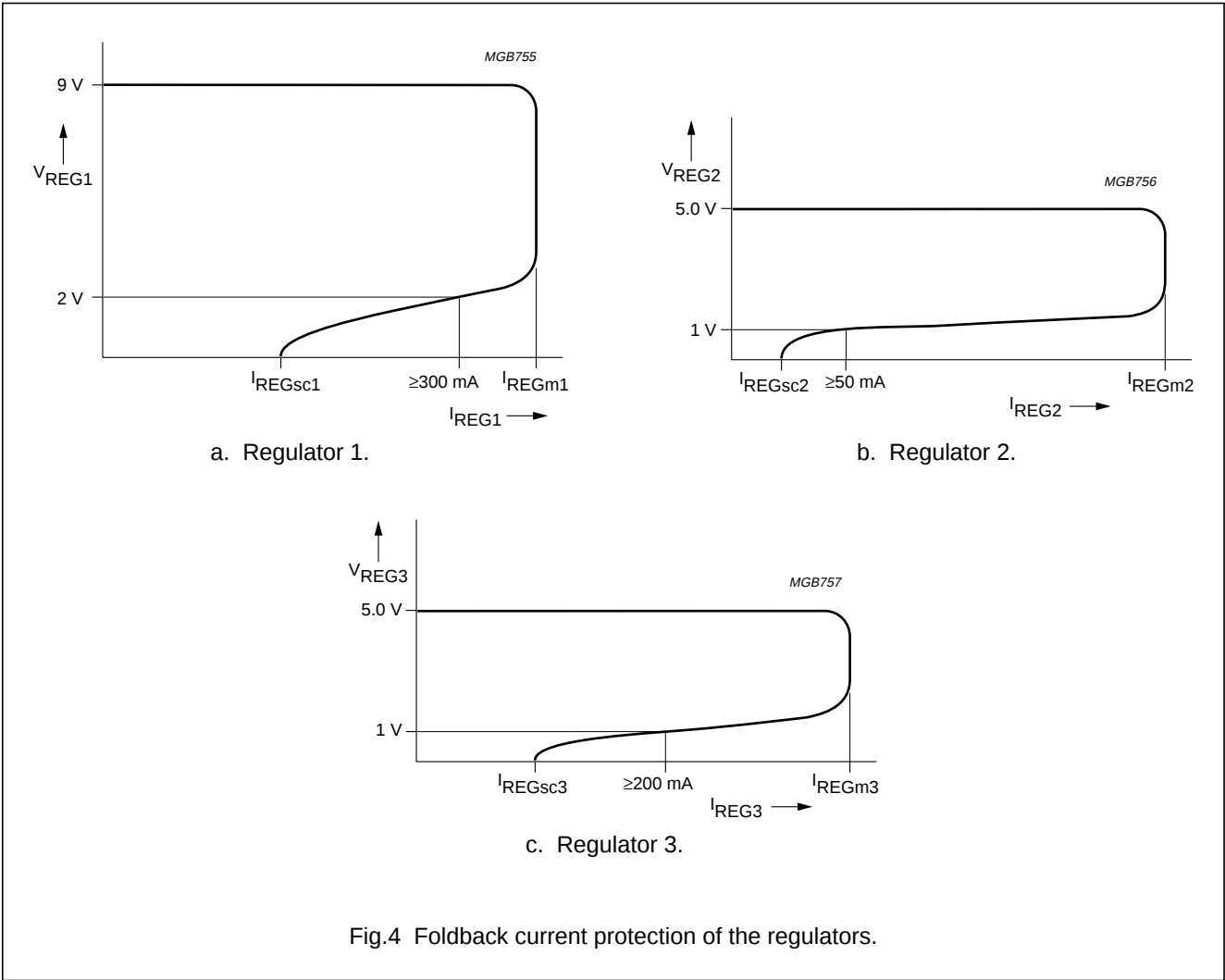
Notes

- Minimum operating voltage, only if V_P has exceeded 6.5 V.
- The quiescent current is measured in the standby mode. So, the enable inputs of regulators 1 and 3 and the switch are grounded and $R2 = \infty$ (see Fig.6).
- The voltage of the regulator sinks as a result of a V_P drop.
- The rise and fall times are measured with a 10 k Ω pull-up resistor and a 50 pF load capacitor.
- The delay time depends on the value of the capacitor:

$$t_d = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (750 \times 10^3) \text{ (ms)}$$
- The drop-out voltage of regulators 1, 2 and 3 is measured between V_P and V_{REGn} .
- At current limit, I_{REGmn} is held constant (see Fig.4 for behaviour of I_{REGmn}).
- The foldback current protection limits the dissipated power at short-circuit (see Fig.4).
- The peak current of 300 mA can only be applied for short periods ($t < 100 \text{ ms}$).
- The drop-out voltage of the power switch is measured between V_P and V_{sw} .
- The maximum output current of the switch is limited to 1.8 A when the supply voltage exceeds 18 V.
A test-mode is built-in. The delay time of the switch will be disabled when a voltage of $V_P + 1 \text{ V}$ is applied to the switch enable input.
- At short circuit, $I_{sw(sc)}$ of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms. A test-mode is built-in. The delay time of the switch will be disabled when a voltage of $V_P + 1 \text{ V}$ is applied to the switch enable input.

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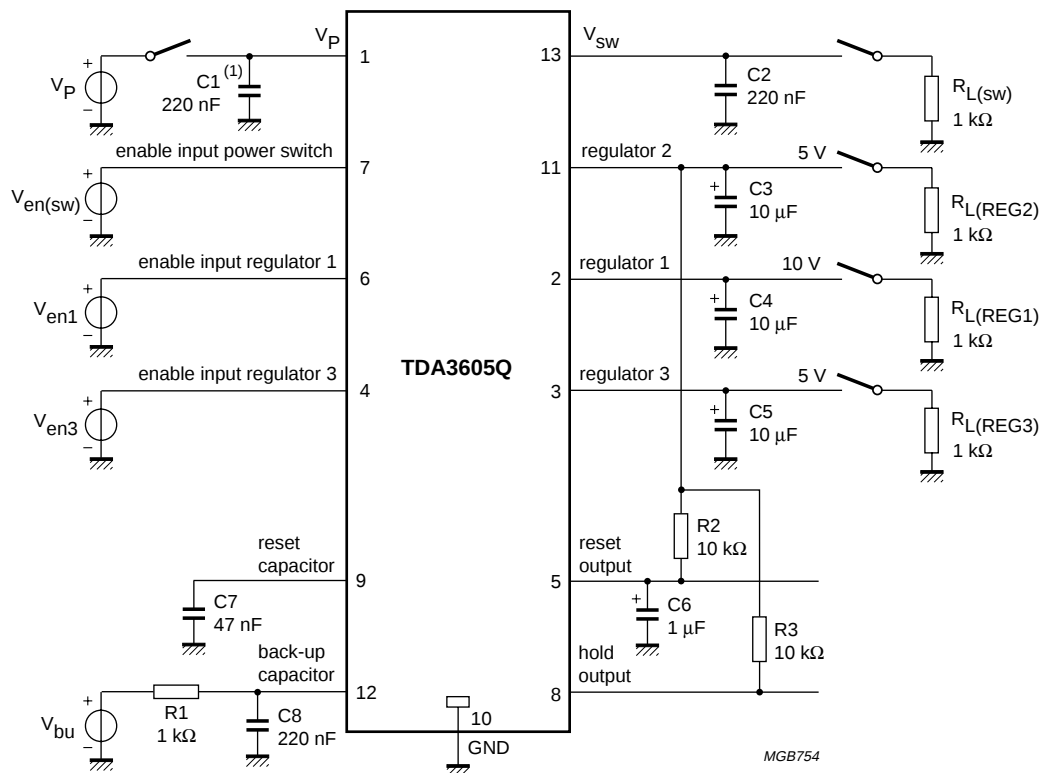


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TEST AND APPLICATION INFORMATION

Test information



(1) Capacitor not required for stability.

Fig.6 Test circuit.

Application information

NOISE

Table 1 Noise figures

REGULATOR	NOISE FIGURE (μV) ⁽¹⁾		
	at OUTPUT CAPACITOR		
	10 μF	47 μF	100 μF
1	—	150	—
2	—	150	—
3	—	200	—

Note

1. Measured at a bandwidth of 200 kHz.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated into a current noise by means of the output capacitors).

When a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μ F is connected directly to pins 3 and 8 (supply and ground) the noise is minimal.

STABILITY

The regulators are made stable with the externally connected output capacitors. The value of the output capacitors can be selected by referring to the graphs illustrated in Figs 7 and 8.

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When an electrolytic capacitor is used the temperature behaviour of this output capacitor can cause oscillations at cold temperature.

The following two examples explain how an output capacitor value is selected.

Example 1

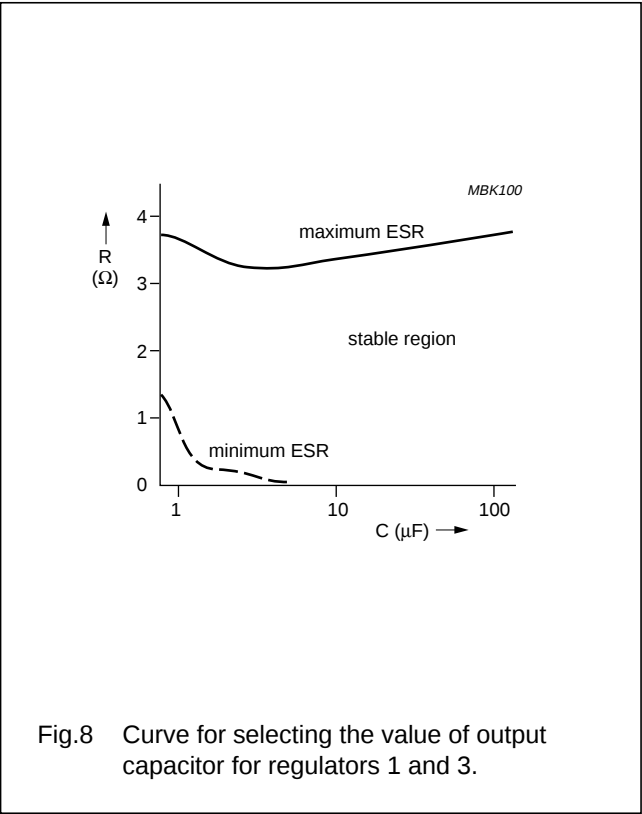
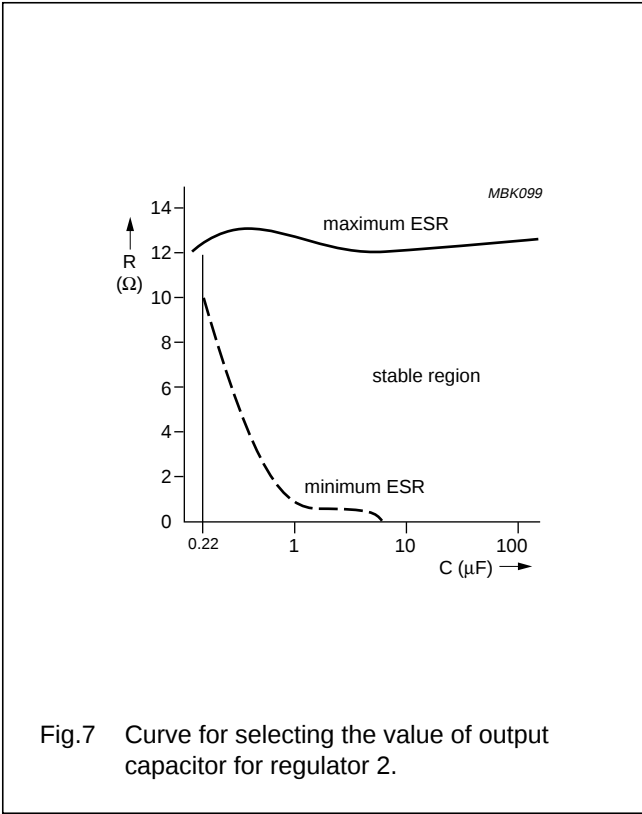
Regulator 1 is made stable with an electrolytic output capacitor of 220 μF ($\text{ESR} = 0.15\ \Omega$). At $-30\ ^\circ\text{C}$ the capacitor value is decreased to 73 μF and the ESR is increased to 1.1 Ω . The regulator will remain stable at $-30\ ^\circ\text{C}$.

Example 2

Regulator 2 is made stable with a 10 μF electrolytic capacitor ($\text{ESR} = 3\ \Omega$). At $-30\ ^\circ\text{C}$ the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω . The regulator will be unstable at $-30\ ^\circ\text{C}$ (see Fig.7).

Solution

Use a tantalum capacitor of 10 μF or a large electrolytic capacitor. The use of tantalum capacitors is recommended to avoid problems with stability at cold temperatures.



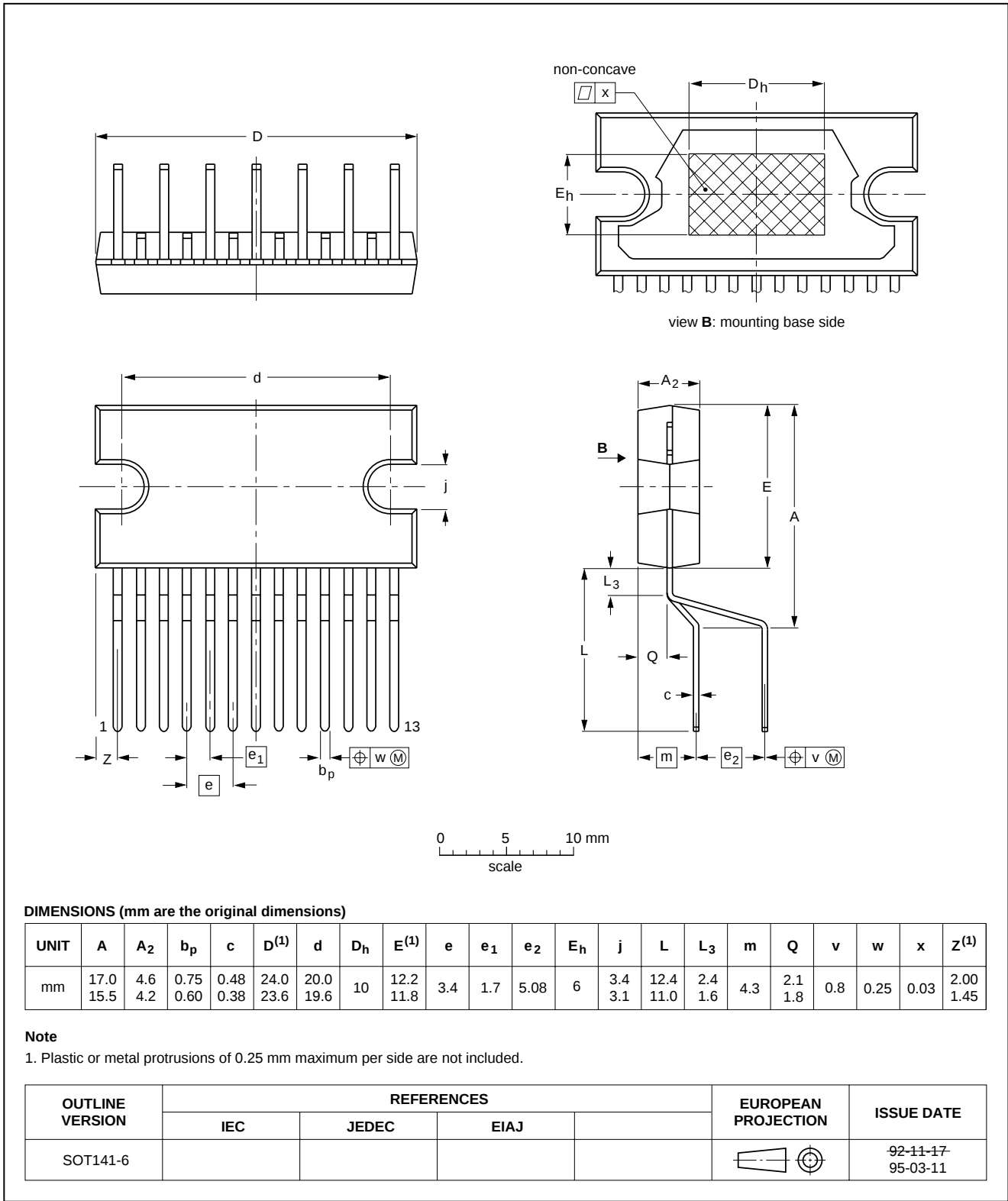
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PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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Printed in The Netherlands

547027/1200/02/pp16

Date of release: 1997 Jul 09

Document order number: 9397 750 02236

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