CMOS 32-Bit Microcontroller

TMP94CS40F

1. OVERVIEW AND FEATURES :

The TMP94CS40 is a high-speed, high-function 32-bit microcontroller developed for control devices used to handle large volumes of data.
The TMP94CS40 comes in a 160-pin mini-flat package. Its features are as follows :

(1) Original high-speed 32-bit CPU (TCS-900/H2 CPU)

- Instruction codes are fully compatible with those for TLCS-900, 900/L, and 900/H.
- 16 MB linear address space
- General-purpose registers and register banks
- Micro DMA : Eight channels, 250 ns/4 bytes (@ 20 MHz internally)

(2) Minimum instruction execution time : 50 ns (@ 20 MHz internally)

(3) Built-in ROM : 4 KB (32-bit, 2-1-1-1 access)
Built-in RAM : 2 KB (32-bit, 1 clock access, program execution possible)

(4) External memory expansion

- Expandable up to 16 MB (common to program and data)
- External data bus width : 8-, 16-, and 32-bit buses can be used together.

(5) Memory controller

- Controls chip select, wait, and bus width (6 blocks).

(6) DRAM controllers : two channels

- Direct interface (8-, 16-, or 32-bit data bus width selectable)

(7) 8-bit timers : four channels

(8) 16-bit timers : four channels

(9) Serial interface : two channels

(10) 10-bit A/D converters : eight channels (with built-in sample and hold circuit)

(11) 8-bit D/A converters : two channels (with built-in CMOS amp)

(12) Watchdog timer

(13) Interrupt function

Built-in I/O interrupts : 18, external interrupts : 10

(14) I/O ports : 64 pins (when external memory is connected via the D0 to D31, A0 to A23, and $\overline{RD}$ pins)

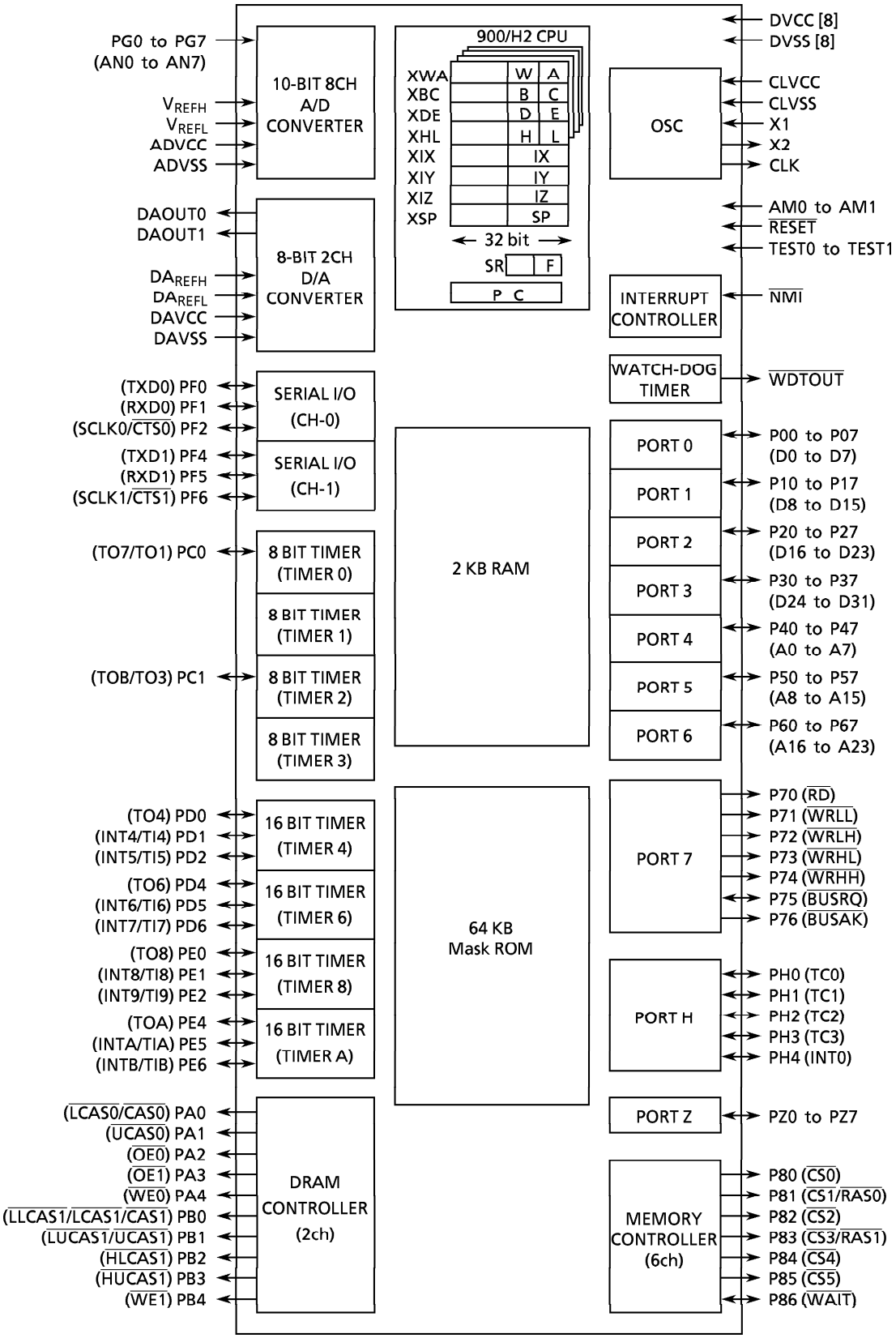


Figure 1 TMP94CS40 Block Diagram

2. PIN ASSIGNMENT AND PIN FUNCTIONS

2.1 PIN ASSIGNMENT (TOP VIEW)

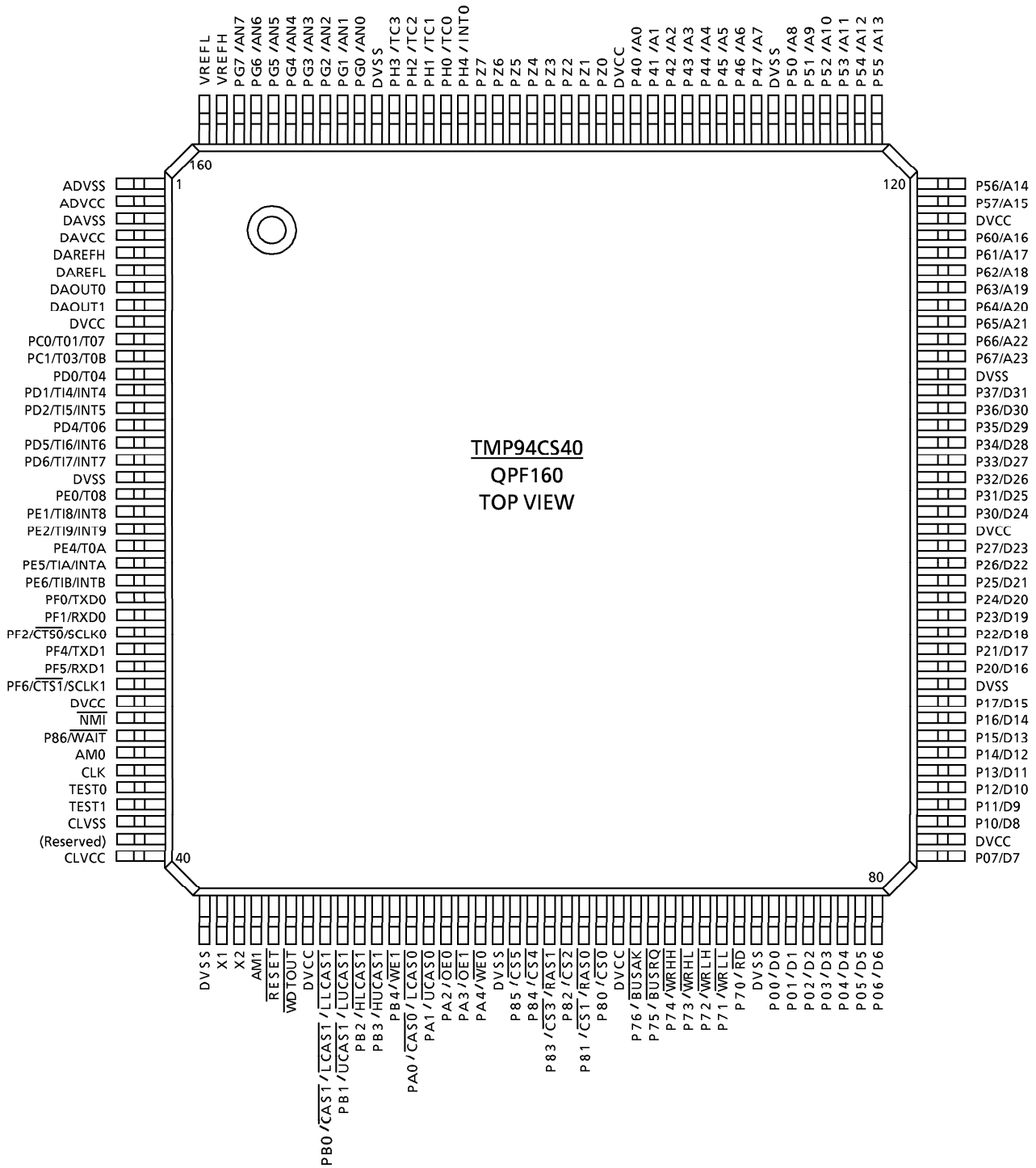


Figure 2.1 Pin Assignment

2.2 PIN NAMES AND FUNCTIONS

The names and functions of the I/O pins are as listed in Table 2.2 below.

Table 2.2

Pin Name	Number of Pins	I/O	Functions
P00 to P07 D0 to D7	8 (TTL)	I/O I/O	Port 0 : I/O port Data 0 to 7 : Data bus 0 to 7 Pin function selectable by the setting of the AM0/1 pin. High impedance at other than external memory access.
P10 to P17 D8 to D15	8 (TTL)	I/O I/O	Port 1 : I/O port Data 8 to 15 : Data bus 8 to 15 Pin function selectable by the setting of the AM0/1 pin. High impedance at other than external memory access.
P20 to P27 D16 to D23	8 (TTL)	I/O I/O	Port 2 : I/O port Data 16 to 23 : Data bus 16 to 23 Pin function selectable by the setting of the AM0/1 pin. High impedance at other than external memory access.
P30 to P37 D24 to D31	8 (TTL)	I/O I/O	Port 3 : I/O port Data 24 to 31 : Data bus 24 to 31 Pin function selectable by the setting of the AM0/1 pin. High impedance at other than external memory access.
P40 to P47 A0 to A7	8	I/O Output	Port 4 : I/O port Address 0 to 7 : Address bus 0 to 7 Pin function selectable by the setting of the AM0/1 pin. No signal change at other than external memory access.
P50 to P57 A8 to A15	8	I/O Output	Port 5 : I/O port Address 8 to 15 : Address bus 8 to 15 Pin function selectable by the setting of the AM0/1 pin. No signal change at other than external memory access.
P60 to P67 A16 to A23	8	I/O Output	Port 6 : I/O port Address 16 to 23 : Address bus 16 to 23 Pin function selectable by setting of the AM0/1 pin. No signal change at other than external memory access.
P70 $\overline{RD}$	1	Output Output	Port 70 : Output port (initialized to 1 output) Pin function selectable by the setting of the AM0/1 pin. Read : Strobe signal used to read external memory No strobe signal output at other than external memory access.
P71 $\overline{WRLL}$	1	Output Output	Port 71 : Output port (initialized to 1 output) Write : Strobe signal used to write to external memory via D0 to D7 No strobe signal output at other than external memory access.
P72 $\overline{WRLH}$	1	Output Output	Port 72 : Output port (initialized to 1 output) Write : Strobe signal used to write to external memory via D8 to D15 No strobe signal output at other than external memory access.

Pin Name	Number of Pins	I/O	Functions
P73 $\overline{WRHL}$	1	Output Output	Port 73 : Output port (initialized to 1 output) Write : Strobe signal used to write to external memory via D16 to D23 No strobe signal output at other than external memory access.
P74 $\overline{WRHH}$	1	Output Output	Port 74 : Output port (initialized to 1 output) Write : Strobe signal used to write to external memory via D24 to D31 No strobe signal output at other than external memory access.
P75 $\overline{BUSRQ}$	1	I/O Input	Port 75 : I/O port Bus request : Signal used to request the memory interface pins to be set to high impedance The following pins are set to high impedance. Note that when the pins function as ports, the pin state does not change. A0 to A23, D0 to D31, $\overline{RD}$, $\overline{WRLL}$, $\overline{WRLH}$, $\overline{WRHL}$, $\overline{WRHH}$, $\overline{CS0}$ to $\overline{CS5}$, $\overline{OE0}$ to $\overline{OE1}$, $\overline{WE0}$ to $\overline{WE1}$, $\overline{RAS}$ group, and $\overline{CAS}$ group
P76 $\overline{BUSAK}$	1	Output Output	Port 75 : Output port (initialized to 1 output) Bus acknowledge : Signal used to indicate $\overline{BUSRQ}$ is accepted
P80 $\overline{CS0}$	1	Output Output	Port 80 : Output port (initialized to 1 output) Chip select 0 : If the address is within the specified address range, outputs low.
P81 $\overline{CS1}$ $\overline{RAS0}$	1	Output Output Output	Port 81 : Output port (initialized to 1 output) Chip select 1 : If the address is within the specified address range, outputs low. Low address strobe 0 : If the address is within the specified address range, outputs $\overline{RAS}$ strobe signal for DRAM.
P82 $\overline{CS2}$	1	Output Output	Port 82 : Output port (initialized to 0 output) Chip select 2 : If the address is within the specified address range, outputs low.
P83 $\overline{CS3}$ $\overline{RAS1}$	1	Output Output Output	Port 83 : Output port (initialized to 1 output) Chip select 3 : If the address is within the specified address range, outputs low. Low address strobe 1 : If the address is within the specified address range, outputs $\overline{RAS}$ strobe signal for DRAM.
P84 $\overline{CS4}$	1	Output Output	Port 84 : Output port (initialized to 1 output) Chip select 4 : If the address is within the specified address range, outputs low.
P85 $\overline{CS5}$	1	Output Output	Port 85 : Output port (initialized to 1 output). Chip select 5 : If the address is within the specified address range, outputs low.
P86 $\overline{WAIT}$	1	I/O Input	Port 86 : I/O port WAIT : Bus wait request signal

Pin Name	Number of Pins	I/O	Functions
PA0 $\overline{CAS0}$ $\overline{LCAS0}$	1	Output Output Output	Port A0 : Output port (initialized to 1 output) Column address strobe 0 : If the address is within the specified address range, outputs $\overline{CAS}$ strobe signal for DRAM. Lower column address strobe 0 : If the address is within the specified address range, outputs lower $\overline{CAS}$ strobe signal for DRAM.
PA1 $\overline{UCAS0}$	1	Output Output	Port A1 : Output port (initialized to 1 output) Upper column address strobe 0 : If the address is within the specified address range, outputs upper $\overline{CAS}$ strobe signal for DRAM.
PA2 $\overline{OE0}$	1	Output Output	Port A2 : Output port (initialized to 1 output) Output enable 0 : Outputs output enable signal for DRAM.
PA3 $\overline{OE1}$	1	Output Output	Port A3 : Output port (initialized to 1 output) Output enable 1 : Outputs output enable signal for DRAM.
PA4 $\overline{WE0}$	1	Output Output	Port A4 : Output port (initialized to 1 output) Write enable 0 : Outputs write enable signal for DRAM.
PB0 $\overline{CAS1}$ $\overline{LCAS1}$ $\overline{LLCAS1}$	1	Output Output Output Output	Port B0 : Output port (initialized to 1 output) Column address strobe 1 : If the address is within the specified address range, outputs upper $\overline{CAS}$ strobe signal for DRAM. Lower column address strobe 1 : If the address is within the specified address range, outputs lower $\overline{CAS}$ strobe signal for DRAM. Low lower column address strobe 1 : If the address is within the specified address range, outputs low lower $\overline{CAS}$ strobe signal for DRAM.
PB1 $\overline{UCAS1}$ $\overline{LUCAS1}$	1	Output Output Output	Port B1 : Output port (initialized to 1 output) Upper column address strobe 1 : If the address is within the specified address range, outputs upper $\overline{CAS}$ strobe signal for DRAM. Low upper column address strobe 1 : If the address is within the specified address range, outputs low upper $\overline{CAS}$ strobe signal for DRAM.
PB2 $\overline{HLCAS1}$	1	Output Output	Port B2 : Output port (initialized to 1 output) High lower column address strobe 1 : If the address is within the specified address range, outputs high lower $\overline{CAS}$ strobe signal for DRAM.
PB3 $\overline{HUCAS1}$	1	Output Output	Port B3 : Output port (initialized to 1 output) High upper column address strobe 1 : If the address is within the specified address range, outputs high upper $\overline{CAS}$ strobe signal for DRAM.
PB4 $\overline{WE1}$	1	Output Output	Port B4 : Output port (initialized to 1 output) Write enable 1 : Outputs write enable signal for DRAM.
PC0 TO1 TO7	1	I/O Output Output	Port C0 : I/O port Timer output 1 : Outputs 8-bit timer 0 or 1. Timer output 7 : Outputs 16-bit timer 7.

Pin Name	Number of Pins	I/O	Functions
PC1 TO3 TOB	1	I/O Output Output	Port C1 : I/O port Timer output 3 : Outputs 8-bit timer 2 or 3. Timer output B : Outputs 16-bit timer B.
PD0 TO4	1	I/O Output	Port D0 : I/O port Timer output 4 : Outputs 16-bit timer 4.
PD1 TI4 INT4	1	I/O Input Input	Port D1 : I/O port Timer input 4 : Inputs 16-bit timer 4. Interrupt request pin 4 : Interrupt request pin with rising/falling edge programmable.
PD2 TI5 INT5	1	I/O Input Input	Port D2 : I/O port Timer input 5 : Inputs 16-bit timer 4. Interrupt request pin 5 : Interrupt request pin at rising edge.
PD4 TO6	1	I/O Output	Port D4 : I/O port Timer output 6 : Outputs 16-bit timer 6.
PD5 TI6 INT6	1	I/O Input Input	Port D5 : I/O port Timer input 6 : Inputs 16-bit timer 6. Interrupt request pin 6 : Interrupt request pin with rising/falling edge programmable.
PD6 TI7 INT7	1	I/O Input Input	Port D6 : I/O port Timer input 7 : Inputs 16-bit timer 6. Interrupt request pin 7 : Interrupt request pin at rising edge.
PE0 TO8	1	I/O Output	Port E0 : I/O port Timer output 8 : Outputs 16-bit timer 8.
PE1 TI8 INT8	1	I/O Input Input	Port E1 : I/O port Timer input 8 : Inputs 16-bit timer 8. Interrupt request pin 8 : Interrupt request pin with rising/falling edge programmable.
PE2 TI9 INT9	1	I/O Input Input	Port E2 : I/O port Timer input 9 : Inputs 16-bit timer 8. Interrupt request pin 9 : Interrupt request pin at rising edge.
PE4 TOA	1	I/O Output	Port E4 : I/O port Timer output A : Outputs 16-bit timer A.
PE5 TIA INTA	1	I/O Input Input	Port E5 : I/O port Timer input A : Inputs 16 bit timer A. Interrupt request pin A : Interrupt request pin with rising/falling edge programmable.
PE6 TIB INTB	1	I/O Input Input	Port E6 : I/O port Timer input B : Inputs 16-bit timer A. Interrupt request pin B : Interrupt request pin at rising edge.

Pin Name	Number of Pins	I/O	Functions
PF0 TXD0	1	I/O Output	Port F0 : I/O port Serial transmit data 0 (open drain output possible)
PF1 RXD0	1	I/O Input	Port F1 : I/O port Serial receive data 0
PF2 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port F2 : I/O port Serial transmit enable 0 Serial clock I/O 0
PF4 TXD1	1	I/O Output	Port F4 : I/O port Serial transmit data 1 (open drain output possible)
PF5 RXD1	1	I/O Input	Port F5 : I/O port Serial receive data 1
PF6 $\overline{CTS1}$ SCLK1	1	I/O Input I/O	Port F6 : I/O port Serial transmit enable 1 Serial clock I/O 1
PG0 to PG7 AN0 to AN7	8	Input Input	Port G : Input port Analog input : Input 10-bit A/D converter.
DAOUT0	1	Output	D/A output 0 : Outputs 8-bit D/A converter 0.
DAOUT1	1	Output	D/A output 1 : Outputs 8-bit D/A converter 1.
PH0 TC0	1	I/O Output	Port H0 : I/O port Terminal count 0 : When micro DMA channel 0 count value reaches 0, outputs high strobe signal.
PH1 TC1	1	I/O Output	Port H1 : I/O port Terminal count 1 : When micro DMA channel 1 count value reaches 0, outputs high strobe signal.
PH2 TC2	1	I/O Output	Port H2 : I/O port Terminal count 2 : When micro DMA channel 2 count value reaches 0, outputs high strobe signal.
PH3 TC3	1	I/O Output	Port H3 : I/O port Terminal count 3 : When micro DMA channel 3 count value reaches 0, outputs high strobe signal.
PH4 INT0	1	I/O Input	Port H4 : I/O port (Schmitt input) Interrupt request pin 0 : Interrupt request pin (Schmitt input) with level or rising edge programmable.
PZ0 to PZ7	8	I/O	Port Z : I/O port
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin : Interrupt request pin at falling edge. Interrupt request at rising edge enabled by program. (Schmitt input).
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin

Pin Name	Number of Pins	I/O	Functions
AM0 to 1	2	Input	Address mode : Select starting external data bus width after reset release. AM1 = 0, AM0 = 0 : Started with 8-bit external data bus. AM1 = 0, AM0 = 1 : Started with 16-bit external data bus. AM1 = 1, AM0 = 0 : Started with 32-bit external data bus. AM1 = 1, AM0 = 1 : Started from built-in ROM.
TEST0 to 1	2	Input	Test : Used fixed to GND.
CLK	1	Output	Clock : Outputs system clock.
X1/X2	2	I/O	Oscillator connecting pins
$\overline{\text{RESET}}$	1	Input	Reset : Initializes the device. (with pull-up resistor, Schmitt input)
VREFH	1	Input	Reference voltage input pin for 10-bit A/D converter (H)
VREFL	1	Input	Reference voltage input pin for 10-bit A/D converter (L)
DAREFH	1	Input	Reference voltage input pin for 8-bit D/A converter (H)
DAREFL	1	Input	Reference voltage input pin for 8-bit D/A converter (L)
ADVCC	1	———	10-bit A/D converter power pin
ADVSS	1	———	10-bit A/D converter GND pin (0 V)
DAVCC	1	———	8-bit D/A converter power pin
DAVSS	1	———	8-bit D/A converter GND pin (0 V)
CLVCC	1	———	Clock doubler power pin
CLVSS	1	———	Clock doubler GND pin
DVCC	8	———	Digital power pins (+ 5 V)
DVSS	8	———	Digital GND pins (0 V)

3. DESCRIPTION OF OPERATION

This section describes the functions and basic operation of the TMP94CS40.
The CUP functions and the built-in I/O functions of the TMP94CS40 are the same as those of the TMP94C241A. For functions not covered here, refer to the documentation for the TMP94C241A.

3.1 CPU

The TMP94CS40 incorporates a high-performance, high-speed 32-bit CPU,
TLCS-900/H2 CPU. For details of the CPU, see Chapter 3, TLCS-900/H2 CPU.
This section describes mostly CPU functions specific to the TMP94CS40.

3.1.1 SELECTION OF STARTING BUS

The TMP94CS40 can select the external data bus width after reset release by setting the AM0 and AM1 pins as listed below :

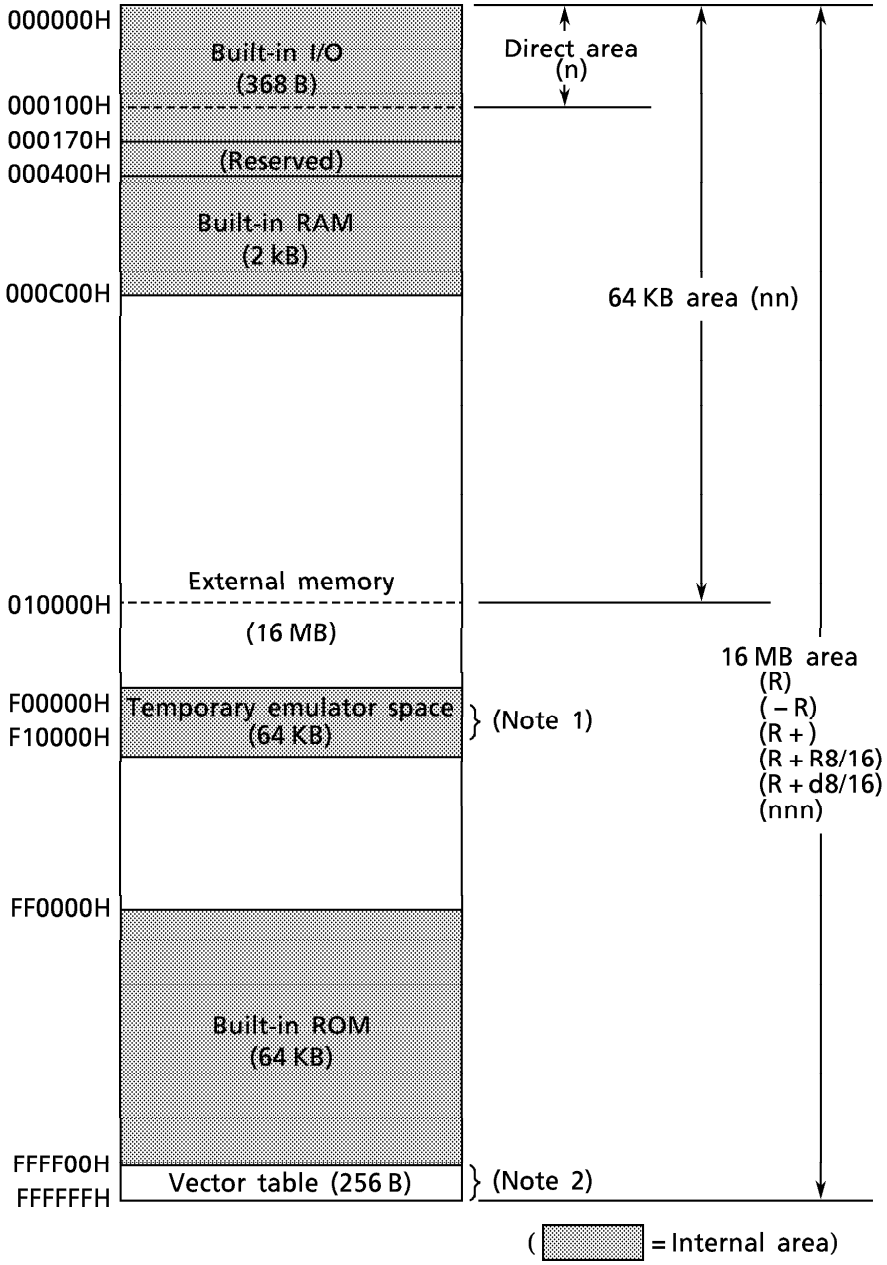
AM1	AM0	Operation after reset release
"0"	"0"	Started with 8-bit data bus
"0"	"1"	Started with 16-bit data bus
"1"	"0"	Started with 32-bit data bus
"1"	"1"	Started from built-in ROM

The settings of the AM0 and AM1 pins are also used to set the data bus width for the address area controlled by the memory controller CS2 pin.
Note that external memory with a data bus whose width is other than those set by the AM0 and AM1 pins can also be connected. For details, see the chapter on Memory Controller for the TMP94C241A.

After reset release, the number of waits for the external memory bus is 1 and access is 3-clock (bus cycle of 150 ns @20 MHz internally). The number of waits can be changed by setting the wait controller register for the memory controller.
If the device is started from the built-in ROM, the device operates using a 32-bit bus and 2-1-1-1 access interleaving.

3.2 MEMORY MAP

Figure 3.2 shows the TMP94CS40 memory map.



(Note 1) Since any 64 KB in the 16 MB space can be used to control the emulator, the user cannot use this space when using the emulator. After reset, the area for controlling the emulator is temporarily mapped to F00000H to F10000H. The user can change mapping addresses as required.

(Note 2) The last 16 B space (FFFFF0H to FFFFFFH) is reserved as an internal area so the user cannot use this space.

Figure 3.2 TMP94CS40 Memory Map

4. ELECTRICAL CHARACTERISTICS (TENTATIVE)

4.1 MAXIMUM RATINGS

TENTATIVE

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	− 0.5~6.5	V
V_{IN}	Input Voltage	− 0.5~Vcc + 0.5	V
ΣI_{OL}	Output Current (Total)	120	mA
ΣI_{OH}	Output Current (Total)	− 120	mA
P_D	Power Dissipation (Ta = 70°C)	600	mW

4.2 DC CHARACTERISTICS

Vcc = 5 V ± 10%, Ta = − 20 to 70°C (X1 = 8 to 10 MHz, operates at double the frequency: 16 to 20 MHz internally.)

Typical values are when Vcc = 5 V and Ta = 25°C.

TENTATIVE

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IL0}	Input Low Voltage P00 - P07 (D0 – 7) P10 - P17 (D8 – 15) P20 - P27 (D16 – 23) P30 - P37 (D24 – 31)	− 0.3	0.8	V	
V_{IL1}	Input Low Voltage P40 - P47 P50 - P57 P60 - P67 P75 P86 PC0 - PC1 PD0 - PD2, PD4 - PD6 PE0 - PE2, PE4 - PE6 PF0 - PF2, PF4 - PF6 PG0 - PG7 PH0 - PH3 PZ0 - PZ7	− 0.3	0.3*Vcc	V	
V_{IL2}	Input Low Voltage PH4 (INT0) $\overline{NMI}$ $\overline{RESET}$	− 0.3	0.25*Vcc	V	
V_{IL3}	Input Low Voltage AM0 - AM1 TEST0 - TEST1	− 0.3	0.3	V	
V_{IL4}	Input Low Voltage X1	− 0.3	0.2*Vcc	V	
V_{IH0}	Input High Voltage P00 - P07 (D0 – 7) P10 - P17 (D8 – 15) P20 - P27 (D16 – 23) P30 - P37 (D24 – 31)	2.2	Vcc + 0.3	V	

TENTATIVE

Symbol	Parameter	Min	Max	Unit	Test Condition
V IH1	Input High Voltage P40 - P47 P50 - P57 P60 - P67 P75 P86 PC0 - PC1 PD0 - PD2, PD4 - PD6 PE0 - PE2, PE4 - PE6 PF0 - PF2, PF4 - PF6 PG0 - PG7 PH0 - PH3 PZ0 - PZ7	0.7*Vcc	Vcc + 0.3	V	
V IH2	Input High Voltage $\overline{\text{PH4}}$ (INT0) $\overline{\text{NMI}}$ $\overline{\text{RESET}}$	−0.75*Vcc	Vcc + 0.3	V	
V IH3	Input High Voltage AM0 - AM1 TEST0 - TEST1	Vcc−0.3	Vcc + 0.3	V	
V IH4	Input High Voltage X1	0.8*Vcc	Vcc + 0.3	V	
V OL	Output Low Voltage		0.45	V	IOL = 1.6 mA
V OH0	Output High Voltage	2.4		V	IOH = − 400 μA
V OH1	Output High Voltage	0.75*Vcc		V	IOH = − 100 μA
V OH2	Output High Voltage	0.9*Vcc		V	IOH = − 20 μA
I LI	Input Leakage Current	0.02 (typ.)	± 5	μA	0.0 V ≦ Vin ≦ Vcc
I LO	Output Leakage Current	0.05 (typ.)	± 10	μA	0.2 V ≦ Vin ≦ Vcc − 0.2 V
I cc0	Operating Current (RUN)	TBD (typ.)	TBD	mA	X1 = 10 MHz (Internally 20 MHz)
I cc1	Operating Current (IDLE)	TBD (typ.)	TBD	mA	X1 = 10 MHz (Internally 20 MHz)
I cc2	Operating Current (STOP)	TBD (typ.)	50	μA	0.2 V ≦ Vin ≦ Vcc − 0.2 V Ta = − 20~70C°
I cc3	Operating Current (STOP)	TBD (typ.)	10	μA	0.2 V ≦ Vin ≦ Vcc − 0.2 V Ta = 0~50C°
V STOP	Power Down Voltage @STOP Voltage which can retain internal states of device (eg, registers, RAM)	2.0	6.0	V	VIL2 = 0.2*Vcc VIH2 = 0.8*Vcc
RRST	Pull Up Resistance $\overline{\text{RESET}}$	50	150	kΩ	
CIO	Pin Capacitance		10	pF	fc = 1 MHz
VTH	Schmitt Width $\overline{\text{PH4}}$ (INT0) $\overline{\text{NMI}}$ $\overline{\text{RESET}}$	0.4	1.0 (typ.)	V	

4.3 AC CHARACTERISTICS

4.3.1 BASIC BUS CYCLES

TENTATIVE

(1) Read cycle Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

No.	Symbol	Parameter	Min	Max	@20 MHz	@16 MHz	Unit
1	t_{OSC}	Oscillation cycle (X1/X2 pin)	100	125	100	125	ns
2	t_{CYC}	System clock cycle (= T)	50	62.5	50	62.5	ns
3	t_{CL}	CLK low pulse width	0.5 × T-15		10	16	ns
4	t_{CH}	CLK high pulse width	0.5 × T-15		10	16	ns
5-1	t_{AD}	A0 to A23 valid → D0 to D31 input @0 wait		2.0 × T-50	50	75	ns
5-2	t_{AD3}	A0 to A23 valid → D0 to D31 input @1 wait		3.0 × T-50	100	138	ns
6-1	t_{RD}	$\overline{RD}$ fall → D0 to D31 input @0 wait		1.5 × T-45	30	49	ns
6-2	t_{RD3}	$\overline{RD}$ fall → D0 to D31 input @1 wait		2.5 × T-45	80	111	ns
7-1	t_{RR}	$\overline{RD}$ low pulse width @0 wait	1.5 × T-20		55	74	ns
7-2	t_{RR3}	$\overline{RD}$ low pulse width @1 wait	2.5 × T-20		105	136	ns
8	t_{AR}	A0 to A23 valid → $\overline{RD}$ fall	0.5 × T-20		5	11	ns
9	t_{RK}	$\overline{RD}$ fall → CLK fall	0.5 × T-20		5	11	ns
10	t_{HA}	A0 to A23 valid → D0 to D31 hold	0		0	0	ns
11	t_{HR}	$\overline{RD}$ rise → D0 to D31 hold	0		0	0	ns
12	t_{APR}	A0 to A23 valid → port input		2.0 × T-70	30	55	ns
13	t_{APH}	A0 to A23 valid → port hold	2.0 × T		100	125	ns
14	t_{TK}	$\overline{WAIT}$ setup time	40		40	40	ns
15	t_{KT}	$\overline{WAIT}$ hold time	0		0	0	ns

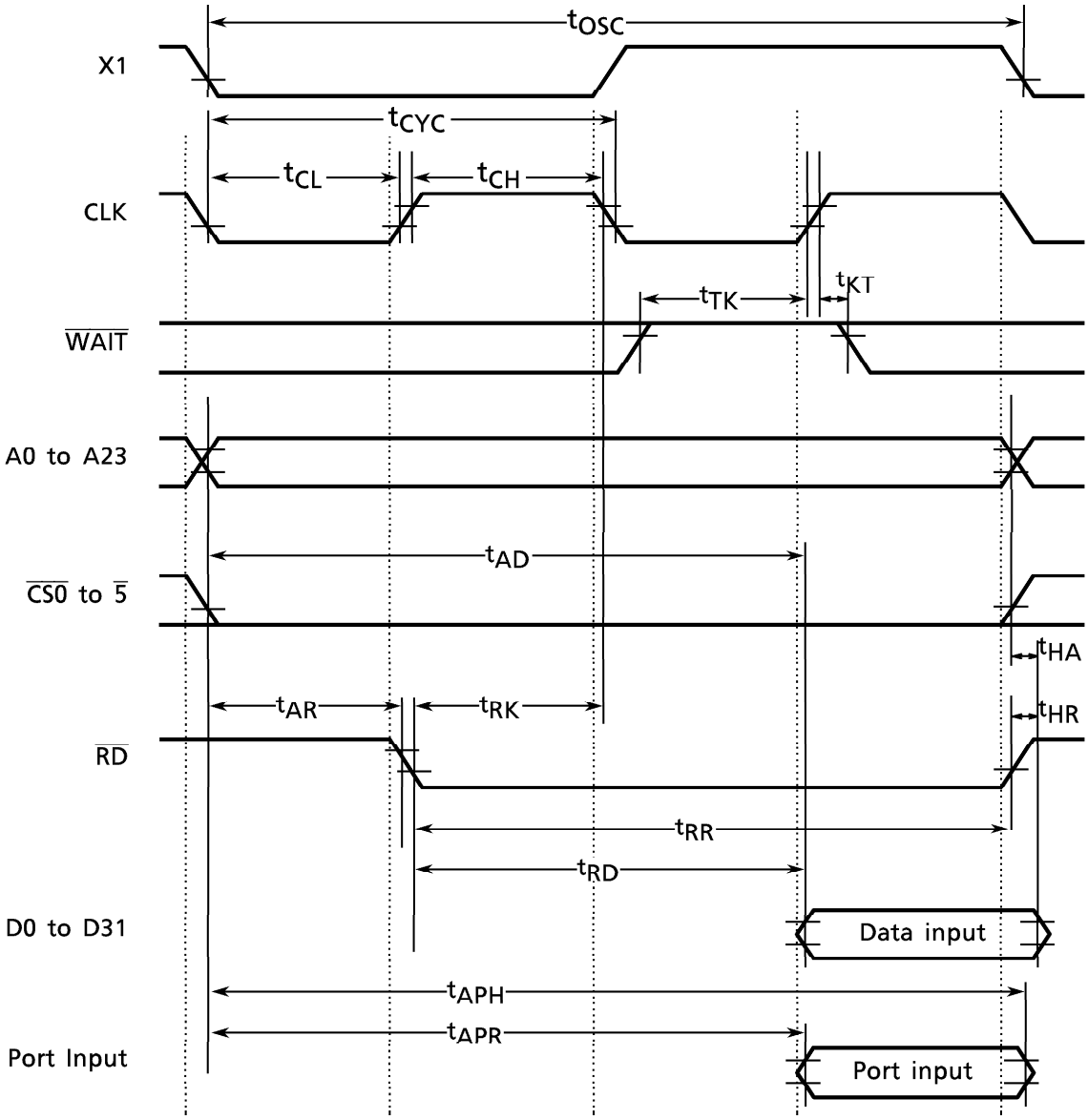
(2) Write cycle Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

No.	Symbol	Parameter	Min	Max	@20 MHz	@16 MHz	Unit
1	t_{OSC}	Oscillation cycle (X1/X2 pin)	100	125	100	125	ns
2	t_{CYC}	System clock cycle (= T)	50	62.5	50	62.5	ns
3	t_{CL}	CLK low pulse width	0.5 × T-15		10	16	ns
4	t_{CH}	CLK high pulse width	0.5 × T-15		10	16	ns
5-1	t_{DW}	D0 to D31 valid → $\overline{WRxx}$ rise @0 wait	1.25 × T-35		28	43	ns
5-2	t_{DW3}	D0 to D31 valid → $\overline{WRxx}$ rise @1 wait	2.25 × T-35		78	106	ns
6-1	t_{WW}	$\overline{WRxx}$ low pulse width @0 wait	1.25 × T-30		33	48	ns
6-2	t_{WW3}	$\overline{WRxx}$ low pulse width @1 wait	2.25 × T-30		83	111	ns
7	t_{AW}	A0 to A23 valid → $\overline{WRxx}$ fall	0.5 × T-20		5	11	ns
8	t_{WK}	$\overline{WRxx}$ fall → CLK fall	0.5 × T-20		5	11	ns
9	t_{WA}	$\overline{WRxx}$ rise → A0 to A23 hold	0.25 × T-5		8	11	ns
10	t_{WD}	$\overline{WRxx}$ rise → D0 to D31 hold	0.25 × T-5		8	11	ns
11	t_{APW}	A0 to A23 valid → port output		2.0 × T + 70	170	195	ns
12	t_{TK}	$\overline{WAIT}$ setup time	40		40	40	ns
13	t_{KT}	$\overline{WAIT}$ hold time	0		0	0	ns

AC test conditions

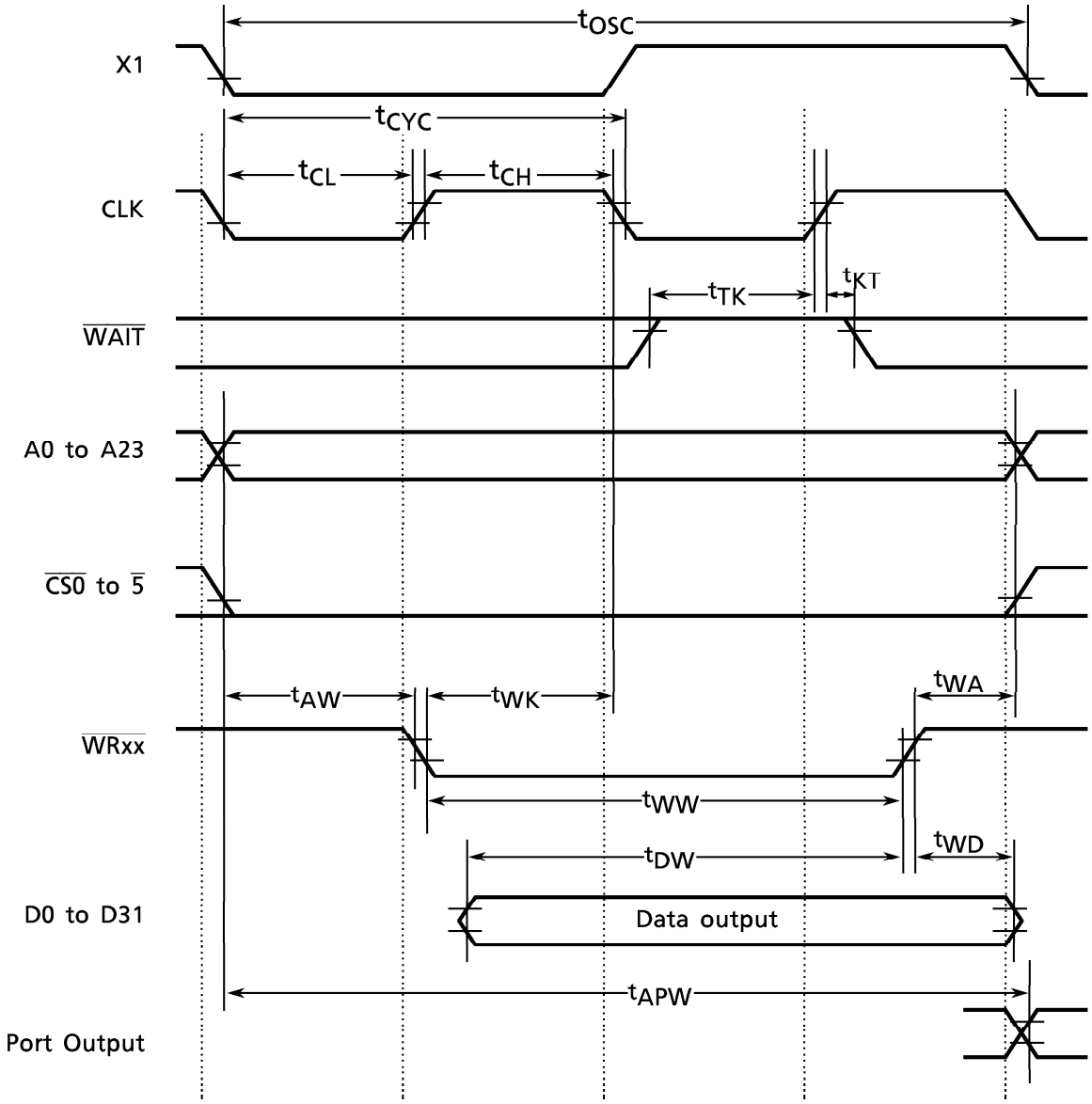
- Output level : P0-P3 (D0-D31), P4-P6 (A0-A23), P70 ($\overline{RD}$), P71-P74 ($\overline{WRxx}$)
  High 2.0 V, Low 0.8 V, CL = 50 pF
  Other than above pins
  High 2.0 V, Low 0.8 V, CL = 50 pF
- Input level : P0-P3 (D0-D31)
  High 2.4 V, Low 0.45 V
  Other than above pins
  High 0.8 × Vcc, Low = 0.2 × Vcc

(1) Read cycle (0 wait)



(Note) The phase relationship between X1 input signal and other signals are undefined. The above chart is an example.

(2) Write cycle (0 wait)

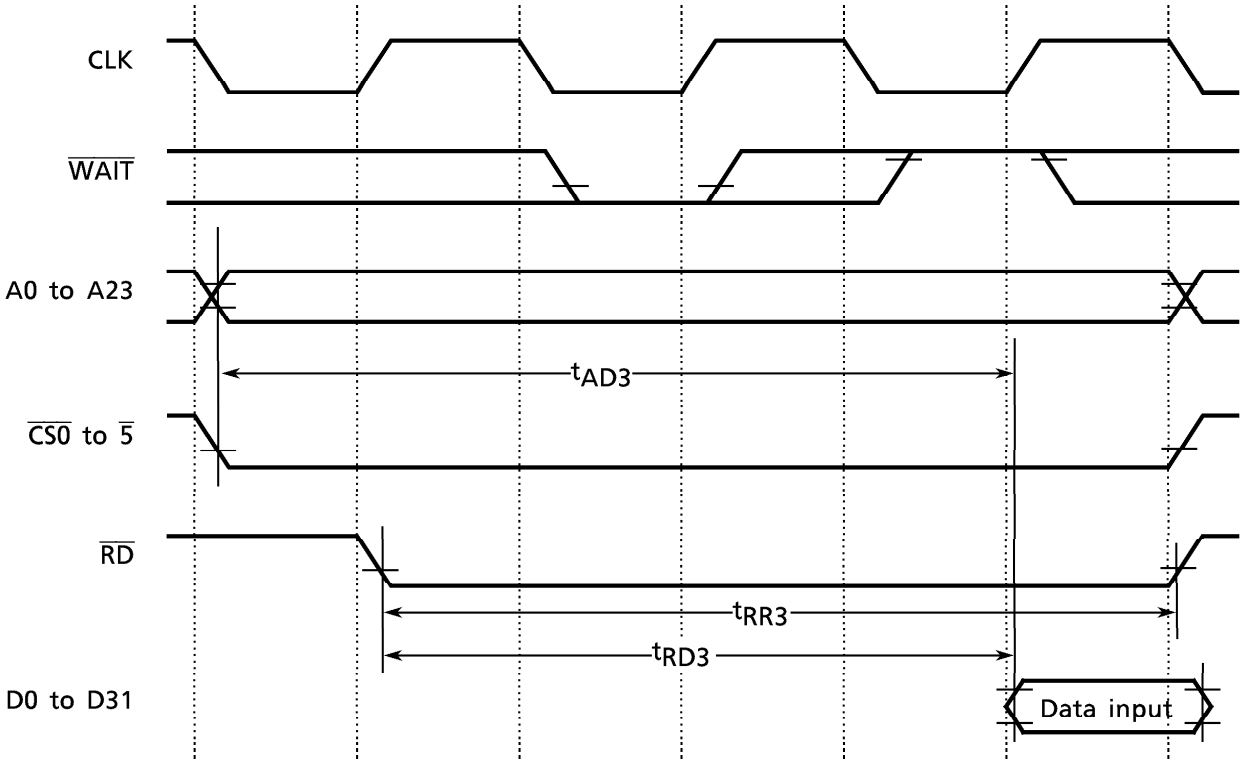


(Note) The phase relationship between X1 input signal and other signals are undefined. The above chart is an example.

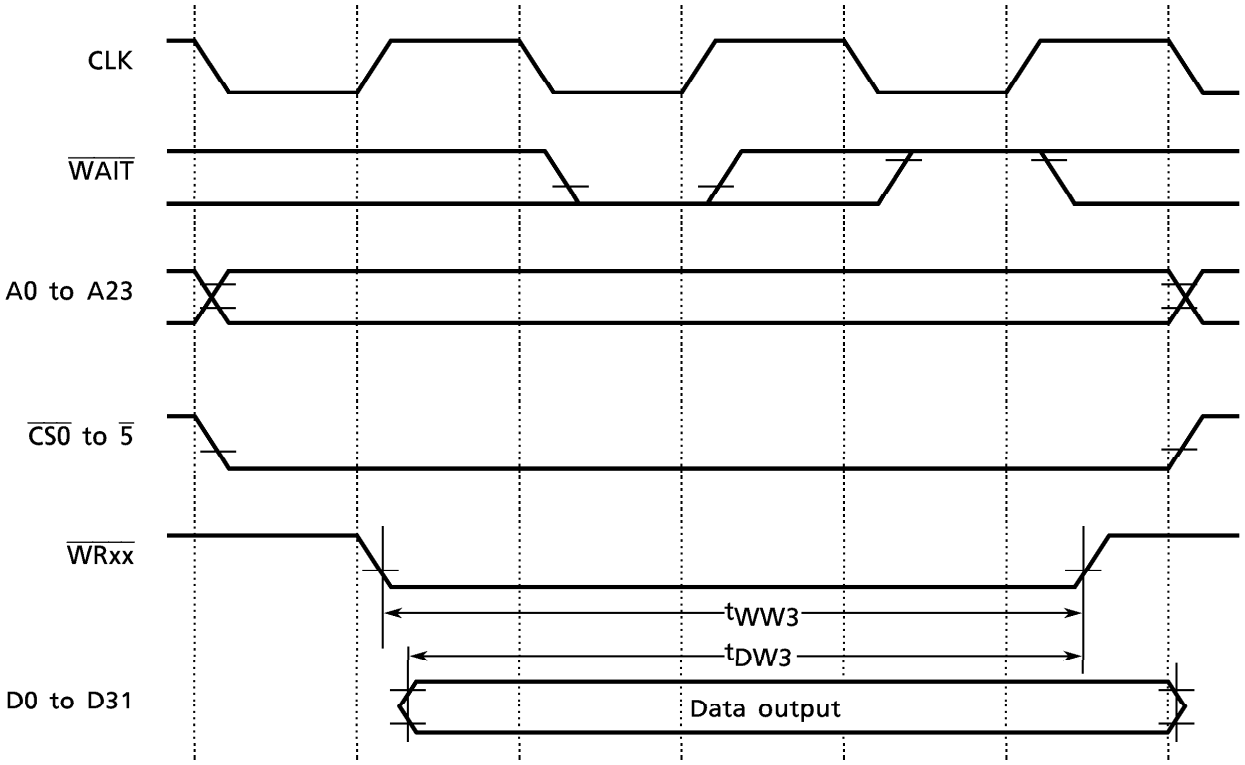
Supplementary:

WRxx represents WRLL, WRLH, WRHL, and WRHH.

(3) Read cycle (1 wait)



(4) Write cycle (1 wait)



4.3.2 PAGE ROM READ CYCLE

(1) 3-2-2-2 mode

TENTATIVE

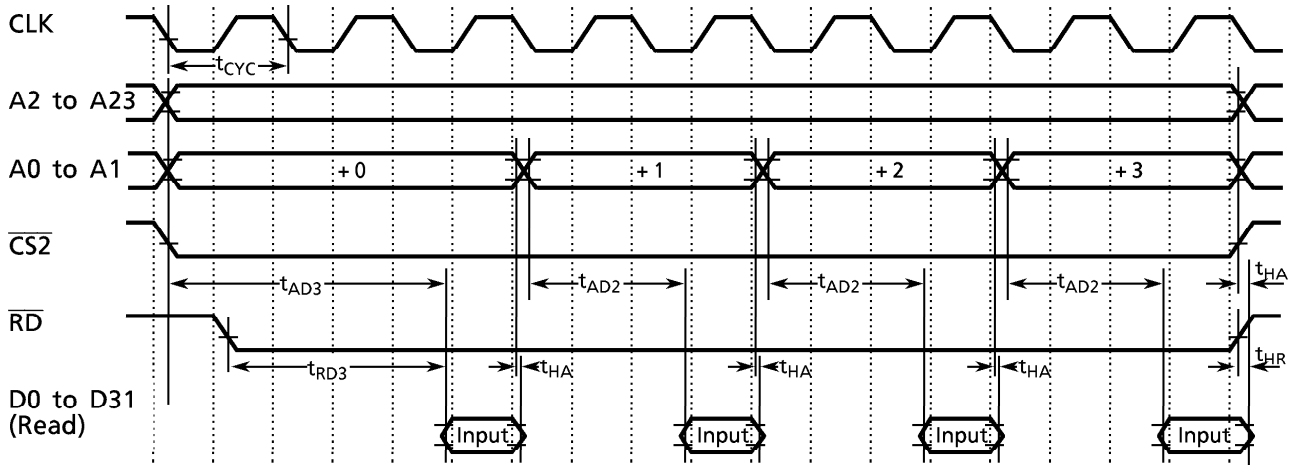
Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

No.	Symbol	Parameter	Min	Max	@20 MHz	@16 MHz	Unit
1	t_{CYC}	System clock cycle (= T)	50	62.5	50	62.5	ns
2	t_{AD2}	A0 to A1 valid → D0 to D31 input		2.0 × T-50	50	75	ns
3	t_{AD3}	A2 to A23 valid → D0 to D31 input		3.0 × T-50	100	138	ns
4	t_{RD3}	$\overline{RD}$ fall → D0 to D31 input		2.5 × T-45	80	111	ns
5	t_{HA}	A0 to A23 invalid → D0 to D31 hold	0		0	0	ns
6	t_{HR}	$\overline{RD}$ rise → D0 to D31 hold	0		0	0	ns

AC test conditions

- Output level : P4-P6 (A0-A23), P70 ($\overline{RD}$)
  High 2.0 V, Low 0.8 V, CL = 50 pF
  CLK, P82 ($\overline{CS2}$)
  High 2.0 V, Low 0.8 V, CL = 50 pF
- Input level : P0-P3 (D0-D31)
  High 2.4 V, Low 0.45 V

(1) Page ROM read cycle (3-2-2-2 mode)



4.3.3 DRAM BUS CYCLES

TENTATIVE

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

No.	Symbol	Parameter	Min	Max	@ 20 MHz	@ 16 MHz	Unit
1	t_{CYC}	System clock cycle (= T)	50	62.5	50	62.5	ns
2	t_{RC}	$\overline{RAS}$ cycle time	3.00 × T		150	188	ns
3	t_{PC}	Page mode cycle time	2.00 × T		100	125	ns
4-1	t_{RAC}	$\overline{RAS}$ access time		1.75 × T-45	43	64	ns
4-2	t_{RAC4}	$\overline{RAS}$ access time (at 4-clock access)		2.75 × T-45	93	127	ns
5	t_{CAC}	$\overline{CAS}$ access time		1.00 × T-40	10	23	ns
6-1	t_{AA}	Column address access time		1.25 × T-45	18	33	ns
6-2	t_{AA2}	Column address access time (in page mode)		2.00 × T-45	55	80	ns
6-3	t_{AA4}	Column address access time (at 4-clock access)		2.25 × T-45	68	96	ns
7	t_{CPA}	$\overline{CAS}$ precharge access time		2.00 × T-45	55	80	ns
8	t_{OFF}	Input data hold time	0		0	0	ns
9	t_{RP}	$\overline{RAS}$ precharge time	1.25 × T-20		43	58	ns
10-1	t_{RAS}	$\overline{RAS}$ pulse width	1.75 × T-20		68	89	ns
10-2	t_{RAS4}	$\overline{RAS}$ pulse width (at 4-clock access)	2.75 × T-20		118	152	ns
11	t_{RSH}	$\overline{RAS}$ hold time	1.00 × T-20		30	43	ns
12	t_{RHCP}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	2.00 × T-20		80	105	ns
13-1	t_{CSH}	$\overline{CAS}$ hold time	1.75 × T-20		68	89	ns
13-2	t_{CSH4}	$\overline{CAS}$ hold time (at 4-clock access)	2.75 × T-20		118	152	ns
14	t_{CAS}	$\overline{CAS}$ pulse width	1.00 × T-20		30	43	ns
15	t_{RCD}	$\overline{RAS}$ - $\overline{CAS}$ delay time	0.75 × T-17		21	30	ns
16	t_{RAD}	$\overline{RAS}$ - column address delay time		0.50 × T + 20	45	51	ns
17	t_{CRP}	$\overline{CAS}$ - $\overline{RAS}$ precharge time	1.25 × T-20		43	58	ns
18-1	t_{CP}	$\overline{CAS}$ precharge time (at refresh)	0.50 × T-15		10	16	ns
18-2	t_{CP2}	$\overline{CAS}$ precharge time (in page mode)	1.00 × T-20		30	43	ns
19	t_{ASR}	Low address setup time	1.25 × T-40		23	38	ns
20	t_{RAH}	Low address hold time	0.50 × T-15		10	16	ns
21-1	t_{ASC}	Column address setup time	0.25 × T-12		1	4	ns
21-2	t_{ASC2}	Column address setup time (in page mode)	1.00 × T-20		30	43	ns
22	t_{CAH}	Column address hold time	1.00 × T-20		30	43	ns
23	t_{AR}	Column address hold time ($\overline{RAS}$ as reference)	1.75 × T-20		68	89	ns
24	t_{RAL}	Column address $\overline{RAS}$ read time	1.25 × T-20		43	58	ns
25	t_{RCS}	Read command setup time	2.00 × T-40		60	85	ns
26	t_{RCH}	Read command hold time ($\overline{CAS}$ as reference)	0.50 × T-20		5	11	ns
27	t_{RRH}	Read command hold time ($\overline{RAS}$ as reference)	0.50 × T-20		5	11	ns
28	t_{WCH}	Write command hold time	1.00 × T-20		30	43	ns
29	t_{WCR}	Write command hold time ($\overline{RAS}$ as reference)	1.75 × T-20		68	89	ns
30	t_{WP}	Write command pulse time	1.50 × T-20		55	74	ns
31	t_{RWL}	Write command $\overline{RAS}$ read time	1.50 × T-20		55	74	ns
32	t_{CWL}	Write command $\overline{CAS}$ read time	1.50 × T-20		55	74	ns
33	t_{DS}	Data output setup time	1.00 × T-30		20	33	ns
34	t_{DH}	Data output hold time	1.00 × T-25		25	38	ns
35	t_{DHR}	Data output hold time ($\overline{RAS}$ as reference)	1.75 × T-5		83	104	ns
36	t_{WCS}	Write command setup time	0.50 × T-20		5	11	ns
37	t_{CSR}	$\overline{CAS}$ setup time	0.75 × T-20		18	27	ns
38	t_{CHR}	$\overline{CAS}$ hold time	1.75 × T-20		68	89	ns
39	t_{RPC}	$\overline{RAS}$ precharge $\overline{CAS}$ active time	0.50 × T-20		5	11	ns
40	t_{ROH}	$\overline{RAS}$ hold time ($\overline{OE}$ as reference)	1.00 × T-20		30	43	ns
41	t_{OEA}	$\overline{OE}$ access time		1.00 × 40	10	23	ns
42	t_{OEZ}	Input data hold time ($\overline{OE}$ as reference)	0		0	0	ns
43	t_{RPS}	$\overline{RAS}$ precharge time (when self-refresh cycle released)	3.25 × T-20		143	183	ns

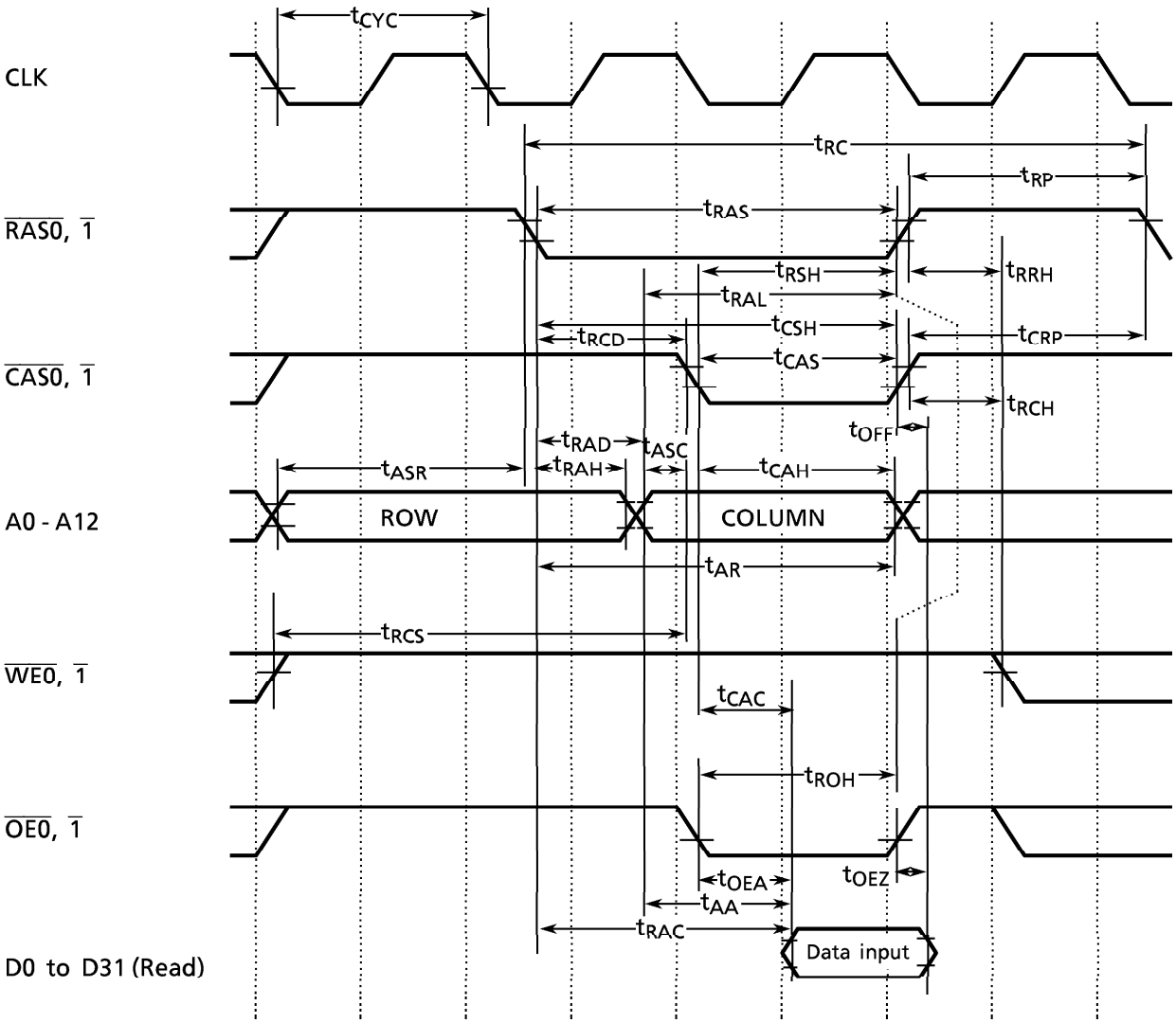
TENTATIVE

No.	Symbol	Parameter	Min	Max	@ 20 MHz	@ 16 MHz	Unit
44	t_{CHS}	$\overline{CAS}$ hold time (when self-refresh cycle released)	– 15		– 15	– 15	ns

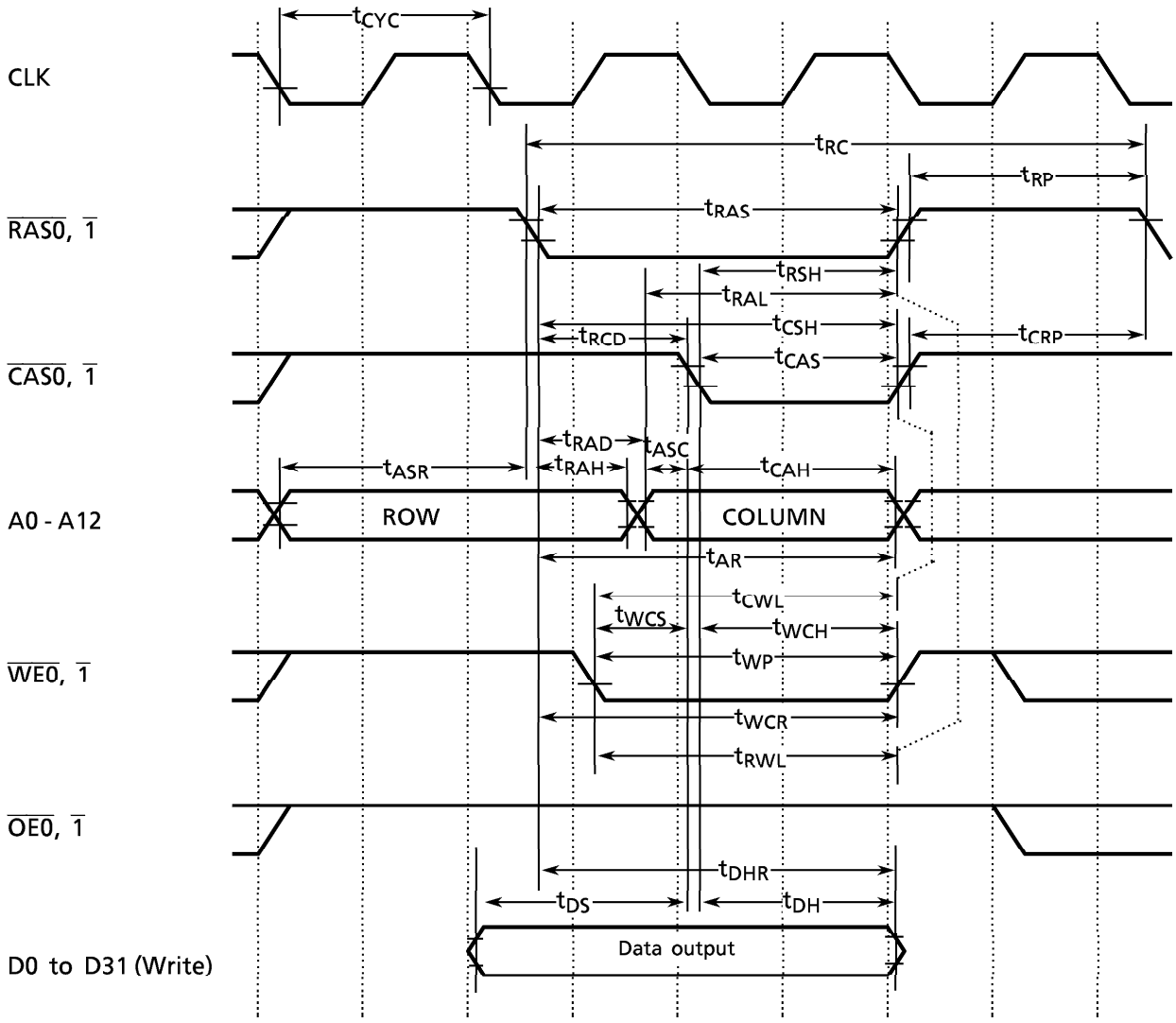
AC test conditions

- Output level : P0-P3 (D0-D31), P4-P6 (A0-A23), P70 ($\overline{RD}$), P71-P74 ($\overline{WRxx}$)
  High 2.0 V, Low 0.8 V, CL = 50 pF
  Other than above pins
  High 2.0 V, Low 0.8 V, CL = 50 pF
- Input level : P0-P3 (D0-D31)
  High 2.4 V, Low 0.45 V
  Other than above pins
  High 0.8 × Vcc, Low = 0.2 × Vcc

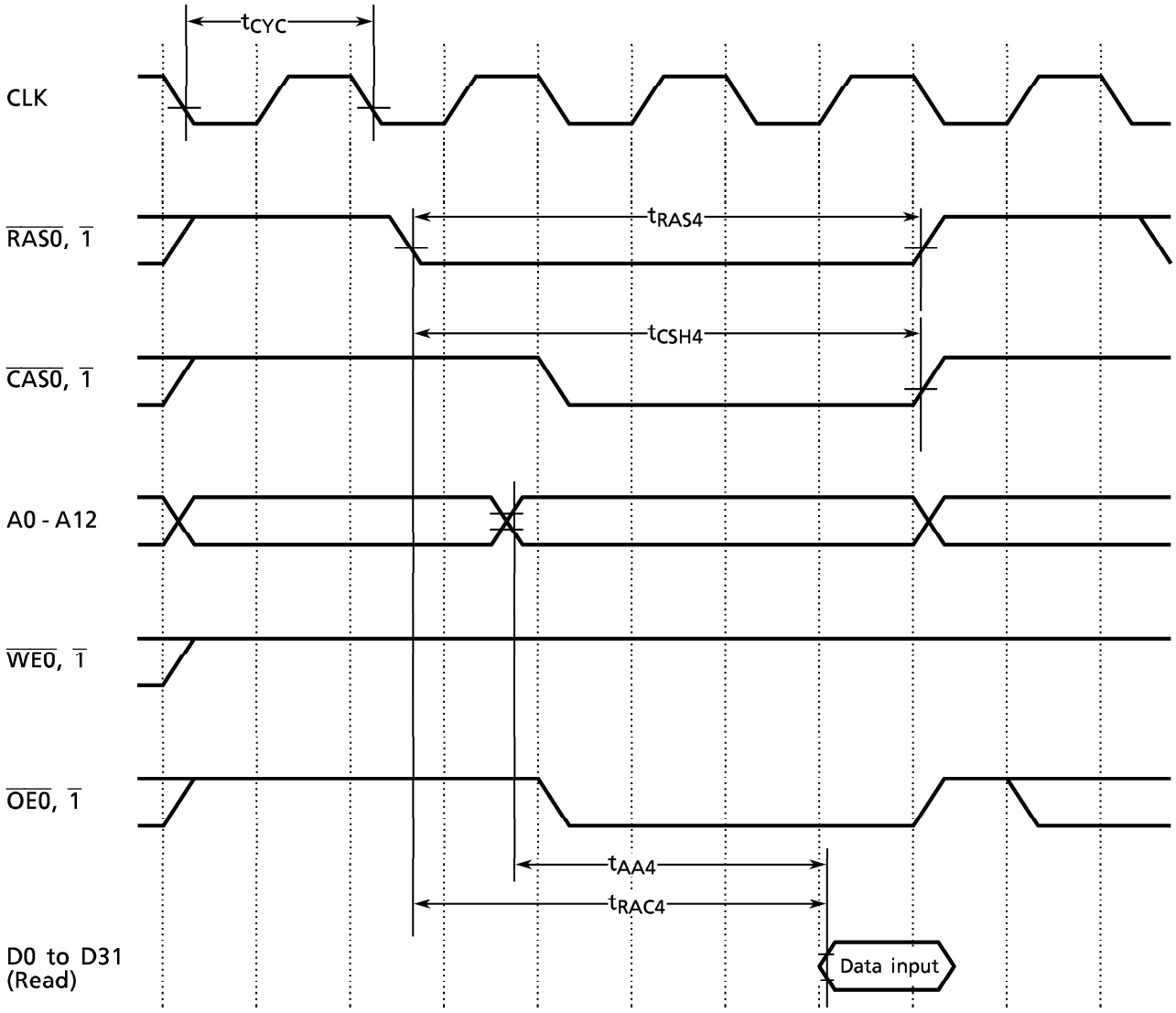
(1) DRAM read cycle (at 3-clock access)



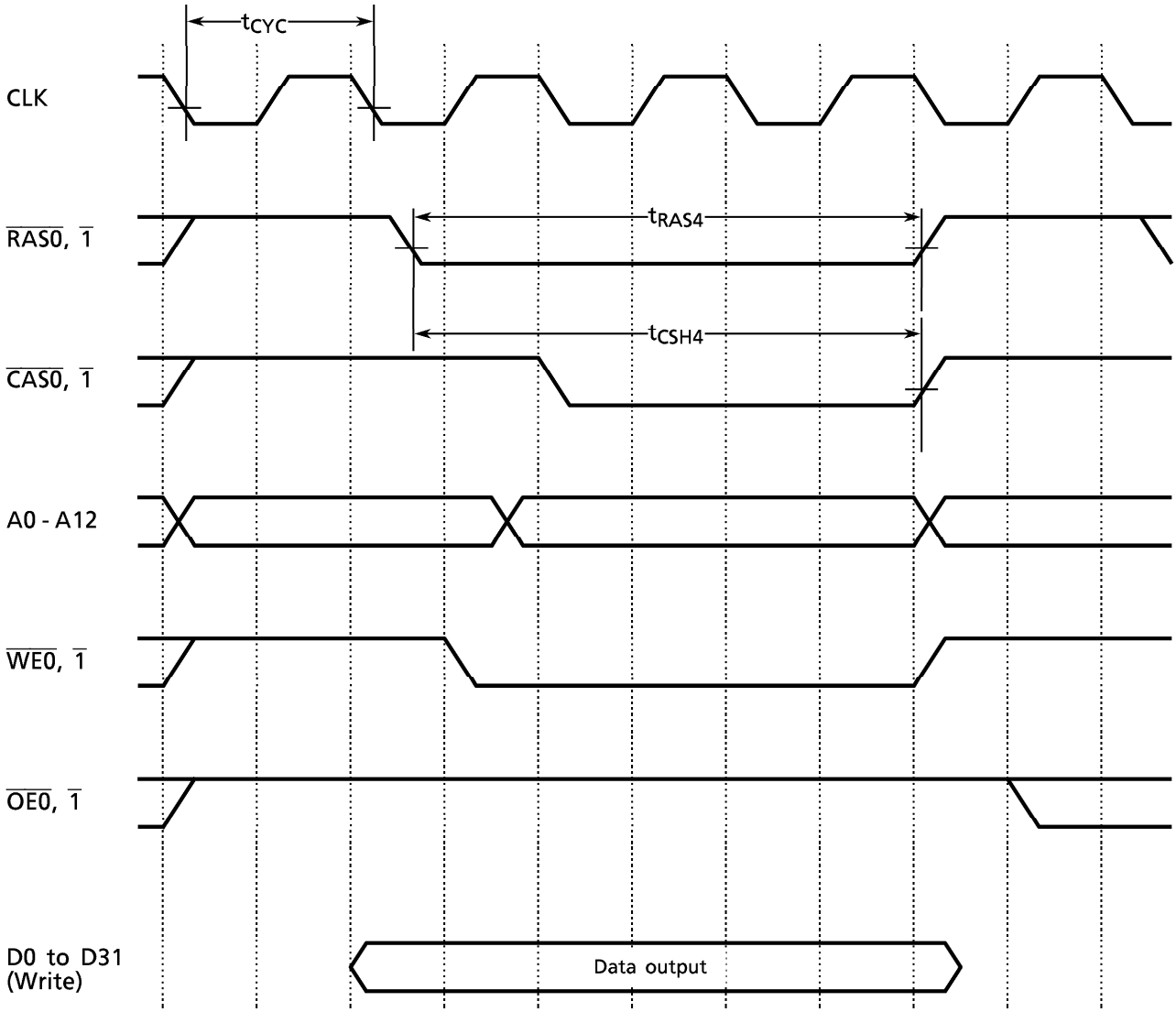
(2) DRAM write cycle (at 3-clock access)



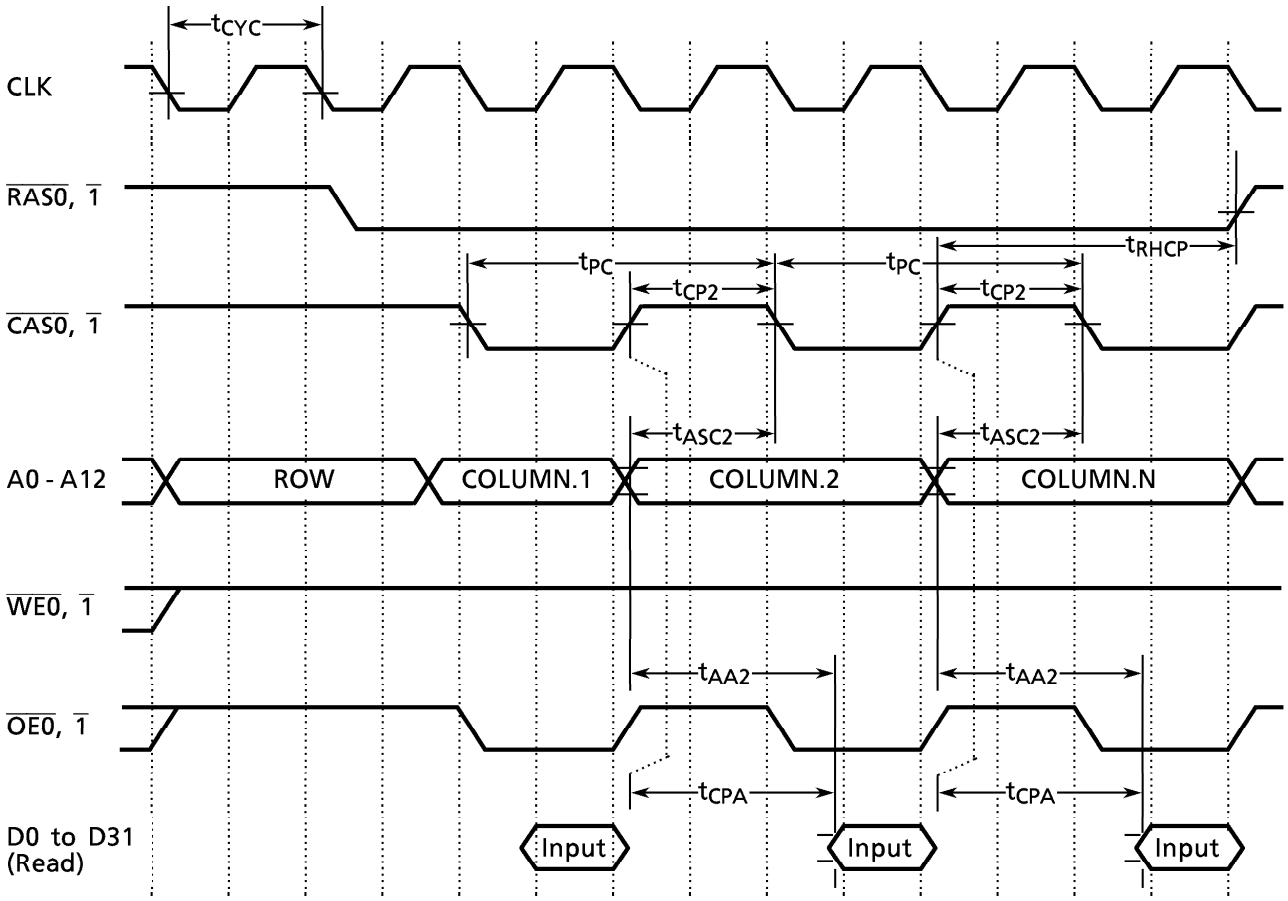
(3) DRAM read cycle (at 4-clock access)



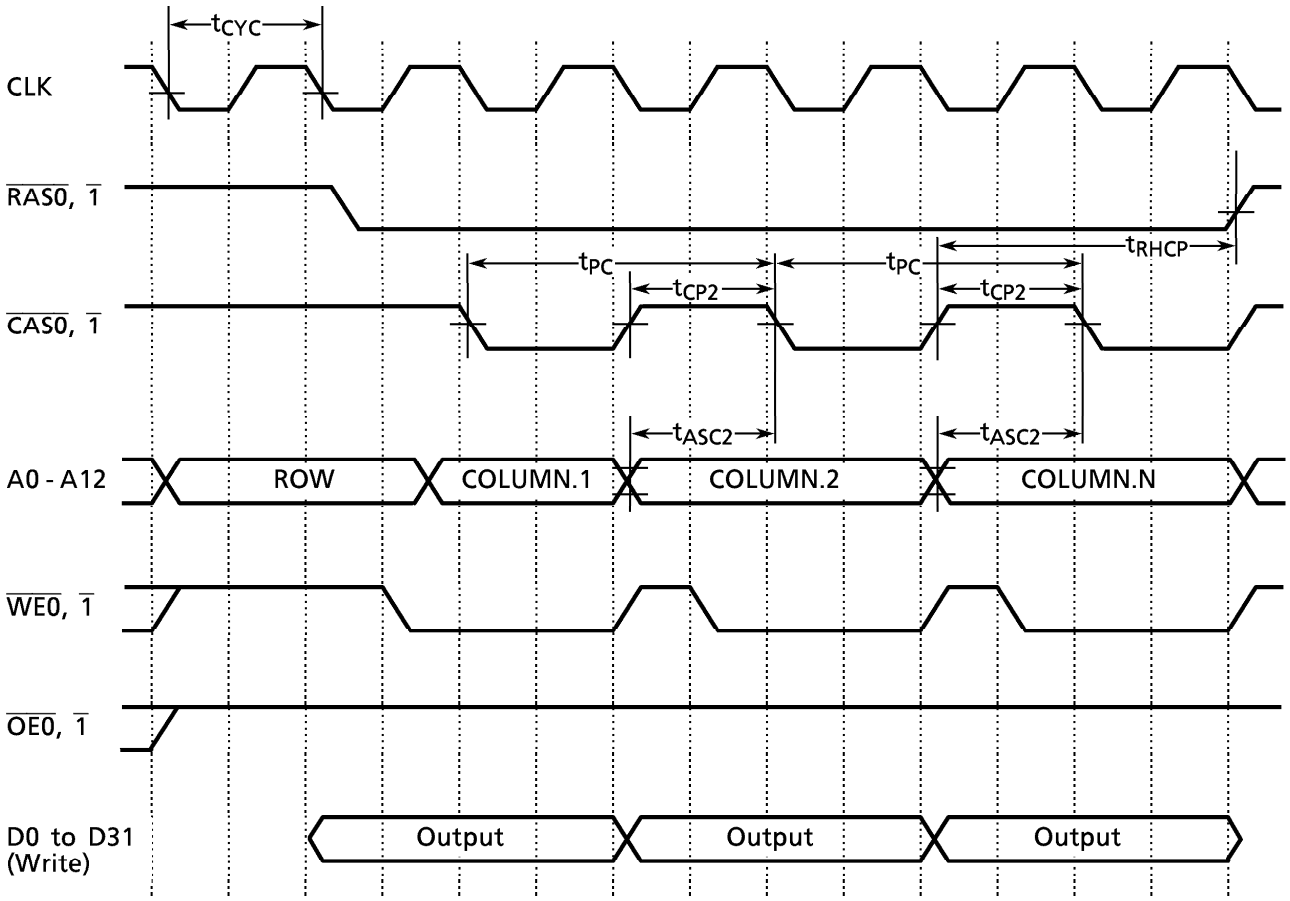
(4) DRAM write cycle (at 4-clock access)



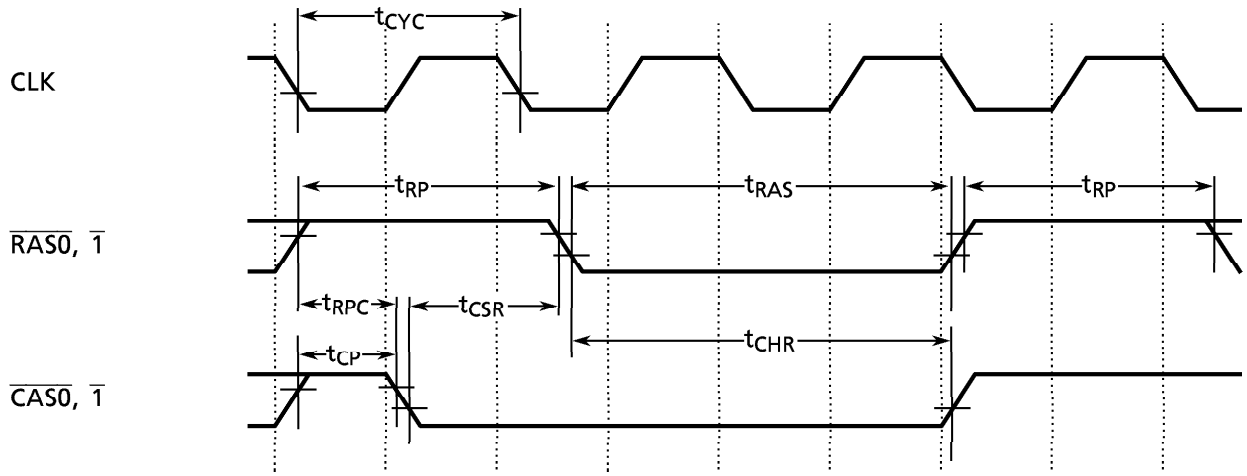
(5) DRAM page mode read cycle (in 3-2-2-2 mode)



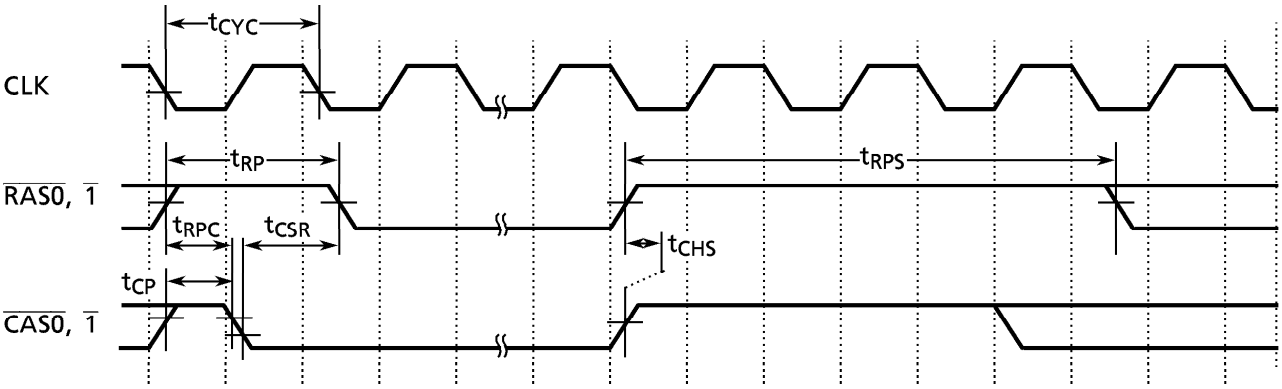
(6) DRAM page mode write cycle (in 3-2-2-2 mode)



(7) DRAM $\overline{CAS}$ before $\overline{RAS}$ interval refresh cycle (in 3-cycle mode)



(8) DRAM $\overline{CAS}$ before $\overline{RAS}$ self-refresh cycle



4.4 EVENT COUNTERS (TI4, TI5, TI6, TI7, TI8, TI9, TIA, TIB)

TENTATIVE

Vcc = 5 V ± 10%, TA = – 20 to 70℃ (Internally 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock cycle	8T + 100		500		600		ns
t_{VCKL}	Clock low-level pulse width	4T + 40		240		290		ns
t_{VCKH}	Clock high-level pulse width	4T + 40		240		290		ns

4.5 SERIAL CHANNEL TIMING

TENTATIVE

(1) SCLK input mode (I/O interface mode)

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16T		0.8		1.0		μs
t_{OSS}	Output data → SCLK rise	t_{SCY}/2 – 5T – 50		100		138		ns
t_{OHS}	SCLK rise output data hold	5T – 100		150		213		ns
t_{HSR}	SCLK rise → input data hold	0		0		0		ns
t_{SRD}	SCLK rise → valid data input		t_{SCY} – 5T – 100		450		588	ns

(2) SCLK output mode (I/O interface mode)

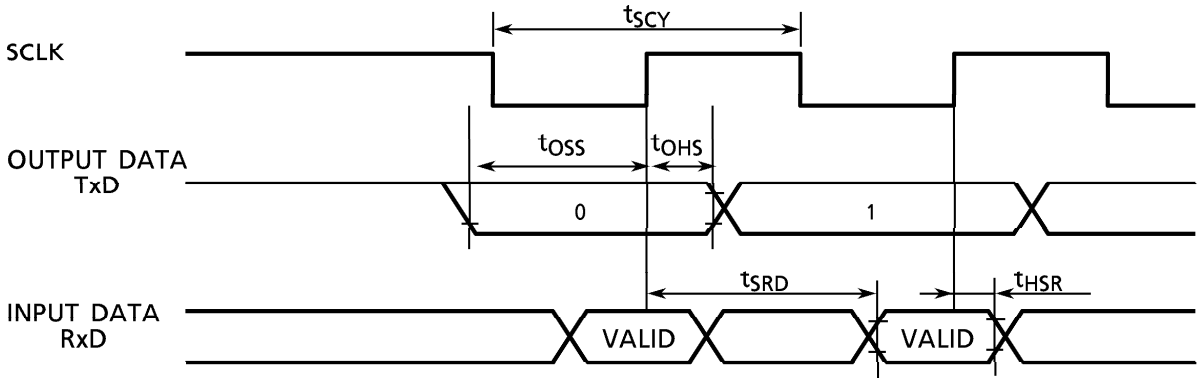
Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16T	8192T	0.8	409.6	1.0	512	μs
t_{OSS}	Output data → SCLK rise	t_{SCY} – 2T – 150		550		725		ns
t_{OHS}	SCLK rise → output data hold	2T – 80		20		45		ns
t_{HSR}	SCLK rise → input data hold	0		0		0		ns
t_{SRD}	SCLK rise → valid data input		t_{SCY} – 2T – 150		550		725	ns

(3) SCLK0 input mode (UART mode)

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	4T + 20		220		270		ns
t_{SCYL}	SCLK low level pulse width	2T + 5		105		130		ns
t_{SCYH}	SCLK high level pulse width	2T + 5		105		130		ns



4.6 10-BIT A/D CONVERTER CHARACTERISTICS

TENTATIVE

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter		Min	Typ	Max	Unit
VREFH	Analog reference voltage (+)		Vcc-0.2 V	Vcc	Vcc	V
VREFL	Analog reference voltage (–)		Vss	Vss	Vss + 0.2 V	
VAIN	Analog input voltage		VREFL		VREFH	
I_{REF} (VREFL = 0 V)	Analog reference voltage supply current					
	Vcc = 5 V ± 10%	<VREFON> = 1		0.5	1.5	mA
	Vcc = 5 V ± 10%	<VREFON> = 0		0.02	5.0	μA
Conversion error	Vcc = 5 V ± 10%	Total error		± 3.0	± 6	LSB

(Note 1) 1LSB = (VREFH__VREFL) / 1024 [V]

(Note 2) The supply current flowing from the AVCC pin is included in the supply current to the digital power pin.

4.7 8-BIT D/A CONVERTER CHARACTERISTICS

TENTATIVE

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DAREFH	Analog reference voltage		4.0		Vcc	V
DAREFL	Analog reference voltage		Vss		Vss	
	Resolution				8	BIT
	Total error	RL = 2.4 kΩ		2.0	TBD	LSB

(Note) RL is the load resistance of the D/A converter output pin.

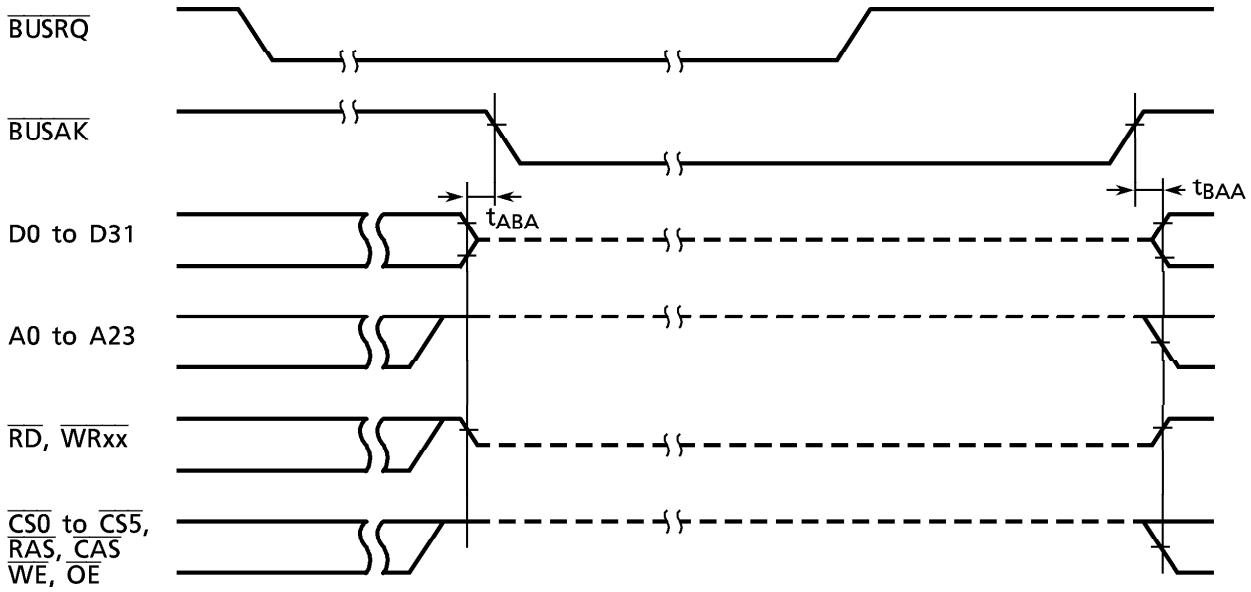
4.8 Interrupt Operation

TENTATIVE

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 low level pulse width	4T		200		250		ns
t_{INTAH}	$\overline{NMI}$, INT0 high level pulse width	4T		200		250		ns
t_{INTBL}	INT4 to INTB low level pulse width	8T + 100		500		600		ns
t_{INTBH}	INT4 to INTB high level pulse width	8T + 100		500		600		ns

4.9 BUS RELEASE TIMING



TENTATIVE

Vcc = 5 V ± 10%, Ta = – 20 to 70°C (Internally 16 to 20 MHz)

Symbol	Parameter	Variable		20 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{ABA}	Time from output buffer off to $\overline{BUSAK}$ fall	0	80	0	80	0	80	ns
t_{BAA}	Time from $\overline{BUSAK}$ rise to output buffer on	0	80	0	80	0	80	ns

(Note) When bus release is requested with $\overline{BUSRQ}$ set to low, if the previous bus cycle is not completed due to a wait, the bus is not released until the wait is released.