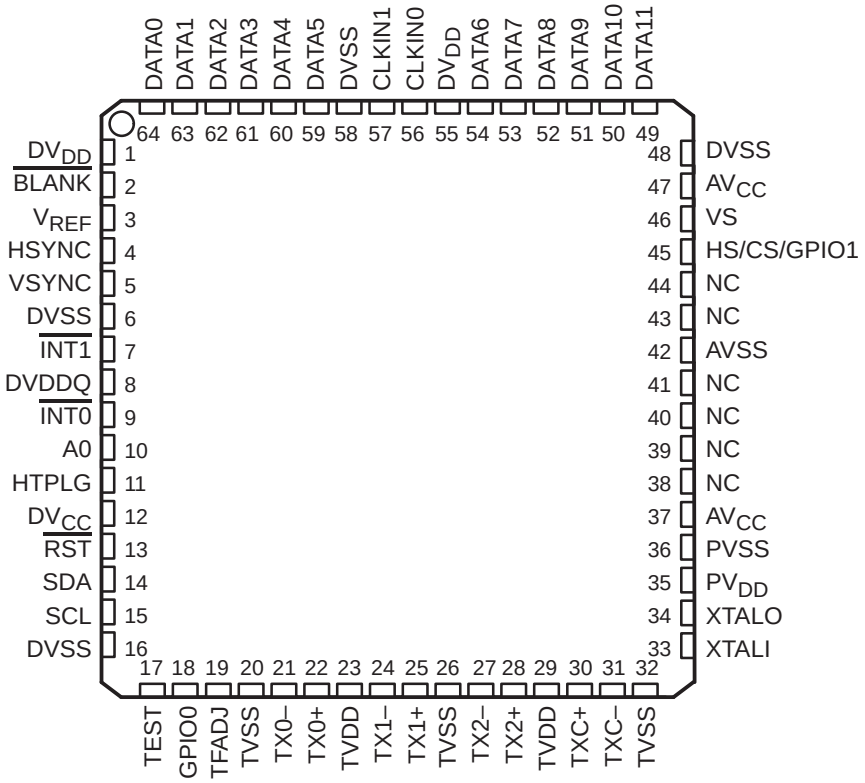
- **Supports UXGA Resolution (Output Pixel Rates up to 165 MHz)**
- **Digital Visual Interface (DVI 1.0) Specification[1]**
- **Seamlessly Interfaces With Intel™ DVO Port on Whitney and Future Intel™ Chipsets**
- **Supports 24-bit RGB and YCrCb Input Formats on a 12-Bit Pixel Port**
- **Programmable Functionality and I²C Serial Interface**
- **Reduced Power Consumption - 1.8 V Digital Core and 3.3 V Analog Circuit**
- **Lowest Noise and Best Power Dissipation Using PowerPAD™ Packaging**
- **Advanced Technology Using TI's 0.18 μm EPIC-5™ CMOS Process**

description

The TFP420 is a PanelBus™ flat panel display product, part of a comprehensive family of end-to-end DVI 1.0 compliant solutions. Targeted primarily at desktop and notebook PCs, the TFP420 finds applications in any design requiring a high-speed digital interface with connectivity to the Intel™ DVO port.

PAP PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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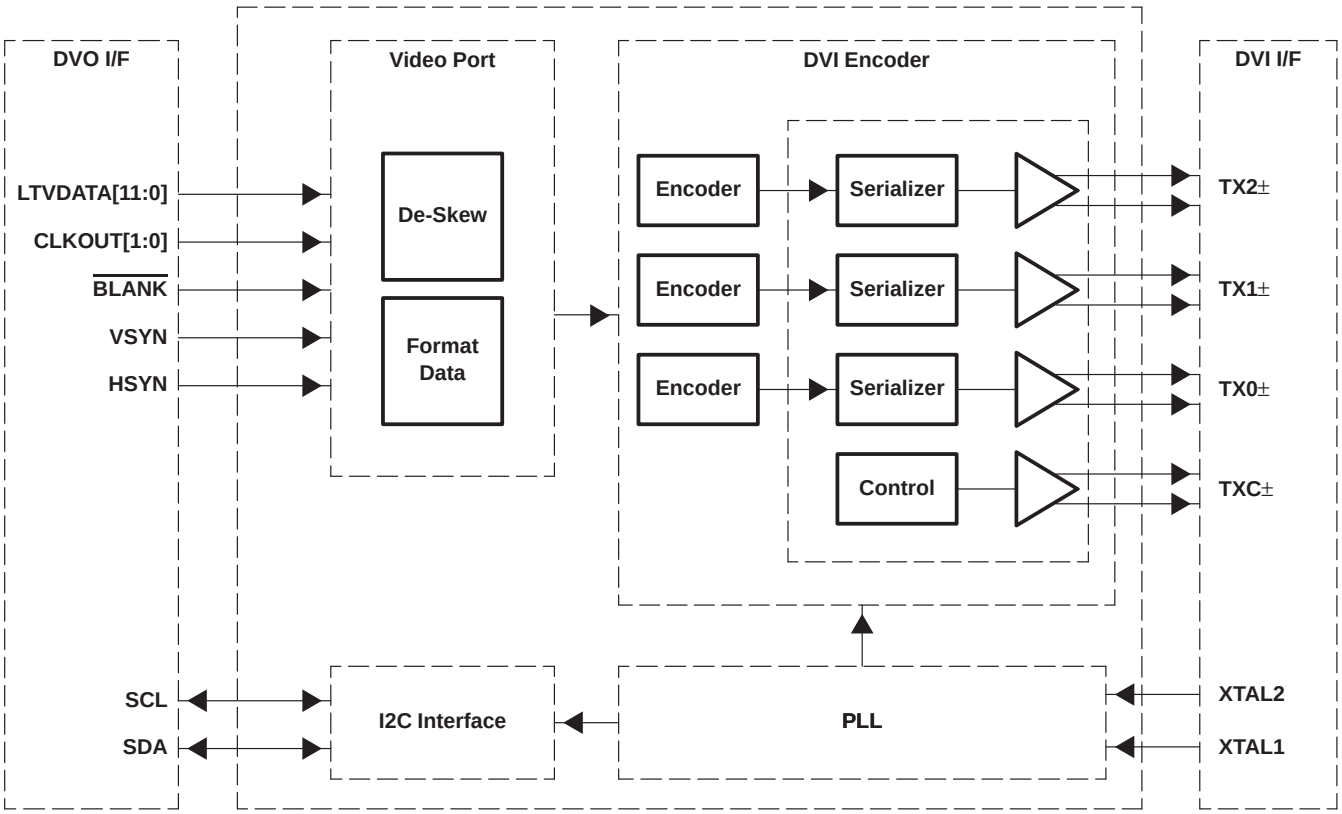
1. The Digital Visual Interface (DVI) specification is an industry standard developed by the digital display working group (DDWG) for high-speed digital connection to digital displays. The TFP420 is compliant to the DVI specification Rev. 1.0.

description (continued)

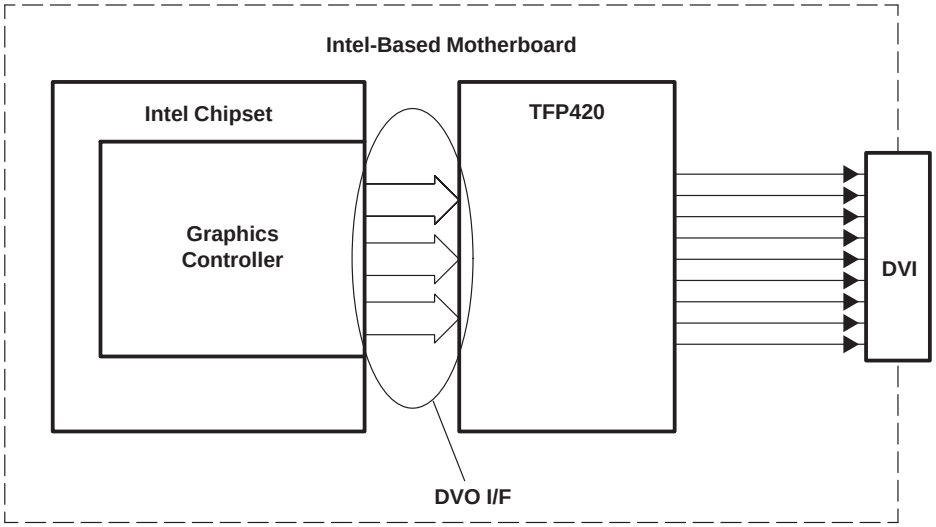
The scalable (1.1 V to 1.8 V) low-swing digital pixel interface provides a low-EMI and high-speed bus that connects seamlessly with Intel's digital video out (DVO) port, perfectly linking the graphics controller and the DVI transmitter. The DVI interface supports display resolutions up to UXGA at 165 MHz in 24-bit true color pixel format.

The TFP420 combines PanelBus™ circuit innovation, TI's advanced 0.18 μm EPIC-5™ CMOS process technology, and PowerPAD™ ultralow ground inductance package technology to provide a reliable, low-power, and low-noise digital interface solution.

functional block diagram



digital video out (DVO) interface diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	POWER RAIL	NO.		
Digital Video Input Port				
$\overline{\text{BLANK}}$	DV_{DD}	2	I	Blanking signal – $\overline{\text{BLANK}}$ is low during blanking interval and high during active video.
CLKIN[1:0]	DV_{DD}	57, 56	I	TFP420 uses CLKIN [1:0] to clock in video data and timing control signals. When used as a differential pair, CLKIN0 connects to the positive end and CLKIN1 connects to the negative end. For single-ended clock input, the clock is connected to CLKIN0 and a reference voltage of VDDQ/2 must be connected to CLKIN1. The graphics controller should use internal DOT clock to generate CLKIN[1:0].
DATA[11:0]	DV_{DD}	49–54, 59–64	I	DATA[11:0] is the pixel port
HSYNC	DV_{DD}	4	I	Horizontal sync input
$\overline{\text{INT0}}$	DV_{DD}	9	I/O	Interrupt for hot plug support (output) $\overline{\text{INT0}}$ is an open drain signal and an assertion low interrupt request informing the graphics controller of flat panel/TV/secondary monitor hot plug or hot unplug event. For normal applications, a 10K pullup resistor must be connected between this terminal and DV_{CC}.
$\overline{\text{INT1}}$	DV_{DD}	7	O	Interrupt for hot plug support $\overline{\text{INT1}}$ is an open drain signal and an assertion low interrupt request informing the graphics controller of flat panel/secondary monitor hot plug or hot unplug event.
V_{REF}	DVDDQ/2	3	A	Digital video input port voltage reference sets the switching threshold of all the signals listed in digital video input port section of this table. V_{REF} must be set to DVDDQ/2, where DVDDQ is the swing of the signals. DVDDQ ranges from 1.1 V to 1.8 V.
VSYNC	DV_{DD}	5	I	Vertical sync input
Reference Crystal				
XTALI	PV_{DD}	33	I	Terminal for reference crystal for the internal PLL. Leave unconnected if an external oscillator is connected to XTAL0.
XTALO	PV_{DD}	34	I	Terminal for reference crystal for the internal PLL or external reference oscillator input.

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	POWER RAIL	NO.		
DVI Output				
TX2+	TVDD	28	A	Red channel positive transmitter output – Positive side of red channel T.M.D.S. low voltage signal differential output pair. Red channel transmits red pixel data in active display and 00 control bits in blank.
TX2–	TVDD	27	A	Red channel negative transmitter output – Negative side of red channel T.M.D.S. low voltage signal differential output pair.
TX1+	TVDD	25	A	Green channel positive transmitter output – Positive side of green channel T.M.D.S. low voltage signal differential output pair. Green channel transmits green pixel data in active display and 00 control bits in blank.
TX1–	TVDD	24	A	Green channel negative transmitter output – Negative side of green channel T.M.D.S. low voltage signal differential output pair.
TX0+	TVDD	22	A	Blue channel positive transmitter output – Positive side of blue channel T.M.D.S. low voltage signal differential output pair. Blue channel transmits blue pixel data in active display and HSYNC, VSYNC control signals in blank.
TX0–	TVDD	21	A	Blue channel negative transmitter output – Negative side of blue channel T.M.D.S. low voltage signal differential output pair.
TXC+	TVDD	30	A	Clock positive transmitter output – Positive side of reference clock T.M.D.S. low voltage signal differential output pair.
TXC–	TVDD	31	A	Clock negative transmitter output – Negative side of reference clock T.M.D.S. low voltage signal differential output pair.
TFADJ	TVDD	19	A	T.M.D.S. drivers full scale adjust control A 2-kΩ resistor must be connected between this terminal and TVSS.
I²C Interface and Miscellaneous				
A0	DV_{CC}	10	I	I²C slave address select
GPIO0	DV_{CC}	18	I/O	General-purpose I/O #0 First general-purpose I/O. This terminal has an internal weak pulldown of 1 MΩ (TBD). With GPIO0 as an input, use an external 10 kΩ resistor to pull up or down to set the state of this terminal.
HS/CS/ GPIO1	AVCC	45	I/O	Digital horizontal sync output – This is the HSYNC signal that connects to the VGA connector. Digital composite sync output – Composite HSYNC and VSYNC. The polarity of this signal is programmable when used for HS/CS. General-purpose I/O #1 – Second general-purpose I/O. This terminal has an internal weak pulldown of 1 MΩ (TBD). With GPIO1 as an input, use an external 10-kΩ resistor to pull up or down to set the state of this terminal.
HTPLG	DV_{CC}	11	I	DVI/P&D/DFP hot plug detect input
NC	AV_{CC}	38–41, 43, 44	A	Reserved
$\overline{RST}$	DV_{CC}	13	I	Reset signal active low.
SCL	DV_{CC}	15	I/O	I²C serial clock input maximum. Clock rate of 400 kHz. Open drained I/O.
SDA	DV_{CC}	14	I/O	I²C Serial data line open drained I/O.
TEST	DV_{CC}	17	I	Test mode enable This terminal must be tied to LOW for normal mode of operation. Connecting this terminal to HIGH puts TFP420 in test mode.
VS	AVCC	46	O	Digital vertical sync output When the analog RGB video output is enabled this signal is the VSYNC that connects to the VGA connector.

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	POWER RAIL	NO.		
Power and Ground				
AV_{CC}	3.3 V	37, 47	P	Analog power
AVSS	0.0 V	42	G	Analog ground
DV_{CC}	3.3 V	12	P	Digital power
DV_{DD}	1.8 V	1, 55	P	Digital power
DVDDQ	1.1 V–1.8 V	8	P	Digital power
DVSS	0.0 V	6, 16, 48, 58	G	Digital ground
PV_{DD}	1.8 V	35	P	Power for PLLs
PVSS	0.0 V	36	G	Ground for PLLs
TVDD	1.8 V	23, 29	P	Analog power for the DVI output drivers
TVSS	0.0 V	20, 26, 32	G	Analog ground for the DVI output drivers

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

External T.M.D.S. termination resistance, RLtmds . . . . . 0 Ω to open circuit
External TFADJ resistor . . . . . 1 kΩ to open circuit
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Maximum total power dissipation, P_D . . . . . 2 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (ALL DATA PRELIMINARY)

		MIN	NOM	MAX	UNIT
Digital supply voltage, DV_{DD}		1.7	1.8	1.9	V
Digital supply voltage, DVDDQ		1.0	1.8	1.9	V
Analog supply voltage, AV_{CC}		3.13	3.3	3.47	V
Analog supply voltage, TVDD		1.7	1.8	1.9	V
Analog supply voltage, PV_{DD}		1.7	1.8	1.9	V
Digital low-level input voltage, DV_{DD} V_{IL} (scalable with $V_{(REF)}$				$V_{(REF)}$–100 mv	V
Digital low-level input voltage, DV_{DD} V_{IH} (scalable with $V_{(REF)}$		$V_{(REF)}$+100 mv			V
Digital low-level input voltage, DV_{CC} V_{IL}				0.8	V
Digital low-level input voltage, DV_{CC} V_{IH}					V
DVI 1280x1024 resolution 60 Hz refresh rate	Digital supply current, DV_{DD}			80	mA
	Digital supply current, DVDDQ			0	
	Analog supply current, TVDD			120	
	Analog supply current, AV_{CC}			6	
	Analog supply voltage, PV_{DD}			100	
Reference voltage, $V_{(REF)}$		0.52	0.9	0.95	V
External T.M.D.S. termination resistor		45	50	55	Ω
External TFADJ resistor		1.4	2	2.6	kΩ
Operating free-air temperature, T_A		0		70	°C

functional description

overview

The TFP420 integrates a PLL, DVI encoder, and three differential pairs of T.M.D.S. drivers. A dedicated high-speed low terminal count video pixel port transfers high-bandwidth digital video data from a graphics controller or other digital video source to the TFP420.

The TFP420 is versatile and highly programmable to provide maximum flexibility for the user. An I^2C host interface is provided to program and configure the TFP420.

I^2C interface

The I^2C interface is used to access the internal TFP420 register. This two-terminal interface consists of one clock line, SCL, and one serial data line, SDA. The basic I^2C access cycles are shown in Figures 1 and 2.

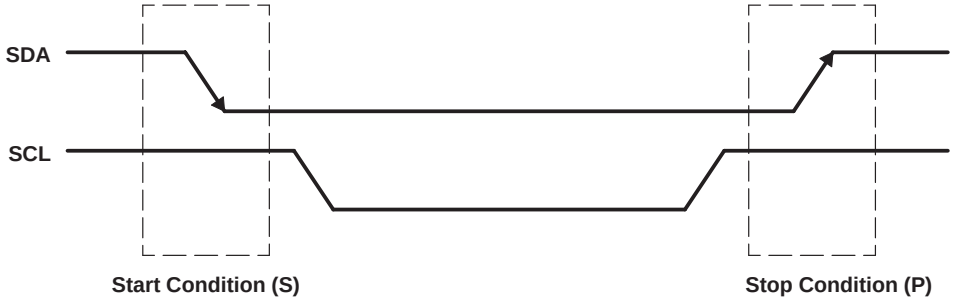


Figure 1. I^2C Start and Stop Conditions

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- A subaddress cycle
- Any number of data cycles
- A stop condition

The start and stop conditions are shown in Figure 2. The high to low transition of SDA while SCL is high defines the start condition. The low to high transition of SDA while SCL is high defines the stop condition. Each cycle, data or address consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains 9 bits as shown in Figure 2.

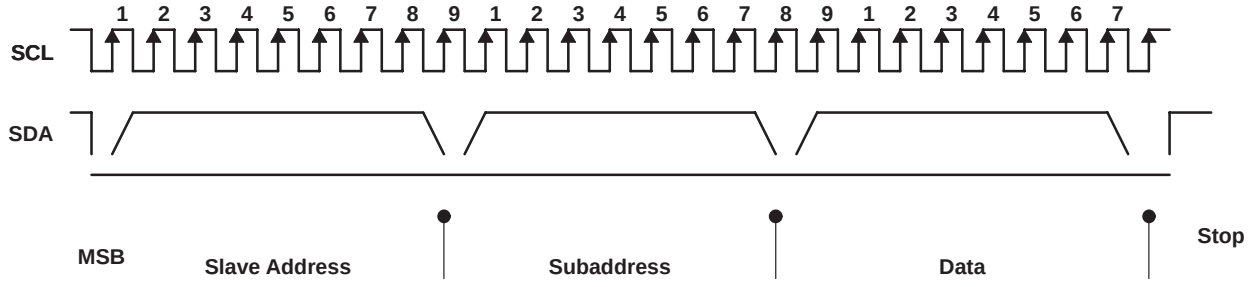


Figure 2. I^2C Access Cycles

I²C interface (continued)

Following a start condition, each I²C device decodes the slave address. The TFP420 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent subaddress and data cycles the TFP420 responds with acknowledge as shown in Figure 3. The subaddress is autoincremented after each data cycle.

The transmitting device must not drive the SDA signal during the acknowledge cycle so that the receiving device may drive the SDA signal low. The not acknowledge, /A, condition is indicated by the master by keeping the SDA signal high just before it asserts the stop, P, condition. This sequence terminates a read cycle as shown in Figure 4.

The slave address consists of 7 bits of address along with 1 bit of read/write information as shown below in Figures 3 and 4. For the TFP420, the possible slave addresses (including the r/w bit) are 0x40 and 0x42 for write cycles and 0x41 and 0x43 for read cycles. Refer to register description, for additional base address information.

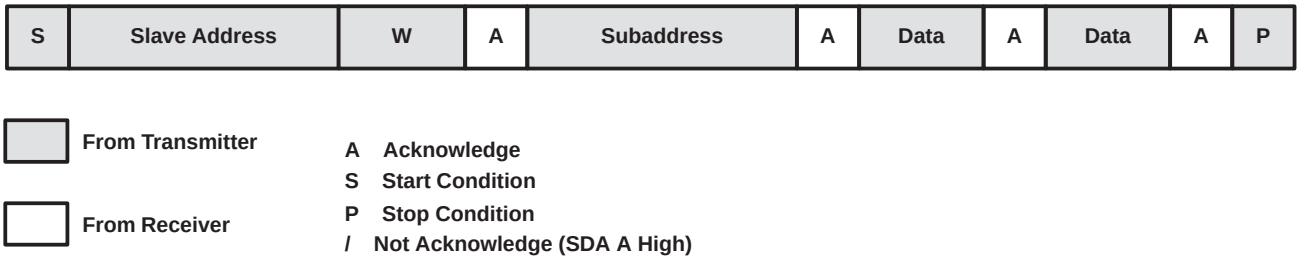


Figure 3. I²C Write Cycle

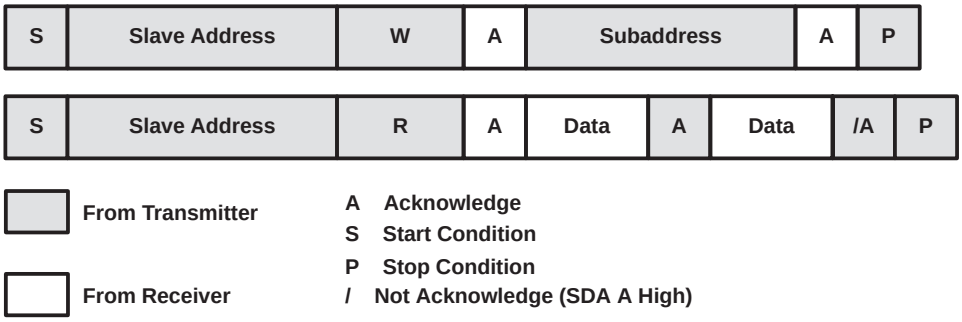


Figure 4. I²C Read Cycle

video port

The TFP420 video port is a low terminal count and high-speed digital interface. The video port consists of a 12-bit data bus (DATA[11:0]), horizontal timing signal (HSYNC), vertical timing signal (VSYNC), blanking control ($\overline{\text{BLANK}}$), clock signals (CLKIN0 and CLKIN1), and interrupt request signals ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$). To reduce the terminal count and the board space, a compact 12-bit pixel bus is used. The bus operates in either single-pump or double-pump mode depending on the selection of the input pixel format (FMT[2:0]). In single pump mode only the first edge of the CLKIN0/CLKIN1 differential clock pair is used to sample the data, timing, and blanking control signals. In double-pump mode, both edges of the clock are used. With the double-pump mode, high pixel transfer rates up to 165 Mpixels/sec can be achieved.

video port (continued)

To ease the timing and EMI issues associated with a high pixel transfer rate, the signaling level of the signals in video port is scalable. The input signals in video port are scalable by adjusting the voltage on the V_{REF} terminal to VDDQ/2. Similarly, the output signals are scalable by adjusting the voltage on the VDDQ terminal to VDDQ, where VDDQ is the desirable full-swing voltage for the video port I/O signals. The differential CLKIN pair provides more robust and reliable sampling for the pixel data and control signals, alleviating tight setup and hold time requirements for high pixel transfer rates. Although differential clocking is the recommended clocking scheme, it is possible to use single-end clocking with reduced timing margin, which may be significant with high clock rates. When single-end clocking is used, CLKIN0 must be connected to the clock and CLKIN1 must be connected to VDDQ/2.

The $\overline{\text{INT1}}$ terminal, when enabled, generates an interrupt to inform the host CPU of events related to hot plug and power management. $\overline{\text{INT1}}$ is open-drained and must be pulled up to VDDQ with a 10-KΩ resistor.

The $\overline{\text{INT0}}$ terminal provides a dedicated interrupt for future applications. Similar to $\overline{\text{INT1}}$, $\overline{\text{INT0}}$ is open-drained. Normally a 10-KΩ pullup resistor is needed to pull the signal to VDDQ. The TFP420 enters a special mode when the $\overline{\text{INT0}}$ is forced to low just before the deassertion of the $\overline{\text{RST}}$.

DVI encoder

The DVI encoder receives RGB pixel data from the video port and encodes the pixel data based on the transition minimized differential signaling (T.M.D.S.) encoding algorithm. The DVI encoder consists of three independent identical channels, each of which is responsible for encoding one color component. The encoding algorithm minimizes the signal transition while maintaining a good dc balance to reduce EMI. The encoded data is then serially shifted to the DVI output drivers for transmission. The low-voltage swing differential output further reduces EMI.

Each channel is encoded independently. Each channel receives 2 bits of control data and 8 bits of color component data. Depending on the state of $\overline{\text{BLANK}}$, the DVI encoder encodes either control data or color components. In either case, the data is encoded to a 10-bit character and serially shifted out with the LSB transmitted first. Blue channel (Channel 0) receives HSYNC and VSYNC as the control data and the blue color component as the pixel data. If $\overline{\text{BLANK}}$ is low, indicating valid blue component data is not transmitting, the DVI encoder of the blue channel encodes the HSYNC and VSYNC signals. If $\overline{\text{BLANK}}$ is high, indicating valid blue component data is transmitting, the DVI encoder encodes the blue component data. The green channel (Channel1) and the red channel (Channel 2) operate in a way similar to the blue channel with the exception that the control bits are hardwired to 0.

There are two possible encoded characters for each pixel data. The DVI encoder keeps track of the difference between the number of ones and zeros that have been sent and selects the character that minimizes the difference in order to maintain the best dc balance.

A serializer serializes the 10-bit character in each channel. An on-chip PLL locks to the CLKIN0 and CLKIN1 and generates the 10X clock to drive the serializer. The 10X clock is also sent to the T.M.D.S. drivers for output.

clock generation

The TFP420 uses the CLKIN signal to generate the required clock for DVI output. The on-chip PLL takes CLKIN as the reference and generates the 10X clock. This clock is used internally by the DVI encoder to encode and clock out the DVI bit stream as well as to output TXC+ and TXC– differential clock along with the DVI data signals.

The CLK_CTRL register provides additional control over the clock signals. DKEN and CLKINDSK[2:0] allow the user to compensate the skew between the CLKIN and the pixel data and control signals. Refer to the description of the CLK_CTRL for details.

functional description (continued)

hot plug/unplug (auto connect/disconnect detection)

The TFP420 supports hot plug/unplug (auto connect/disconnect detection) for the DVI link. The connection status of DVI link and HTPLG sense terminal is provided by the CON_STATUS register. The RXCON bit indicates if a DVI receiver is connected to the TXC+ and TXC–. HPCON bit reflects the current state of the HTPLG terminal connected to the monitor via DVI connector. HTPLG terminal is 3-V tolerant with an internal digital debouncing circuit to allow for direct connection to the DVI connector.

Whenever one or more connection status bits change states, the corresponding bit in the IN_STATUS bit is set to 1 to record the changes. An interrupt can also be generated as an option. The interrupt for each type of connect/disconnect event can be individually enabled or disabled by writing a 1 or 0 to the corresponding bit in the INT_ENABLE register. Notice that INT_ENABLE register does not affect the state of the INT_STATUS bits. A host can either poll the INT_STATUS bits or rely on the interrupt to learn about the states or the change of states of the connections. The interrupt continues to be asserted until 1 is written to the corresponding interrupt bit in the INT_STATUS register to reset the bit back to 0. Writing 0 to an interrupt status bit has no effect.

register map

The TFP420 is a standard I^2C slave device. All the registers can be written and read through the I^2C interface. The I^2C base address of the TFP420 is dependent on terminal 10 (A0) as shown in Table 1.

Table 1. Base I^2C Address

Terminal 10	WRITE ADDRESS (HEX)	READ ADDRESS (HEX)
0	40	41
1	42	43

REGISTER	RW	SUBADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VEN_ID	R	00	Ven_id[7:0]							
	R	01	Ven_id[15:8]							
DEV_ID	R	02	Dev_Id[7:0]							
	R	03	Dev_id[15:8]							
REV_ID	R	04	Rev_Id[7:0]							
RESERVED		05–39	RESERVED							
F_CONTROL	RW	3A	Cbar	Intcko	RGBF		Fmt[3:0]			
CLK_CTRL	RW	3B				Ckindsk[3:0]				Ckencse
VIDOUT_CTRL	RW	3C					Vidout[3:0]			
SYNC_CTRL0	RW	3D	Syn_g	Fid_pol	Vs_fid	Hs_com	Vsen	Hsen	Tvsen	Thsen
CON_STATUS	R	3E			Daccon3	Daccon2	Daccon1	Daccon0	Hpcon	Rxcon
INT_STATUS	RW	3F							Hpevnt	Rxevnt
INT_ENABLE	RW	40							Hpen	Rxen
GP_CTRL	RW	41	Gio1_en		Gp1_in	Gp0_in	Gp1_oe	Gp0_oe	Gp1_out	Gp0_out
RESERVED		42–FF	RESERVED							

register description

VEN_ID **Subaddress = 00** **Read Only** **Default = 0x4C**

7	6	5	4	3	2	1	0
VEN_ID[7:0]							

Subaddress = 01 **Read Only** **Default = 0x01**

7	6	5	4	3	2	1	0
VEN_ID[15:8]							

This read-only register contains the 16-bit Texas Instruments vendor ID for the TFP420. VEN_ID[15:0] is hardwired to 0x014C.

DEV_ID **Subaddress = 02** **Read Only** **Default = 0x22**

7	6	5	4	3	2	1	0
DEV_ID[7:0]							

Subaddress = 03 **Read Only** **Default = 0x64**

7	6	5	4	3	2	1	0
DEV_ID[15:8]							

This read-only register contains the 16-bit device ID for the TFP420.

REV_ID **Subaddress = 04** **Read Only** **Default = 0x01**

7	6	5	4	3	2	1	0
REV_ID[7:0]							

This read-only register contains the revision ID for the TFP420. The revision ID will identify different revisions of the device. REV_ID[7:0] is hardwired to 0x01.

STATUS **Subaddress = 05** **Read Only**

F_CONTROL **Subaddress = 3A** **Default = 0x8D**

7	6	5	4	3	2	1	0
RSVD	RSVD	RGBF		FMT[3:0]			

Format Control Register. This register specifies the input video source and format.

RGBF RGB /YCrCb input coding range

- 0(*) The input RGB data are in binary format with coding range 0–255
  The input YCrCb data are in binary format with coding range 0–255
- 1 The input RGB data are in binary format with coding range 16–235
  The input YCrCb data are in binary format conforming to ITU–601 standard

FMT[3:0] These four bits specify the video input data stream format and timing as shown in the table below.
H indicates the sampling point at the crossover of the rising edge of CLKIN0 and the falling edge of CLKIN1
L indicates the sampling point at the crossover of the falling edge of CLKIN0 and the rising edge of CLKIN1

register description (continued)

digital input video data and sync format

FMT[3:2] = 00(*)								
Color space	RGB							
Pixel format	(8,8,8)							
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
FMT[1:0]								
DATA[11:0]	00(*)		01		10		11	
	H	L	H	L	H	L	H	L
DATA[11]	R[7]	G[3]	G[3]	R[7]	R[7]	G[4]	G[4]	R[7]
DATA[10]	R[6]	G[2]	G[2]	R[6]	R[6]	G[3]	G[3]	R[6]
DATA[9]	R[5]	G[1]	G[1]	R[5]	R[5]	G[2]	G[2]	R[5]
DATA[8]	R[4]	G[0]	G[0]	R[4]	R[4]	B[7]	B[7]	R[4]
DATA[7]	R[3]	B[7]	B[7]	R[3]	R[3]	B[6]	B[6]	R[3]
DATA[6]	R[2]	B[6]	B[6]	R[2]	G[7]	B[5]	B[5]	G[7]
DATA[5]	R[1]	B[5]	B[5]	R[1]	G[6]	B[4]	B[4]	G[6]
DATA[4]	R[0]	B[4]	B[4]	R[0]	G[5]	B[3]	B[3]	G[5]
DATA[3]	G[7]	B[3]	B[3]	G[7]	R[2]	G[0]	G[0]	R[2]
DATA[2]	G[6]	B[2]	B[2]	G[6]	R[1]	B[2]	B[2]	R[1]
DATA[1]	G[5]	B[1]	B[1]	G[5]	R[0]	B[1]	B[1]	R[0]
DATA[0]	G[4]	B[0]	B[0]	G[4]	G[1]	B[0]	B[0]	G[1]
FMT[3:2] = 01								
Color space	YCrCb							
Pixel format	4:4:4							
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
FMT[1:0]								
DATA[11:0]	00		01		10		11	
	H	L	H	L	H	L	H	L
DATA[11]	Cr[7]	Y[3]	Y[3]	Cr[7]	Cr[7]	Y[4]	Y[4]	Cr[7]
DATA[10]	Cr[6]	Y[2]	Y[2]	Cr[6]	Cr[6]	Y[3]	Y[3]	Cr[6]
DATA[9]	Cr[5]	Y[1]	Y[1]	Cr[5]	Cr[5]	Y[2]	Y[2]	Cr[5]
DATA[8]	Cr[4]	Y[0]	Y[0]	Cr[4]	Cr[4]	Cb[7]	Cb[7]	Cr[4]
DATA[7]	Cr[3]	Cb[7]	Cb[7]	Cr[3]	Cr[3]	Cb[6]	Cb[6]	Cr[3]
DATA[6]	Cr[2]	Cb[6]	Cb[6]	Cr[2]	Y[7]	Cb[5]	Cb[5]	Y[7]
DATA[5]	Cr[1]	Cb[5]	Cb[5]	Cr[1]	Y[6]	Cb[4]	Cb[4]	Y[6]
DATA[4]	Cr[0]	Cb[4]	Cb[4]	Cr[0]	Y[5]	Cb[3]	Cb[3]	Y[5]
DATA[3]	Y[7]	Cb[3]	Cb[3]	Y[7]	Cr[2]	Y[0]	Y[0]	Cr[2]
DATA[2]	Y[6]	Cb[2]	Cb[2]	Y[6]	Cr[1]	Cb[2]	Cb[2]	Cr[1]
DATA[1]	Y[5]	Cb[1]	Cb[1]	Y[5]	Cr[0]	Cb[1]	Cb[1]	Cr[0]
DATA[0]	Y[4]	Cb[0]	Cb[0]	Y[4]	Y[1]	Cb[0]	Cb[0]	Y[1]

digital input video data and sync format (continued)

FMT[3:2] = 10								
Color space	YCrCb							
Pixel format	4:2:2							
FMT[1:0] = 00								
Scan	Interlaced							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cb0[7]		Y0[7]		Cr0[7]		Y1[7]	
DATA[6]	Cb0[6]		Y0[6]		Cr0[6]		Y1[6]	
DATA[5]	Cb0[5]		Y0[5]		Cr0[5]		Y1[5]	
DATA[4]	Cb0[4]		Y0[4]		Cr0[4]		Y1[4]	
DATA[3]	Cb0[3]		Y0[3]		Cr0[3]		Y1[3]	
DATA[2]	Cb0[2]		Y0[2]		Cr0[2]		Y1[2]	
DATA[1]	Cb0[1]		Y0[1]		Cr0[1]		Y1[1]	
DATA[0]	Cb0[0]		Y0[0]		Cr0[0]		Y1[0]	
FMT[1:0] = 01								
Scan	Interlaced							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cr0[7]		Y0[7]		Cb0[7]		Y1[7]	
DATA[6]	Cr0[6]		Y0[6]		Cb0[6]		Y1[6]	
DATA[5]	Cr0[5]		Y0[5]		Cb0[5]		Y1[5]	
DATA[4]	Cr0[4]		Y0[4]		Cb0[4]		Y1[4]	
DATA[3]	Cr0[3]		Y0[3]		Cb0[3]		Y1[3]	
DATA[2]	Cr0[2]		Y0[2]		Cb0[2]		Y1[2]	
DATA[1]	Cr0[1]		Y0[1]		Cb0[1]		Y1[1]	
DATA[0]	Cr0[0]		Y0[0]		Cb0[0]		Y1[0]	

digital input video data and sync format (continued)

FMT[3:2] = 10								
Color space	YCrCb							
Pixel format	4:2:2							
FMT[1:0] = 10								
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
DATA[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
DATA[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
DATA[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
DATA[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
DATA[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
DATA[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
DATA[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]
FMT[1:0] = 11								
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cr0[7]	Y0[7]	Cb0[7]	Y1[7]	Cr2[7]	Y2[7]	Cb2[7]	Y3[7]
DATA[6]	Cr0[6]	Y0[6]	Cb0[6]	Y1[6]	Cr2[6]	Y2[6]	Cb2[6]	Y3[6]
DATA[5]	Cr0[5]	Y0[5]	Cb0[5]	Y1[5]	Cr2[5]	Y2[5]	Cb2[5]	Y3[5]
DATA[4]	Cr0[4]	Y0[4]	Cb0[4]	Y1[4]	Cr2[4]	Y2[4]	Cb2[4]	Y3[4]
DATA[3]	Cr0[3]	Y0[3]	Cb0[3]	Y1[3]	Cr2[3]	Y2[3]	Cb2[3]	Y3[3]
DATA[2]	Cr0[2]	Y0[2]	Cb0[2]	Y1[2]	Cr2[2]	Y2[2]	Cb2[2]	Y3[2]
DATA[1]	Cr0[1]	Y0[1]	Cb0[1]	Y1[1]	Cr2[1]	Y2[1]	Cb2[1]	Y3[1]
DATA[0]	Cr0[0]	Y0[0]	Cb0[0]	Y1[0]	Cr2[0]	Y2[0]	Cb2[0]	Y3[0]

digital input video data and sync format (continued)

FMT[3:2] = 11								
Color space	YCrCb							
Pixel format	4:2:2							
FMT[1:0] = 00								
Scan	Interlaced							
Sync	F, V and H bits in the SAV and EAV codes are embedded in the video stream							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cb0[7]		Y0[7]		Cr0[7]		Y1[7]	
DATA[6]	Cb0[6]		Y0[6]		Cr0[6]		Y1[6]	
DATA[5]	Cb0[5]		Y0[5]		Cr0[5]		Y1[5]	
DATA[4]	Cb0[4]		Y0[4]		Cr0[4]		Y1[4]	
DATA[3]	Cb0[3]		Y0[3]		Cr0[3]		Y1[3]	
DATA[2]	Cb0[2]		Y0[2]		Cr0[2]		Y1[2]	
DATA[1]	Cb0[1]		Y0[1]		Cr0[1]		Y1[1]	
DATA[0]	Cb0[0]		Y0[0]		Cr0[0]		Y1[0]	
FMT[1:0] = 01								
Scan	Interlaced							
Sync	F, V and H bits in the SAV and EAV codes are embedded in the video stream							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cr0[7]		Y0[7]		Cb0[7]		Y1[7]	
DATA[6]	Cr0[6]		Y0[6]		Cb0[6]		Y1[6]	
DATA[5]	Cr0[5]		Y0[5]		Cb0[5]		Y1[5]	
DATA[4]	Cr0[4]		Y0[4]		Cb0[4]		Y1[4]	
DATA[3]	Cr0[3]		Y0[3]		Cb0[3]		Y1[3]	
DATA[2]	Cr0[2]		Y0[2]		Cb0[2]		Y1[2]	
DATA[1]	Cr0[1]		Y0[1]		Cb0[1]		Y1[1]	
DATA[0]	Cr0[0]		Y0[0]		Cb0[0]		Y1[0]	
FMT[1:0] = 10 Reserved								
FMT[1:0] = 11 Reserved								

register description (continued)

7	6	5	4	3	2	1	0
			CKINDSK[3:0]				RSVD

CKINDSK [3:0] CLKIN deskew control

0000 –8 T
0001 –7 T
0010 –6 T
0011 –5 T
0100 –4 T
0101 –3 T
0110 –2 T
0111 –T
1000(*) No Skew
1001 T
1010 2 T
1011 3 T
1100 4 T
1101 5 T
1110 6 T
1111 7 T

Where T = approximately 100 ps.

VIDOUT_CTRL **Subaddress = 3C** **Default = 0x00**

7	6	5	4	3	2	1	0
				VIDOUT[3:0]			

VIDOUT[3:0] Video output mode
0000(*) DVI
0001–1110 Reserved
1111 Power down

I²C interface continues to be active in power down modes.

register description (continued)

SYNC_CTRL0 **Subaddress = 3D** **Default = 0x03**

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	HS_COM	VSEN	HSEN	TYSEN	THSEN

THSEN DVI HSYNC enable
- 0 HSYNC is transmitted as 0
- 1(*) HSYNC is transmitted as received from the video port

TVSEN DVI VSYNC enable
- 0 VSYNC is transmitted as 0
- 1(*) VSYNC is transmitted as received from the video port

HSEN HS enable
- 0(*) HS is in inactive state (LOW)
- 1 HS outputs digital horizontal/composite sync

VSEN VS enable
- 0(*) VS is in inactive state (LOW)
- 1 VS outputs digital vertical sync

HS_COM HS function select
- 0(*) HS outputs horizontal sync
- 1 HS outputs composite sync

CON_STATUS **Subaddress = 3E** **Read Only**

7	6	5	4	3	2	1	0
		RSVD	RSVD	RSVD	RSVD	HPCON	RXCON

RXCON
- 0 DVI receiver is not connected
- 1 DVI receiver is connected

HPCON
- 0 Hot plug is not connected
- 1 Hot plug is connected

INT_STATUS **Subaddress = 3F** **Read Only**

7	6	5	4	3	2	1	0
						HPEVNT	RXEVNT

RXEVNT
- 0 RXCON bit has not changed
- 1 RXCON bit has changed

HPEVNT
- 0 HPCON bit has not changed
- 1 HPCON bit has changed

To clear a bit, write 1 to the bit to clear. Writing 0 will not change the bit status.

INT_ENABLE **Subaddress = 40** **Default = 0x00**

7	6	5	4	3	2	1	0
						hpen	rxen

RXEN
- 0(*) RXEVNT interrupt disabled
- 1 RXEVNT interrupt enabled

HPEN
- 0(*) HPEVNT interrupt disabled
- 1 HPEVNT interrupt enabled

register description (continued)

GP_CTRL **Subaddress = 41** **Default = 0x80**

7	6	5	4	3	2	1	0
GIO1_EN	Reserved	GP1_IN	GP0_IN	GP1_OE	GP0_OE	GP1_OUT	GP0_OUT

GP0_OUT General-purpose output bit. The state of this bit shows on GPIO0 terminal if GP0_OE is set to 1. Otherwise, GPIO0 terminal goes to a high impedance state.
- 0(*) GPIO0 terminal outputs LOW
- 1 GPIO0 terminal outputs HIGH

GP1_OUT General-purpose output bit. The state of this bit shows on GPIO1 terminal if GP1_OE is set to 1. Otherwise, GPIO1 terminal goes to a high impedance state.
- 0(*) GPIO1 terminal outputs LOW
- 1 GPIO1 terminal outputs HIGH

GP0_OE General-purpose bit output enable.
- 0(*) GPIO0 output goes to a high impedance state.
- 1 GPIO0 output is enabled

GP1_OE General-purpose bit output enable.
- 0(*) GPIO1 output goes to a high impedance state.
- 1 GPIO1 output is enabled

GP0_IN General-purpose input bit. This bit shows the state of GPIO0 terminal.
- 0(*) GPIO0 terminal is LOW
- 1 GPIO0 terminal is HIGH

GP0_IN General-purpose input bit. This bit shows the state of GPIO1 terminal.
- 0(*) GPIO1 terminal is LOW
- 1 GPIO1 terminal is HIGH

GIO1_EN .GPIO1 terminal enable
- 0(*) HC/CS/GPIO1 outputs Horizontal or composite sync
- 1 HC/CS/GPIO1 is used as the second general-purpose I/O terminal.

GIO1_EN	GP1_OUT	GP1_OE	HS_COM	HSEN	VSEN	Terminal 45
0	X	X	0	0	X	LOW
0	X	X	1	0	0	LOW
0	X	X	1	0	1	VS
0	X	X	1	1	0	HS
0	X	X	1	1	1	CS
1	0	0	X	X	X	3-state
1	0	1	X	X	X	LOW
1	1	0	X	X	X	3-state
1	1	1	X	X	X	HIGH

PowerPAD™ 64TQFP package

The TFP420 is packaged in TI's thermally enhanced PowerPAD™ 64TQFP packaging. The PowerPAD™ package is a 10 mm x 10 mm x 1.4mm TQFP outline with 0.5mm lead-pitch. The PowerPAD™ package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 64TQFP PowerPAD™ package offers a backside solder plane that connects directly to the die mount pad for enhanced thermal conduction. The system designer has the option to solder this backside plane to a thermal/ ground plane on the PCB. Since the die pad is electrically connected to the TFP420 chip substrate and hence ground, the backside PowerPAD™ connection to a PCB ground plane can improve ground bounce and power supply noise.

The connection of the PowerPAD™ to a PCB thermal/ground plane is optional.

The following table outlines the thermal properties of the TI 64-TQFP PowerPAD™ package. The 64-TQFP non-PowerPAD™ package is included only for reference.

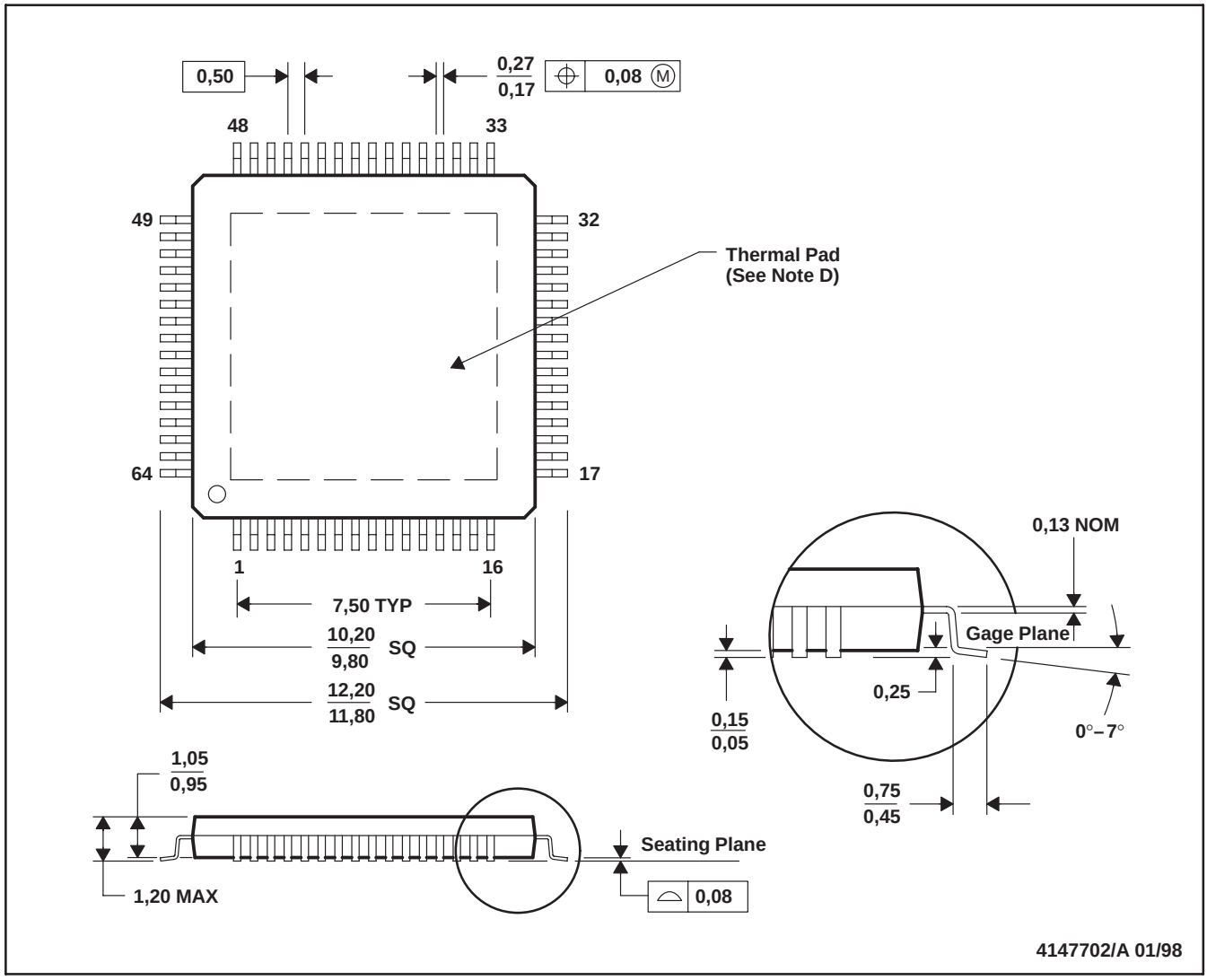
TI 64-TQFP (10 × 10 × 1.4 mm)/0.5 mm lead-pitch

PARAMETER	WITHOUT PowerPAD™	PowerPAD™ NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ CONNECTED TO PCB THERMAL PLANE†
Theta–JA†‡	45°C/W	27.3°C/W	17.3°C/W
Theta–JC†‡	3.11°C/W	0.12°C/W	0.12°C/W
Maximum power dissipation†‡§	1.6 W	2.7 W	4.3 W
Maximum TFP6422 pixel rate	TBD	TBD	TBD

† Specified with 2 oz. Cu PCB plating.
‡ Airflow is at 0 LFM (no airflow)
§ Measured at ambient temperature, T_A = 70°C.

MECHANICAL DATA

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

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