- **Supports UXGA Resolution (Output Pixel Rates up to 165 MHz)**
- **Digital Visual Interface (DVI 1.0) Specification and Video Specifications Compliant[1]**
- **Seamlessly Interfaces With Intel DVO Port on Whitney and Future Intel Chipsets**
- **Supports 24-bit RGB and YCrCb Input Formats on a 12-Bit Pixel Port**
- **Supports CCIR-656 YCbCr 4:2:2 Input Format on an 8-Bit Port**
- **Analog Composite Video Out Formats:**
  - **NTSC-M**
  - **PAL-B,D,G,H,I**
  - **PAL-M**
  - **PAL-N**
  - **PAL-Nc**
- **Simultaneous Composite and S-Video(Y/C Component) or YPrPb Component Output**
- **SCART Interface (Simultaneous Composite and Interlaced RGB Output)**
- **Programmable Functionality and I²C Serial Interface[2]**
- **Four 10-Bit DACs**
- **2X Over-Sampling and Optimized Filters for Luma and Chroma Channels**
- **Reduced Power Consumption – 1.8 V Digital Core and 3.3 V Analog Circuit**
- **Lowest Noise and Best Power Dissipation Using PowerPAD™ Packaging**
- **Advanced Technology Using TIs 0.18 μm EPIC-5™ CMOS Process**
- **TFP6424 Incorporates Macrovision 7.11 Support**

PRODUCT PREVIEW

description

The Texas Instruments TFP6422 and TFP6424 are PanelBus™ flat panel display products, part of a comprehensive family of end-to-end DVI 1.0 compliant solutions. Targeted primarily at digital entertainment / set-top-box applications, Internet PCs/appliances, PC-to-TV, and connectivity to DVD players and digital camcorders/cameras, the TFP6422/6424 finds applications in any design requiring a high-speed digital interface combined with TV-out support.

The scalable (1.1 V to 1.8 V) low-swing digital pixel interface provides a low-EMI and high-speed bus that connects seamlessly with Intels Digital Video Out (DVO) port, perfectly linking the graphics controller and the DVI transmitter. The DVI interface supports display resolutions up to UXGA at 165 MHz in 24-bit true color pixel format.

The TFP6422/6424 combines a high performance DVI transmitter and a high performance NTSC/PAL video encoder into a single chip in a compact 64-pin TQFP package, providing a cost–effective video output solution for the most demanding multimedia applications. The video encoder provides advanced horizontal and vertical scaling for overscan compensation and features a 5-tap adaptive anti–flicker filter. These features combine to produce high quality display of noninterlaced data on traditional interlaced TV.

The TFP6422/6424 combines PanelBus™ circuit innovation with TIs advanced 0.18 μm EPIC-5™ CMOS process technology along with TI PowerPAD™ ultra-low ground inductance package technology to provide a reliable, low-powered, low noise solution with integrated high-speed digital interface and highest quality TV output.

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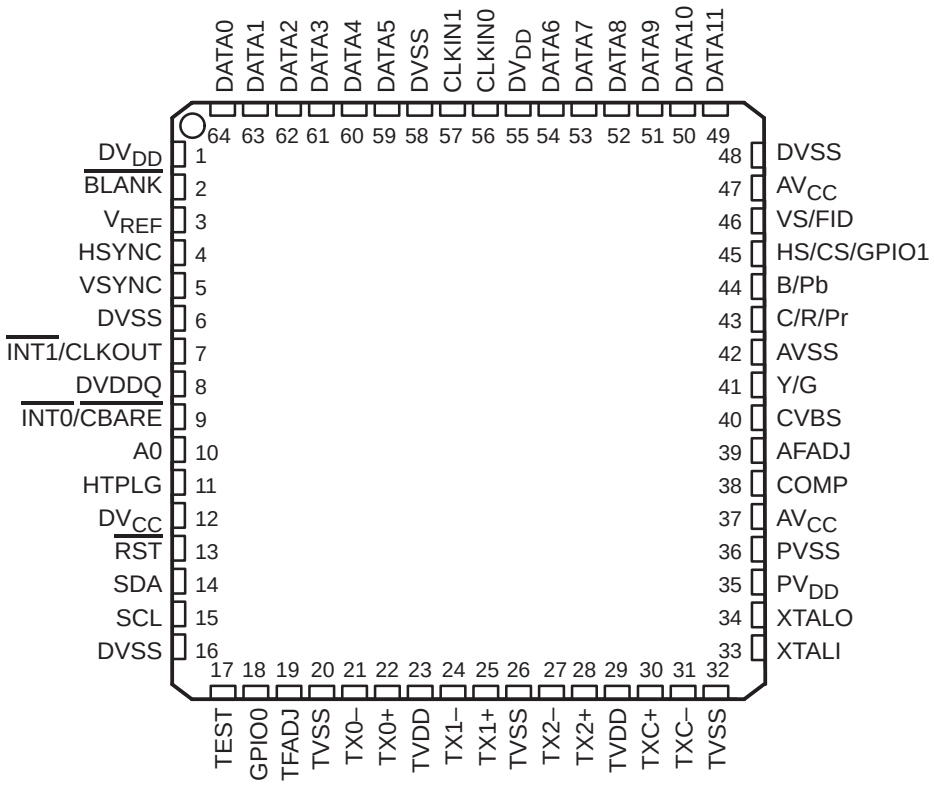
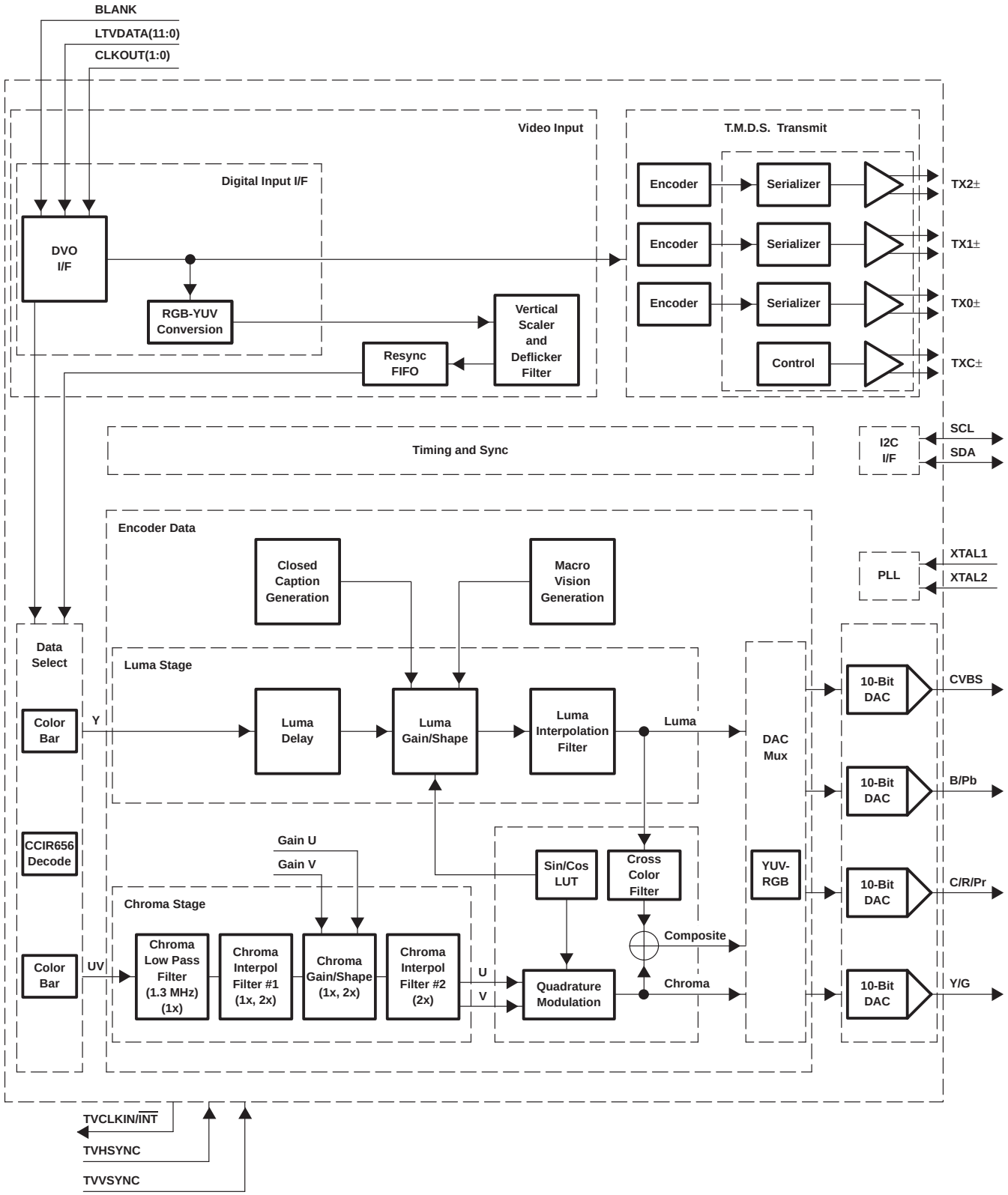
1. The Digital Visual Interface (DVI) specification is an industry standard developed by the Digital Display Working Group (DDWG) for high–speed digital connection to digital displays. The TFP6422 and TFP6424 are compliant to the DVI Specification Rev. 1.0. Both are also compliant to the SMPTE 170M NTSC composite video, and CCIR624/CCIR601 PAL composite video specifications.
2. Programmable functionality includes: arbitrary horizontal and vertical downscaling ratio, sync, black and blank levels, color burst amplitude, luminance and chrominance gains, luminance delay, subcarrier frequency, overscan compensation, flicker removal and SCH.



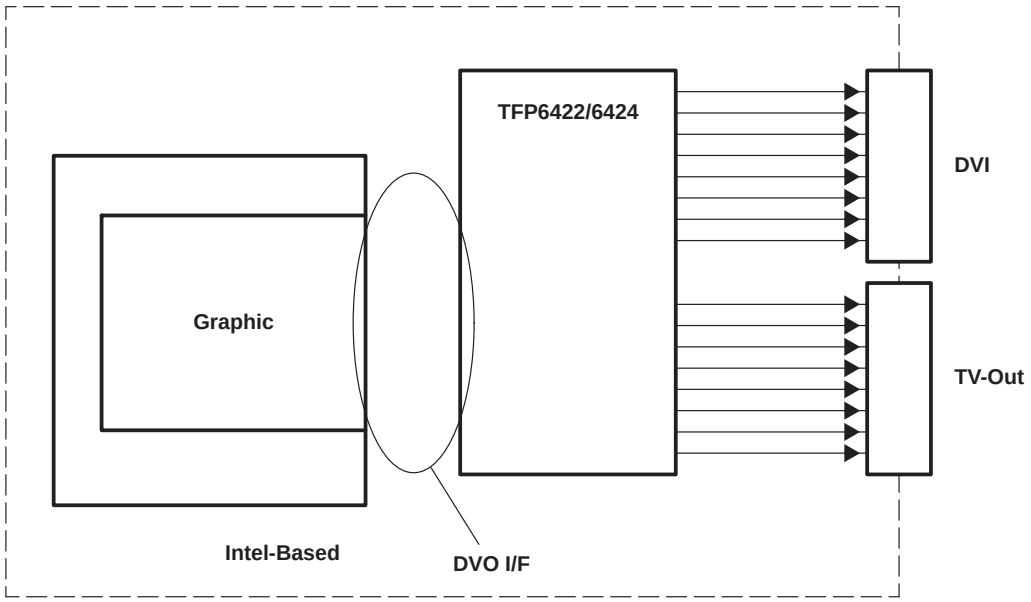
PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

digital video out (DVO) interface diagram



Terminal Functions

TERMINAL NAME	TERMINAL POWER RAIL	TERMINAL NO.	I/O	DESCRIPTION
Digital Video Input Port				
$\overline{\text{INT0}}$/$\overline{\text{CBARE}}$	DV_{DD}	9	I/O	$\overline{\text{Interrupt}}$ for hot plug support (Output) $\overline{\text{INT0}}$ is an open drain signal and an assertion low interrupt request informing the graphics controller of Flat Panel/TV/secondary monitor hot–plug or hot unplug event. For normal applications, a 10K pull-up resistor must be connected between this pin and DV_{CC}. Color bar display enable at reset (Input) For diagnostics purpose, this pin can be pulled down via a pulldown resistor to enable the video encoder to output the color bar test signal upon the completion of reset. The state of this pin is sensed immediately after the low-to-high transition of $\overline{\text{RST}}$. If the state of this pin is LOW, the video encoder will be enabled and output the color bar test signal. If the state of this pin is HIGH, DVI transmitter will be enabled and analog video will be disabled.
CLKIN[1:0]	DV_{DD}	57, 56	I	TFP6422/6424 uses CLKIN [1:0] to clock in video data and timing control signals. When used as a differential pair, CLKIN0 connects to the positive end and CLKIN1 connects to the negative end. For single–ended clock input, the clock is connected to CLKIN0 and a reference voltage of VDDQ/2 must be connected to CLKIN1. During TV mode, CLKIN [1:0] must be connected to CLKOUT or a clock signal derived from the graphics controller. During LCD mode, the graphics controller should use internal DOT clock to generate CLKIN[1:0].

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL POWER RAIL	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{INT1}}$/CLKOUT	DV_{DD}	7	O	**This pin can be programmed as clock or interrupt output.** Clock out – The internal TV encoder PLL drives CLKOUT. The frequency of CLKOUT is programmable and depends on TV standards, and the desired horizontal and vertical overscan compensation ratios. An external graphic controller may use CLKOUT directly to source video pixel data to DATA[11:0] bus and to clock out timing control signals HSYNC, VSYNC and $\overline{\text{BLANK}}$, or alternatively, use CLKOUT as a reference signal to generate a clock internally to clock out the video pixel data and timing control. In the first case, the CLKOUT should be connected directly to CLKIN. In the second case, the clock signal generated by the graphics controller should be connected to CLKIN[1:0] if the clock is a differential pair, or CLKIN[0] if the clock is single-ended with CLKIN1 connected to VDDQ/2. Interrupt for hot plug support $\overline{\text{INT1}}$ is an open drain signal and an assertion low interrupt request informing the graphics controller of Flat Panel/secondary monitor hot–plug or hot unplug event. When this pin is programmed as CLKOUT, INT0# is used for hot plug support.
HSYNC	DV_{DD}	4	I	Horizontal sync input
VSYNC	DV_{DD}	5	I	Vertical sync input
$\overline{\text{BLANK}}$	DV_{DD}	2	I	Blanking signal – $\overline{\text{BLANK}}$ is low during blanking interval and high during active video.
DATA[11:0]	DV_{DD}	49–54, 59–64	I	DATA[11:0] is the pixel port
Reference Crystal				
XTALO	PVDD	34	I	Terminal for reference crystal for the internal video encoder PLL or external reference oscillator input.
XTALI	PVDD	33	I	Terminal for reference crystal for the internal video encoder PLL. Leave unconnected if an external oscillator is connected to XTAL0.
DVI Output				
TX2+	TVDD	28	A	Red channel positive transmitter output – positive side of red channel T.M.D.S. low voltage signal differential output pair. Red channel transmits red pixel data in active display and 00 control bits in blank.
TX2–	TVDD	27	A	Red channel negative transmitter output – Negative side of red channel T.M.D.S. low voltage signal differential output pair.
TX1+	TVDD	25	A	Green channel positive transmitter output – Positive side of green channel T.M.D.S. low voltage signal differential output pair. Green channel transmits green pixel data in active display and 00 control bits in blank.
TX1–	TVDD	24	A	Green channel negative transmitter output – Negative side of green channel T.M.D.S. low voltage signal differential output pair.
TX0+	TVDD	22	A	Blue channel positive transmitter output – Positive side of blue channel T.M.D.S. low voltage signal differential output pair. Blue channel transmits blue pixel data in active display and HSYNC, VSYNC control signals in blank.
TX0–	TVDD	21	A	Blue channel negative transmitter output – Negative side of blue channel T.M.D.S. low voltage signal differential output pair.
TXC+	TVDD	30	A	Clock positive transmitter output – Positive side of reference clock T.M.D.S. low voltage signal differential output pair.
TXC–	TVDD	31	A	Clock negative transmitter output – Negative side of reference clock T.M.D.S. low voltage signal differential output pair.
TFADJ	TVDD	19	A	T.M.D.S. drivers full scale adjust control A 2 kΩ resistor must be connected between this pin and TVSS.

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL POWER RAIL	TERMINAL NO.	I/O	DESCRIPTION
Analog Video Out				
CVBS	AVCC	40	A	Analog composite video output
Y/G	AVCC	41	A	Analog luminance video output Analog green output
C/R/Pr	AVCC	43	A	Analog chrominance output Analog red output Analog Pr output
B/Pb	AVCC	44	A	Analog blue output Component Pb output
COMP	AVCC	38	A	Compensation for the internal reference amplifier A 0.1 µF capacitor should be connected between this pin and AVCC.
AFADJ	AVCC	39	A	Full scale adjust control. A 920-Ω resistor should be connected between this pin and AVSS to control the full-scale output current on the analog outputs.
I2C Interface and Miscellaneous				
SCL	DV_{CC}	15	I/O	I2C serial clock input maximum. Clock rate of 400 kHz. Open drained I/O.
SDA	DV_{CC}	14	I/O	I2C Serial data line open drained I/O.
$\overline{RST}$	DV_{CC}	13	I	Reset signal active low.
HTPLG	DV_{CC}	11	I	DVI/P&D/DFP hot plug detect input
A0	DV_{CC}	10	I	I2C slave address select
HS/CS/GPIO1	AVCC	45	I/O	This signal is only active when RGB analog output is enabled. Digital horizontal sync output – This is the HSYNC signal that connects to the VGA connector. Digital composite sync output – Composite HSYNC and VSYNC. The polarity of this signal is programmable when used for HS/CS. General-purpose I/O #1 – Second general–purpose I/O. This pin has an internal weak pull–down of 1 MΩ (TBD). With GPIO1 as an input, use an external 10 kΩ resistor to pull up or down to set the state of this pin.
VS/FID	AVCC	46	O	Digital vertical sync output When the analog RGB video output is enabled this signal is the VSYNC that connects to the VGA connector. Digital field ID When the analog video output is interlaced (composite video, S–video, or interlaced component video), this signal indicates if the current field is ODD (first field) or EVEN (second field). The polarity of this signal is programmable.
GPIO0	DV_{CC}	18	I/O	General-purpose I/O #0 First general–purpose I/O. This pin has an internal weak pull-down of 1 MΩ (TBD). With GPIO0 as an input, use an external 10 kΩ resistor to pull up or down to set the state of this pin.
TEST	DV_{CC}	17	I	Test Mode Enable This pin must be tied to LOW for normal mode of operation. Connecting this pin to HIGH puts TFP6422/6424 in test mode.
Digital Video Input Port Voltage Reference				
V_{REF}	DVDDQ/2	3	A	Digital video input port voltage reference. – Sets the switching threshold of all the signals listed in Digital Video Input Port section of this table. VREF must be set to DVDDQ/2, where DVDDQ is the swing of the signals. DVDDQ ranges from 1.1 V to 1.8 V.

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL POWER RAIL	TERMINAL NO.	I/O	DESCRIPTION
Power and Ground				
DV_{DD}	1.8 V	1, 55	P	Digital Power
DVSS	0.0 V	6, 16, 48, 58	G	Digital ground
DV_{CC}	3.3 V	12	P	Digital power
TVDD	1.8 V	23, 29	P	Analog power for the DVI output drivers
TVSS	0.0 V	20, 26, 32	G	Analog ground for the DVI output drivers
AVCC	3.3 V	37, 47	P	Analog power for the video DACs
AVSS	0.0 V	42	G	Analog ground for the video DACs
PVDD	1.8 V	35	P	Power for PLLs
PVSS	0.0 V	36	G	Ground for PLLs

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

External DACs load resistance, RLdac . . . . . 0 Ω to open circuit
External T.M.D.S. termination resistance, RLtmds . . . . . 0 Ω to open circuit
External AFADJ resistor . . . . . 0 Ω to open circuit
External TFADJ resistor . . . . . 1 kΩ to open circuit
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Maximum total power dissipation, P_D . . . . . 2 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (ALL DATA PRELIMINARY)

		MIN	NOM	MAX	UNIT
Digital supply voltage, DV_{DD}		1.7	1.8	1.9	V
Digital supply voltage, DV_{CC}		3.13	3.3	3.47	V
Digital supply voltage, DVDDQ		1.0	1.8	1.9	V
Analog supply voltage, AVCC		3.13	3.3	3.47	V
Analog supply voltage, TVDD		1.7	1.8	1.9	V
Analog supply voltage, PVDD		1.7	1.8	1.9	V
Digital low–level input voltage, DV_{DD} V_{IL} (Scalable with VREF)				VREF– 100 mv	V
Digital low–level input voltage, DV_{DD} V_{IH} (Scalable with VREF)		VREF+ 100 mv			V
Digital low–level input voltage, DV_{CC} V_{IL}				0.8	V
Digital low–level input voltage, DV_{CC} V_{IH}					V
DVI 1280x1024 Resolution 60 Hz Refresh Rate	Digital supply current, DVDD			80	mA
	Digital supply current, DVDDQ			0	
	Analog supply current, TVDD			120	
	Analog supply current, AVCC			6	
	Analog supply voltage, PVDD			100	

PRODUCT PREVIEW

recommended operating conditions (ALL DATA PRELIMINARY) (continued)

		MIN	NOM	MAX	UNIT
Simultaneous composite and S–video	Digital supply current, DV_{DD}			150	mA
	Digital supply current, DVDDQ			20	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			135	
	Analog supply voltage, PVDD			100	
Composite video	Digital supply current, DV_{DD}			150	mA
	Digital supply current, DVDDQ			20	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			45	
	Analog supply voltage, PVDD			100	
S–video	Digital supply current, DV_{DD}			150	mA
	Digital supply current, DVDDQ			20	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			90	
	Analog supply voltage, PVDD			100	
Interlaced YPrPb component video	Digital supply current, DV_{DD}			150	mA
	Digital supply current, DVDDQ			20	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			135	
	Analog supply voltage, PVDD			100	
SCART (simultaneous composite and interlaced RGB)	Digital supply current, DV_{DD}			150	mA
	Digital supply current, DVDDQ			20	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			180	
	Analog supply voltage, PVDD			100	
Progressive RGB	Digital supply current, DV_{DD}			80	mA
	Digital supply current, DVDDQ			0	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			135	
	Analog supply voltage, PVDD			10	
Simultaneous composite and interlaced YPrPb component Video	Digital supply current, DV_{DD}			150	mA
	Digital supply current, DVDDQ			20	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			180	
	Analog supply voltage, PVDD			100	
Power Down	Digital supply current, DV_{DD}			10	mA
	Digital supply current, DVDDQ			0	
	Analog supply current, TVDD			0	
	Analog supply current, AVCC			0	
	Analog supply voltage, PVDD			10	
Reference voltage, V_{REF}		0.52	0.9	0.95	V
External DAC load resistor, Rldac, double termination			37.5		Ω
External T.M.D.S. termination resistor		45	50	55	Ω
External AFADJ resistor			TBD		Ω
External TFADJ resistor		1.4	2	2.6	kΩ
Output load resistance, DAC, C_L			25		pF
Operating free-air temperature, T_A		0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

dc digital I/O specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level digital input voltage†			2		DV_{DD}	V
V_{IL}	Low level digital input voltage†			0		0.8	V
I_{OH}	High level output drive current‡	ST = High,	V_{OH} = 2.4 V	TBD	18	TBD	mA
		ST = Low,	V_{OH} = 2.4 V	TBD	9	TBD	
I_{OL}	Low level output drive current‡	ST = High,	V_{OL} = 0.8 V	TBD	18	TBD	mA
		ST = Low,	V_{OL} = 0.8 V	TBD	9	TBD	
I_{OZ}	Hi-Z output current	$\overline{PD}$ = Low or $\overline{PDO}$ = Low		-10		10	µA
$V_{IK(–)}$	Input clamp voltage	I_{CL} = –18 mA		DGND-0.8			V
$V_{IK(+)}$		I_{CL} = 18 mA		DGND+0.8			
$V_{OK(\_)}$	Output clamp voltage	I_{CL} = –18 mA		DGND-0.8			
$V_{OK(+)}$		I_{CL} = 18 mA		DGND+0.8			

† Digital inputs are labeled DI in I/O column of Terminal Functions Table.
‡ Digital outputs are labeled DO in I/O column of Terminal Functions Table.

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Input differential voltage (see Note 1)		150		1200	mv
V_{IC}	Input common mode voltage (see Note 1)		AV_{DD}–300		AV_{DD}–37	mv
V_I	Open circuit analog input voltage		AV_{DD}–10		AV_{DD}+10	mv
$I_{DD(2PIX)}$	Normal 2-pix/clock power supply current (see Note 2)	Pixel Rate = 56 MHz 2-pix/clock	TBD	TBD	TBD	mA
I_{PD}	Power down current (see Note 3)	$\overline{PD}$ = Low	TBD	TBD	TBD	µA

NOTES: 1. Specified as dc characteristic with no overshoot or undershoot.
2. Alternating 2-pixel black/2-pixel white pattern. ST = high, $\overline{STAG}$ = high, QE[23:0] and QO[23:0] C_L = 10 pF.
3. Analog inputs are open circuit (transmitter is disconnected from TFP201).

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Differential input sensitivity†		150		1560	mV_{p-p}
$t_{(1)}$	Analog input intra-pair (+ to -) differential skew time				0.4	t_{bit}‡
$t_{(2)}$	Analog Input inter-pair or channel-to-channel skew time				1	t_{pix}§
$t_{(3)}$	Worse case differential input clock jitter tolerance¶				TBD	ns
$t_{r(1)}$	Rise time of data and control signals#, ‖	ST = Low, C_L=5 pF ST = High, C_L=10 pF			2.9 3.1	ns
$t_{f(1)}$	Fall time of data and control signals#, ‖	ST = Low, C_L=5 pF ST = High, C_L=10 pF			2.84 3.2	ns
$t_{r(2)}$	Rise time of ODCK clock#	ST = Low, C_L=5 pF ST = High, C_L=10 pF			TBD	ns
$t_{f(2)}$	Fall time of ODCK clock#	ST = Low, C_L=5 pF ST = High, C_L=10 pF			TBD	ns
$t_{su(1)}$	Setup time, data and control signal to falling edge of ODCK (OCK_INV = low)‖	ST = Low, C_L=5 pF ST = High, C_L=10 pF	TBD			ns
$t_{h(1)}$	Hold time, data and control signal to falling edge of ODCK (OCK_INV = low)‖	ST = Low, C_L=5 pF ST = High, C_L=10 pF	TBD			ns
$t_{su(2)}$	Setup time, data and control signal to rising edge of ODCK (OCK_INV = high)‖	ST = Low, C_L=5 pF ST = High, C_L=10 pF	TBD			ns
$t_{h(2)}$	Hold time, data and control signal to rising edge of ODCK (OCK_INV = high)‖	ST = Low, C_L=5 pF ST = High, C_L=10 pF	TBD			ns
$f_{(ODCK)}$	ODCK frequency	PIX = Low (1-PIX/CLK)	25		112	MHz
		PIX = High (2-PIX/CLK)	12.5		56	
	ODCK duty-cycle		40%	50%	60%	
$t_{d(1)}$	Propagation delay time from $\overline{PD}$ low to Hi-Z outputs				9	ns
$t_{d(2)}$	Propagation delay time from $\overline{PDO}$ low to Hi-Z outputs				9	ns
$t_{d(3)}$	Delay time from $\overline{PD}$ rising edge to inputs active					ns
$t_{d(4)}$	Pulse duration, minimum time $\overline{PD}$ low					ns
$t_{t(1)}$	Transition time between DE transition to SCDT low☆			1e6		t_{pix}
$t_{t(2)}$	Transition time between DE transition to SCDT high☆			1280		t_{pix}
$t_{s(1)}$	Delay time, ODCK latching edge to QE[23:0] data output	$\overline{STAG}$ = Low, Pixs = High		0.25		t_{pix}

† Specified as ac parameter to include sensitivity to overshoot, undershoot and reflection.
‡ t_{bit} is 1/10 the pixel time, tpix
§ t_{pix} is the pixel time defined as the period of the RxC input clock. The period of ODCK is equal to t_{pix} in 1-pixel/clock mode or $2t_{pix}$ when in 2-pixel/clock mode.
¶ Measured differentially at 50% crossing using ODCK output clock as trigger.
# Rise and fall times measured as time between 20% and 80% of signal amplitude.
‖ Data and control signals are : QE[23:0], QO[23:0], DE, HSYNC, VSYNC and CTL[3:1]
☆Link active or inactive is determined by amount of time detected between DE transitions. SCDT indicates link activity.

PRODUCT PREVIEW

functional description

overview

TFP6422 and TFP6424 integrates multiple video output interfaces in a single device in a compact 64-pin TQFP package. It supports all the most commonly used PC and consumer video standards as follows:

- DVI
- Composite video
  - NTSC–M
  - PAL–B,D,G,H,I
  - PAL–M
  - PAL–N
  - PAL–Nc
- S–Video
- SCART interface
- YPrPb Component video
- Analog RGB output

TFP6422 and TFP6424 integrates video encoder, color space converter, horizontal and vertical scaler, flicker-reduction filter, two PLLs, four DACs, DVI encoder, and three differential pairs of T.M.D.S. drivers. A dedicated high-speed low-pin count video pixel port transfers high-bandwidth digital video data from a graphics controller or other digital video source to the TFP6422 and TFP6424. All video modes share the same video pixel port.

The TFP6422 and TFP6424 is versatile and highly programmable to provide maximum flexibility for the users. An I^2C host interface is provided to program and configure the TFP6422 and TFP6424.

The TFP6424 also conforms to the Macrovision 7.11 copy protection scheme.

default modes after reset

Depending on the state of the $\overline{\text{INT0}}$/$\overline{\text{CBARE}}$ pin, TFP6422 and TFP6424 is reset to one of two default modes. If $\overline{\text{INT0}}$/$\overline{\text{CBARE}}$ is pullup, TFP6422 and TFP6424 will be initialized to be in DVI transmitter mode. If $\overline{\text{INT0}}$/$\overline{\text{CBARE}}$ pin is pull-down, TFP6422 and TFP6424 will be initialized to be in simultaneous composite and S-video out mode, and will display an internally generated color bar.

I^2C interface

The I^2C interface is used to access the internal TFP6422 and TFP6424 registers. This two–pin interface consists of one clock line, SCL, and one serial data line, SDA. The basic I^2C access cycles are shown in Figures 1 and 2.

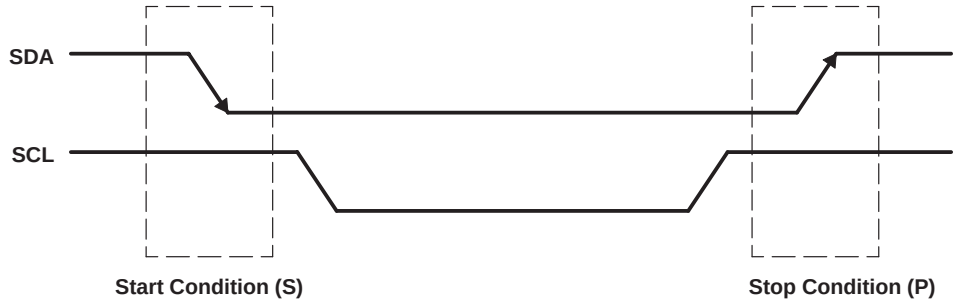


Figure 1. I^2C Stop and Stop Conditions

PRODUCT PREVIEW

I²C interface (continued)

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- A subaddress cycle
- Any number of data cycles
- A stop condition

The start and stop conditions are shown in Figure 2. The high to low transition of SDA while SCL is high defines the start condition. The low to high transition of SDA while SCL is high defines the stop condition. Each cycle, data or address, consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains 9 bits as shown in Figure 2.

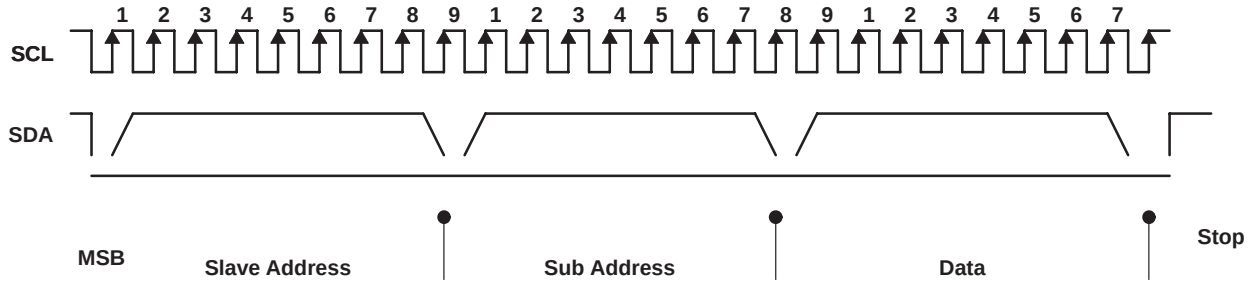


Figure 2. I²C Access Cycles

Following a start condition, each I²C device decodes the slave address. The TFP6422 and TFP6424 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent subaddress and data cycles the TFP6422 and TFP6424 responds with acknowledge as shown in Figure 3. The subaddress is auto-incremented after each data cycle.

The transmitting device must not drive the SDA signal during the acknowledge cycle so that the receiving device may drive the SDA signal low. The not acknowledge, $\overline{A}$, condition is indicated by the master by keeping the SDA signal high just before it asserts the stop, P, condition. This sequence terminates a read cycle as shown in Figure 4.

The slave address consists of 7 bits of address along with 1 bit of read/write information as shown below in Figures 3 and 4. For the TFP6422 and TFP6424, the possible slave addresses (including the r/w bit) are 0x40, 0x42 for write cycles and 0x41 and 0x43 for read cycles. Refer to register description, for additional base address information.

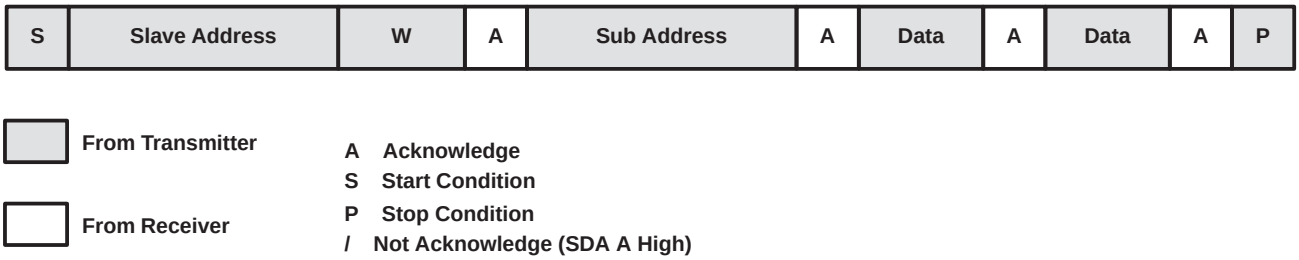


Figure 3. I²C Write Cycle

functional description (continued)

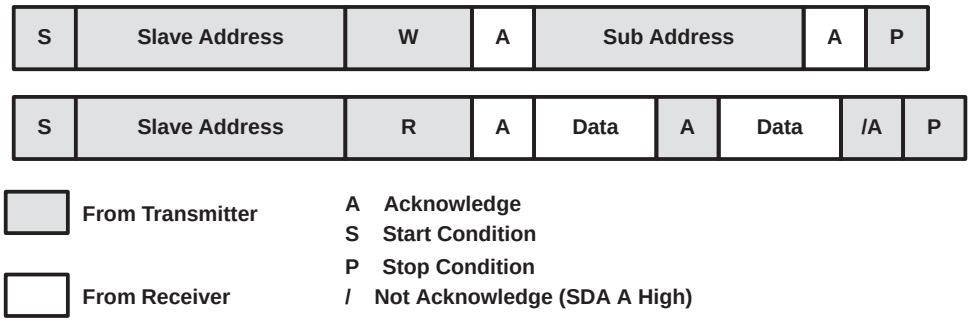


Figure 4. I²C Read Cycle

video port

The TFP6422/6424 Video Port is a low pin count, high-speed digital interface for a variety of digital video formats. The video port consists of a 12-bit data bus (DATA[11:0]), horizontal timing signal (HSYNC), vertical timing signal (VSYNC), blanking control ($\overline{\text{BLANK}}$), clock signals (CLKOUT, CLKIN0 and CLKIN) and interrupt request signals ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$). To reduce the pin count and the board space, a compact 12-bit pixel bus is used. The bus operates in either single-pump or double-pump mode depending on the selection of the input pixel format (FMT[2:0]). In single pump mode only the first edge of the CLKIN0/CLKIN1 differential clock pair is used to sample the data, timing and blanking control signals. In double-pump mode, both edges of the clock are used. With the double-pump mode high pixel transfer rates, up to 165 Mpixels/sec, can be achieved.

To ease the timing and EMI issues associated with a high pixel transfer rate, the signaling level of the signals in Video Port is scalable. The input signals in video port are scalable by adjusting the voltage on the V_{REF} pin to VDDQ/2. Similarly, the output signals are scalable by adjusting the voltage on the VDDQ pin to VDDQ, where VDDQ is the desirable full-swing voltage for the video port I/O signals. The differential CLKIN pair provides more robust and reliable sampling for the pixel data and control signals, alleviating tight setup and hold time requirements for high pixel transfer rates. Although differential clocking is the recommended clocking scheme, it is possible to use single-end clocking with reduced timing margin, which may be significant with high clock rates. When single-end clocking is used, CLKIN0 must be connected to the clock and CLKIN1 must be connected to VDDQ/2.

$\overline{\text{INT1}}$ and CLKOUT share the same pin. The function of the pin is defaulted to $\overline{\text{INT1}}$ immediately after reset. Reprogramming this may be done by writing to INTCKO bit. $\overline{\text{INT1}}$ generates an interrupt to inform the host CPU of events related to hot plug and power management. INT1# is open-drained and must be pulled up to VDDQ with a 10K resistor. When programmed for CLKOUT function, CLKOUT pin outputs the clock generated by the on-chip PLL. CLKOUT provides a reference clock which an external device, such as a graphics controller, may to generate the CLKIN0 and CLKIN1 signals. CLKOUT signal is also tightly coupled to the progressive to interlace conversion and overscan compensation functions. Refer to clock generation section for details for clock generation and overscan compensation.

$\overline{\text{INT0}}$ provides a dedicated interrupt for applications that need both CLKOUT signal and the interrupt signal. Similar to $\overline{\text{INT1}}$, $\overline{\text{INT0}}$ is open–drained and normally a 10K pull-up resistor is needed to pull the signal to VDDQ. TFP6422 and TFP6424 enters a special mode when $\overline{\text{INT0}}$ is forced to low just before the deassertion of $\overline{\text{RST}}$. In this special mode, TFP6422 and TFP6424 is in simultaneous composite and S-video output mode, and outputs an internally generated 100% color bar signal. No I²C programming is required to enable this feature. This feature is very useful for initial system diagnostics during product development, but is not recommended in the final product.

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functional description (continued)

digital input video formats

Utilizing its multiple digital input video formats, TFP6422 and TFP6424 provides a flexible interface to the external digital video sources such as compressed video from DVD, streaming video content from the Web, cable or any broadband media, graphics and text images typical for PCs. The digital input video formats are characterized by the following properties:

- Color space: RGB or YCbCr
- Pixel format: 4:4:4 or 4:2:2
- Color component order: Normal (Cb first) or reverse (Cr first)
- Scan format: Progressive or interlaced
- Synchronization: External sync or embedded sync

Although it is not cost effective to support all possible permutations of formats, TFP6422 and TFP6424 does support the most commonly used formats required by most of the applications. Refer to the video output section for the details of the supported digital input video formats.

The digital input video formats supported for a particular configuration are related to the video output formats. When TFP6422 and TFP6424 is programmed for one of TV video output modes, all digital input video formats listed in Table 3 are supported. When TFP6422 and TFP6424 is in either DVI or progressive RGB output mode, only RGB input formats are supported.

data manager

Data Manager resides at the very beginning of the processing pipeline. Data manager is responsible for receiving pixel data from the video port, and based on the selected input pixel format and output video format, performs format conversions and dispatches the converted pixel data to the proper video processing unit to create the required video output. The input pixel formats supported by TFP6422/6424 are described in detail in the F_CONTROL register, sub address 3A.

When TV video output mode is enabled (VIDOUT[3:0] = 0001, 0010, 0011, 0100 or 0101), data manager receives the pixel data in various formats from the video port and converts them to internal YUV representation required by the TV encoder for further TV video encoding process. When DVI output mode is enabled, the input pixel format must be set for 24-bit RGB mode (FMT[3:2] = 00) for correct operation and data manager passes the RGB data to the DVI encoder without processing. When RGB output mode is enabled, similar to DVI output mode, Data manager passes the RGB data to the video output DACs, converting the digital RGB pixel data to analog RGB video output.

Data manager consists of two functional units: RGB-to-YCbCr color space converter and chrominance decimator. The RGB-to-YCbCr color space converter converts the 24-bit RGB pixel data to 24-bit YCbCr representation with 8 bits in each of Y, Cb and Cr components. If the input pixel data is already in 24–bit YCrCb format, the data is bypasses the color space converter. The remaining Cb and Cr color components enter the 2-to-1 chrominance decimator which reduces the chrominance bandwidth and the amount of chrominance data by half. The reduction of chrominance data decreases the amount of buffering required for vertical scaling process by the scaling processor. If the input pixel data is already in 4:2:2 YCbCr format, both the RGB-to-YCrCb color space converter and chrominance decimator are bypassed.

functional description (continued)

Table 1. 100/100 Color Bar Table in 2's Complement

COLOR	Y (Hex)	Cr (Hex)	Cb (Hex)
White	6B	00	00
Yellow	52	12	90
Cyan	2A	90	26
Green	11	A2	B6
Magenta	EA	5E	4A
Red	D1	70	DA
Blue	A9	EE	70
Black	90	00	00

For diagnostic purposes, data manager can be forced to output 100/100 color bar YCbCr data by setting CBAR bit to 1. CBAR bit can be set to 1 through I^2C interface or can be defaulted to 1 after reset by pulling down $\overline{INT0}$/$\overline{CBARE}$ Pin (Pin 9). For normal operations, $\overline{INT0}$ pin should be pulled up.

DVI encoder

The DVI encoder receives RGB pixel data from Data Manager and encodes the pixel data based on the T.M.D.S. (Transition Minimized Differential Signaling) encoding algorithm. The DVI Encoder consists of three independent identical channels, each of which is responsible for encoding one color component. The encoding algorithm minimizes the signal transition while maintaining a good DC balance to reduce EMI. The encoded data is then serially shifted to the DVI output drivers for transmission. The low–voltage swing differential output further reduces EMI.

Each channel is encoded independently. Each channel receives 2 bits of control data and 8 bits of color component data. Depending on the state of BLANK#, the DVI encoder either encodes control data or color components. In either case, the data is encoded to 10–bit character and serially shifted out with the LSB transmitted first. Blue channel (Channel 0) receives HSYNC and VSYNC as the control data and the blue color component as the pixel data. If BLANK# is low, indicating valid blue component data is not transmitting, the DVI encoder of the blue channel encodes the HSYNC and VSYNC signals based on Table TBD. If BLANK# is high, indicating valid blue component data is transmitting, the DVI encoder encodes the blue component data based on the table in Appendix A. The Green channel (Channel1) and Red channel (Channel 2) operate in a way similar to Blue channel with the exception that the control bits are hardwired to '0'.

There are two possible encoded characters for each pixel data. The DVI encoder keeps tracks of the difference between the number of ones and zeros that have been sent and selects the character that minimizes the difference in order to maintain the best DC balance. Appendix A of this product datasheet contains a table mapping of the 256 8–bit RGB pixel data to one of two possible 10 bit T.M.D.S. characters.

A serializer serializes the 10–bit character in each channel. An on–chip PLL locks to the CLKIN0 and CLKIN1 and generates the 10X clock to drive the serializer. The 10X clock is also sent to the T.M.D.S. drivers for output.

scaling processor

The Scaling Processor scales down the input image in both horizontal and vertical directions. In addition to scaling, the Scaling Processor filters the image in the vertical direction and removes annoying flickers, which are common when computer–generated graphics or text, especially static images, are displayed on the TV. Scaling Processor uses a 5–tap adaptive filter for vertical scaling and filtering, whose coefficients are dynamically adjusted on a line–by–line basis to maintain optimal performance. To preserve maximum horizontal details, Scaling Processor scales internal encoding clock to process horizontal scaling.

scaling processor (continued)

The Scaling Processor is enabled when the video output mode is one of the TV output modes (VIDOUT[3:0] = 0001 through 0101) and the video input is progressive (FMT[[3:0] = any value other than 1000, 1001, 1100 and 1101).

Vertical scaling ratio registers VRATIOQ, VRATIOR, VRATIOQ2 and VRATIOR2 control the vertical scaling ratio. The proper values of the vertical scaling ratio registers are computed as a function of the number of lines from the input frame (defined in FLENS registers) and the number of the lines in the desired output frame (defined in FLEN registers). Arbitrary scaling ratio from 0.5 to 1.0 is supported. Refer to the description of the vertical scaling ratio registers for details.

VFLTR_CTRL register controls the filter characteristics of the vertical filter. The vertical filter performs both the vertical interpolation and deflicker filtering. INPT bit determines whether the nearest neighboring interpolated pixel (zero phase) or the interpolated dynamically adjusted pixel is to be used. The bandwidth of the vertical filter is also programmable. DEFLKR[2:0] defines the filter bandwidth, which ranges from near all–pass to a very narrow band. When selecting the bandwidth for an application, users must consider the trade–off between the sharpness of the image and the amount of flickers present in the image. Refer to the description of VFLTR_CTRL for details.

Horizontal scaling process is determined by the desired number of pixels in an input scan line and the nominal number of pixels in a scan line in the output frame. The desired number of pixels in a scan line is defined by the LLEN registers, while the nominal number of pixels in a scan line is determined by the SQP bit and FFRQ bit. See the description of BSTAMP register for details. The nominal number of pixels in a scan line determines the default video encoding timing when horizontal scaling is disabled. When horizontal scaling is enabled, an internal horizontal scaling ratio is computed and the internal video encoding time base is adjusted to account for the scaling ratio. The horizontal scaling also affects the subcarrier frequency and the close caption carrier frequency due to the change of the video encoding clock frequency. Both frequencies must be scaled proportionally in order to maintain the correct frequencies. Please refer to S_CARR and CC_CARR registers for details.

Scaling process is also tightly coupled to the video encoding clock and the clock of the video port. The clocks must be scaled precisely to guarantee correct operations. See Clock Generation for details.

clock generation

There are five clock signals in TFP6422/6424. XTALI/XTALO, CLKOUT, CLKIN0/CLKIN1, CLKENC and TXC–/TXC+.

XTALI and XTALO are terminals for the 14.31818 MHz crystal. When TFP6422/6424 is in TV video output modes, the on–chip PLL uses the 14.31818 MHz clock as a reference to generate CLKOUT and CLKENC. CLKOUT is output to an external device such as a graphics controller. The external device then uses CLKOUT as a reference and generates and outputs a clock signal back to the CLKIN0 and CLKIN1 pins on TFP6422/6424. CLKIN0 and CLKIN1 clock out the video pixel and control to the TFP6422/6424 Video Port. The clock connected to CLKIN0 and CLKIN1 can be differential or single–ended. When the clock is differential, CLKIN0 is the positive side of the clock and CLKIN1 is the negative side. In the case of single–ended, the clock connects to CLKIN0 and CLKIN1 is tied to VDDQ/2. CLKENC is an internal clock, thus not accessible externally. It is used by the internal video encoder core to encode the TV video output signal. Depending on the applications, it is also possible to connect CLKOUT directly to CLKIN0 signal.

clock generation (continued)

The frequencies of CLKENC and CLKOUT are controlled by PLL_X registers and PLL_Y registers, respectively. They must be related to each other, to other parameters and register values, in a precise manner for correct video encoding operations. The following equations describe their relationship.

CLKENC = 2*LLEN * Fh
CLKOUT = S*((FLENS+1)/(FLEN+1))*CLKENC

Where

LLEN = Number of pixels in a scan line
FLENS+1 = Number of lines in the input frame
FLEN+1 = Number of lines in the output frame
Fh = Line Frequency
S is an integer scaling factor that relates the frequencies between CLKIN and CLKOUT by CLKIN = CLKOUT/S. S accounts for the frequency divider used by the external device to divide CLKOUT to generate CLKIN. S takes on the value of 1 or 2.

Refer to the description of PLL_X registers and PLL_Y registers for the procedure to compute the values of PLL_X registers and PLL_Y registers to satisfy the relationship described above.

When TFP6422/6424 is in DVI or progressive RGB video output mode, similar to the case of TV video output modes, differential or single–ended CLKIN is used to clock the pixel data and control signals to TFP6422/6424. However, as opposed to TV video output modes, which use the clock signal on XTALI and XTAL0 as the reference, TFP6422/6424 uses CLKIN signal to generate the required clock for DVI and progressive RGB video output. The on–chip PLL takes CLKIN as the reference and generates the 10X clock. This clock is used internally by the DVI encoder to encode and clock out the DVI bit stream as well as to output TXC+ and TXC– differential clock along with the DVI data signals.

CLK_CTRL register provides additional control over the clock signals. CLKENCSE bit allows the internal video encoding clock CLKENC to bypass the PLL and connect directly to CLKIN. DKEN and CLKINDSK[2:0] allow the user to compensate the skew between CLKIN and the pixel data and control signals. Refer to the description of CLK_CTRL for details.

timing synchronization

When TFP6422/6424 is in TV video output modes, Video Encoder maintains a set of counters as an internal time reference to schedule various video encoding processes to take place, which include active video insertion, color burst insertion, horizontal sync and vertical sync pulse generation. The horizontal counters keep track of the current horizontal time base in terms of half pixels. The vertical counters maintain vertical time based in terms of half line. The field counters manage the field sequence. All the counters must be synchronized to the input video data and control signals for correct operation.

The synchronization is achieved by resetting the counters at the periodical synchronization events. Use HTRIGGER registers and VTRIGGER registers to program the values that the counters are reset to. These registers can be used to define the horizontal phase and vertical phase relationship between the input image and the output image.

When the input digital video is in interlace mode with embedded synchronization (FMT[3:0] = 1100 or 1101), the ‘F’ bit in the SAV and EAV codes is used to synchronize the vertical counter and the field counter, and the ‘H’ bit is used to synchronize the horizontal counter. At the ‘0’ to ‘1’ transition of ‘F’ bit, the field counter is reset to indicate EVEN field (second field) and the vertical counter is reset to the value defined in the VTRIGGER registers. At the ‘0’ to ‘1’ transition of ‘H’ bit, the horizontal counter is reset to the values defined in the HTRIGGER registers.

timing synchronization (continued)

When the input digital video is in interlace mode with external synchronization (FMT[3:0] = 1000 or 1001), the rising edge of the VSYNC resets the vertical counter and the rising edge of HSYNC resets the horizontal counter. The field counter in this case is free–running and does not reset. However, the FID pin outputs the current field ID(EVEN or ODD).

When the input digital video is in progressive mode with external sync, the Scaling Processor performs the scaling and the video port clock (CLKIN0 and CLKIN1) runs at a different frequency than the internal video encoding clock (CLKENC). As a result, the digital video input timing is somewhat decoupled from the internal video encoder timing. In this case, VSYNC (in the CLKIN domain) resets both the vertical counter and the horizontal counter (in CLKENC domain). Special precaution is taken in the synchronization logic to handle the potential metastability caused by a signal travelling across two different clock domains. The field counter does not reset and runs freely. The FID pin outputs the current field ID (EVEN or ODD).

When the input digital video is in progressive mode with embedded sync, the ‘0’ to ‘1’ transition of ‘V’ bit resets the vertical counter and the ‘0’ to ‘1’ transition of ‘H’ bit resets the horizontal counter. The field counter does not reset and runs freely. The FID pin outputs the current filed ID (EVEN or ODD).

The timing synchronization described above is not applicable when TFP6422/6424 is in DVI output or progressive RGB output mode.

As mentioned previously, when the Scaling Processor is enabled (TV video output mode and progressive digital video input), the time base of Video Encoder core is decoupled from the timing of the Video Port. A FIFO is placed between two domains to transfer the pixels across two domains. Video Encoder in this case acts as a master that sources the pixel data from the FIFO. The point of time at each output scan line when Video Encoder begins to request data is critical. It must be properly chosen not to overflow the FIFO. The point of time when each output scan line starts to request pixel data is controlled by BPIX registers. To avoid overflowing the FIFO, the HTRIGGER registers must be adjusted based on the value in BPIX.

See the descriptions of HTRIGGER, VTRIGGER and BPIX for details.

hot plug/unplug (auto connect/disconnect detection)

TFP6422/6424 supports Hot Plug/Unplug (auto connect/disconnect detection) for DVI link as well as the analog video connections. The connection status of DVI link, HOTPLUG sense pin and DACs output, is provided by the CON_STATUS register. RXCON bit indicates if a DVI receiver is connected to the TXC+ and TXC–. HPCON bit reflects the current state of the HTPLUG pin connected to the monitor via DVI connector. HTPLUG pin is 5V tolerant with an internal digital debouncing circuit to allow for direct connection to the DVI connector. DACCON[0:3] bits reflect the connection status on the output of the DACs on CVBS, Y/G, C/R/Pr and B/Pr pins.

Whenever one or more connection status bits change states, the corresponding bit in the IN_STATUS bit is to ‘1’ to record the changes. An interrupt can also be generated as an option. The interrupt for each type of connect/disconnect event can be individually enabled or disabled by writing a ‘1’ or ‘0’ to the corresponding bit in the INT_ENABLE register. Notice that INT_ENABLE register does not affect the state of the INT_STATUS bits. A host can either poll the INT_STATUS bits or rely on the interrupt to learn about the states or the change of states of the connections. The interrupt continues to be asserted until ‘1’ is written to the corresponding interrupt bit in the INT_STATUS register to reset the bit back to ‘0’. Writing ‘0’ to an interrupt status bit has no effect.

hot plug/unplug (auto connect/disconnect detection) (continued)

The hot plug/unplug detection indicated by HTPLUG bit is always enabled regardless of whether or not TFP6422 is in DVI video output mode. The DVI receiver detection indicated by RXCON is only enabled when DVI is not in fully off state. In other words, even if TFP6422 is not in DVI video output mode, it is still capable of detecting Hot Plug/Unplug. However it can detect only DVI receiver connect/disconnect events if DVI is not in fully off state. When TFP6422 is in one of the analog video output modes, the DAC connect/disconnect detection is automatically enabled for the DACs that are currently used to output analog video. In all video output modes, for the DACs that are inactive (in power-down mode), the connect/disconnect detection is normally disabled unless AVCDEN bit is set to 0. During the period that a particular type of connect/disconnect detection is disabled, the corresponding status bit in CON_STATUS register maintains its state just prior to disabling the detection.

power management

When TFP6422 and TFP6424 is in a particular video output mode, it shuts down the unused circuit(s) to save power. For example, when TV6422 and TV6424 is in DVI output mode, video encoder and all of four DACs are shut down. Only the PLLs and DVI encoder are active. When TFP6422 and TFP6424 is composite video output mode, both the DVI encoder and DVI drivers are powered down and only one DAC is active to output the composite video. The rest of the DACs are powered down. Refer to VIDOUT_CTRL for details.

video output

Table 2. Color Bar Test Pattern Values

	R	G	B	R†	G†	B†	Y	Cb	Cr
White	255	255	255	235	235	235	235	128	128
Yellow	255	255	0	235	235	0	210	16	146
Cyan	0	255	255	0	235	235	170	166	16
Green	0	255	0	0	235	0	145	54	34
Magenta	255	0	255	235	0	235	106	202	222
Red	255	0	0	235	0	0	81	90	240
Blue	0	0	255	0	0	235	41	240	110
Black	0	0	0	16	16	16	16	128	128

† These figures are only valid for non-switching lines. For switching lines, change the sign of the figures.

Table 3. 100/0/100/0 PAL (mV)

VIDOUT[3:0]	VIDEO OUTPUT TYPE	DVI DRIVERS PINS 21, 22, 24, 25, 27, 28, 30, 31	DACs			
			PIN 40	PIN 41	PIN 43	PIN 44
0000	DVI	DVI signals	PD	PD	PD	PD
0001	Simultaneous composite and S-video	PD	CVBS	Y	C	PD
0010	Composite video	PD	CVBS	PD	PD	PD
0011	S-video	PD	PD	Y	C	PD
0100	Interlaced YPrPb	PD	PD	Y	Pr	Pb
0101	SCART	PD	CVBS	G	R	B
0110	Progressive RGB	PD	PD	G	R	B
0111	Simultaneous composite and interlaced YPrPb	PD	CVBS	Y	Pr	Pb
1000	DACs connection detection	PD	HC	HC	HC	HC
1111	Powerdown	PD	PD	PD	PD	PD

Legend: PD = powerdown, CVBS = composite video, Y = luminance, C = chrominance, Pr = red color difference, Pb = blue color difference, R = red, G = green, B = blue, HC = half of the full-scale current = 17.4 mA

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DVI

composite video

Table 4. 100/7.5/100/7.5 NTSC Composts (IRE)

	LUMINANCE LEVEL (IRE)	U LEVEL (IRE)	V LEVEL (IRE)	CHROMI-NANCE LEVEL (IRE)	MINIMUM CHROMINANCE EXCURSION (IRE)6	MAXIMUM CHROMINANCE EXCURSION (IRE)	CHROMINANCE PHASE (DEGREE)
White	100.0	0.0	0.0	0.0	100.0	100.0	–
Yellow	89.5	–40.3	9.2	82.7	48.1	130.8	167.1
Cyan	72.3	13.6	–56.9	116.9	13.9	130.8	283.5
Green	61.8	–26.7	–47.6	109.2	7.2	116.4	240.7
Magenta	45.7	26.7	47.6	109.2	–8.9	100.3	60.7
Red	35.2	–13.6	56.9	116.9	–23.3	93.6	103.5
Blue	18.0	40.3	–9.2	82.7	–23.3	59.4	347.1
Black	7.5	0.0	0.0	0.0	7.5	7.5	–
Blank	0.0	0.0	0.0	0.0	0.0	0.0	–
Sync	–40.0	0.0	0.0	0.0	–	–	
Burst	0.0	–20.0	0.0	40.0	–20.0	20.0	180.0

Table 5. 100/7.5/100/7.5 NTSC Composts (mV)

	LUMINANCE LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	CHROMINANCE LEVEL (mV)	MINIMUM CHROMINANCE EXCURSION (mV)	MAXIMUM CHROMINANCE EXCURSION (mV)	CHROMINANCE PHASE (DEGREE)
White	1020	0	0	0	1020	1020	–
Yellow	945	–288	66	591	650	1241	167.1
Cyan	823	97	–406	835	405	1241	283.5
Green	748	–191	–340	780	358	1138	240.7
Magenta	633	191	340	780	243	1023	60.7
Red	557	–97	406	835	140	975	103.5
Blue	435	288	–66	591	140	731	347.1
Black	360	0	0	0	360	360	–
Blank	306	0.0	0.0	0.0	0.0	0.0	–
Sync	20	0	0	0	20	20	–
Burst	306	–143	0	286	163	449	180.0

Table 6. 100/0/100/0 NTSC (IRE)

	LUMINANCE LEVEL (IRE)	U LEVEL (IRE)	V LEVEL (IRE)	CHROMINANCE LEVEL (IRE)	MINIMUM CHROMINANCE EXCURSION (IRE)	MAXIMUM CHROMINANCE EXCURSION (IRE)	CHROMINANCE PHASE (DEGREE)
White	100.0	0.0	0.0	0.0	100.0	100.0	–
Yellow	88.6	–43.6	10.0	89.4	43.9	133.3	167.1
Cyan	70.1	14.7	–61.5	126.4	6.9	133.3	283.5
Green	58.7	–28.9	–51.5	118.1	–0.3	117.7	240.7
Magenta	41.3	28.9	51.5	118.1	–17.7	100.3	60.7
Red	29.9	–14.7	61.5	126.4	–33.3	93.1	103.5
Blue	11.4	43.6	–10.0	89.4	–33.3	56.1	347.1
Black	0.0	0.0	0.0	0.0	0.0	0.0	–
Blank	0.0	0.0	–	–	–	–	–
Sync	–40.0	0.0	–	–	–	–	–
Burst	0.0	–20.0	0.0	40.0	–20.0	20.0	180.0

Table 7. 100/0/100/0 NTSC (mV)

	LUMINANCE LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	CHROMINANCE LEVEL (mV)	MINIMUM CHROMINANCE EXCURSION (mV)	MAXIMUM CHROMINANCE EXCURSION (mV)	CHROMINANCE PHASE (DEGREE)
White	1020	0	0	0	1020	1020	
Yellow	939	–311	71	639	620	1258	167.1
Cyan	807	105	–439	903	355	1258	283.5
Green	725	–206	–368	843	304	1147	240.7
Magenta	601	206	368	843	179	1023	60.7
Red	520	–105	439	903	68	971	103.5
Blue	388	311	–71	639	68	707	347.1
Black	306	0	0	0	306	306	–
Blank	306	0	–	–	–	–	–
Sync	20	0	–	–	–	–	–
Burst	306	–143	0	286	163	449	180.0

Table 8. 100/0/100/0 PAL (IRE)

	LUMINANCE LEVEL (IRE)	U LEVEL (IRE)	V LEVEL (IRE)	CHROMINANCE LEVEL (IRE)	MINIMUM CHROMINANCE EXCURSION (IRE)	MAXIMUM CHROMINANCE EXCURSION (IRE)	CHROMINANCE PHASE† (DEGREE)
White	100.0	0.0	0.0	0.0	100.0	100.0	–
Yellow	88.6	–43.6	10.0	89.4	43.9	133.3	167.1
Cyan	70.1	14.7	–61.5	126.4	6.9	133.3	283.5
Green	58.7	–28.9	–51.5	118.1	–0.3	117.7	240.7
Magenta	41.3	28.9	51.5	118.1	–17.7	100.3	60.7
Red	29.9	–14.7	61.5	126.4	–33.3	93.1	103.5
Blue	11.4	43.6	–10.0	89.4	–33.3	56.1	347.1
Black	0.0	0.0	0.0	0.0	0.0	0.0	–
Blank	0.0	–	–	–	–	–	–
Sync	–43.0	–	–	–	–	–	–
Burst	0.0	–15.2	15.2	43.0	–25.5	21.5	135.0

† These figures are only valid for non-switching lines. For switching lines, subtract the figures from 360.

Table 9. 100/0/100/0 PAL (mV)

	LUMINANCE LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	CHROMINANCE LEVEL (mV)	MINIMUM CHROMINANCE EXCURSION (mV)	MAXIMUM CHROMINANCE EXCURSION (mV)	CHROMINANCE PHASE† (DEGREE)
White	1020	0	0	0	1020	1020	–
Yellow	941	–305	70	625	628	1253	167.1
Cyan	811	103	–430	884	369	1253	283.5
Green	732	–202	–360	826	319	1144	240.7
Magenta	610	202	360	826	197	1023	60.7
Red	530	–103	430	884	88	972	103.5
Blue	401	305	–70	625	88	714	347.1
Black	321	0	0	0	321	321	–
Blank	321	–	–	–	–	–	–
Sync	20	–	–	–	–	–	–
Burst	321	–106	106	301	171	471	135.0

† These figures are only valid for non-switching lines. For switching lines, subtract the figures from 360.

S-video

Table 10. 100/7.5/100/7.5 NTSC S-Video C Channel (mV)

	DC OFFSET LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	CHROMINANCE LEVEL (mV)	MINIMUM CHROMINANCE EXCURSION (mV)	MAXIMUM CHROMINANCE EXCURSION (mV)	CHROMINANCE PHASE (DEGREE)
White	652	0	0	0	652	652	–
Yellow	652	–288	66	591	357	948	167.1
Cyan	652	97	–406	835	235	1070	283.5
Green	652	–191	–340	780	262	1042	240.7
Magenta	652	191	340	780	262	1042	60.7
Red	652	–97	406	835	235	1070	103.5
Blue	652	288	–66	591	357	948	347.1
Black	652	0	0	0	652	652	–
Blank	652	–	–	–	–	–	–
Burst	652	–143	0	307	499	806	180.0

Table 11. 100/0/100/0 NTSC S-Video C Channel (mV)

	DC OFFSET LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	CHROMINANCE LEVEL (mV)	MINIMUM CHROMINANCE EXCURSION (mV)	MAXIMUM CHROMINANCE EXCURSION (mV)	CHROMINANCE PHASE (DEGREE)
White	652	0	0	0	652	652	–
Yellow	652	–288	66	639	333	972	167.1
Cyan	652	97	–406	903	201	1104	283.5
Green	652	–191	–340	842	231	1074	240.7
Magenta	652	191	340	843	231	1074	60.7
Red	652	–97	406	903	201	1104	103.5
Blue	652	288	–66	639	333	972	347.1
Black	652	0	0	0	652	652	–
Blank	652	–	–	–	–	–	–
Burst	652	–143	0	307	499	806	180.0

Table 12. 100/0/100/0 PAL S-Video C Channel (mV)

	DC OFFSET LEVEL (mV)	U LEVEL (mV)	V LEVEL† (mV)	CHROMINANCE LEVEL (mV)	MINIMUM CHROMINANCE EXCURSION (mV)	MAXIMUM CHROMINANCE EXCURSION (mV)	CHROMINANCE PHASE‡ (DEGREE)
White	652	0	0	0	652	652	–
Yellow	652	–305	70	625	340	965	167.1
Cyan	652	103	–430	884	210	1094	283.5
Green	652	–202	–360	826	240	1065	240.7
Magenta	652	202	360	826	240	1065	60.7
Red	652	103	430	884	210	1094	103.5
Blue	652	305	–70	625	340	965	347.1
Black	652	0	–	0	652	652	–
Blank	652	–	–	–	–	–	–
Burst	652	–106	106	301	502	803	180.0

† These figures are only valid for non-switching lines. For switching lines, change the sign of the figures.
‡ These figures are only valid for non-switching lines. For switching lines, subtract the figures from 360.

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YPbPr

Table 13. 100/7.5/100/7.5 NTSC YPbPr (mV)

	LUMINANCE LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	DC OFFSET Level (mV)	Pb LEVEL (mV)	Pr LEVEL (mV)
White	1020	0	0	652	652	652
Yellow	945	–350	57	652	303	709
Cyan	823	118	–350	652	770	303
Green	748	–232	–293	652	421	359
Magenta	633	232	293	652	884	945
Red	557	–118	350	652	534	1002
Blue	435	350	–57	652	1002	596
Black	360	0	0	652	652	652
Blank	306	–	–	–	–	–
Sync	20	–	–	–	–	–

Table 14. 100/0/100/0 NTSC YPbPr (mV)

	LUMINANCE LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	DC OFFSET Level (mV)	Pb LEVEL (mV)	Pr LEVEL (mV)
White	1020	0	0	652	652	652
Yellow	939	–350	57	652	303	709
Cyan	807	118	–350	652	770	303
Green	725	–232	–293	652	421	359
Magenta	601	232	293	652	884	945
Red	520	–118	350	652	534	1002
Blue	388	350	–57	652	1002	596
Black	306	0	0	652	652	652
Blank	306	–	–	–	–	–
Sync	20	–	–	–	–	–

Table 15. 100/0/100/0 PAL YPbPr (mV)

	LUMINANCE LEVEL (mV)	U LEVEL (mV)	V LEVEL (mV)	DC OFFSET Level (mV)	Pb LEVEL (mV)	Pr LEVEL (mV)
White	1020	0	0	652	652	652
Yellow	941	–350	57	652	303	709
Cyan	811	118	–350	652	770	303
Green	732	–232	–293	652	421	359
Magenta	610	232	293	652	884	945
Red	530	–118	350	652	534	1002
Blue	401	350	–57	652	1002	596
Black	321	0	0	652	652	652
Blank	321	–	–	–	–	–
Sync	20	–	–	–	–	–

SCART

Table 16. SCART RGB (mV)

	RED LEVEL (mV)	GREEN LEVEL (mV)	BLUE LEVEL (mV)
White	1020	1020	1020
Yellow	1020	1020	320
Cyan	320	1020	1020
Green	320	1020	320
Magenta	1020	320	1020
Red	1020	320	320
Blue	320	320	1020
Black	320	320	320
Blank	320	320	320
Sync	–	20	–

Table 17. Progressive RGB (mV)

	RED LEVEL (mV)	GREEN LEVEL (mV)	BLUE LEVEL (mV)
White	1020	1020	1020
Yellow	1020	1020	320
Cyan	320	1020	1020
Green	320	1020	320
Magenta	1020	320	1020
Red	1020	320	320
Blue	320	320	1020
Black	320	320	320
Blank	320	320	320
Sync	–	20	–

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luminance encoding

A programmable gain is first applied to the luminance data output from Data Manager or Scaling Processor depending on whether the Scaling Processor is bypassed or enabled. The luminance gain is defined by GAIN_Y register at subaddresses 5F and 60. The horizontal sync, vertical sync and setup insertion are then performed. Both black level and blank level are programmable through BLACK_LEVEL and BLANK_LEVEL registers at subaddresses 5D and 5E, respectively.

All the transition edges of the luminance signal, such as sync edges and active video edges, are properly shaped and filtered to limit the bandwidth within the standards.

luminance low-pass and interpolation filter

After all the necessary components of luminance signal have been added, the resultant signal is low–passed and interpolated to 2X–pixel rate. This 2X interpolation simplifies the external analog reconstruction filter design and improves the signal–to–noise ratio. Refer to Figures 8 and 9 for the filter frequency responses.

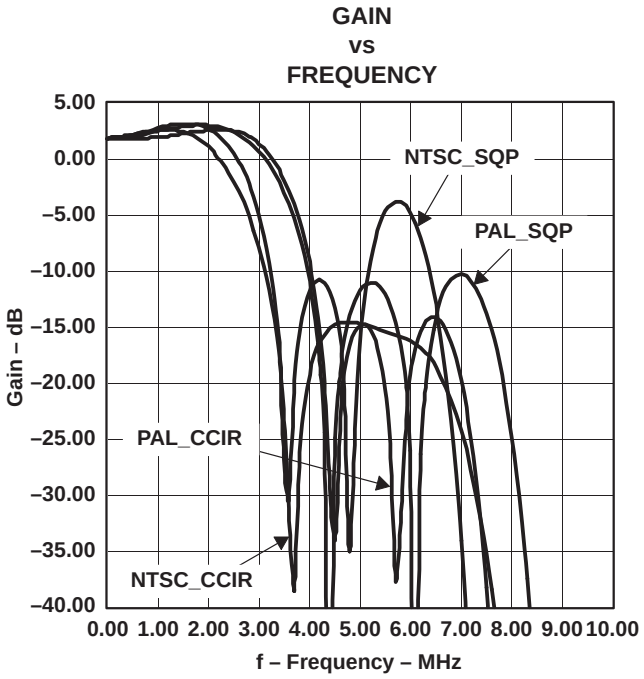

Figure 5. Luma Filter Frequency Response

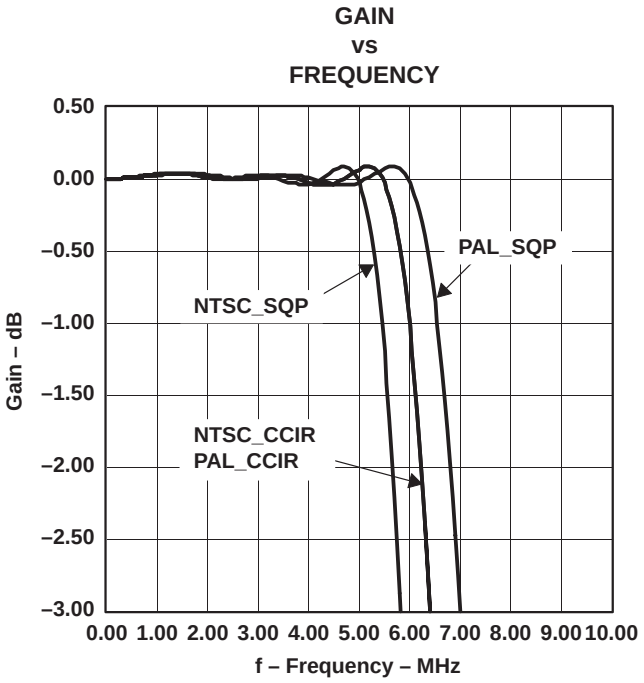

Figure 6. Luma Interpolation Filter Frequency Response

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cross color reduction filter

An optional cross color reduction filter can be applied to the luminance signal before the luminance signal combines with the chrominance signal to form the composite signal. The cross color reduction filter reduces the interference between luminance and chrominance in the composite signal. This filter does not apply to S-video.

chrominance encoding

A pair of programmable gains adjusts the time-multiplexed U/V signal. The gain for U and the gain for V are independently controlled by GAIN_U and GAIN_V register bits respectively at subaddresses 5B, 5C, 5D and 5E. The gain-adjusted signal then passes through a chrominance lowpass filter to limit the bandwidth of the U/V signal. See Figure 7 for the filter frequency response. The chrominance lowpass filter can be bypassed by setting CBW bit of M_CONTROL register at subaddress 61 to 0. This setting enlarges the bandwidth on U/V for S-video output.

The lowpass U/V signal is then subjected to a 1-to-4 interpolation through a two-stage interpolation filter. The data rate for both U and V is now at 2X-pixel rate.

The U and V signals are then quadrature-modulated by the internally generated subcarrier signal to form the chrominance (C) signal. The subcarrier reference signal color burst is inserted right before the active video.

chrominance encoding (continued)

The frequency, the phase of the modulating subcarrier and the amplitude of the color burst are all programmable. The S_CARR registers at subaddresses 63,64,65 and 66 control the subcarrier frequency. The values of the registers are computed based on the desired subcarrier frequency and the internal video encoding clock CLKENC using the equation in the register description. C_PHASE register at subaddress 5A controls the phase of the subcarrier. The phase of the color subcarrier is reset to C_PHASE. Four modes of color subcarrier reset are provided: reset every two lines, every two fields or every eight fields. Users can use C_PHASE register to adjust SCH (subcarrier to horizontal sync phase). BSTAP[6:0] of BSTAMP register at subaddress 62 sets the amplitude of the color burst. PAL bit of M_CONTROL register enables Phase Alternation Line encoding. A sweeping subcarrier is generated to encode the chrominance signal, when PAL bit is set to 1. Otherwise a normal subcarrier is generated. Phase Alternation Line refers to the encoding scheme in which subcarrier alternate between two phases every scan line. There are two possible alternation sequences and PALPHS bit of M_CONTROL register selects one of the sequences.

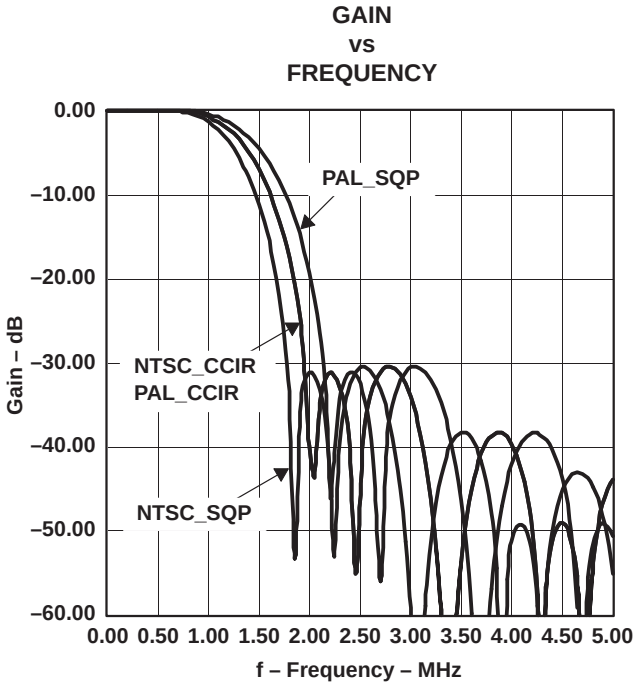

Figure 7. Chroma Filter Frequency Response

closed caption encoding

TFP6422 and TFP6424 can be programmed to encode closed caption data and extended data in the selected line. The closed caption data are sent to TFP6422 and TFP6424 through I^2C. The data stream consists of seven-bit US-ASCII code and one odd parity bit as shown in Figure 8.

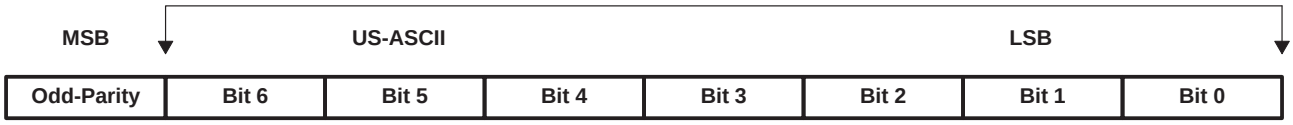

Figure 8. Closed Caption Data Format

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closed caption encoding (continued)

The standard service encodes closed caption only in the ODD field, while the extended service encodes closed caption in both fields. L21ENA, when set to 1, enables closed caption encoding in ODD field and L21ENB, when set to 1, enables closed caption encoding in EVEN field.

Use SLINE register at subaddress 6B to program the scan line where closed caption is to be encoded.

Four closed caption data registers contain the data to be encoded. Registers LINE21_O0 and LINE21_O1 contain the first byte and the second byte of close caption data to be encoded in the ODD field. Registers LINE21_E0 and LINE21_E1 contain the first byte and the second byte of data to be encoded in the EVEN field. Immediately after the closed caption data is written to the registers either in the ODD field or EVEN field, the corresponding closed caption status bit, CCE or CCO in STATUS register at subaddress 02, is reset to 0 to indicate that the closed caption data is available in the closed caption data registers and yet to be encoded. Immediately after the closed caption is encoded, CCE or CCO bit is set to 1 to indicate that the closed caption data has been encoded and is ready to accept new data. Null character is automatically inserted if the closed caption data is not written to the closed caption data registers in time for encoding.

The run–in clock frequency is 5034960.5 Hz ($32xf_{line}$ of NTSC). The closed caption data is encoded in the format of NRZ (Nonreturn to Zero). Additionally, the data translates to IRE scale in the following manner:

0 = 0 IRE; 1 = 50 IRE.

The following four diagrams present the parameters of closed caption line data implemented in different standards.

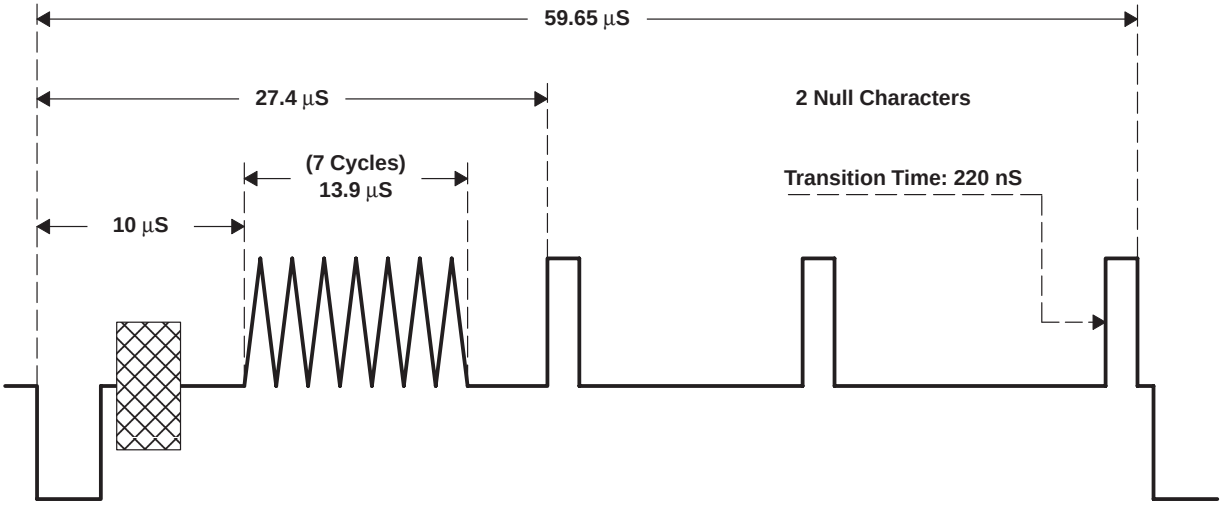

Figure 9. NTSC CCIR601 Rate Closed Caption Line

closed caption encoding (continued)

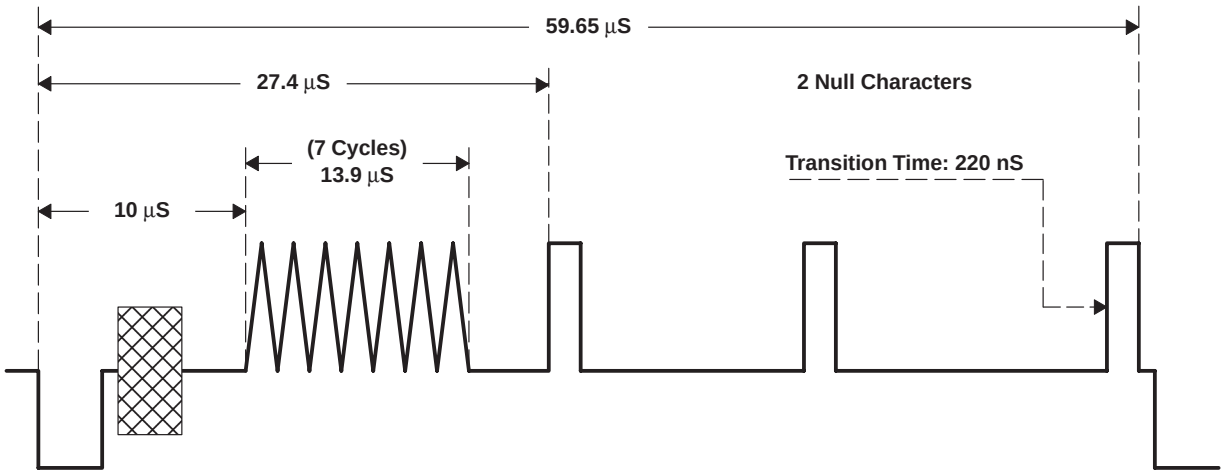

Figure 10. PAL CCIR601 Pixel Rate Closed Caption Line

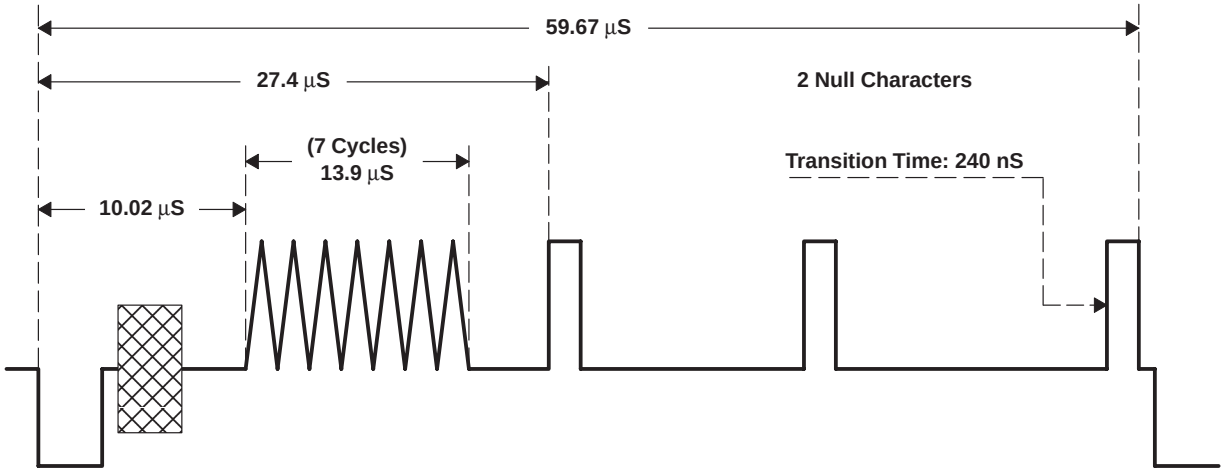

Figure 11. NTSC Square Pixel Rate Closed Caption Line

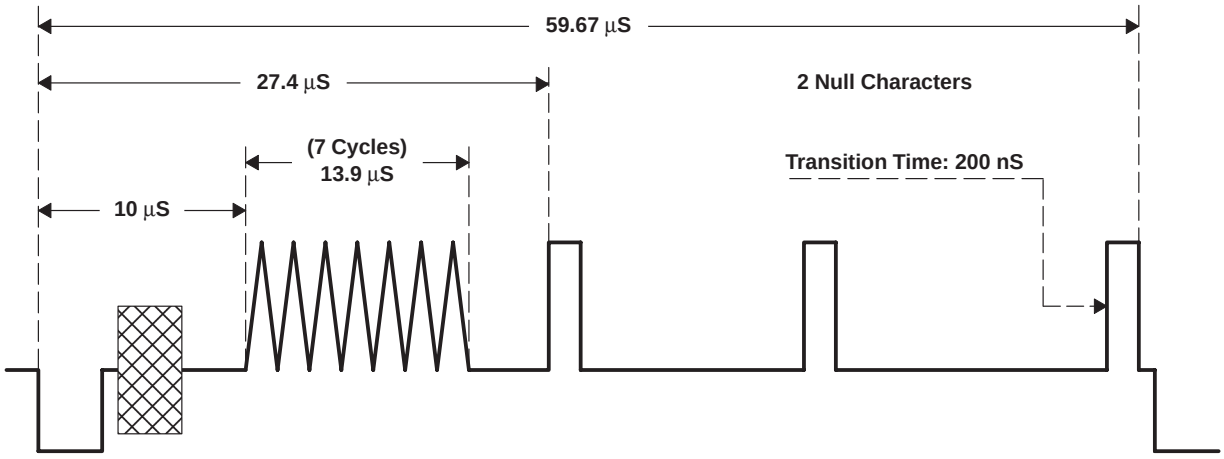

Figure 12. PAL Square Pixel Rate Closed Caption Line

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closed caption encoding (continued)

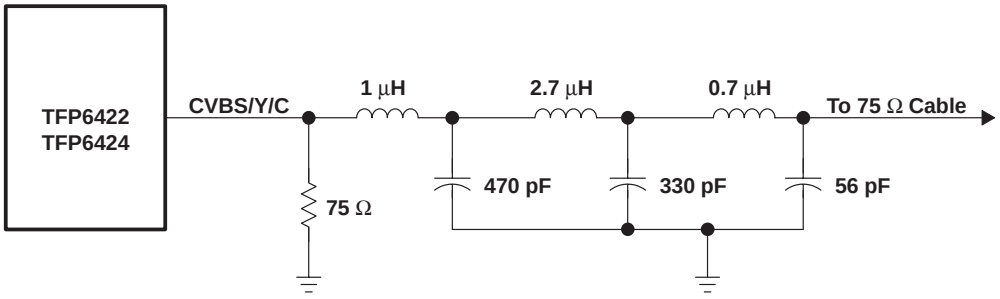

Figure 13. Output Filtering

register map

TFP6422 and TFP6424 is a standard I²C slave device. All the registers can be written and read through the I²C interface. The I²C base address of TFP6422 and TFP6424 is dependent on pin 10 (A0) as shown in Table 18 below.

Table 18. Base I²C Address

PIN 10	WRITE ADDRESS (HEX)	READ ADDRESS (HEX)
0	40	41
1	42	43

REGISTER	RW	SUBADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VEN_ID	R	00	Ven_id[7:0]							
	R	01	Ven_id[15:8]							
DEV_ID	R	02	Dev_Id[7:0]							
	R	03	Dev_id[15:8]							
REV_ID	R	04	Rev_Id[7:0]							
STATUS	R	05				Cce	Cco	Fsq[2:0]		
RESERVED		05–39	RESERVED							
F_CONTROL	RW	3A	Cbar	Intcko	RGBF		Fmt[3:0]			
CLK_CTRL	RW	3B				Ckindsk[3:0]				Ckencse
VIDOUT_CTRL	RW	3C					Vidout[3:0]			
SYNC_CTRL0	RW	3D	Syn_g	Fid_pol	Vs_fid	Hs_com	Vsen	Hsen	Tvsen	Thsen
CON_STATUS	R	3E			Daccon3	Daccon2	Daccon1	Daccon0	Hpcon	Rxcon
INT_STATUS	RW	3F							Hpevnt	Rxevnt
INT_ENABLE	RW	40							Hpen	Rxen
GP_CTRL	RW	41	Gio1_en		Gp1_in	Gp0_in	Gp1_oe	Gp0_oe	Gp1_out	Gp0_out
LLEN	RW	42	Llen[7:0]							
	RW	43						Llen[10:8]		
Flens	RW	44	Flens[7:0]							
	RW	45						Flens[10:8]		
PLL_X	RW	46	Pll_x[7:0]							
	RW	47	Pll_x[15:8]							
	RW	48	Pll_x[23:16]							
	RW	49	Pll_x_sf[1:0]		Pll_x[29:24]					

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REGISTER	RW	SUBADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PLL_Y	RW	4A	Pll_y[7:0]							
	RW	4B	Pll_y[15:8]							
	RW	4C	Pll_y[23:16]							
	RW	4D	Pll_y_sf[1:0]		Pll_y[29:24]					
PLL_BWRNG	RW	4E	Pll_bw[1:0]		Pll_adj	Pll_sel	Pll_hi[1:0]		Pll_lo[1:0]	
PLL_STATUS	R	4F	Pll_status[7:0]							
FIFO_DLY	RW	50	Fifo_dly[7:0]							
	RW	51	Fifo_dly[15:8]							
VRATIOR2	RW	52	Vratior2[7:0]							
VRATIOQ2	RW	53		Vratioq2[4:0]					Vratior2[29:8]	
VRATIOR	RW	54	Vratior [7:0]							
VRATIOQ	RW	55		Vratioq[4:0]					Vratior[9:8]	
VFLTR_CTRL	RW	56	Sc_load				Deflkr			Intp
HFLTR_CTRL	RW	57						Cintp[1:0]		Yintp
CC_CARR	RW	58	Fcc[7:0]							
	RW	59	Fcc[15:8]							
C_PHASE	RW	5A	Cphs[7:0]							
GAIN_U	RW	5B	Gu[7:0]							
GAIN_V	RW	5C	Gv[7:0]							
BLACK_LEVEL	RW	5D	Gu[8]	Black[6:0]						
BLANK_LEVEL	RW	5E	Gv[8]	Blank[6:0]						
GAIN_Y		5F	Gy[7:0]							
X_COLOR	RW	60		Xce	Gy[8]	Xcbw[1:0]		Lcd[2:0]		
M_CONTROL	RW	61			Palphs	Cbw[2:0]			Pal	Ffrq
BSTAMP	RW	62	Sqp	Bstap[6:0]						
S_CARR1	RW	63	Fsc[7:0]							
S_CARR2	RW	64	Fsc[15:8]							
S_CARR3	RW	65	Fsc[23:16]							
S_CARR4	RW	66	Fsc[31:24]							
LINE21_O0	RW	67	L21o[7:0]							
LINE21_O1	RW	68	L21o[15:8]							
LINE21_E0	RW	69	L21e[7:0]							
LINE21_E1	RW	6A	L21e[15:8]							
LN_SEL	RW	6B				Sline[4:0]				
RESERVED	RW	6C	RESERVED							
L21	RW	6D							L21ena	L21enb
HTRIGGER	RW	6E	Htrig[7:0]							
	RW	6F						Htrig]10:8]		
VTRIGGER	RW	70	Vtrig[7:0]							
	RW	71	Presa	Presb	Sblank				Vtrig[9:8]	
RESERVED		72–76	RESERVED							
BAVID	RW	77	Bavid7:0]							
EAVID	RW	78	Eavid[7:0]							
BEAVID	RW	79		Eavid[10:8]				Bavid[10:8]		
FLEN	RW	7A	Flen[7:0]							

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REGISTER	RW	SUBADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FAL	RW	7B	Fal[7:0]							
LAL	RW	7C	Lal[7:0]							
FLAL	RW	7D			Lal[8]	Fal[8]			Flen[9:8]	
SYN_CTRL1	RW	7E	Free	Esav	Ignp	Nblkns	Vblkm[1:0]		Hblkm[1:0]	
BORDER_Y	RW	7F	Border_y[7:0]							
BORDER_CR	RW	80	Border_cr[7:0]							
BORDER_CB	RW	81	Border_cb[7:0]							
BPIX	RW	82	BPIX[7:0]							
	RW	83						BPIX[10:8]		
VTRIG_CTRL	RW	84							A_vtrig	F_vtrig
RESERVED		85–8F	RESERVED							
RESERVED		90–A1	RESERVED							
RESERVED		A2–AF	RESERVED							
PLL_TST0	RW	B0	PLL test registers							
PLL_TST1	RW	B1								
PLL_TST2	RW	B2								
PLL_TST3	RW	B3								
FUSE_TST0	RW	B4	Fuse test registers							
FUSE_TST1	RW	B5								
FUSE_TST2	RW	B6								
FUSE_TST3	RW	B7								
TMDS_TST0	RW	C0	T.M.D.S. test registers							
TMDS_TST1	RW	C1								
TMDS_TST2	RW	C2								
TMDS_TST3	RW	C3								
TMDS_TST4	RW	C4								
TMDS_TST5	RW	C5								
TMDS_TST6	RW	C6								
TMDS_TST7	RW	C7								
TMDS_TST8	RW	C8								
TMDS_TST9	RW	C9								
TMDS_TST10	RW	CA								
TMDS_TST11	RW	CB								
TMDS_TST12	RW	CC								
TMDS_TST13	RW	CD								
TMDS_TST14	RW	CE								
TMDS_TST15	RW	CF								
DAC_TST	RW	D0	DAC test register							
RESERVED		D1–FF	Reserved							

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register description

The default register settings are indicated with (*). If two defaults are indicated, the state of $\overline{\text{INT0}}$ / $\overline{\text{CBARE}}$ at reset will determine which default is used.

VEN_ID **Subaddress = 00** **Read Only** **Default = 0x4C**

7	6	5	4	3	2	1	0
VEN_ID[7:0]							

Subaddress = 01 **Read Only** **Default = 0x01**

7	6	5	4	3	2	1	0
VEN_ID[15:8]							

This read-only register contains the 16–bit Texas Instruments vendor ID for the TFP6422/6424. VEN_ID[15:0] is hardwired to 0x014C.

DEV_ID **Subaddress = 02** **Read Only** **Default = 0x22/23**

7	6	5	4	3	2	1	0
DEV_ID[7:0]							

Subaddress = 03 **Read Only** **Default = 0x64**

7	6	5	4	3	2	1	0
DEV_ID[15:8]							

This read-only register contains the 16-bit device ID for the TFP6422 and TFP6424. The revision ID will identify different revisions of the device. For TFP6422, DEV_ID[15:0] is hardwired to 0x6422. For TFP6424, DEV_ID[15:0] is hardwired to 0x6424.

REV_ID **Subaddress = 03** **Read Only** **Default = 0x01**

7	6	5	4	3	2	1	0
REV_ID[7:0]							

This read-only register contains the revision ID for the TFP6422 and TFP6424. The revision ID will identify different revisions of the device. REV_ID[7:0] is hardwired to 0x01.

STATUS **Subaddress = 05** **Read Only**

7	6	5	4	3	2	1	0
			CCE	CCO	FSQ[2:0]		

CCE Closed caption status for even field. This bit is set immediately after the data in registers LINE21_E0 and LINE21_E1 have been encoded to closed caption. This bit is reset when both of these registers are written.

CCO Closed caption status for odd field. This bit is set immediately after the data in registers LINE21_O0 and LINE21_O1 have been encoded to closed caption. This bit is reset when both of these registers are written.

FSQ[2:0] Field sequence ID. For PAL, all three FSQ[2:0] are used whereas for NTSC only FSQ[1:0] is meaningful. Furthermore, FSQ[0] represents ODD field when it is 0 and EVEN field when it is 1.

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F_CONTROL **Subaddress = 3A** **Default = 0x8D**

7	6	5	4	3	2	1	0
CBAR	INTCKO	RGBF		FMT[3:0]			

Format Control Register. This register specifies the input video source and format.

CBAR Select Video Data Source.
- 0(*) Use external video source
- 1(*) Use internal color bars

INTCKO $\overline{\text{INT1}}$/CLKOUT pin function select
- 0(*) $\overline{\text{INT1}}$
- 1 CLKOUT

RGBF RGB /YCrCb input coding range
- 0(*) The input RGB data are in binary format with coding range 0–255
  The input YCrCb data are in binary format with coding range 0–255
- 1 The input RGB data are in binary format with coding range 16–235
  The input YCrCb data are in binary format conforming to ITU–601 standard

FMT[3:0] These four bits specify the video input data stream format and timing as shown in the table below.
H indicates the sampling point at the crossover of the rising edge of CLKIN0 and the falling edge of CLKIN1
L indicates the sampling point at the crossover of the falling edge of CLKIN0 and the rising edge of CLKIN1

Digital Input Video Data and Sync Format

FMT[3:2] = 00(*)								
Color space	RGB							
Pixel format	(8,8,8)							
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
	FMT[1:0]							
DATA[11:0]	00(*)		01		10		11	
	H	L	H	L	H	L	H	L
DATA[11]	R[7]	G[3]	G[3]	R[7]	R[7]	G[4]	G[4]	R[7]
DATA[10]	R[6]	G[2]	G[2]	R[6]	R[6]	G[3]	G[3]	R[6]
DATA[9]	R[5]	G[1]	G[1]	R[5]	R[5]	G[2]	G[2]	R[5]
DATA[8]	R[4]	G[0]	G[0]	R[4]	R[4]	B[7]	B[7]	R[4]
DATA[7]	R[3]	B[7]	B[7]	R[3]	R[3]	B[6]	B[6]	R[3]
DATA[6]	R[2]	B[6]	B[6]	R[2]	G[7]	B[5]	B[5]	G[7]
DATA[5]	R[1]	B[5]	B[5]	R[1]	G[6]	B[4]	B[4]	G[6]
DATA[4]	R[0]	B[4]	B[4]	R[0]	G[5]	B[3]	B[3]	G[5]
DATA[3]	G[7]	B[3]	B[3]	G[7]	R[2]	G[0]	G[0]	R[2]
DATA[2]	G[6]	B[2]	B[2]	G[6]	R[1]	B[2]	B[2]	R[1]
DATA[1]	G[5]	B[1]	B[1]	G[5]	R[0]	B[1]	B[1]	R[0]
DATA[0]	G[4]	B[0]	B[0]	G[4]	G[1]	B[0]	B[0]	G[1]

FMT[3:2] = 01								
Color space	YCrCb							
Pixel format	4:4:4							
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
	FMT[1:0]							
DATA[11:0]	00		01		10		11	
	H	L	H	L	H	L	H	L
DATA[11]	Cr[7]	Y[3]	Y[3]	Cr[7]	Cr[7]	Y[4]	Y[4]	Cr[7]
DATA[10]	Cr[6]	Y[2]	Y[2]	Cr[6]	Cr[6]	Y[3]	Y[3]	Cr[6]
DATA[9]	Cr[5]	Y[1]	Y[1]	Cr[5]	Cr[5]	Y[2]	Y[2]	Cr[5]
DATA[8]	Cr[4]	Y[0]	Y[0]	Cr[4]	Cr[4]	Cb[7]	Cb[7]	Cr[4]
DATA[7]	Cr[3]	Cb[7]	Cb[7]	Cr[3]	Cr[3]	Cb[6]	Cb[6]	Cr[3]
DATA[6]	Cr[2]	Cb[6]	Cb[6]	Cr[2]	Y[7]	Cb[5]	Cb[5]	Y[7]
DATA[5]	Cr[1]	Cb[5]	Cb[5]	Cr[1]	Y[6]	Cb[4]	Cb[4]	Y[6]
DATA[4]	Cr[0]	Cb[4]	Cb[4]	Cr[0]	Y[5]	Cb[3]	Cb[3]	Y[5]
DATA[3]	Y[7]	Cb[3]	Cb[3]	Y[7]	Cr[2]	Y[0]	Y[0]	Cr[2]
DATA[2]	Y[6]	Cb[2]	Cb[2]	Y[6]	Cr[1]	Cb[2]	Cb[2]	Cr[1]
DATA[1]	Y[5]	Cb[1]	Cb[1]	Y[5]	Cr[0]	Cb[1]	Cb[1]	Cr[0]
DATA[0]	Y[4]	Cb[0]	Cb[0]	Y[4]	Y[1]	Cb[0]	Cb[0]	Y[1]

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FMT[3:2] = 10								
Color space	YCrCb							
Pixel format	4:2:2							
FMT[1:0] = 00								
Scan	Interlaced							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cb0[7]		Y0[7]		Cr0[7]		Y1[7]	
DATA[6]	Cb0[6]		Y0[6]		Cr0[6]		Y1[6]	
DATA[5]	Cb0[5]		Y0[5]		Cr0[5]		Y1[5]	
DATA[4]	Cb0[4]		Y0[4]		Cr0[4]		Y1[4]	
DATA[3]	Cb0[3]		Y0[3]		Cr0[3]		Y1[3]	
DATA[2]	Cb0[2]		Y0[2]		Cr0[2]		Y1[2]	
DATA[1]	Cb0[1]		Y0[1]		Cr0[1]		Y1[1]	
DATA[0]	Cb0[0]		Y0[0]		Cr0[0]		Y1[0]	
FMT[1:0] = 01								
Scan	Interlaced							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cr0[7]		Y0[7]		Cb0[7]		Y1[7]	
DATA[6]	Cr0[6]		Y0[6]		Cb0[6]		Y1[6]	
DATA[5]	Cr0[5]		Y0[5]		Cb0[5]		Y1[5]	
DATA[4]	Cr0[4]		Y0[4]		Cb0[4]		Y1[4]	
DATA[3]	Cr0[3]		Y0[3]		Cb0[3]		Y1[3]	
DATA[2]	Cr0[2]		Y0[2]		Cb0[2]		Y1[2]	
DATA[1]	Cr0[1]		Y0[1]		Cb0[1]		Y1[1]	
DATA[0]	Cr0[0]		Y0[0]		Cb0[0]		Y1[0]	

FMT[3:2] = 10								
Color space	YCrCb							
Pixel format	4:2:2							
FMT[1:0] = 10								
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
DATA[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
DATA[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
DATA[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
DATA[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
DATA[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
DATA[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
DATA[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]
FMT[1:0] = 11								
Scan	Progressive							
Sync	HSYNC, VSYNC and $\overline{\text{BLANK}}$							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cr0[7]	Y0[7]	Cb0[7]	Y1[7]	Cr2[7]	Y2[7]	Cb2[7]	Y3[7]
DATA[6]	Cr0[6]	Y0[6]	Cb0[6]	Y1[6]	Cr2[6]	Y2[6]	Cb2[6]	Y3[6]
DATA[5]	Cr0[5]	Y0[5]	Cb0[5]	Y1[5]	Cr2[5]	Y2[5]	Cb2[5]	Y3[5]
DATA[4]	Cr0[4]	Y0[4]	Cb0[4]	Y1[4]	Cr2[4]	Y2[4]	Cb2[4]	Y3[4]
DATA[3]	Cr0[3]	Y0[3]	Cb0[3]	Y1[3]	Cr2[3]	Y2[3]	Cb2[3]	Y3[3]
DATA[2]	Cr0[2]	Y0[2]	Cb0[2]	Y1[2]	Cr2[2]	Y2[2]	Cb2[2]	Y3[2]
DATA[1]	Cr0[1]	Y0[1]	Cb0[1]	Y1[1]	Cr2[1]	Y2[1]	Cb2[1]	Y3[1]
DATA[0]	Cr0[0]	Y0[0]	Cb0[0]	Y1[0]	Cr2[0]	Y2[0]	Cb2[0]	Y3[0]

FMT[3:2] = 11								
Color space	YCrCb							
Pixel format	4:2:2							
FMT[1:0] = 00								
Scan	Interlaced							
Sync	F, V and H bits in the SAV and EAV codes are embedded in the video stream							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cb0[7]		Y0[7]		Cr0[7]		Y1[7]	
DATA[6]	Cb0[6]		Y0[6]		Cr0[6]		Y1[6]	
DATA[5]	Cb0[5]		Y0[5]		Cr0[5]		Y1[5]	
DATA[4]	Cb0[4]		Y0[4]		Cr0[4]		Y1[4]	
DATA[3]	Cb0[3]		Y0[3]		Cr0[3]		Y1[3]	
DATA[2]	Cb0[2]		Y0[2]		Cr0[2]		Y1[2]	
DATA[1]	Cb0[1]		Y0[1]		Cr0[1]		Y1[1]	
DATA[0]	Cb0[0]		Y0[0]		Cr0[0]		Y1[0]	
FMT[1:0] = 01								
Scan	Interlaced							
Sync	F, V and H bits in the SAV and EAV codes are embedded in the video stream							
DATA[11:0]	0H	0L	1H	1L	2H	2L	3H	3L
DATA[11]								
DATA[10]								
DATA[9]								
DATA[8]								
DATA[7]	Cr0[7]		Y0[7]		Cb0[7]		Y1[7]	
DATA[6]	Cr0[6]		Y0[6]		Cb0[6]		Y1[6]	
DATA[5]	Cr0[5]		Y0[5]		Cb0[5]		Y1[5]	
DATA[4]	Cr0[4]		Y0[4]		Cb0[4]		Y1[4]	
DATA[3]	Cr0[3]		Y0[3]		Cb0[3]		Y1[3]	
DATA[2]	Cr0[2]		Y0[2]		Cb0[2]		Y1[2]	
DATA[1]	Cr0[1]		Y0[1]		Cb0[1]		Y1[1]	
DATA[0]	Cr0[0]		Y0[0]		Cb0[0]		Y1[0]	
FMT[1:0] = 10 Reserved								
FMT[1:0] = 11 Reserved								

CLK_CTRL **Subaddress = 3B** **Default = 0xAA**

7	6	5	4	3	2	1	0
			CKINDSK[3:0]				CKENCSE

CKENCSE Video encoder core clock select
- 0 The clock signal generated by the on-chip clock generator PLL_Y is selected to encode the video
- 1(*) CLKIN is selected to encode the video

CKINDSK [3:0] CLKIN deskew control

0000 –8 T
0001 –7 T
0010 –6 T
0011 –5 T
0100 –4 T
0101 –3 T
0110 –2 T
0111 –T
1000(*) No Skew
1001 T
1010 2 T
1011 3 T
1100 4 T
1101 5 T
1110 6 T
1111 7 T

Where T = approximately 100 ps.

VIDOUT_CTRL **Subaddress = 3C** **Default = 0x00/01**

7	6	5	4	3	2	1	0
				VIDOUT[3:0]			

VIDOUT[3:0] Video output mode

0000(*)	DVI
0001(*)	Simultaneous composite and S–video
0010	Composite video
0011	S–video
0100	Interlaced YPrPb component video (525 or 625 lines)
0101	SCART (Simultaneous composite and interlaced RGB)
0110	Progressive RGB
0111	Simultaneous composite and interlaced YPrPb component video
1000	DACs connection testWrite 1000 to test the connection of four DACs. Read the connection status for each DAC from DACCON[3:0] bits in CON_STATUS register. See CON_STATUS for details.
1001–1110	Reserved
1111	Power down

VIDOUT[2:0] defaults to 0000 after reset if INT0# pin is pulled high or defaults to 0001 if $\overline{\text{INT0}}$ pin is pulled low during reset.

I^2C interface continues to be active in power down modes.

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SYNC_CTRL0 **Subaddress = 3D** **Default = 0x03**

7	6	5	4	3	2	1	0
SYNC_G	FID_POL	VS_FID	HS_COM	VSEN	HSEN	TYSEN	THSEN

THSEN DVI HSYNC enable
- 0 HSYNC is transmitted as 0
- 1(*) HSYNC is transmitted as received from the video port

TVSEN DVI VSYNC enable
- 0 VSYNC is transmitted as 0
- 1(*) VSYNC is transmitted as received from the video port

HSEN HS enable
- 0(*) HS is in inactive state (LOW)
- 1 HS outputs digital horizontal / composite sync

VSEN VS enable
- 0(*) VS is in inactive state (LOW)
- 1 VS outputs digital vertical sync

HS_COM HS function select
- 0(*) HS outputs horizontal sync
- 1 HS outputs composite sync

VS_FID VS function select
- 0(*) VS outputs vertical sync
- 1 VS outputs field ID

FID_POL FID polarity
- 0(*) ODD field = 0 EVEN field = 1
- 1 ODD field = 1 EVEN field = 0

SYNC_G RGB sync on green
- 0(*) No Sync on Green
- 1 Sync on Green

CON_STATUS **Subaddress = 3E** **Read Only**

7	6	5	4	3	2	1	0
		DACCON3	DACCON2	DACCON1	DACCON0	HPCON	RXCON

RXCON
- 0 DVI receiver is not connected
- 1 DVI receiver is connected

HPCON
- 0 Hot plug is not connected
- 1 Hot plug is connected

DACCON0
- 0 DAC0 output is not connected
- 1 DAC0 output is connected

DACCON1
- 0 DAC1 output is not connected
- 1 DAC1 is connected

DACCON2
- 0 DAC2 output is not connected
- 1 DAC2 output is connected

DACCON3
- 0 DAC3 output is not connected
- 1 DAC3 output is connected

INT_STATUS **Subaddress = 3F** **Read Only**

7	6	5	4	3	2	1	0
						HPEVNT	RXEVNT

RXEVNT 0 RXCON bit has not changed
1 RXCON bit has changed

HPEVNT 0 HPCON bit has not changed
1 HPCON bit has changed

To clear a bit, write 1 to the bit to clear. Writing 0 will not change the bit status.

INT_ENABLE **Subaddress = 40** **Default = 0x00**

7	6	5	4	3	2	1	0
						hpen	rxen

RXEN 0(*) RXEVNT interrupt disabled
1 RXEVNT interrupt enabled

HPEN 0(*) HPEVNT interrupt disabled
1 HPEVNT interrupt enabled

GP_CTRL **Subaddress = 41** **Default = 0x80**

7	6	5	4	3	2	1	0
GIO1_EN	Reserved	GP1_IN	GP0_IN	GP1_OE	GP0_OE	GP1_OUT	GP0_OUT

GP0_OUT General-purpose output bit. The state of this bit shows on GPIO0 pin if GP0_OE is set to 1. Otherwise, GPIO0 pin is 3-stated.
0(*) GPIO0 pin outputs LOW
1 GPIO0 pin outputs HIGH

GP1_OUT General-purpose output bit. The state of this bit shows on GPIO1 pin if GP1_OE is set to 1. Otherwise, GPIO1 pin is 3-stated.
0(*) GPIO1 pin outputs LOW
1 GPIO1 pin outputs HIGH

GP0_OE General-purpose bit output enable.
0(*) GPIO0 output is disabled and 3-stated
1 GPIO0 output is enabled

GP1_OE General-purpose bit output enable.
0(*) GPIO1 output is disabled and 3-stated.
1 GPIO1 output is enabled

GP0_IN General-purpose input bit. This bit shows the state of GPIO0 pin.
0(*) GPIO0 pin is LOW
1 GPIO0 pin is HIGH

GP0_IN General-purpose input bit. This bit shows the state of GPIO1 pin.
0(*) GPIO1 pin is LOW
1 GPIO1 pin is HIGH

GIO1_EN .GPIO1 pin enable
0(*) HC/CS/GPIO1 outputs Horizontal or composite sync
1 HC/CS/GPIO1 is used as the second general-purpose I/O pin.

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GIO1_EN	GP1_OUT	GP1_OE	HS_COM	HSEN	VSEN	Pin 45
0	X	X	0	0	X	LOW
0	X	X	0	1	X	HS
0	X	X	1	0	0	LOW
0	X	X	1	0	1	VS
0	X	X	1	1	0	HS
0	X	X	1	1	1	CS
1	0	0	X	X	X	3-state
1	0	1	X	X	X	LOW
1	1	0	X	X	X	3-state
1	1	1	X	X	X	HIGH

LLEN **Subaddress = 42** **Default = 0x59**

7	6	5	4	3	2	1	0
LLEN[7:0]							

Subaddress = 43 **Default = 0x03**

7	6	5	4	3	2	1	0
					LLEN[10:8]		

LLEN[10:0] Line length or total number of pixels in a scan line including active video and blanking. Total number of pixels in a scan line = LLEN

FLENS **Subaddress = 44** **Default = 0x0C**

7	6	5	4	3	2	1	0
FLENS[7:0]							

Subaddress = 45 **Default = 0x02**

7	6	5	4	3	2	1	0
					FLENS[10:8]		

FLENS[10:0] The frame length or total number of lines in a frame including active video and blanking from the source image. Total number of lines in a frame from the source image = FLENS + 1

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PLL_X **Subaddress = 46** **Default = 0xC9**

7	6	5	4	3	2	1	0
PLL_X[7:0]							

Subaddress = 47 **Default = 0x35**

7	6	5	4	3	2	1	0
PLL_X[15:8]							

Subaddress = 48 **Default = 0xD9**

7	6	5	4	3	2	1	0
PLL_X[23:16]							

Subaddress = 49 **Default = 0x94**

7	6	5	4	3	2	1	0
PLL_X_SF		PLL_X[29:24]					

PLL_X[29:0] 30-bit frequency control for the PLL that generates the internal video encoding clock.

PLL_X_SF[1:0] PLL scaling factor

Use the following equations to calculate PLL_X:

X = Round (5 × 2^(30 – PLL_X_SF) × Fref/(Fh × LLEN) × (FLENS+1)))
X1 = X × (FLENS+1)
Adjust PLL_X_SF such that 2^30 < X1 <= 2^31
PLL_X = X1–2^30
Where
Fref = Reference clock = 14.31818 MHz
Fh = Line frequency of the output video
LLEN = Length of a scan line in pixels
FLENS+1 = Length of a frame of source image in lines
The reset default values generate an internal 27 MHz video encoding clock.

PLL_Y **Subaddress = 4A** **Default = 0xC9**

7	6	5	4	3	2	1	0
PLL_Y[7:0]							

Subaddress = 4B **Default = 0x35**

7	6	5	4	3	2	1	0
PLL_Y[15:8]							

Subaddress = 4C **Default = 0xD9**

7	6	5	4	3	2	1	0
PLL_Y[23:16]							

Subaddress = 4D **Default = 0x94**

7	6	5	4	3	2	1	0
PLL_Y_SF		PLL_Y[29:24]					

PLL_Y[29:0] 30-bit frequency control for the PLL that generates the video PORT CLKOUT.

PLL_Y_SF[1:0] PLL_Y_SF scaling factor

Use the following equations to calculate PLL_Y:

For 1X output clock,

Y1 = X × (FLEN+1) × 2^(PLL_X_SF–PLL_Y_SF)
Adjust PLL_F_SF such that 2^30 < Y1 <= 2^31
PLL_Y = Y1–2^30
A clock derived from the CLKOUT with the same frequency must be connected to CLKIN for the correct operation.

For 2X output clock,

Y1 = X × (FLEN+1) × 2^(PLL_X_SF–PLL_Y_SF–1)
Adjust PLL_F_SF such that 2^31 < Y1 <= 2^30
PLL_Y = Y1–2^30
A clock derived from the CLKOUT with half the frequency must be connected to CLKIN for the correct operation.

Where:

FLEN +1 = Total number of lines per frame in the output video including active lines and vertical blanking
FLENS+1 = Total number of lines per frame in the input video including active lines and vertical blanking
The reset default values generate a 27 MHz clock on CLKOUT pin.

PLL_BWRNG **Subaddress = 4E** **Default = 0x00**

7	6	5	4	3	2	1	0
PLL_BW[1:0]		PLL_ADJ	PLL_SEL	PLL_HI[1:0]		PLL_LO[1:0]	

PLL_BW[1:0] PLL filter bandwidth control. PLL_BW[1:0] selects the bandwidth of the PLL loop filter when TFP6422/6424 is in DVI output mode (VIDOUT[2:0] = 000). The default value is 00 after reset. Users should always use the default value except when the signal conditions on the reference clock (CLKIN0 and CLKIN1) are too noisy. The narrower bandwidth results in better noise and jitter immunity of the reference clock at the expense of longer lock time.

- 00(*) Normal bandwidth
- 01 Wide bandwidth
- 10 Narrow bandwidth
- 11 Reserved

In nonDVI output modes, PLL_BW[1:0] is ignored and the loop filter bandwidth is fixed internally and cannot be changed.

PLL_ADJ PLL range adjustment select

- 0(*) PLL range adjustment is automatic
- 1 PLL range is manually adjusted by programming PLL_SEL, PLL_LO[1:0] and PLL_HI[1:0]

PLL_SEL PLL select

- 0(*) Low–range PLL is selected
- 1 High–range PLL is selected

PLL_HI[1:0] High–range PLL range select

- 00(*) Highest Frequency
- 01
- 10
- 11 Lowest frequency

PLL_LO[1:0] Low–range PLL range select

- 00(*) Highest frequency
- 01
- 10
- 11 Lowest frequency

PRODUCT PREVIEW

PLL_STATUS **Subaddress = 4F** **Read Only**

7	6	5	4	3	2	1	0
		STATUS_HI[2:0]			STATUS_LO[2:0]		

STATUS_LO[2:0] Low-range PLL lock status
- 001 The low-range PLL is not locked due to the selected frequency range being too low. PLL_LO[1:0] needs to be adjusted to move to a higher frequency range.
- 110 The low-range PLL is not locked due to the selected frequency range being too high. PLL_LO[1:0] needs to be adjusted to move to a lower frequency range.
- Other Low-range PLL is locked. Do not adjust PLL_LO[1:0]

STATUS_HI[2:0] High-range PLL lock status
- 001 The high-range PLL is not locked due to the selected frequency range being too low. PLL_HI[1:0] needs to be adjusted to move to a higher frequency range.
- 110 The high-range PLL is not locked due to the selected frequency range being too high. PLL_HI[1:0] needs to be adjusted to move to a lower frequency range.
- Other Low-range PLL is locked. Do not adjust PLL_HI[1:0]

FIFO_DLY **Subaddress = 50** **Default = 0xBC**

7	6	5	4	3	2	1	0
FIFO_DLY[7:0]							

Subaddress = 51 **Default = 0x02**

7	6	5	4	3	2	1	0
FIFO_DLY[15:8]							

FIFO_DLY[15:0] FIFO delay control1

PRODUCT PREVIEW

VRATIOQ2
VRATIOR2 **Subaddress = 52** **Default = 0x00**

7	6	5	4	3	2	1	0
VRATIOR2[7:0]							

Subaddress = 53 **Default = 0x00**

7	6	5	4	3	2	1	0
	VRATIQR2[4:0]					VRATIOR2[9:8]	

VRATIOQ2[4:0] Quotient part of the second vertical scaling ratio control

VRATIOR2[9:0] Remainder part of the second vertical scaling ratio control

Internal vertical scaling ratio control = VRATIOQ2 + VRATIOR2/(FLEN+1)

Use the following equations to calculate VRATIOQ2 and VRATIOR2:

VRATIOQ2 = FLOOR (((FLENS+1)/(FLEN+1) –1) * 64)

VRATIOR2 = 64* (FLENS–FLEN) – VRATIOQ * (FLEN+1)

Where

FLEN +1 = Total number of lines per frame in the output video including active lines and vertical blanking

FLENS+1 = Total number of lines per frame in the input video including active lines and vertical blanking

FLOOR(X) returns the greatest integer that is less then X.

VRATIOQ
VRATIOR **Subaddress = 54** **Default = 0x00**

7	6	5	4	3	2	1	0
VRATIOR[7:0]							

Subaddress = 53 **Default = 0x00**

7	6	5	4	3	2	1	0
	VRATIQ[4:0]					VRATIOR[9:8]	

VRATIOQ[4:0] Quotient part of the second vertical scaling ratio control

VRATIOR[9:0] Remainder part of the second vertical scaling ratio control

Internal vertical scaling ratio control = VRATIOQ + VRATIOR/(FLEN+1)

Use the following equations to calculate VRATIOQ and VRATIOR:

VRATIOQ = FLOOR (((FLENS+1)/(FLEN+1) –1) * 32)

VRATIOR = 32* (FLENS–FLEN) – VRATIOQ * (FLEN+1)

Where

FLEN +1 = Total number of lines per frame in the output video including active lines and vertical blanking

FLENS+1 = Total number of lines per frame in the input video including active lines and vertical blanking

FLOOR(X) returns the greatest integer that is less then X.

PRODUCT PREVIEW

VFLTR_CTRL **Subaddress = 56** **Default = 0x00**

7	6	5	4	3	2	1	0
SC_LOAD			SCBYPS	DEFLKR			INTP

INTP Vertical interpolation control for 5-tap interpolation filter
- 0(*) Single-phase nearest neighbor
- 1 Adaptive 32-phase interpolation

DEFLKR Vertical deflicker filter cut-off frequency control
- 000(*) Near all-pass
- 001 –6dB at 3/8 cycle per line
- 010 –6dB at 5/16 cycle per line
- 011 –6dB at 1/4 cycle per line
- 100 –6dB at 3/16 cycle per line
- 101–111 Reserved

SCBYPS Scaler Bypass
- 0(*) Scaler is enabled
- 1 Scaler is bypassed

SC_LOAD Load bit for scaling related registers to perform overscan compensation
- 0(*) No effects.
- 1 Enables the content of the I^2C registers for overscan compensation to be loaded into the internal hardware registers. A 0 to 1 transition at SC_LOAD bit will trigger the loading.

SC_LOAD affects the following register bits:
- CKENCSE
- CKOUTSE
- PLL_X [27:0]
- PLL_X_SF[1:0]
- PLL_Y[27:0]
- PLL_Y_SF[1:0]
- LLEN[10:0]
- LLEN_EN
- FLENS[10:0]
- VRATIOR[9:0]
- VRATIOQ[4:0]
- VRATIOR2[9:0]
- VRATIOQ2[4:0]

HFLTR_CTRL **Subaddress = 57** **Default = 0x00**

7	6	5	4	3	2	1	0
					CINTP		YINTP

YINTP Luminance interpolation filter control
- 0(*) The luminance interpolation filter is enabled
- 1 The luminance interpolation filter is bypassed

CINTP Chrominance interpolation filter control
- 00(*) The chrominance interpolation filter is enabled
- 01 The first section of the chrominance interpolation filter is bypassed
- 10 The second section of the chrominance interpolation filter is bypassed
- 11 Both sections of the filter are bypassed

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CC_CARR1,2 **Subaddress = 58** **Default = 0x31**

7	6	5	4	3	2	1	0
FCC[7:0]							

Subaddress = 59 **Default = 0x26**

7	6	5	4	3	2	1	0
FCC[15:8]							

FCC[15:0] Close caption carrier frequency control

For 60 Hz system,
FCC = 2^18* 0.5035*10^6/(LLEN*Fh)
For 50 Hz systems,
FCC = 2^18* 0.500*10^6/(LLEN*Fh)
Where
LLEN = Total number of pixels in a scan line
Fh = Line frequency

C_PHASE **Subaddress = 5A** **Default = 0x00**

7	6	5	4	3	2	1	0
CPHS[7:0]							

CPHS[7:0] Phase of the encoded video color subcarrier (including the color burst) relative to H–sync. The adjustable step is 360/256 degrees.

GAIN_U **Subaddress = 5B** **Default = 0x02**

7	6	5	4	3	2	1	0
GU[7:0]							

GU[7:0] Gain control for Cb signal. The MSB, GU[8], is located at subaddress 5D, bit 7. Following are typical programming examples for NTSC and PAL standards.

NTSC with 7.5 IRE pedestal:	WHITE – BLACK = 92.5 IRE	GAIN_U = 0x102
NTSC with no pedestal:	WHITE – BLACK = 100 IRE	GAIN_U = 0x117
PAL with no pedestal:	WHITE – BLACK = 100 IRE	GAIN_U = 0x111

GAIN_V **Subaddress = 5C** **Default = 0x6C**

7	6	5	4	3	2	1	0
GV[7:0]							

GU[7:0] Gain control for Cr signal. The MSB, GV[8], is located at subaddress 5E, bit 7. Following are typical programming examples for NTSC and PAL standards.

NTSC with 7.5 IRE pedestal:	WHITE – BLACK = 92.5 IRE	GAIN_V = 0x16C
NTSC with no pedestal:	WHITE – BLACK = 100 IRE	GAIN_V = 0x189
PAL with no pedestal:	WHITE – BLACK = 100 IRE	GAIN_V = 0x181

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BLACK_LEVEL **Subaddress = 5D** **Default = 0xC3**

7	6	5	4	3	2	1	0
GU[8]	BLACK[6:0]						

GU[8] The most significant bit of Gain_U register. See Gain_U register for more details.

BLACK[6:0] Black level setting. Following are typical programming examples for NTSC/PAL standards.

NTSC with 7.5 IRE pedestal:	WHITE – BLACK = 92.5 IRE	BLACK_LEVEL = 0x43
NTSC with no pedestal:	WHITE – BLACK = 100 IRE	BLACK_LEVEL = 0x38
PAL with no pedestal:	WHITE – BLACK = 100 IRE	BLACK_LEVEL = 0x3B

BLANK_LEVEL **Subaddress = 5E** **Default = 0xB8**

7	6	5	4	3	2	1	0
GV[8]	BLANK[6:0]						

GV[8] The most significant bit of Gain_V register. See Gain_V register for more details.

BLANK[6:0] Blank level setting. Following are typical programming examples for NTSC/PAL standards.

NTSC with 7.5 IRE pedestal:	WHITE – BLACK = 92.5 IRE	BLANK_LEVEL = 0x38
NTSC with no pedestal:	WHITE – BLACK = 100 IRE	BLANK_LEVEL = 0x38
PAL with no pedestal:	WHITE – BLACK = 100 IRE	BLANK_LEVEL = 0x3B

GAIN_Y **Subaddress = 5F** **Default = 0x2F**

7	6	5	4	3	2	1	0
GY[7:0]							

GU[7:0] Gain control for Y signal. The MSB, bit 8, is located at address 60, bit 5. Following are typical programming examples for NTSC and PAL standards.

NTSC with 7.5 IRE pedestal:	WHITE – BLACK = 92.5 IRE	GAIN_Y = 0x12F
NTSC with no pedestal:	WHITE – BLACK = 100 IRE	GAIN_Y = 0x147
PAL with no pedestal:	WHITE – BLACK = 100 IRE	GAIN_Y = 0x140

ANALOG VIDEO OUTPUT TYPE	SYNC IRE/mV	SETUP IRE/mV	PEAK WHITE IRE/mV	UV EXCURSION (mV)	Y_GAIN	U_GAIN	V_GAIN	BLACK_LEVEL	BLANK_LEVEL
Composite or S-video	–40(286)	7.5(54)	100	–	0x12F	0x102	0x16C	0x43	0x38
	–40(286)	0(0)	100	–	0x147	0x117	0x189	0x38	0x38
	–43(300)	0(0)	100	–	0x140	0x111	0x181	0x3B	0x3B
YPrPb	–40(286)	7.5(54)	100	±330	0x12F	0x102	0x16C	0x43	0x38
	–40(286)	0(0)	100	±357	0x147	0x117	0x189	0x38	0x38
	–43(300)	0(0)	100	±350	0x140	0x111	0x181	0x3B	0x3B
	–40(286)	7.5(54)	100	±350	0x12F	0x111	0x181	0x43	0x38
	–40(286)	0(0)	100	±350	0x147	0x111	0x181	0x38	0x38
	–43(300)	0(0)	100	±350	0x140	0x111	0x181	0x3B	0x3B

X_COLOR **Subaddress = 4D** **Default = 0x94**

7	6	5	4	3	2	1	0
	XCE	GU[8]	XCBW[1:0]		LCD[2:0]		

Cross Color and Chroma delay compensation register.

XCE Cross color reduction enable for composite video output. Cross color does not affect S-video output
0(*) Cross color reduction is disabled
1 Cross color is enabled

XCBW[1:0] Cross color reduction filter selection
00 The notch is at 32.8 % of the frequency of the encoding pixel clock
01 The notch is at 26.5 % of the frequency of the encoding pixel clock
10 The notch is at 30.0 % of the frequency of the encoding pixel clock
11 The notch is at 29.2 % of the frequency of the encoding pixel clock

LCD[2:0] These three bits can be used for chroma channel delay compensation. Table below shows the delay corresponding to LCD[2:0] settings.

LCD[2:0]			DELAY ON LUMA CHANNEL
0	0	0	0
0	0	1	0.5 pixel clock period
0	1	0	1.0 pixel clock period
0	1	1	1.5 pixel clock period
1	X	X	2.0 pixel clock period

M_CONTROL **Subaddress = 61** **Default = 0x05**

7	6	5	4	3	2	1	0
		PALPHS	CBW[2:0]			PAL	FFRQ

Mode control register. This register provides various operating mode controls including DAC power management.

PALPHS PAL switch phase setting
0(*) PAL switch phase is nominal
1 PAL switch phase is inverted compared to nominal

CBW[2:0] Chrominance lowpass filter bandwidth control
000(*)–6db at 21.8 % of encoding pixel clock frequency
001 –6db at 19.8 % of encoding pixel clock frequency
010 –6db at 18.0 % of encoding pixel clock frequency
011 Reserved
100 Reserved
101 –6db at 23.7 % of encoding pixel clock frequency
110 –6db at 26.8 % of encoding pixel clock frequency
111 Chrominance lowpass filter bypass

PAL Phase alternation line encoding selection
0(*) Phase alternation line encoding disabled
1 Phase alternation line encoding enabled

FFRQ Field rate selection.
0 50 Hz
1(*) 60 Hz

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BSTAMP **Subaddress = 62** **Default = 0x38**

7	6	5	4	3	2	1	0
SQP	BSTAP[6:0]						

Color burst amplitude.

SQP Square-pixel sampling rate.
0(*) CCIR601 sampling rate
1 Square-pixel sampling rate

BSTAP[6:0] Setting of amplitude of color burst.

The SQP and FFRQ bits determine the total number of horizontal pixels displayed per scan line as shown in the following register.

MODE	SQP	FFRQ	NO. OF PIXEL PER LINE
CCIR601 PAL	0	0	864
CCIR601 NTSC	0	1	858
Square pixel PAL	1	0	944
Square pixel NTSC	1	1	780

S_CARR1,2,3,4 **Subaddress = 63.64.65,66** **Default = 0x1F, 0x7C, 0xF0, 0x21**

7	6	5	4	3	2	1	0
FCS[7:0]							
FSC[15:8]							
FSC[23:16]							
FSC[31:24]							

Color Subcarrier Frequency Registers.

FSC[31:0] These four bytes' data are used to program color subcarrier frequency. These four bytes are determined by the following formula.

$S\_CARR = ROUND((Fsc/Fclkenc) * 2^{32})$

Where Fsc = Frequency of the subcarrier
Fclkenc = Frequency of the internal video encoding clock
= 2*LLEN *Fh
LLEN = Number of pixels in a scan line
Fh = Line frequency

Refer to the description of LLEN registers (subaddresses 0x42 and 0x43).

The following register lists some common values for S_Carr.

STANDARD	PIXEL TYPE	SUBCARRIER FREQUENCY (Fsc)	Fclkin	S_Carr (Dec)	S_Carr (Hex)
M/NTSC	Rectangular	3.579545 MHz	27 MHz	569408543(*)	21F07C1F
B,D,G,H,I,N/PAL	Rectangular	4.43361875 MHz	27 MHz	705268427	2A098ACB
N/PAL; Argentina	Rectangular	3.58205625 MHz	27 MHz	569807942	21F69446
	Rectangular	3.5756083125 MHz	27 MHz	568782819	21E6EFE3
M/NTSC	Square	3.579545 MHz	24.5454 MHz	626349397	25555555
B,D,G,H,I,N/PAL	Square	4.43361875 MHz	29.50 MHz	645499916	26798C0C
N/PAL; Argentina	Square	3.58205625 MHz	29.50 MHz	521519134	1F15C01E
	Square	3.5756083125 MHz	24.5454 MHz	625661101	254AD4AD

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PIXEL TYPE	SUBCARRIER FREQUENCY (Fsc)	CLOCK (Fclock)	S_Carr (Dec)	S_Carr (Hex)
Rectangular	3.5795452 MHz	27 MHz	569408543(*)	21F07C1F
Rectangular	4.43361875 MHz	27 MHz	705268427	2A098ACB
Rectangular	3.58205625 MHz	27 MHz	569807942	21F69446
Rectangular	3.5756083125 MHz	27 MHz	568782819	21E6EFE3
Square	3.579545 MHz	24.5454 MHz	626349397	25555555
Square	4.43361875 MHz	29.50 MHz	645499916	26798C0C
Square	3.58205625 MHz	29.50 MHz	521519134	1F15C01E
Square	3.5756083125 MHz	24.5454 MHz	625661101	254AD4AD

LINE21_O0 **Subaddress = 67** **Default = 0x00**

7	6	5	4	3	2	1	0
L21O[7:0]							

L21O[7:0] The least significant byte of the closed caption data in the odd field.

LINE21_O1 **Subaddress = 68** **Default = 0x00**

7	6	5	4	3	2	1	0
L21O[15:8]							

L21O[15:8] The most significant byte of the closed caption data in the odd field.

LINE21_E0 **Subaddress = 69** **Default = 0x00**

7	6	5	4	3	2	1	0
L21E[15:8]							

L21E[7:0] The least significant byte of the extended service data in the even field.

LINE21_E1 **Subaddress = 6A** **Default = 0x00**

7	6	5	4	3	2	1	0
L21E[15:8]							

L21E[15:8] The least significant byte of the extended service data in the even field.

LN_SEL **Subaddress = 6B** **Default = 0x0B**

7	6	5	4	3	2	1	0
			SLINE[4:0]				

SLINE[4:0] Selects the line where closed caption or extended service data are encoded.

L21 **Subaddress = 6D** **Default = 0x00**

7	6	5	4	3	2	1	0
						L21ENA	L21ENB

L21ENA This bit controls the closed caption encoding. See following register for programming information.

L21ENB This bit controls the closed caption encoding. See following register for programming information.

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L21ENA	L21ENB	Line21 ENCODING MODE
0(*)	0(*)	Line21 encoding OFF
0	1	Enables encoding in 1st field (odd field)
1	0	Enables encoding in 2nd field (even field)
1	1	Enables encoding in both fields

HTRIGGER0 **Subaddress = 6E** **Default = 0x00**

7	6	5	4	3	2	1	0
HTRIG[7:0]							

HTRIG[7:0] LSB of horizontal trigger phase, which sets HSYNC. HTRIG is expressed in half-pixels or clk2x periods.

HTRIGGER1 **Subaddress = 6F** **Default = 0x00**

7	6	5	4	3	2	1	0
					HTRIG[10:8]		

HTRIG[11:8] MSB of horizontal trigger phase, which sets HSYNC. HTRIG is expressed in half-pixels or clk2x periods.

VTRIGGER0 **Subaddress = 70** **Default = 0x00**

7	6	5	4	3	2	1	0
VTRIG[7:0]							

Subaddress = 71 **Default = 0xC0**

7	6	5	4	3	2	1	0
PRESA	PRESB	SBLANK				VTRIG[9:8]	

PRESA Phase reset A. Used as shown in the register below.

PRESB Phase reset B. Used as shown in the register below. Color subcarrier phase is reset to C_Phase (subaddress 5A) upon reset.

SBLANK Vertical blanking setting
0(*) Vertical blanking is defined by the setting of FAL and LAL registers.
1 Vertical blanking is forced automatically during field synchronization and equalization.

VTRIG[9:0] Vertical trigger reference for VSYNC. These bits specify the phase between VSYNC input and the lines in a field. The VTRIG field is expressed in units of half-line.

PRESA	PRESB	PHASE RESET MODE
0	0	No resest
0	1	Reset every two lines
1	0	Reset every eight fields
1(*)	1(*)	Reset every four fields

BAVID **Subaddress = 77** **Default = 0x00**

7	6	5	4	3	2	1	0
BAVID[7:0]							

Beginning of active video.

BAVID[7:0]

EAVID **Subaddress = 78** **Default = 0x00**

7	6	5	4	3	2	1	0
EAVID[7:0]							

End of active video.

EAVID[7:0]

BEAVID **Subaddress = 79** **Default = 0x00**

7	6	5	4	3	2	1	0
	EAVID[10:8]				BAVID[10:8]		

Overflow register for BAVID and EAVID fields.

FLEN **Subaddress = 7A** **Default = 0x0C**

7	6	5	4	3	2	1	0
FLEN[7:0]							

Field Length

FLEN[7:0] These bits define the number of half_lines in each field. The upper 2 bits of this register are located in FLAL register.

Length of field = (FLEN + 1) half_lines

FAL **Subaddress = 7B** **Default = 0x12**

7	6	5	4	3	2	1	0
FAL[7:0]							

First Active Line of Field

FAL[7:0] These bits define the first active line of a field. The MSB is located in register FLAL.

LAL **Subaddress = 7C** **Default = 0x03**

7	6	5	4	3	2	1	0
LAL[7:0]							

Last Active Line of Field

LAL[7:0] These bits define the last active line of a field. The MSB is located in register FLAL.

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flal **Subaddress = 7d** **Default = 0x22**

7	6	5	4	3	2	1	0
		LAL[8]	FAL[8]			FLEM[9:8]	

Overflow bits from FLEN, FAL and LAL Registers.

LAL[8] These bits define the last active line of a field. The LSB is located in register LAL.

FAL[8] These bits define the first active line of a field. The LSB is located in register FAL.

FLEN[9:8] These bits define the number of half_lines in each field. The lower 8 bits of this register are located in FLEN register.

SYN_CTRL1 **Subaddress = 7E** **Default = 0x00 or 0x80**

7	6	5	4	3	2	1	0
FREE	ESAV	IGNP	NBLNKS	VBLKM[1:0]		HBLKM[1:0]	

FREE Free running
- 0(*) Free running disabled.
- 1(*) Free running enabled. HSYNC and VSYNC are ignored.

Reset to 0 if the CBAR pin is high upon reset otherwise reset to 1.

ESAV Enable to detect F and V bits only on EAV in CCIR656 input mode
- 0(*) Detection of F and V bits on both EAV and SAV
- 1 Detection of F and V bits only on EAV.

IGNP Ignore protection bits in CCIR656 input mode
- 0(*) Protection bits are not ignored.
- 1 Protection bits are ignored

NBLNKS Blank shaping
- 0(*) Blank shaping enabled
- 1 Blank shaping disabled

VBLKM[1:0] Vertical blanking mode
- 00(*) Internal default blanking
- 01 Internal default blanking AND internal programmable blanking defined by FAL and LAL
- 10 Internal blanking and external blanking defined by $\overline{\text{BLANK}}$
- 11 Internal blanking AND internal programmable blanking defined by FAL and LAL AND external blanking defined by $\overline{\text{BLANK}}$

HBLKM[1:0] Horizontal blanking mode
- 00(*) Internal default blanking
- 01 Internal programmable blanking defined by SAVID and EAVID
- 10 External blanking defined by $\overline{\text{BLANK}}$
- 11 Internal programmable blanking defined by SAVID and EAVID AND external blanking defined by $\overline{\text{BLANK}}$

BORDER_Y **Subaddress = 7F** **Default = 0x10**

7	6	5	4	3	2	1	0
BORDER_Y[7:0]							

BORDER_Y[7:0] Y component of the border color

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BORDER_CR **Subaddress = 80** **Default = 0x80**

7	6	5	4	3	2	1	0
BORDER_CR[7:0]							

BORDER_CR[7:0] CR component of the border color

BORDER_CB **Subaddress = 81** **Default = 0x80**

7	6	5	4	3	2	1	0
BORDER_CB[7:0]							

BORDER_CB[7:0] CB component of the border color

BPIX **Subaddress = 82** **Default = 0x4A**

7	6	5	4	3	2	1	0
BPIX[7:0]							

BPIX[10:0] Begin of pixels. Defines the location in a line where the first pixel appears. Only applicable when the input pixels are in progressive mode. BAPIX[10:0] is ignored when the input pixels are in interlace mode.

MV_REG0~MV_REG31 **Subaddress = 90:A1** **Default = 0x00**

7	6	5	4	3	2	1	0

MV_REG[0:17] In TFP6422, registers to control the Macrovision™ 7.11 copy protection process.
In TFP6424, any access, read or write to these registers will shut down all four outputs of the DACs.

PLL_TST0 **Subaddress = B0**

7	6	5	4	3	2	1	0
PLL_FTR[7:0]							

PLL_FTR[7:0] PLL Filter control

PLL_TST1 **Subaddress = B1**

7	6	5	4	3	2	1	0

PLL_TST1 Subaddress = B2

PLL_TST3 Subaddress = B3

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FUS_TST0–3 **Subaddress = B4–B7**

7	6	5	4	3	2	1	0
FUSEA[7:0]							

7	6	5	4	3	2	1	0
FUSEA[15:8]							

7	6	5	4	3	2	1	0
FUSEB[7:0]							

7	6	5	4	3	2	1	0
FUSEB[15:8]							

TMDS_TST0 **Subaddress = C0**
TMDS_TST1 **Subaddress = C1**
TMDS_TST2 **Subaddress = C2**
TMDS_TST3 **Subaddress = C3**
TMDS_TST4 **Subaddress = C4**
TMDS_TST5 **Subaddress = C5**
TMDS_TST6 **Subaddress = C6**
TMDS_TST7 **Subaddress = C7**
TMDS_TST8 **Subaddress = C8**
TMDS_TST9 **Subaddress = C9**
TMDS_TST10 **Subaddress = CA**
TMDS_TST11 **Subaddress = CB**
TMDS_TST12 **Subaddress = CC**
TMDS_TST13 **Subaddress = CD**
TMDS_TST14 **Subaddress = CE**
TMDS_TST15 **Subaddress = CF**

DAC_TST **Subaddress = D0** **Default = 0x00**

7	6	5	4	3	2	1	0
			DAC_DX	DACX3	DACX2	DACX1	DACX0

DAC_DX Direct DAC output
- 0* DACs are in normal operation
- 1 Video port DATA[9:0] is directly connected to DACs for testing output. DACX[3:0] will select which DACs to output.

DACX3
- 0 DAC3 at pin 40 is shut down
- 1 DAC3 outputs DATA [9:0]

DACX2
- 0 DAC2 at pin 41 is shut down
- 1 DAC2 outputs DATA [9:0]

DACX1
- 0 DAC1 at pin 43 is shut down
- 1 DAC1 outputs DATA [9:0]

DACX0
- 0 DAC0 at pin 44 is shut down
- 1 DAC0 outputs DATA [9:0]

PRODUCT PREVIEW

PowerPAD™ 64TQFP package

The TFP6422/6424 is packaged in TIs thermally enhanced PowerPAD 64TQFP packaging. The PowerPAD™ package is a 10 mm x 10 mm x 1.4mm TQFP outline with 0.5mm lead-pitch. The PowerPAD™ package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 64TQFP PowerPAD™ package offers a backside solder plane that connects directly to the die mount pad for enhanced thermal conduction. The system designer has the option to solder this backside plane to a thermal/ ground plane on the PCB. Since the die pad is electrically connected to the TFP6422/6424 chip substrate and hence ground, the backside PowerPAD™ connection to a PCB ground plane can improve ground bounce and power supply noise.

The connection of the PowerPAD™ to a PCB thermal/ground plane is purely optional.

The following table outlines the thermal properties of the TI 64-TQFP PowerPAD™ package. The 64-TQFP non-PowerPAD™ package is included only for reference.

TI 64-TQFP (10 × 10 × 1.4 mm)/0.5 mm lead-pitch

PARAMETER	WITHOUT PowerPAD	POWERPAD NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD CONNECTED TO PCB THERMAL PLANE†
Theta–JA†‡	45°C/W	27.3°C/W	17.3°C/W
Theta–JC†‡	3.11°C/W	0.12°C/W	0.12°C/W
Maximum power dissipation†‡§	1.6 W	2.7 W	4.3 W
Maximum TFP6422 pixel rate	TBD	TBD	TBD

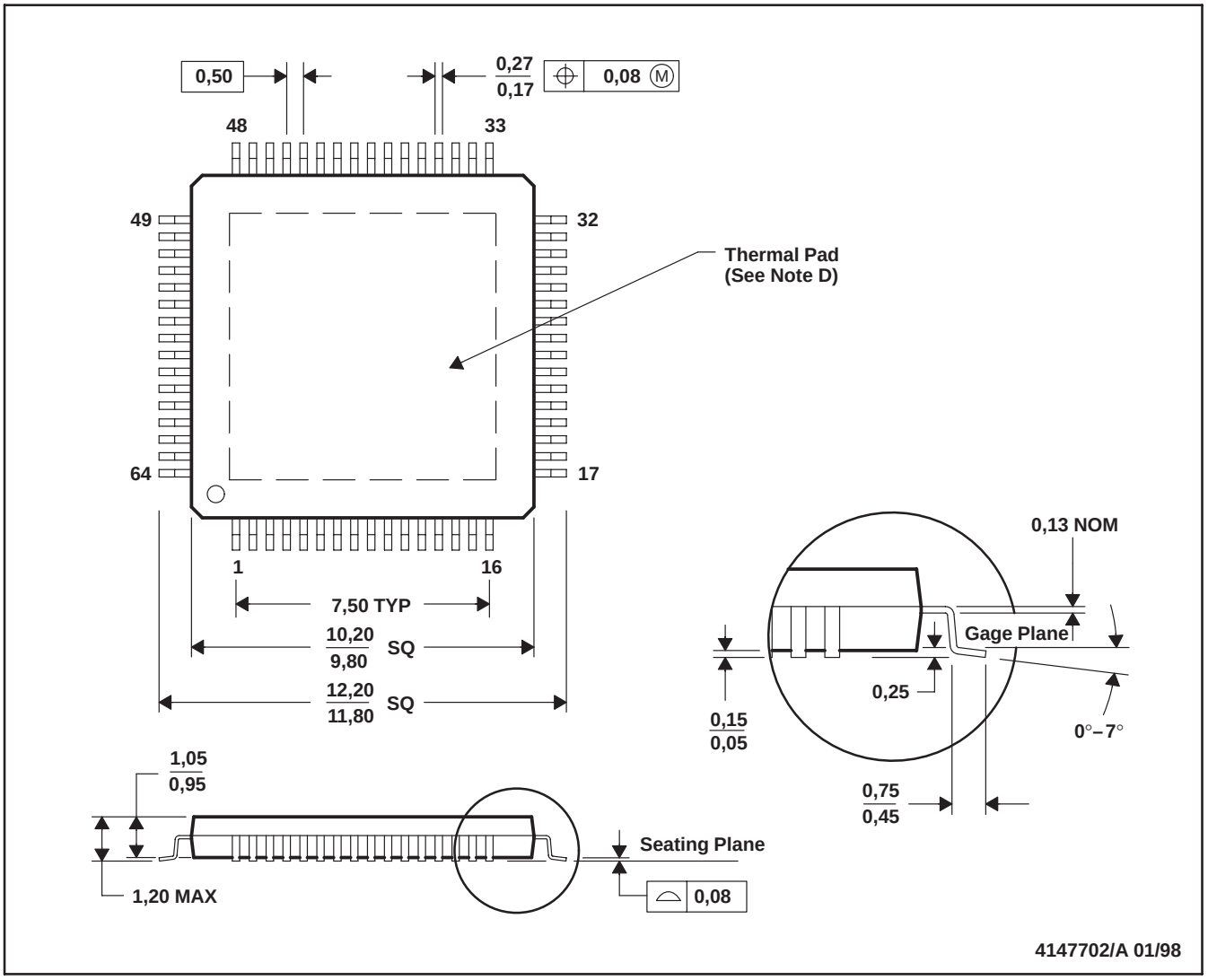
† Specified with 2 oz. Cu PCB plating.
‡ Airflow is at 0 LFM (no airflow)
§ Measured at ambient temperature, T_A = 70°C.

PRODUCT PREVIEW

PRODUCT PREVIEW

MECHANICAL DATA

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

APPENDIX A

T.M.D.S. encoding for control characteris and 8-bit pixel data

For each input code, 2 output codes are possible. The DVI transmitter keeps track of the number of ones and zeros sent and transmits the character that best approximates a dc balance.

2–BIT CONTROL TO T.M.D.S. CHARACTER ENCODING. (DE= Low)		
HSYNC CTL0 CTL2	VSYNC CTL1 CTL3	T.M.D.S. 10–bit character (LSB – MSB)
0	0	0010101011
1	0	1101010100
0	1	0010101010
1	1	1101010101

8–BIT PIXEL DATA TO T.M.D.S. CHARACTER ENCODING (DE = High)							
PIXEL		T.M.D.S. CHARACTER		PIXEL		T.M.D.S. CHARACTER	
Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb	Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb
0	00000000	0100000000	1111111111	128	10000000	0110000000	1101111111
1	00000001	0111111111	1100000000	129	10000001	0101111111	1110000000
2	00000010	0111111110	1100000001	130	10000010	0101111110	1110000001
3	00000011	0100000001	1111111110	131	10000011	0110000001	1101111110
4	00000100	0111111100	1100000011	132	10000100	0101111100	1110000011
5	00000101	0100000011	1111111100	133	10000101	0110000011	1101111100
6	00000110	0100000010	1111111101	134	10000110	0110000010	1101111101
7	00000111	0111111101	1100000010	135	10000111	0101111101	1110000010
8	00001000	0111111000	1100000111	136	10001000	0101111000	1110000111
9	00001001	0100000111	1111111000	137	10001001	0110000111	1101111000
10	00001010	0100000110	1111111001	138	10001010	0110000110	1101111001
11	00001011	0111111001	1100000110	139	10001011	0101111001	1110000110
12	00001100	0100000100	1111111011	140	10001100	0110000100	1101111011
13	00001101	0111111011	1100000100	141	10001101	0101111011	1110000100
14	00001110	0111111010	1100000101	142	10001110	0011010000	1000101111
15	00001111	0100000101	1111111010	143	10001111	0000101111	1011010000
16	00010000	0111110000	1100001111	144	10010000	0101110000	1110001111
17	00010001	0100001111	1111110000	145	10010001	0110001111	1101110000
18	00010010	0100001110	1111110001	146	10010010	0110001110	1101110001
19	00010011	0111110001	1100001110	147	10010011	0101110001	1110001110
20	00010100	0100001100	1111110011	148	10010100	0110001100	1101110011
21	00010101	0111110011	1100001100	149	10010101	0101110011	1110001100
22	00010110	0111110010	1100001101	150	10010110	0011011000	1000100111
23	00010111	0100001101	1111110010	151	10010111	0000100111	1011011000
24	00011000	0100001000	1111110111	152	10011000	0110001000	1101110111

8–BIT PIXEL DATA TO T.M.D.S. CHARACTER ENCODING (DE = High)							
PIXEL		T.M.D.S. CHARACTER		PIXEL		T.M.D.S. CHARACTER	
Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb	Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb
25	00011001	0111110111	1100001000	153	10011001	0101110111	1110001000
26	00011010	0111110110	1100001001	154	10011010	0011011100	1000100011
27	00011011	0100001001	1111110110	155	10011011	0000100011	1011011100
28	00011100	0111110100	1100001011	156	10011100	0011011110	1000100001
29	00011101	0100001011	1111110100	157	10011101	0000100001	1011011110
30	00011110	0010100000	1001011111	158	10011110	0000100000	1011011111
31	00011111	0001011111	1010100000	159	10011111	0011011111	1000100000
32	00100000	0111100000	1100011111	160	10100000	0101100000	1110011111
33	00100001	0100011111	1111100000	161	10100001	0110011111	1101100000
34	00100010	0100011110	1111100001	162	10100010	0110011110	1101100001
35	00100011	0111100001	1100011110	163	10100011	0101100001	1110011110
36	00100100	0100011100	1111100011	164	10100100	0110011100	1101100011
37	00100101	0111100011	1100011100	165	10100101	0101100011	1110011100
38	00100110	0111100010	1100011101	166	10100110	0011001000	1000110111
39	00100111	0100011101	1111100010	167	10100111	0000110111	1011001000
40	00101000	0100011000	1111100111	168	10101000	0110011000	1101100111
41	00101001	0111100111	1100011000	169	10101001	0101100111	1110011000
42	00101010	0111100110	1100011001	170	10101010	0011001100	1000110011
43	00101011	0100011001	1111100110	171	10101011	0000110011	1011001100
44	00101100	0111100100	1100011011	172	10101100	0011001110	1000110001
45	00101101	0100011011	1111100100	173	10101101	0000110001	1011001110
46	00101110	0010110000	1001001111	174	10101110	0000110000	1011001111
47	00101111	0001001111	1010110000	175	10101111	0011001111	1000110000
48	00110000	0100010000	1111101111	176	10110000	0110010000	1101101111
49	00110001	0111101111	1100010000	177	10110001	0101101111	1110010000
50	00110010	0111101110	1100010001	178	10110010	0011000100	1000111011
51	00110011	0100010001	1111101110	179	10110011	0000111011	1011000100
52	00110100	0111101100	1100010011	180	10110100	0011000110	1000111001
53	00110101	0100010011	1111101100	181	10110101	0000111001	1011000110
54	00110110	0010111000	1001000111	182	10110110	0000111000	1011000111
55	00110111	0001000111	1010111000	183	10110111	0011000111	1000111000
56	00111000	0111101000	1100010111	184	10111000	0011000010	1000111101
57	00111001	0100010111	1111101000	185	10111001	0000111101	1011000010
58	00111010	0010111100	1001000011	186	10111010	0000111100	1011000011
59	00111011	0001000011	1010111100	187	10111011	0011000011	1000111100
60	00111100	0010111110	1001000001	188	10111100	0000111110	1011000001
61	00111101	0001000001	1010111110	189	10111101	0011000001	1000111110
62	00111110	0001000000	1010111111	190	10111110	0011000000	1000111111
63	00111111	0010111111	1001000000	191	10111111	0000111111	1011000000

8–BIT PIXEL DATA TO T.M.D.S. CHARACTER ENCODING (DE = High)							
PIXEL		T.M.D.S. CHARACTER		PIXEL		T.M.D.S. CHARACTER	
Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb	Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb
64	01000000	0111000000	1100111111	192	11000000	0101000000	1110111111
65	01000001	0100111111	1111000000	193	11000001	0110111111	1101000000
66	01000010	0100111110	1111000001	194	11000010	0110111110	1101000001
67	01000011	0111000001	1100111110	195	11000011	0101000001	1110111110
68	01000100	0100111100	1111000011	196	11000100	0110111100	1101000011
69	01000101	0111000011	1100111100	197	11000101	0101000011	1110111100
70	01000110	0111000010	1100111101	198	11000110	0011101000	1000010111
71	01000111	0100111101	1111000010	199	11000111	0000010111	1011101000
72	01001000	0100111000	1111000111	200	11001000	0110111000	1101000111
73	01001001	0111000111	1100111000	201	11001001	0101000111	1110111000
74	01001010	0111000110	1100111001	202	11001010	0011101100	1000010011
75	01001011	0100111001	1111000110	203	11001011	0000010011	1011101100
76	01001100	0111000100	1100111011	204	11001100	0011101110	1000010001
77	01001101	0100111011	1111000100	205	11001101	0000010001	1011101110
78	01001110	0010010000	1001101111	206	11001110	0000010000	1011101111
79	01001111	0001101111	1010010000	207	11001111	0011101111	1000010000
80	01010000	0100110000	1111001111	208	11010000	0110110000	1101001111
81	01010001	0111001111	1100110000	209	11010001	0101001111	1110110000
82	01010010	0111001110	1100110001	210	11010010	0011100100	1000011011
83	01010011	0100110001	1111001110	211	11010011	0000011011	1011100100
84	01010100	0111001100	1100110011	212	11010100	0011100110	1000011001
85	01010101	0100110011	1111001100	213	11010101	0000011001	1011100110
86	01010110	0010011000	1001100111	214	11010110	0000011000	1011100111
87	01010111	0001100111	1010011000	215	11010111	0011100111	1000011000
88	01011000	0111001000	1100110111	216	11011000	0011100010	1000011101
89	01011001	0100110111	1111001000	217	11011001	0000011101	1011100010
90	01011010	0010011100	1001100011	218	11011010	0000011100	1011100011
91	01011011	0001100011	1010011100	219	11011011	0011100011	1000011100
92	01011100	0010011110	1001100001	220	11011100	0000011110	1011100001
93	01011101	0001100001	1010011110	221	11011101	0011100001	1000011110
94	01011110	0001100000	1010011111	222	11011110	0011100000	1000011111
95	01011111	0010011111	1001100000	223	11011111	0000011111	1011100000
96	01100000	0100100000	1111011111	224	11100000	0110100000	1101011111
97	01100001	0111011111	1100100000	225	11100001	0101011111	1110100000
98	01100010	0111011110	1100100001	226	11100010	0011110100	1000001011
99	01100011	0100100001	1111011110	227	11100011	0000001011	1011110100
100	01100100	0111011100	1100100011	228	11100100	0011110110	1000001001
101	01100101	0100100011	1111011100	229	11100101	0000001001	1011110110
102	01100110	0010001000	1001110111	230	11100110	0000001000	1011110111

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8–BIT PIXEL DATA TO T.M.D.S. CHARACTER ENCODING (DE = High)							
PIXEL		T.M.D.S. CHARACTER		PIXEL		T.M.D.S. CHARACTER	
Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb	Dec.	Binary msb–lsb	Char1 lsb – msb	Char2 lsb – msb
103	01100111	0001110111	1010001000	231	11100111	0011110111	1000001000
104	01101000	0111011000	1100100111	232	11101000	0011110010	1000001101
105	01101001	0100100111	1111011000	233	11101001	0000001101	1011110010
106	01101010	0010001100	1001110011	234	11101010	0000001100	1011110011
107	01101011	0001110011	1010001100	235	11101011	0011110011	1000001100
108	01101100	0010001110	1001110001	236	11101100	0000001110	1011110001
109	01101101	0001110001	1010001110	237	11101101	0011110001	1000001110
110	01101110	0001110000	1010001111	238	11101110	0011110000	1000001111
111	01101111	0010001111	1001110000	239	11101111	0000001111	1011110000
112	01110000	0111010000	1100101111	240	11110000	0011111010	1000000101
113	01110001	0100101111	1111010000	241	11110001	0000000101	1011111010
114	01110010	0010000100	1001111011	242	11110010	0000000100	1011111011
115	01110011	0001111011	1010000100	243	11110011	0011111011	1000000100
116	01110100	0010000110	1001111001	244	11110100	0000000110	1011111001
117	01110101	0001111001	1010000110	245	11110101	0011111001	1000000110
118	01110110	0001111000	1010000111	246	11110110	0011111000	1000000111
119	01110111	0010000111	1001111000	247	11110111	0000000111	1011111000
120	01111000	0010000010	1001111101	248	11111000	0000000010	1011111101
121	01111001	0001111101	1010000010	249	11111001	0011111101	1000000010
122	01111010	0001111100	1010000011	250	11111010	0011111100	1000000011
123	01111011	0010000011	1001111100	251	11111011	0000000011	1011111100
124	01111100	0001111110	1010000001	252	11111100	0011111110	1000000001
125	01111101	0010000001	1001111110	253	11111101	0000000001	1011111110
126	01111110	0010000000	1001111111	254	11111110	0000000000	1011111111
127	01111111	0001111111	1010000000	255	11111111	0011111111	1000000000

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