TSB12LV22 (OHCI-Lynx) Implementation Guide

APPLICATION BRIEF: SLLA025

Grant Ley
BuS Solutions Software Group

Mixed Signal and Logic Products
June 1998

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1998, Texas Instruments Incorporated

TRADEMARKS

CONTACT INFORMATION

US Product Information Center	(972) 644-5580
US Product Information Fax	(972) 480-7800
US Product Information Email	sc-infomaster@ti.com
US 1394 Web Site	http://www.ti.com/sc/1394

Contents

Figures

Tables

TSB12LV22 (OHCI-Lynx) Implementation Guide

Abstract

This implementation guide assists platform hardware developers designing with the TSB12LV22 1394 Open Host Controller Interface (OHCI) Link Layer Controller (LLC), referred to herein as the OHCI-Lynx.

The document includes an overview of the TSB12LV22 function and features, terminal assignments and pinout illustrations, TSB12LV22 I/O electrical characteristics, identification of required passive components and recommendations for system implementation, and phy/link signal isolation considerations.

Product Support

Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- *Galvanic Isolation of the IEEE 1394-1995 Serial Bus*, Literature number SLLA001

World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Introduction

This implementation guide assists platform hardware developers designing with the TSB12LV22 1394 Open Host Controller Interface (OHCI) Link Layer Controller (LLC), referred to herein as the OHCI-Lynx.

The document is divided into five sections:

- ☐ Overview of the TSB12LV22 function and features
- ☐ Terminal assignments and pinout illustrations
- ☐ I/O electrical characteristics of the TSB12LV22
- ☐ Identification of required passive components and recommendations for system implementation
- ☐ Considerations for phy/link signal isolation

TSB12LV22 (OHCI-Lynx) Function and Features

The Texas Instruments OHCI-Lynx is a PCI-to-1394 host controller compatible with the PCI, IEEE1394, and 1394 Open Host Controller Interface Specifications and Standards. The chip provides the IEEE1394 link function and is compatible with serial bus data rates of 100, 200, and 400 Mbits per second.

As required by the 1394 Open Host Controller Interface Specification, internal control registers are memory mapped and non-prefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI and provides Plug and Play compatibility. Furthermore, the OHCI-Lynx is compliant with the PCI Power Management Interface Specification, per PC 98 requirements.

The OHCI-Lynx provides PCI bus master bursting and is capable of transferring a cacheline of data at 132Mbytes/sec after connection to the memory controller. Because PCI latency can be rather large even on a PCI Revision 2.1 system, deep FIFOs are provided to buffer 1394 data.

Physical write posting buffers are provided to enhance serial bus performance. Multiple isochronous channels provide simultaneous operation of real-time applications. The OHCI-Lynx also provides integrated bus holder buffers on the phy/link interface signals for simple and cost-effective single capacitor isolation.

An advanced CMOS process is used to achieve low power consumption while operating at PCI clock rates up to 33MHz.

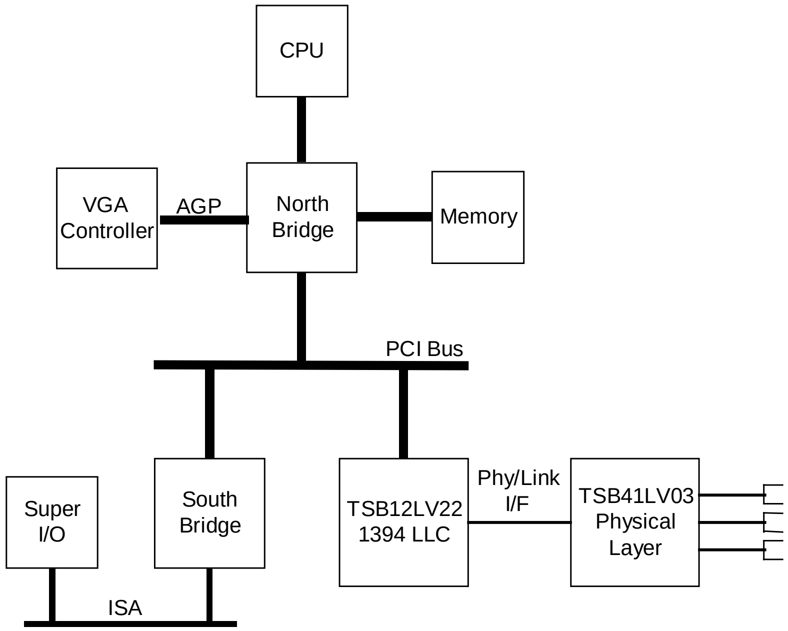
TSB12LV22 Feature Set

- ☐ IEEE1394 Open Host Controller Interface Specification 1.0 Compliant
- ☐ IEEE1394-1995 Compliant and Compatible with Proposal 1394A
- ☐ PCI Local Bus Specification Revision 2.1 Compliant and PCI 2.2 ready
- ☐ PCI Power Management Interface Specification 1.0 Compliant
- ☐ 3.3 Volt Core Logic with Universal PCI Interface
- ☐ Supports Serial Bus Data Rates of 100, 200, and 400Mbit/s
- ☐ Supports Physical Write posting of up to three outstanding transactions
- ☐ Serial ROM Interface supports 2-wire devices
- ☐ Supports External Cycle Timer Control for Customized Synchronization
- ☐ PCI Burst Transfers and Deep FIFOs to tolerate Large Host Latency
- ☐ Provides up to four general purpose I/Os
- ☐ Supports TI Patent-pending Single-Capacitor Bus Holder Isolation
- ☐ Fabricated in Advanced Low-Power CMOS Process
- ☐ Packaged in 100 LQFP

OHCI-Lynx System Implementation

Figure 1 illustrates a platform using the TSB12LV22, which, along with the TSB41LV03, provides the necessary interface to implement a three-port IEEE1394 node.

Figure 1. Typical System Architecture



Terminal Assignments

Figure 2 illustrates the TSB12LV22 pinout. Table 1 and Table 2 provide the signal names and pin numbers sorted numerically and alphabetically.

Figure 2. TSB21LV22 Pinout

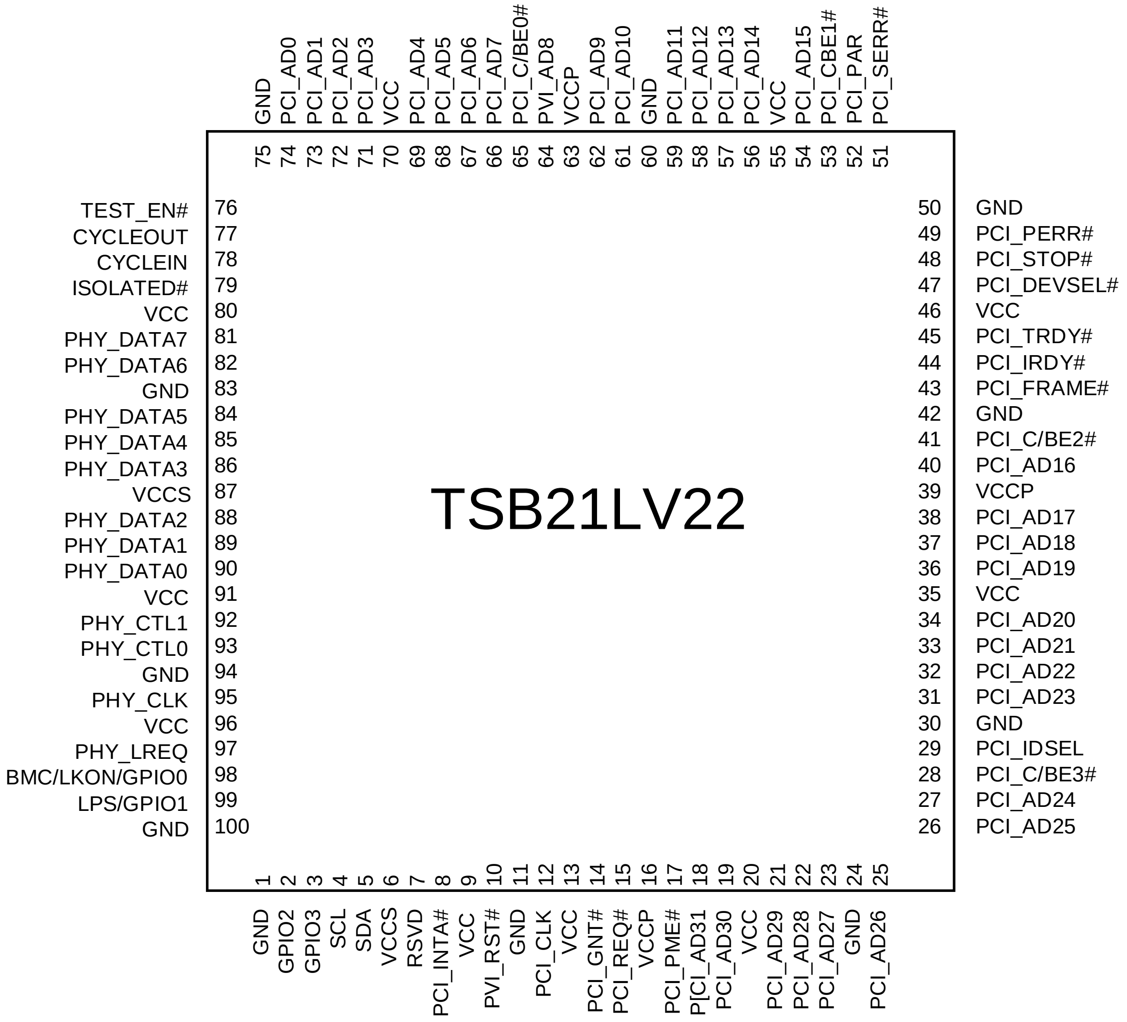


Table 1. Terminal Assignments Sorted Numerically

No.	**Terminal Name**	**No.**	**Terminal Name**	**No.**	**Terminal Name**	**No.**	**Terminal Name**
1	GND	26	PCI_AD25	51	PCI_SERR#	76	TEST_EN#
2	GPIO2	27	PCI_AD24	52	PCI_PAR	77	CYCLEOUT
3	GPIO3	28	PCI_CBE3#	53	PCI_CBE1#	78	CYCLEIN
4	SCL	29	PCI_IDSEL	54	PCI_AD15	79	ISOLATED#
5	SDA	30	GND	55	VCC	80	VCC
6	VCCS	31	PCI_AD23	56	PCI_AD14	81	PHY_DATA7
7	RSVD	32	PCI_AD22	57	PCI_AD13	82	PHY_DATA6
8	PCI_INTA#	33	PCI_AD21	58	PCI_AD12	83	GND
9	VCC	34	PCI_AD20	59	PCI_AD11	84	PHY_DATA5
10	PCI_RST#	35	VCC	60	GND	85	PHY_DATA4
11	GND	36	PCI_AD19	61	PCI_AD10	86	PHY_DATA3
12	PCI_CLK	37	PCI_AD18	62	PCI_AD9	87	VCCS
13	VCC	38	PCI_AD17	63	VCCP	88	PHY_DATA2
14	PCI_GNT#	39	VCCP	64	PCI_AD8	89	PHY_DATA1
15	PCI_REQ#	40	PCI_AD16	65	PCI_C/BE0#	90	PHY_DATA0
16	VCCP	41	PCI_CBE2#	66	PCI_AD7	91	VCC
17	PCI_PME#	42	GND	67	PCI_AD6	92	PHY_CTL1
18	PCI_AD31	43	PCI_FRAME#	68	PCI_AD5	93	PHY_CTL0
19	PCI_AD30	44	PCI_IRDY#	69	PCI_AD4	94	GND
20	VCC	45	PCI_TRDY#	70	VCC	95	PHY_CLK
21	PCIAD_29	46	VCC	71	PCI_AD3	96	VCC
22	PCIAD_28	47	PCI_DEVSEL#	72	PCI_AD2	97	PHY_LREQ
23	PCIAD_27	48	PCI_STOP#	73	PCI_AD1	98	BMC/LKON/GPIO0
24	GND	49	PCI_PERR#	74	PCI_AD0	99	LPS/GPIO1
25	PCIAD_26	50	GND	75	GND	100	GND

Table 2. Terminal Assignments Sorted Alphabetically

Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.
BMC/LKON/GPIO0	98	PCI_AD07	66	PCI_C/BE0#	65	PHY_DATA3	86
CYCLEIN	78	PCI_AD08	64	PCI_CBE1#	53	PHY_DATA4	85
CYCLEOUT	77	PCI_AD09	62	PCI_CBE2#	41	PHY_DATA5	84
GND	1	PCI_AD10	61	PCI_CBE3#	28	PHY_DATA6	82
GND	11	PCI_AD11	59	PCI_CLK	12	PHY_DATA7	81
GND	24	PCI_AD12	58	PCI_DEVSEL#	47	PHY_LREQ	97
GND	30	PCI_AD13	57	PCI_FRAME#	43	RSVD	7
GND	42	PCI_AD14	56	PCI_GNT#	14	SCL	4
GND	50	PCI_AD15	54	PCI_IDSEL	29	SDA	5
GND	60	PCI_AD16	40	PCI_INTA#	8	TEST_EN#	76
GND	75	PCI_AD17	38	PCI_IRDY#	44	VCC	9
GND	83	PCI_AD18	37	PCI_PAR	52	VCC	13
GND	94	PCI_AD19	36	PCI_PERR#	49	VCC	20
GND	100	PCI_AD20	34	PCI_PME#	17	VCC	35
GPIO2	2	PCI_AD21	33	PCI_REQ#	15	VCC	46
GPIO3	3	PCI_AD22	32	PCI_RST#	10	VCC	55
ISOLATED#	79	PCI_AD23	31	PCI_SERR#	51	VCC	70
LPS/GPIO1	99	PCI_AD24	27	PCI_STOP#	48	VCC	80
PCI_AD00	74	PCI_AD25	26	PCI_TRDY#	45	VCC	91
PCI_AD01	73	PCI_AD26	25	PHY_CLK	95	VCC	96
PCI_AD02	72	PCI_AD27	23	PHY_CTL0	90	VCCP	16
PCI_AD03	71	PCI_AD28	22	PHY_CTL1	89	VCCP	39
PCI_AD04	69	PCI_AD29	21	PHY_DATA0	88	VCCP	63
PCI_AD05	68	PCI_AD30	19	PHY_DATA1	93	VCCS	6
PCI_AD06	67	PCI_AD31	18	PHY_DATA2	92	VCCS	87

I/O Electrical Characteristics

Table 3 provides the recommended operating conditions for the inputs and outputs of the TSB12LV22. Figure 3 shows a 3-state bi-directional buffer for reference. Electrical characteristics for the inputs and outputs are shown in Table 4. Note that the PCI interface signals meet the AC requirements of the PCI release 2.1 specification.

Figure 3. 3-State Bi-Directional Buffer

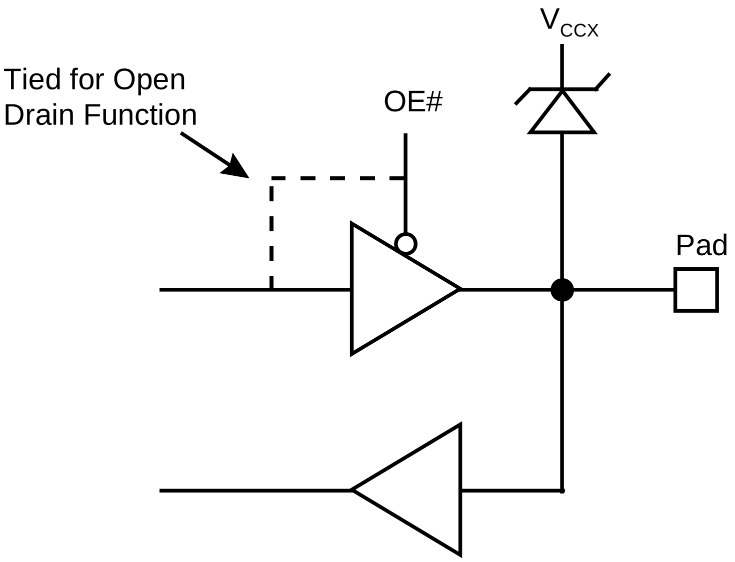


Table 3 Recommended Operating Conditions

		Operation	**Min**	**Nom**	**Max**	**Unit**
V_{CC}	Core voltage	Commercial	3	3.3	3.6	V
V_{CCP}	PCI I/O clamping voltage	Commercial	3		5.5	V
V_{CCS}	Other I/O clamping rail	Commercial	3	5	5.5	V
V_{IH}†	High-level input voltage	PCI	0.475 V_{CCP}		V_{CCP}	V
	PHY I/F		2		V_{CCS}	
	Miscellaneous‡		2		V_{CCS}	
V_{il}†	Low-level input voltage	PCI	0		0.325 V_{CC}	V
	PHY I/F		0		0.8	
	Miscellaneous‡		0		0.8	
V_I	Input voltage	PCI	0		V_{CCP}	V
	PHY I/F		0		V_{CCS}	
	Miscellaneous‡		0		V_{CCS}	
V_O¶	Output voltage	PCI	0		V_{CCP}	V
	PHY I/F		0		V_{CCS}	
	Miscellaneous‡		0		V_{CCS}	
t_t	Input transition time (t_r and t_f)	PCI	0		6	ns
T_A	Operating ambient temperature		0	25	70	°C
T_J#	Virtual junction temperature		0	25	115	°C

† Applies to external inputs and bi-directional buffers without hysteresis.

‡ Miscellaneous pins are: GPIO(0:3), SDA, SCL, CYCLEOUT.

¶ Applies to external output buffers.

The junction temperatures reflect simulation conditions. Customer is responsible for verifying junction temperature.

Table 4. Electrical Characteristics for Recommended Operating Conditions

			Operation	**Test Conditions**	**Min**	**Max**	**Unit**
V_{OH}	High-level output voltage	PCI		I_{OH} = - 0.5 mA I_{OM} = - 2 mA	0.9 V_{CC} 2.4		V
		PHY I/F		I_{OH} = - 4 mA I_{OH} = - 8 mA	2.8 V_{CC} - 0.6		
		Miscellaneous[‡]		I_{OH} = - 4 mA	V_{CC} - 0.6		
V_{ol}[†]	Low-level output voltage	PCI		I_{OL} = 1.5 mA I_{OL} = 6 mA		0.1 V_{CC} 0.55	V
		PHY I/F		I_{OL} = 4 mA I_{OL} = 8 mA		0.4 0.5	
		Miscellaneous[‡]		I_{OL} = 4 mA		0.5	
I_{OZ}	3-state output high-impedance	Output pins	3.6V	V_O = V_{CC} or GND		± 20	µA
I_{IL}	Low-level input current	Input pins	3.6V	V_I = GND[‡]		± 20	µA
		I/O pins[†]	3.6V	V_I = GND[‡]		± 20	
I_{IH}	High-level input current	PCI [†]	3.6V	V_I = V_{CC}[‡]		± 20	µA
		OTHERS [†]	3.6V	V_I = V_{CC}[‡]		± 20	

[†] For I/O pins, input leakage (I_{IL} and I_{IH}) includes I_{OZ} of the disabled output.

[‡] Miscellaneous pins are: GPIO(0:3), SDA, SCL, CYCLEOUT.

Passive Component Requirements

Required Pull-Up/Pull-Down Resistors

Several signals on the TSB12LV22 require a pull-up or pull-down resistor. Table 5 provides a list of required resistors.

Table 5. Required Pull-Up/Pull-Down Resistors

Signal	**Resistor**	**Recommended Value (Ω)**	**Condition**
SDA	Pull-up	2.7K	Required if implementation includes a serial EEPROM.
SCL	Pull-up	2.7K	Required if implementation includes a serial EEPROM.
ISOLATED#	Pull-up (Default)	4.7K	Required if not implementing bus holder isolation.
	Pull-down	220	Required if implementing bus holder isolation.
CYCLEIN	Pull-down	220	Required if not implementing optional external 8 kHz clock.
BMC/LKON/GPIO0	Pull-up	4.7K	Required if configured as a general-purpose input.
LPS/GPI01	Pull-down (Default)	1.0K	Required on the phy side of isolation barrier, if implemented, when configured as LPS to disable PHYCLK from the phy when the link is not powered.
	Pull-up	4.7K	Required if configured as a general-purpose input. (Default)
GPI02	Pull-up	4.7K	Required if configured as a general-purpose input. (Default)
GPI03	Pull-up	4.7K	Required if configured as a general-purpose input.
TEST_EN#	Pull-up	4.7K	Required.

NOTE:

All pull-up/pull-down resistor value recommendations are provided as guidelines only. The best value for an individual design may vary depending upon board characteristics, standard design rules and practices, etc.

PCI Bus Requirements

The following paragraph summarizes paragraph 4.3.3 of the PCI Local Bus Specification Revision 2.1 and is provided for reference only. Please refer to the PCI Local Bus Specification for a full discussion on pull-up resistors required for PCI local bus implementations.

All PCI control signals require pull-up resistors on the motherboard to guarantee that they are at a stable state when no agent is actively driving the signal. Pull-ups should be implemented on the motherboard only. Expansion boards or add-in cards should not provide pull-up resistors for the PCI control signals. The following PCI signals require pull-up resistors:

- FRAME#
- TRDY#
- IRDY#
- DEVSEL#
- STOP#
- SERR#
- PERR#
- LOCK#
- INTA#
- INTB#
- INTC#
- INTD#
- REQ64# (when used)
- ACK64# (when used)

Pull-ups are not required on point-to-point or shared 32-bit signals, as bus parking guarantees their stability. If the 64-bit data path expansion signals, AD(63:32), C/BE(7:4)#, and PAR64, are connected they must be pulled-up as well. Table 7 lists the 32-bit PCI signals implemented on the TSB12LV22 that require pull-up resistors on the system board.

Minimum and maximum values for required PCI pull-up resistors can be calculated using the following formulas:

$$R\,\mathrm{min} = \left[V_{CC(\max)} - V_{ol}\right] \Big/ \left[I_{ol} + \left(16 \cdot I_{il}\right)\right]$$

where 16 = maximum number of loads

$$R\text{max} = \left[V_{CC(\min)} - V_X\right] / \left[num\_loads \times I_{ih}\right]$$

where

V_X= 2.7V for 5V signaling

V_X= 0.7 V_{CC} for 3.3V signaling

Minimum and typical values for both 5V and 3.3V signaling environments are shown in Table 6.

Table 6. Minimum and Typical PCI Pull-Up Resistor Values

Signaling Rail	**R_{min}**	**R_{typ}**	**R_{max}**
5V	963 Ω	2.7 kΩ ± 10%	Dependent on number of loads (see formula)
3.3V	2.42 kΩ	8.2 kΩ ± 10%	Dependent on number of loads (see formula)

Table 7. 32-Bit PCI Signal System Board Pull-Up Requirements

PCI Signal	**Pull-Up Voltage**
FRAME#	V_{CCP}
TRDY#	V_{CCP}
IRDY#	V_{CCP}
DEVSEL #	V_{CCP}
STOP#	V_{CCP}
SERR#	V_{CCP}
PERR#	V_{CCP}
INTA#	V_{CCP}

Bypass Capacitors

Standard design rules for the supply bypass should be followed. Low inductance ceramic chip capacitors are best for bypass capacitors. A value of 0.1 µF is recommended for each of the power supply pins: V_{CC}, V_{CCS}, V_{CCP}.

Isolation Considerations

The TSB12LV22 provides the necessary support to implement Texas Instruments’ patent-pending bus holder isolation. If implementing isolation, a single 0.001 µF isolation capacitor should be provided for each interface signal between the physical and link layers. The phy/link interface signals include PHY_DATA(0:7), PHY_CTL(0:1), PHY_LREQ, PHY_CLK, LPS (if implemented), and BMC (if implemented).

Isolated ground planes should be capacitively coupled to provide a signal return path for currents. A parallel combination of a 1 MΩ resistor, a 0.1 µF capacitor, and another 0.1 µF to 10 µF capacitor aids in error-free operation.

Figure 4 shows an example of an isolated host implementation. For more information on galvanic isolation please refer to *Galvanic Isolation of the IEEE 1394-1995 Serial Bus*, literature number SLLA001.

Figure 4. Example of Host Isolation