PRODUCT INFORMATION

FEATURES

- Complete single-chip channelized DS3 solution
- RISC processor with royalty-free DD-AMPS™ firmware (Drivers, Data link, Alarms, Messaging, Performance/configuration objects, and Signaling)
- Host communication via royalty-free, message-based, POSIX-compatible API
- Integrated 672 x 4,096-channel DS0 cross connect supports grooming, broadcast, off-bus hairpinning, and bonding
- Integrated DS1/E1 cross connect
- Integrated G.747 function to Mux/De-Mux 21 E1s to/from DS3.
- 28 DS1 or 21 E1 line interfaces or 1 DS3 line interface
- Combination of unframed DS1/E1, transmission DS1/E1, link channel interface (LCI), and either MVIP or H.100/H.110 as terminal side interfaces
- Selectable DS3 clear channel functionality
- On-chip maintenance of 15-minute performance objects per IETF RFCs 2495, 2496, and 2494.
- Support 2 SS7 and 28 ISDN-PRI signaling channels
- Two DS1/E1 monitor ports for monitoring any DS1/E1 clock and data
- Test Access Port (IEEE 1149.1 boundary scan)
- +3.3 volt input/output leads, +5 volt tolerant
- +3.3 volt and +1.8 volt power supplies
- 456-lead plastic ball grid array package (27 mm x 27 mm); pin- and API-compatible with T3BwP (TXC-06826)
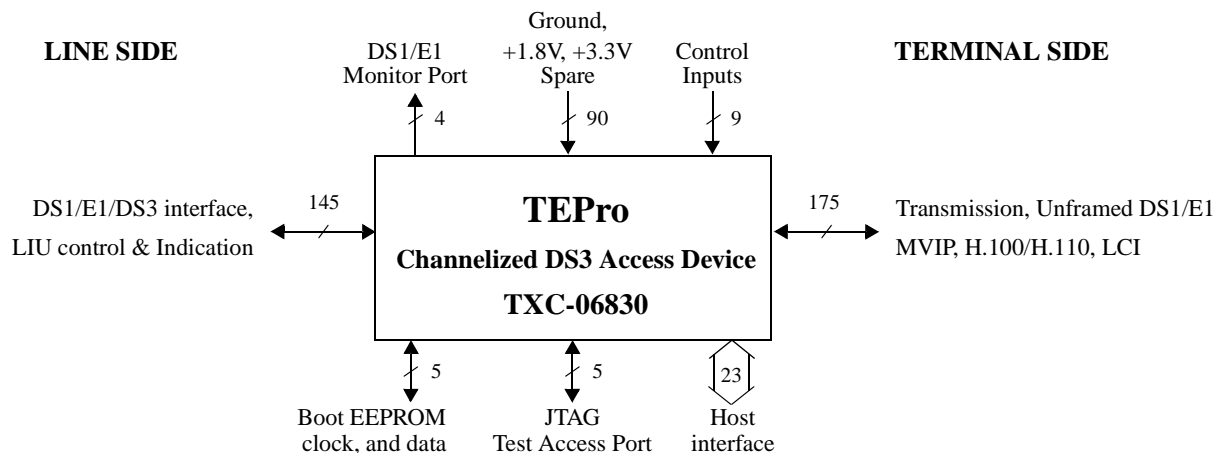
DESCRIPTION

TEPro™ (TXC-06830) is a RISC processor-based device that supports the requirements of next-generation channelized DS3 access systems. TEPro integrates an M13 multiplexer, G.747 Mux/De-Mux framer, 28 DS1 / 21 E1 framers, T1/E1 cross connect and a 672 x 4,096-channel DS0 cross connect with an embedded high-performance microprocessor to provide a complete channelized DS3 solution on a single chip. The embedded processor firmware handles device drivers, data links, alarms, messaging, MIB performance objects, and signaling functions and allows communication to an external host via high-level API messages. The firmware is provided by TranSwitch and loaded from an external serial EEPROM at device boot-up.

The TEPro can be configured to support a variety of modes of operation, which allows for design flexibility. TEPro supports a combination of unframed DS1/E1, transmission DS1/E1 and H.100/H.110 bus or MVIP interfaces on the terminal side and either DS3 or DS1/E1 on the line side. For TDM applications, all 672 DS0 channels can be switched to any of the 4,096 H.100/H.110 bus channels. The TEPro can also be enabled to provide DS3 C-bit parity for unchannelized services. The on-chip firmware provides the control and management plane functionality to the host to configure, control and monitor all DS3, DS1, E1, DS0 and digital cross connect functions. The standards-based MIB functionality is provided for network management.
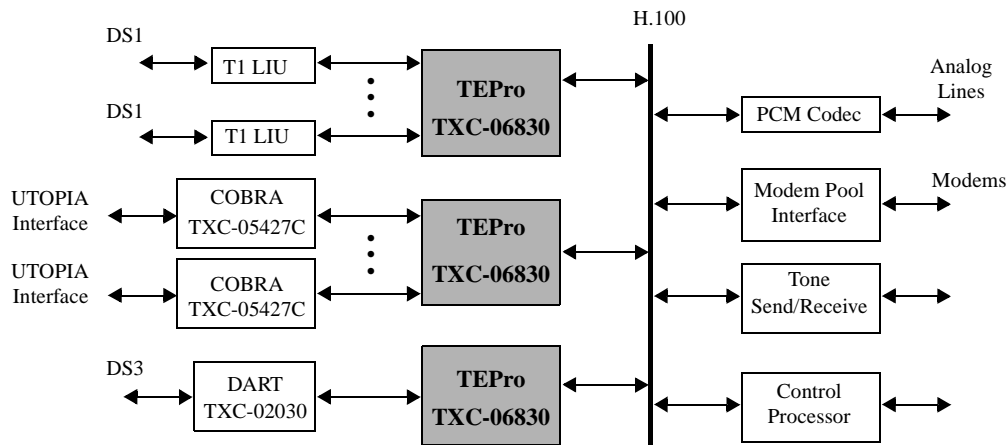
APPLICATIONS

- T-carrier termination equipment: muxes, inverse muxes, cross connects, groomers
- CT (Computer Telephony) network interface boards
- VoP (Voice over Packet/Cell) gateways
- MSADs (Multi-Service Access Devices)
- DSLAMs (Digital Subscriber Loop Access Multiplexers)
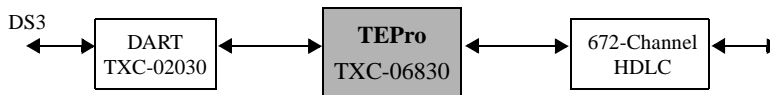- ECUs (Echo Cancellation Units)

Proprietary TranSwitch Corporation Information for use Solely by its Customers

LINE SIDE

Ground, +1.8V, +3.3V Spare

DS1/E1 Monitor Port / 4

Control Inputs / 9

/ 90

TERMINAL SIDE

DS1/E1/DS3 interface, LIU control & Indication / 145

TEPro
Channelized DS3 Access Device
TXC-06830

175 / Transmission, Unframed DS1/E1 MVIP, H.100/H.110, LCI

Boot EEPROM clock, and data / 5

JTAG Test Access Port / 5

Host interface / 23

Proprietary TranSwitch Corporation Information for use Solely by its Customers

☐ APPLICATION DIAGRAMS

Telephony Application

DS3 Remote Access Concentrator Application

☐ RELATED PRODUCTS

- TXC-02030   Advanced E3/DS3 Receiver/Transmitter VLSI Device (DART)
- TXC-03103   Quad T1 Framer-*Plus* VLSI Device (QT1F-*Plus*)
- TXC-03305   DS3/DS1 Mux/Demux VLSI Device (M13X)
- TXC-03452B   Level 3 Mapper VLSI Device (L3M)
- TXC-03453   Triple Level 3 Mapper VLSI Device (TL3M)
- TXC-04222   21/28 Channel Dual Bus High Density mapper VLSI Device (TEMx28)
- TXC-05150   Cell Delineation Block VLSI Device (CDB)
- TXC-05427C   COnstant Bit Rate ATM Adaptation Layer 1 VLSI Device (COBRA)
- TXC-06101   SONET STS-1 Overhead Terminator (PHAST-1)
- TXC-06103   STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator with Telecom Bus
                     Interface VLSI Device (PHAST-3N)

☐ FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products, including details of available operational firmware.