INDIVIDUAL PROGRAMMABLE OVERVOLTAGE PROTECTION FOR TWO SLICS

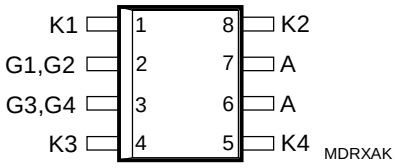
- **Independent Overvoltage Protection for Two SLICs in Short Loop Applications:**
  - **Wide 0 to -90 V Programming Range**
  - **Low 5 mA max. Gate Triggering Current**
  - **High 150 mA min. (85 °C) Holding Current**
  - **Specified 1.2/50 & 0.5/700 Limiting Voltage**
  - **Full -40 °C to 85 °C Temperature Range**
- **Rated for Common Impulse Waveforms**

VOLTAGE IMPULSE FORM	CURRENT IMPULSE SHAPE	I_{TSP} A
10/1000 µs	10/1000 µs	20
10/700 µs	5/310 µs	25
1.2/50 µs	8/20 µs	60
2/10 µs	2/10 µs	85

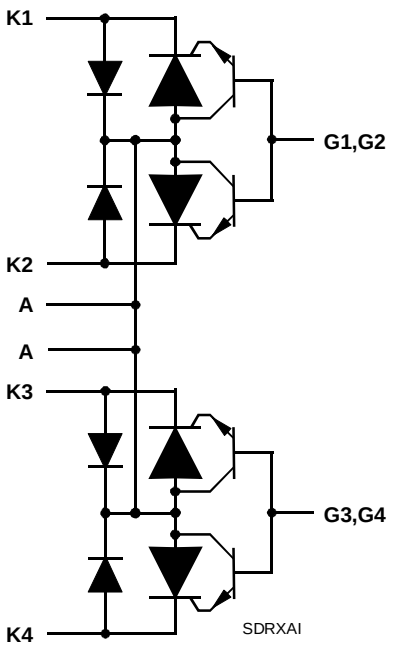
- **Small Outline Surface Mount Package**
  - **Available Ordering Options**

CARRIER	ORDER #
Tube	TISP6NTP2AD
Taped and reeled	TISP6NTP2ADR

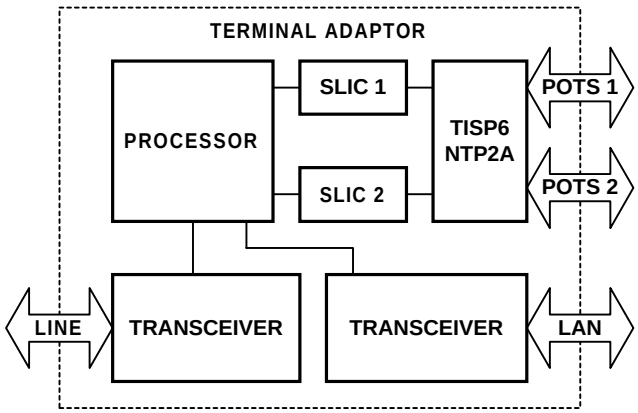
D PACKAGE
(TOP VIEW)



device symbol



typical TISP6NTP2A router application



description

The TISPNTP2A has been designed for short loop systems such as:
- WILL (Wireless In the Local Loop)
- FITL (Fibre In The Loop)
- DAML (Digital Added Main Line, Pair Gain)
- SOHO (Small Office Home Office)
- ISDN-TA (Integrated Services Digital Network - Terminal Adaptors)

These systems often have the need to source two POTS (Plain Old Telephone Service) lines, one for a telephone and the other for a facsimile machine. In a single surface mount package, the TISPNTP2A protects the two POTS line SLICs (Subscriber Line Interface Circuits) against overvoltages caused by lightning, a.c. power contact and induction.

The TISP6NTP2A has an array of four buffered P-gate forward conducting thyristors with twin commoned gates and a common anode connection. Each thyristor cathode has a separate terminal connection. An antiparallel anode-cathode diode is connected across each thyristor. The buffer transistors reduce the gate supply current.

TEXAS INSTRUMENTS

Designed and manufactured by Power Innovations, Bedford, UK. under private label for Texas Instruments.

In use, the cathodes of an TISP6NTP2A thyristors are connected to the four conductors of two POTS lines (see applications information). Each gate is connected to the appropriate negative voltage battery feed of the SLIC driving that line pair. By having separate gates, each SLIC can be protected at a voltage level related to the negative supply voltage of that individual SLIC. The anode of the TISP6NTP2A is connected to the SLIC common.

Positive overvoltages are clipped to common by forward conduction of the TISP6NTP2A antiparallel diode. Negative overvoltages are initially clipped close to the SLIC negative supply by emitter follower action of the TISP6NTP2A buffer transistor. If sufficient clipping current flows the TISP6NTP2A thyristor will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of the TISP6NTP2A prevents d.c. latchup.

absolute maximum ratings

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, I_G = 0, -40 °C ≤ T_J ≤ 85 °C	V_{DRM}	-100	V
Repetitive peak gate-cathode voltage, V_{KA} = 0, -40 °C ≤ T_J ≤ 85 °C	V_{GKRM}	-90	V
Non-repetitive peak on-state pulse current, -40 °C ≤ T_J ≤ 85 °C, (see Notes 1 and 2)			
10/1000 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)	I_{TSP}	20	A
0.2/310 µs (I3124, open-circuit voltage wave shape 0.5/700 µs)		25	
5/310 µs (ITU-T K20 & K21, open-circuit voltage wave shape 10/700 µs)		25	
8/20 µs (IEC 61000-4-5:1995, open-circuit voltage wave shape 1.2/50 µs)		60	
2/10 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)		85	
Non-repetitive peak on-state current, 50/60 Hz, -40 °C ≤ T_J ≤ 85 °C, (see Notes 1 and 2)			
100 ms	I_{TSM}	7	A
1 s		2.7	
5 s		1.5	
300 s		0.45	
900 s		0.43	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Note 1)	I_{GSM}	25	A
Operating free-air temperature range	T_A	-40 to +85	°C
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.
2. These non-repetitive rated currents are peak values for either polarirty. The rated current values may be applied to any cathode-anode terminal pair. Additionally, all cathode-anode terminal pairs may have their rated current values applied simultaneously (in this case the anode terminal current will be four times the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.

recommended operating conditions

		MIN	TYP	MAX	UNIT
C_G	Gate decoupling capacitor	100	220		nF
R1, R2	Series resistor for GR-1089-CORE first-level surge survival	40			Ω
	Series resistor for ITU-T recommendation K20	12			
	Series resistor for ITU-T recommendation K21	20			
	Series resistor for IEC 61000-4-5:1995, class 5, 1.2/50 or 10/700	4			

electrical characteristics for any section, T_{amb} = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	$V_D = V_{DRM}$, $I_G = 0$	T_J = 25 °C			-5	µA
			T_J = 85 °C			-50	µA
$V_{(BO)}$	Breakover voltage	I_T = -20 A, IEC 61000-4-5:1995 combination impulse generator, V_{GG} = -50 V				-70	V
		I_T = -18 A, I3124 impulse generator, V_{GG} = -50 V				-70	
$t_{(BR)}$	Breakdown time	I_T = -18 A, I3124 impulse generator, $V_{(BR)}$ < -50 V				2	µs
V_F	Forward voltage	I_F = 0.6 A, t_w = 500 µs, V_{GG} = -50 V				3	V
		I_F = 18 A, t_w = 500 µs, V_{GG} = -50 V				5	
V_{FRM}	Peak forward recovery voltage	I_F = 20 A, IEC 61000-4-5:1995 combination impulse generator, V_{GG} = -50 V				15	V
		I_F = 18 A, I3124 impulse generator, V_{GG} = -50 V				15	
t_{FR}	Forward recovery time	I_F = 18 A, I3124 impulse generator, V_{GG} = -50 V	V_F > 10 V			2	µs
			V_F > 5 V			4	
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -50 V, T_J = 85 °C		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GKRM}$, $V_{AK} = 0$	T_J = 25 °C			-5	µA
			T_J = 85 °C			-50	µA
I_{GAT}	Gate reverse current, on state	I_T = -0.6 A, t_w = 500 µs, V_{GG} = -50 V				-1	mA
I_{GAF}	Gate reverse current, forward conducting state	I_F = 0.6 A, t_w = 500 µs, V_{GG} = -50 V				-40	mA
I_{GT}	Gate trigger current	I_T = -5 A, $t_{p(g)} \geq$ 20 µs, V_{GG} = -50 V				5	mA
V_{GT}	Gate trigger voltage	I_T = -5 A, $t_{p(g)} \geq$ 20 µs, V_{GG} = -50 V				2.5	V
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 3)	V_D = -3 V			100	pF
			V_D = -50 V			60	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.52 W, T_A = 85°C, 5 cm^2, FR4 PCB			160	°C/W

PARAMETER MEASUREMENT INFORMATION

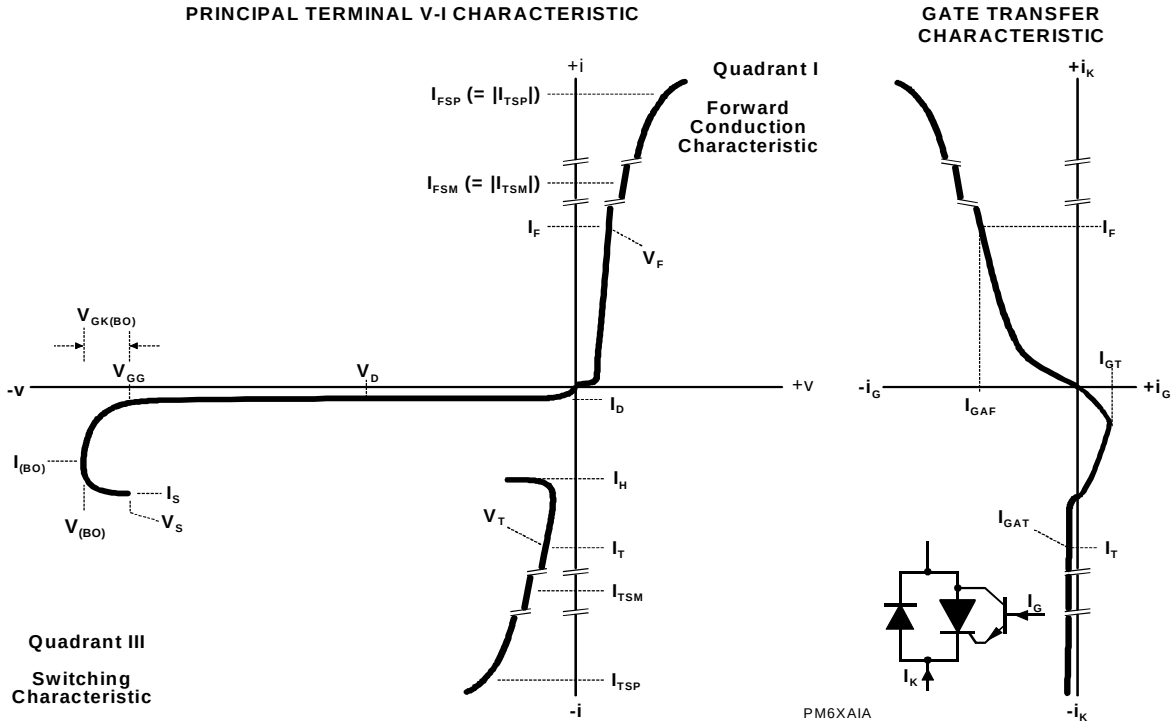


Figure 1. PRINCIPAL TERMINAL AND GATE TRANSFER CHARACTERISTICS

APPLICATIONS INFORMATION

operation of gated protectors

2 and 3 show how the TISP6NTP2A limits overvoltages. The TISP6NTP2A thyristor sections limit negative overvoltages and the diode sections limit positive overvoltages.

Negative overvoltages (2) are initially clipped close to the SLIC negative supply rail value (V_{BAT}) by the conduction of the transistor base-emitter and the thyristor gate-cathode junctions. If sufficient current is available from the overvoltage, then the thyristor will crowbar into a low voltage ground referenced on-state condition. As the overvoltage subsides the high holding current of the crowbar thyristor prevents d.c. latchup. The common gate of each thyristor pair is connected the appropriate SLIC battery feed voltage (V_{BAT1} or V_{BAT2}).

The negative protection voltage, $V_{(BO)}$, will be the sum of the gate supply (V_{BAT}) and the peak gate(terminal)-cathode voltage (V_{GT}). Under a.c. overvoltage conditions V_{GT} will be less than 2.5 V. The integrated transistor buffer in the TISP6NTP2A greatly reduces protectors source and sink current loading on the V_{BAT} supply. Without the transistor, the thyristor gate current would charge the V_{BAT} supply. An electronic power supply is not usually designed to be charged like a battery. As a result, the electronic supply would switch off and the thyristor gate current would provide the SLIC supply current. Normally the SLIC current would be less than

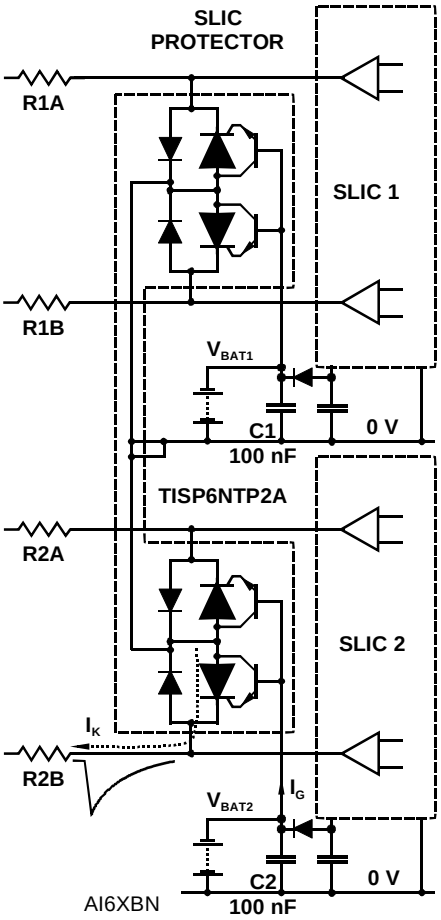


Figure 2. NEGATIVE OVERVOLTAGE CONDITION

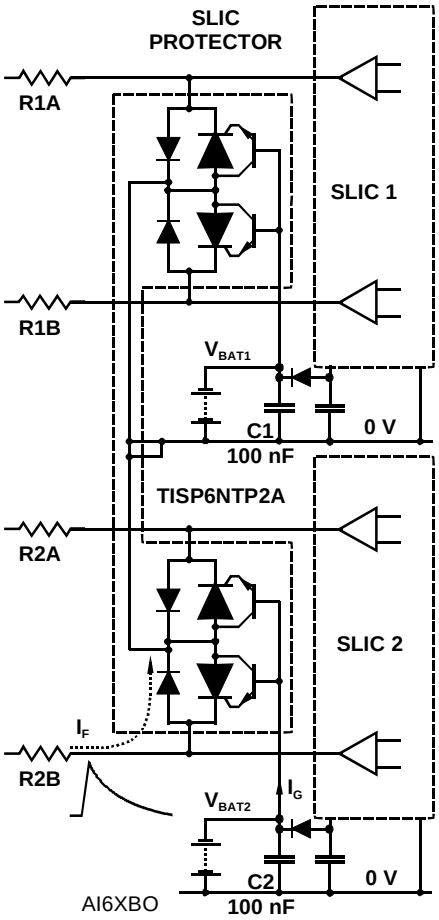


Figure 3. POSITIVE OVERVOLTAGE CONDITION

the gate current, which would cause the supply voltage to increase and destroy the SLIC by a supply overvoltage. The integrated transistor buffer removes this problem.

Fast rising impulses will cause short term overshoots in gate-cathode voltage. The negative protection voltage under impulse conditions will also be increased if there is a long connection between the gate decoupling capacitor and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 60 A/µs can cause inductive voltages of 0.6 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised.

Positive overvoltages (3) are clipped to ground by forward conduction of the diode section in the TISP6NTP2A. Fast rising impulses will cause short term overshoots in forward voltage (V_{FRM}).

central office application to Bellcore GR-1089-CORE issue 1

The most stressful impulse for first-level surge testing (section 4.5.7) is the 1000 V, 10/1000 impulse. To limit the circuit current to the TISP6NTP2A rating of 20 A requires the total circuit resistance to be 1000/20 = 50 Ω. Subtracting the generator fictive source impedance of 10 Ω gives 40 Ω as the required series resistor value for the TISP6NTP2A (R1A, R1B, R2A and R2B). The various first level impulse current levels are shown in table 1. The maximum 1.2/50 and 2/10 current levels of 56 A are below the TISP6NTP2A ratings of 60 A and 85 A. In table 1 the designation 2x20 means that each conductor has a simultaneous peak current of 20 A and 2x20 = 40 A flows in the anode (ground) connection.

table 1. first-level surge currents

WAVE SHAPE	OPEN-CIRCUIT VOLTAGE V	SHORT-CIRCUIT CURRENT A	GENERATOR RESISTANCE Ω	WIRES TESTED	TOTAL SERIES RESISTANCE Ω	I_T A
2/10	2500	500	5	BOTH	22.5	2x56
1.2/50 8/20	2500	500	2 + 3/wire	SINGLE	45	56
				BOTH	28.5	2x53
10/1000	1000	100	10	SINGLE	50	20
				BOTH	25	2x20

central office application to ITU-T recommendation K.20

The test level of 1000 V 10/700 delivers a peak short-circuit current level of 25 A, which is equal to the TISPNTP2A rated value. A series resistor (R1A, R1B, R2A and R2B) is required to ensure coordinated operation with the primary protector at the 4000 V test level. The resistor value will be set by the sparkover voltage of the primary protector. A sparkover voltage of 300 V will give a 300/25 = 12 Ω series resistor.

local subscribers line equipment to ITU-T recommendation K.21

The test level of 1500 V 10/700 delivers a peak short-circuit current level of 37.5 A. To limit the circuit current to the TISP6NTP2A rating of 25 A requires the total circuit resistance to be 1500/25 = 60 Ω. Subtracting the generator fictive source impedance of 40 Ω gives 20 Ω as the required series resistor value for the TISPNTP2A. Even at the 1500 V test level this resistor develops 25x20 = 500 V, which should ensure the coordination with the primary protector sparkover.

indoor POTS lines to ITU-T recommendation K.21. K.22 and IEC 61000-4-5: 1995

Internal POTS lines from WILL and ISDN-TA equipment are in a relatively unexposed environment. If these lines are galvanically isolated (floating), the return path for any induced surges can only be through equipment capacitance or insulation breakdown.

The most stressful condition would be when the POTs lines are not galvanically isolated. Such a case is when an ISDN-TA has a common connection between the incoming ISDN line and the internal POTs lines. The ISDN line is likely to be ground referenced and may have primary protection at the subscriber connection. If the primary protection operates, it provides a direct return to ground.

ITU-T recommendation K22 for a floating 4-conductor T/S bus uses a 1 kV 1.2/50 or 2/10 impulse, capacitively coupled via 8 nF to the bus conductors. Very little circulating current is likely to flow during K22 testing. If the T/S bus has a ground return then the testing changes to ITU-T recommendation K21. The required series resistor values for K21 and the TISP6NTP2A have been calculated earlier.

In IEC 61000-4-5: 1995 the highest specified test level is class 5. For unshielded symmetrically operated lines, class 5 testing uses a 4000 V combination wave (1.2/50, 8/20) generator to apply a simultaneous impulse to all conductors. For the four conductors of the two POTs lines, the currents are equalised by the use of specified 160 Ω feed resistors. As the generator fictive source impedance is 2 Ω the peak current in each conductor is 4000/(2x4 + 160) = 24 A. This is less than the 60 A TISP6NTP2A rating.

If the lines are long and exit the building, testing is done with a 10/700 generator. In this case the feed resistors are 100 Ω. and the fictive impedance is 15 Ω. The peak current in each conductor will be 4000/(15x4 + 100) = 25 A. This value is the same as the TISP6NTP2A rating.

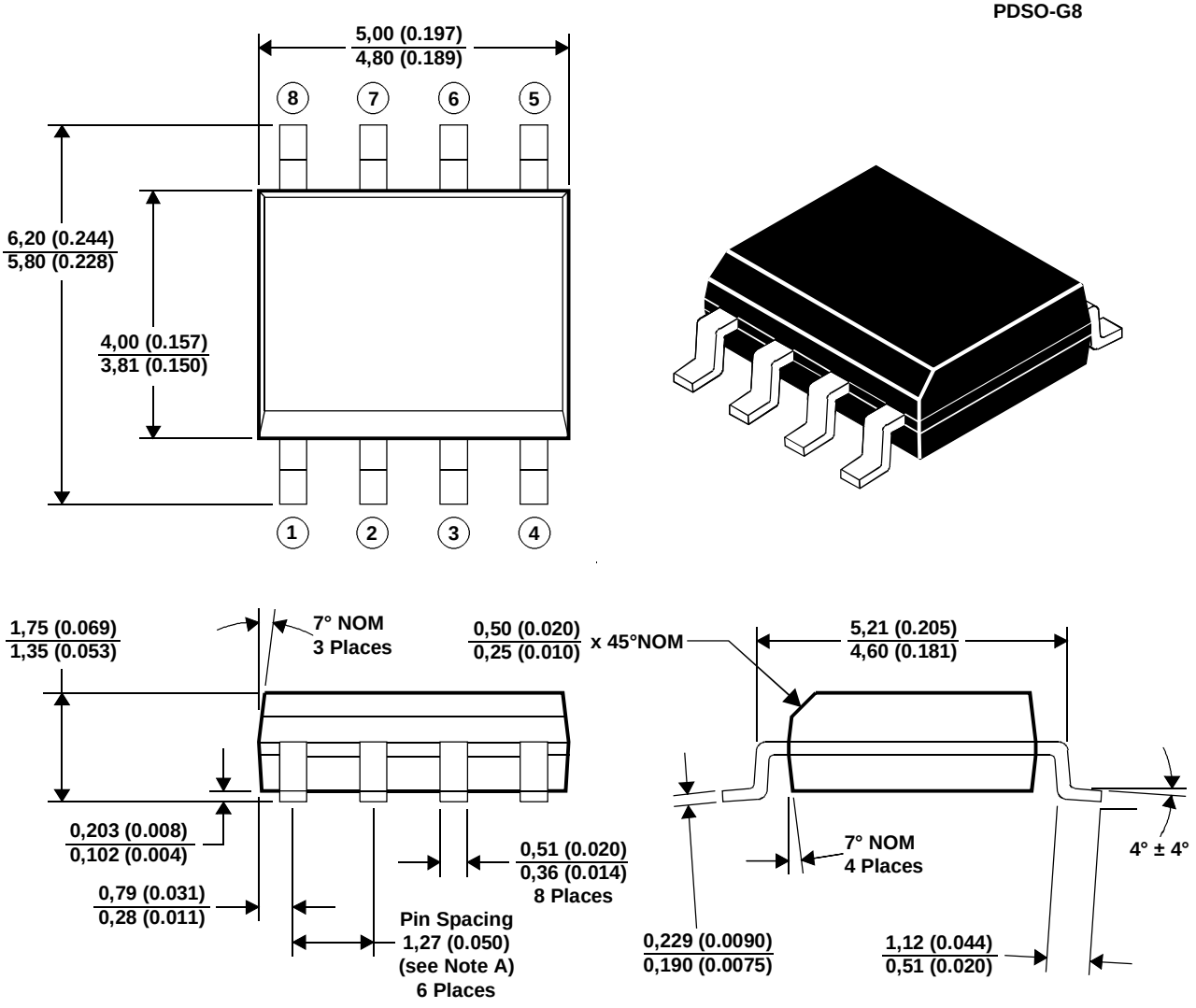
As the equipment connected to the POTs line may have uncoordinated protection, it is desirable to provided the ring-tip pair current sharing to the TISP6NTP2A by series resistors (R1A, R1B, R2A and R2B). A value of 4 Ω should be sufficient to ensure sharing.

MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



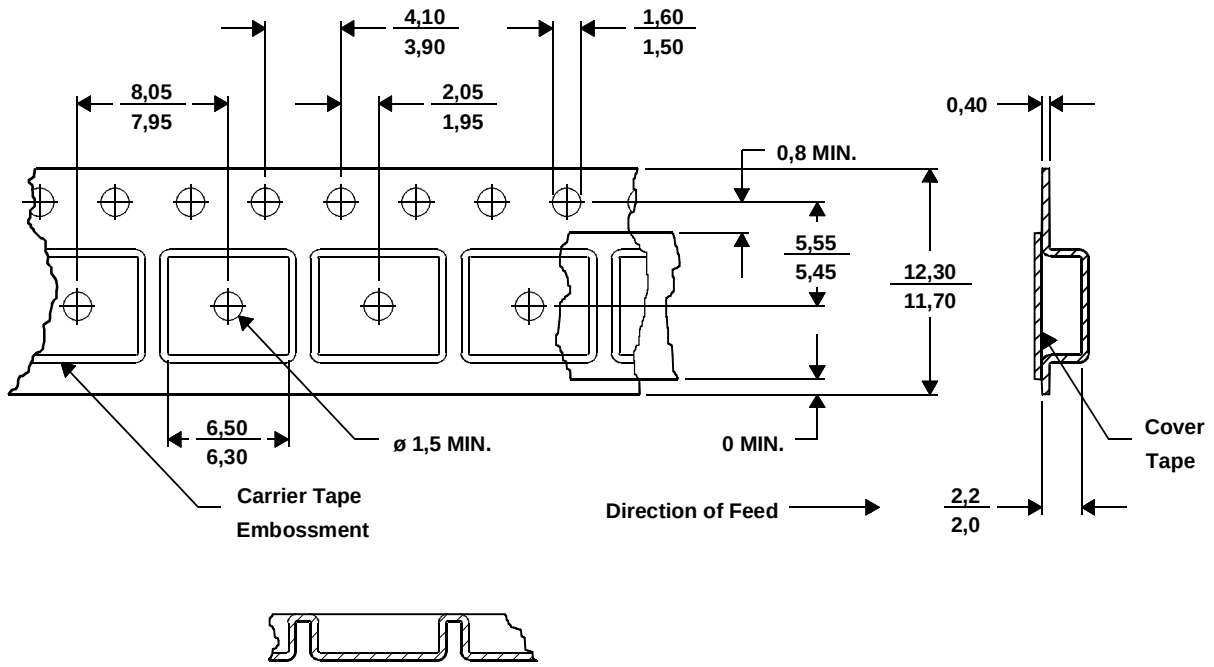
MDXXAA

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

MECHANICAL DATA

D008
tape dimensions

D008 Package (8 pin SOIC) Single-Sprocket Tape



ALL LINEAR DIMENSIONS IN MILLIMETERS

NOTES: A. Taped devices are supplied on a reel of the following dimensions:- MDXXAT

Reel diameter:	330 +0,0/-4,0 mm
Reel hub diameter:	100 ±2,0 mm
Reel axial hole:	13,0 ±0,2 mm

B. 2500 devices are on a reel.

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