TEXAS INSTRUMENTS

ThunderLan™ PCB Design Guidelines

Application Guide

1995

Networking Products Group

Printed in U.S.A., July 1995

SPWA002

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Networking Products—Semiconductor Group

SPWA002
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INTRODUCTION

The Texas Instruments (TI) ThunderLAN™ (TLAN) TNETE100 is a single chip Ethernet™ controller for the Peripheral Component Interconnect (PCI) local bus that includes an integrated 10Base-T/UTP (Unshielded Twisted Pair) and 10Base-5/AUI (Attachment Unit Interface) physical layer interface (PHY). When equipped with the appropriate external modular PHY, ThunderLAN can handle 100-Mbps Ethernet protocols to accommodate growth in the user's networking bandwidth demand. This document contains suggestions for layout of logic, physical layer, and power supply bypass components and their attachment to the connected system and other physical layer functions. TI suggests thorough testing and measurement of system parameters using the TNETE100 device to allow high quality operation in a network meeting IEEE 802.3 (10Base-5 and 10Base-T) approved standards and 802.3u (100Base-T) and 802.12 (100VG) draft standards.

Table 1 lists the contacts for receiving assistance with any questions concerning TI's ThunderLAN controller.

Table 1. Customer Assistance Contacts

TYPE OF INFORMATION	ASSOCIATED CONTACT
Asking about product operation or reporting suspected problems	TNETE Technical Support Line on the Internet: **TLANHOT@micro.ti.com** or send a FAX to: **(713) 274–4027**
Requesting more information about Texas Instruments Networking Products	Texas Instruments Incorporated Market Communications Manager, MS 736 P.O. Box 1443 Houston, Texas 77251–1443
Ordering Texas Instruments documentation	TI Literature Response Center: **(800) 477–8924**
Reporting mistakes in this document or any other TI documentation	Texas Instruments Incorporated Technical Publications Manager, MS 702 P.O. Box 1443 Houston, Texas 77251–1443 Electronic mail: comments@books.sc.ti.com

The ThunderLAN high-performance Ethernet architecture provides compatibility with the Medium Access and Electrical Interface sections of ISO/IEC IEEE Std. 802.3 and Blue Book Ethernet for 10Base-T (UTP) and 10Base-5 (AUI) compliant solutions. The TNETE100 allows for high performance, 100-Mbps Ethernet solutions for 100Base-T or 100VG-AnyLAN topologies when used with the appropriate physical media-dependent interface module at the device's Media Independent Interface (MII). Physical layer (PHY) modules supporting the MII interface can be used with the TNETE100 to realize any of the 100Base-Tx, 100Base-T4, 100Base-Fx or 100VG 100-Mbps cabling schemes. The PCI-compliant, glueless attached system interface operates at speeds up to 33 MHz and offers jumperless autoconfiguration using PCI configuration read/write cycles. This PCI interface has been developed in conjunction with leaders in the semiconductor and computer industries and has been vigorously tested on multiple platforms to ensure compatibility across a wide variety of available PCI products.

The TNETE110, a 10–Mbit–only device using the ThunderLAN architecture, excels in its simplicity of board design, given its high level of silicon integration, since it facilitates a complete 10Base-T solution (when used with appropriate network termination magnetics) requiring no external memory or PCI bus glue logic. The TLAN is packaged in a Quad Flat Package (QFP) surface mount package deploying 144

pins. Future releases of the TNETE product family are expected in the Thin Quad Flat Package (TQFP) surface mount package also deploying 144 pins. Low-power CMOS technology drives down power consumption for the media access contol (MAC) and 10Base-T physical layer solution.

Figure 1 shows the pin configuration for the TNETE100. Layout of the TNETE device allows for convenient grouping of functional signals into six principle domains, which minimizes printed circuit board (PCB) trace crossing in typical applications.

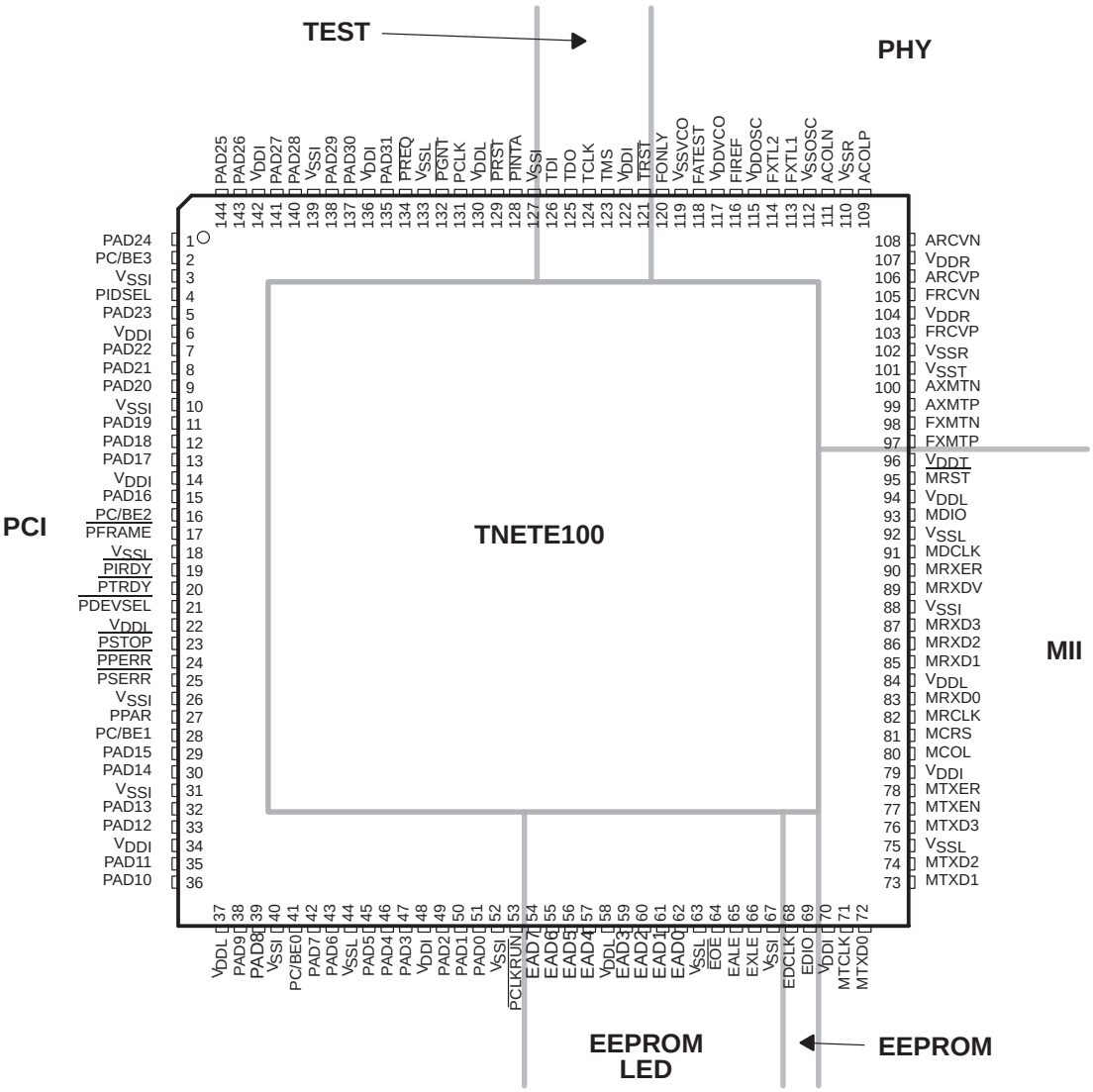

Figure 1. TNETE100-Pin Configuration

These design guidelines can assist the engineer in the hardware design of a TNETE-equipped LAN adapter card, based on laboratory and product design efforts at TI and other companies. Circuit schematics and a brief discussion of a typical application for a 100-Mbps VG-AnyLAN adapter occurs in the next section. Layout guidelines associated with particular circuit functions, plus special considerations in routing signals

within these regions and interconnecting these with other circuit functions are detailed. Finally, recommendations for the segmentation of power and ground regions as well as the filtering and bypassing of these regions using passive components also are detailed.

CIRCUIT SCHEMATICS

Network Interface Card Application

Figure 2 shows a 100-Mbps adapter solution using the TNETE100. A 100-Mbps VG solution requires the addition of a Physical Media Dependent (PMD) and Physical Media Independent (PMI) module with an MII interface to complete the solution.

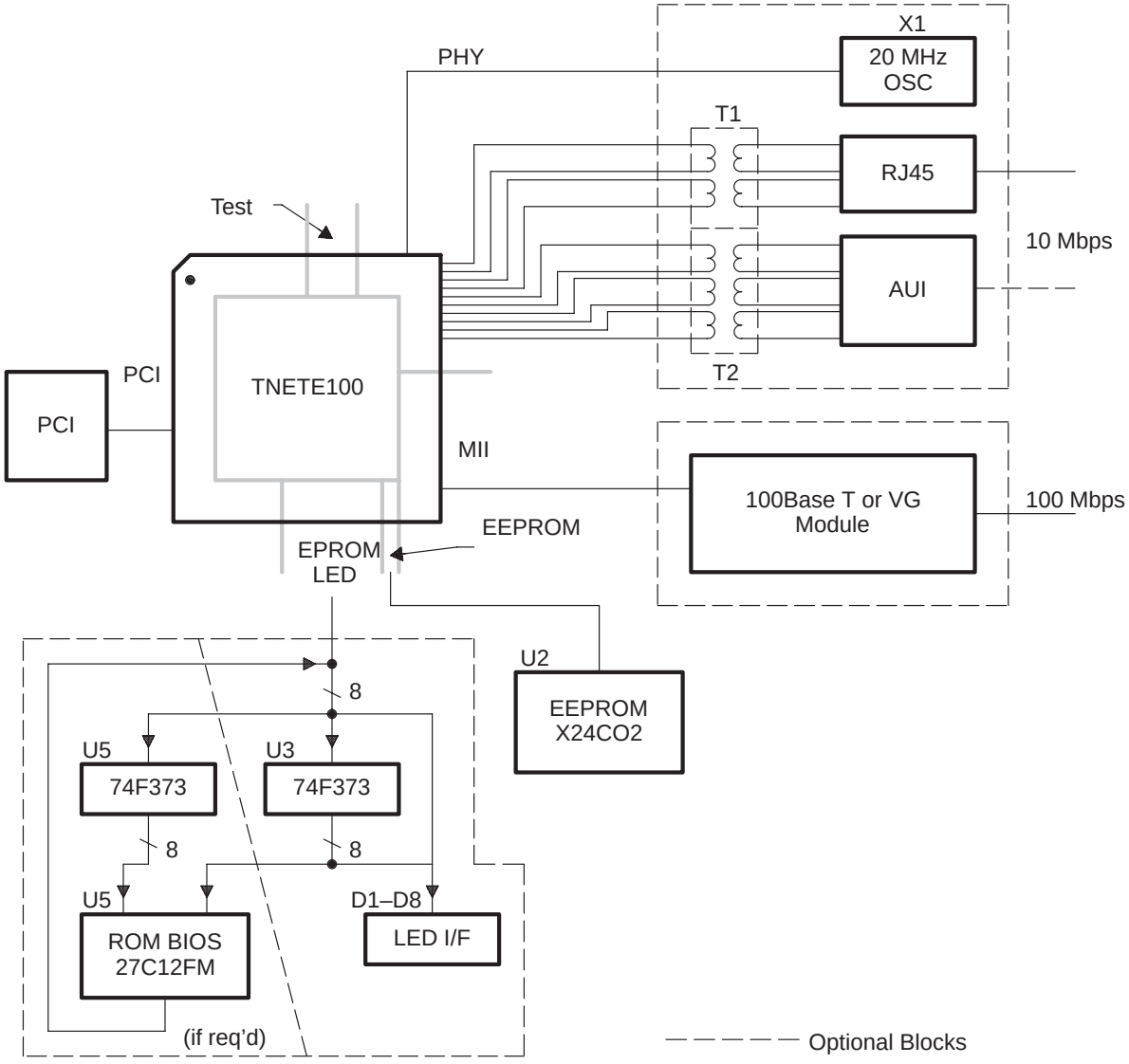

Figure 2. 10/100-Mbps NIC Application

The actual physical interface to the network is made by the PMI/PMD modular system. Data packets received from the network are terminated by the PMI/PMD according to the unique physical layer characteristics of the communication channel. These PMI/PMD modules are self-contained units that provide the appropriate cabling interface at the network and a four-channel stream structure described by the MII specification. The PMI interface can be implemented by another TI product, the TNETE211, which is a ThunderLAN-to-IEEE 802.12 PMD Interface for the 100VG-AnyLAN. In the case of 100VG-AnyLAN, four transmission-pair channels are driven simultaneously by the PMD with data that is scrambled into five-bit data quintets and encoded into six-bit (5B6B) symbols. Since the TNETE100's MII forms a natural 802.3u media interface, the PMI must additionally convert the high-speed serial format of 100Base-X MAC frame data octets into the five-bit data quintets that are then encoded into the 5B6B symbols required by the PMD for the 802.12 100Base-VG topology. More information on the conversion process is available in the appropriate IEEE documents and TI's TNETE211 Data Sheet (Literature Number SPWS019).

The rest of the active functions are provided within the TNETE100 device. Included is an Ethernet LAN controller that processes the 10- and 100-Mbps media access protocols. In the transmit channel, 64-bit data passed from the PCI interface logic is serialized and assembled into properly framed data packets with a computed cyclic redundancy code (CRC) appended. The packets are then received by the MII interface transceivers for output to the PMI/PMD module. In the reverse direction, sent packets from the MII interface are scanned for address matching and checked for a valid CRC field. If valid packets are received, they are deserialized and disassembled into 64-bit data fields for delivery to the PCI host interface.

The ThunderLAN architecture uses first-in, first-out (FIFO) pointer registers that include a collection of pointers and counters for controlling circular buffer FIFOs in time division multiplexed (TDM) synchronous random access memory (SRAM). The TDM function provides guaranteed bandwidth to the PCI bus controller and the LAN Controller via 64-bit wide channels on an equal basis for distributing data between each of these processes.

The ThunderLAN PCI Interface converts the 64-bit data in an internal multiplexed SRAM to 32-bit, 33-MHz data for DMA to/from the PCI bus. Included in this function are a configuration serial EEPROM interface to store characteristics needed to identify the PCI client in the arbitration process, a basic input/output system (BIOS) interface to an optional x8 EPROM to store system BIOS information and a light emitting diode (LED) interface for local monitoring. The LED interface can be implemented using an octal transparent latch. Figure 3 provides more detail on implementing the EEPROM and LED options.

Since the TNETE100 includes a 10Base-T PHY, the device can serve as a low-cost single chip, PCI-based 10-Mbps Ethernet solution. Figure 2 shows a 20-MHz clock oscillator and a UTP transformer connected to the PHY interface of the TNETE100. Power supply filtering and bypassing components, though not specifically shown in this figure, are critical to the performance of the adapter solution and are separately considered in the final section. This 10Base-T clock circuitry configuration is shown in more detail in Figure 4.

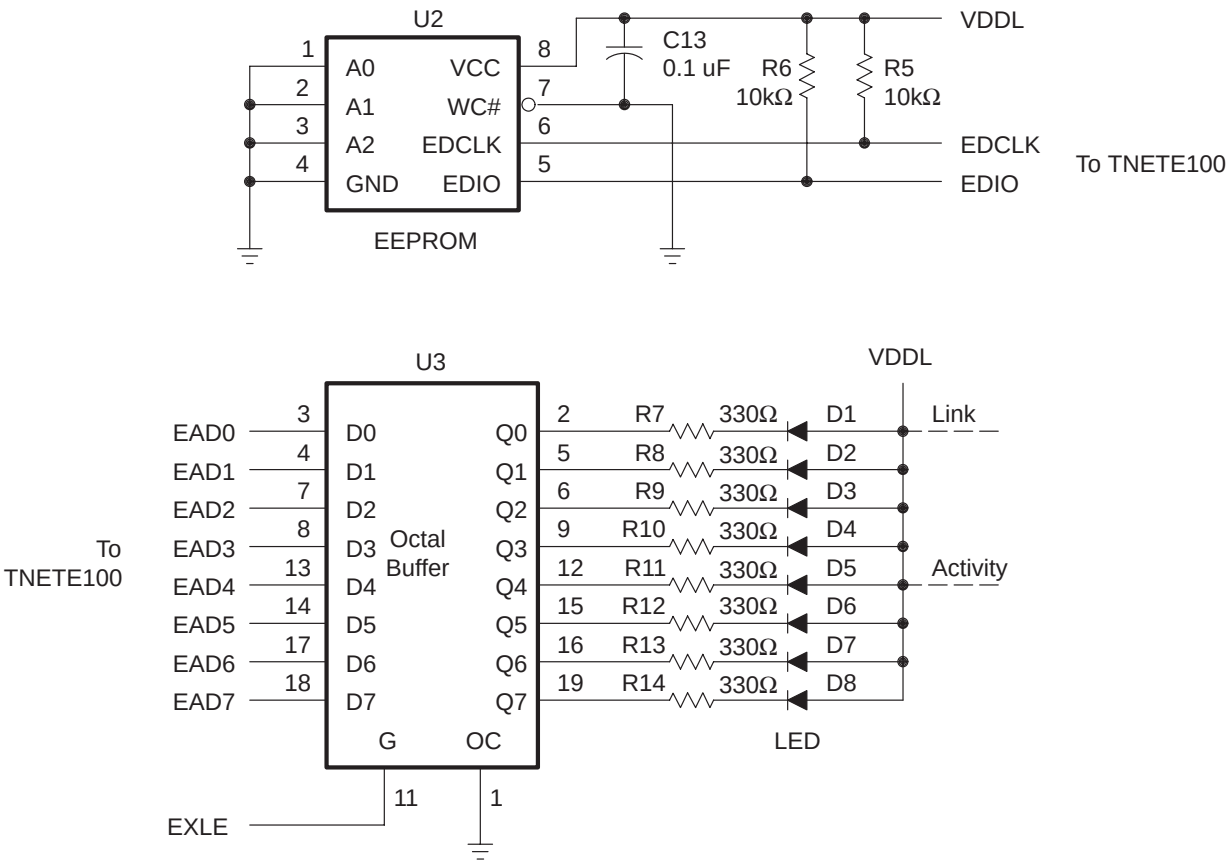

Figure 3. Serial EEPROM and LED Indicator Circuitry

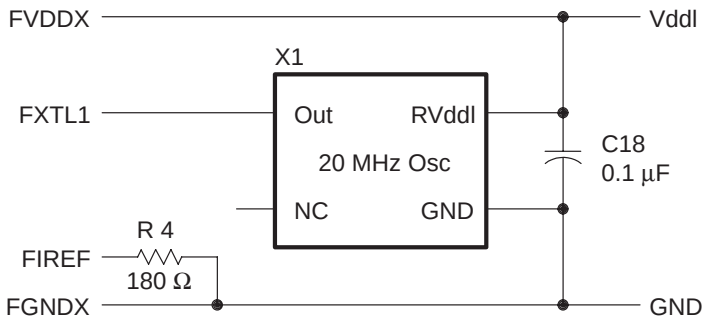

Figure 4. Clock Circuitry for 10Base-T Configuration

Interface to Dual-Media Shielded Twisted Pair/Unshielded Twisted Pair (STP/UTP)

Details of the UTP media interface are shown in Figure 5 and Figure 6 for 10Base-T only and 100/10-Mbps solutions. A modular UTP interface transformer assembly from Fil-Mag, Valor or other suppliers provides the necessary interface. The cabling pinouts for 100VG-AnyLAN and 10Base-T are shown in Table 2 and Table 3, respectively.

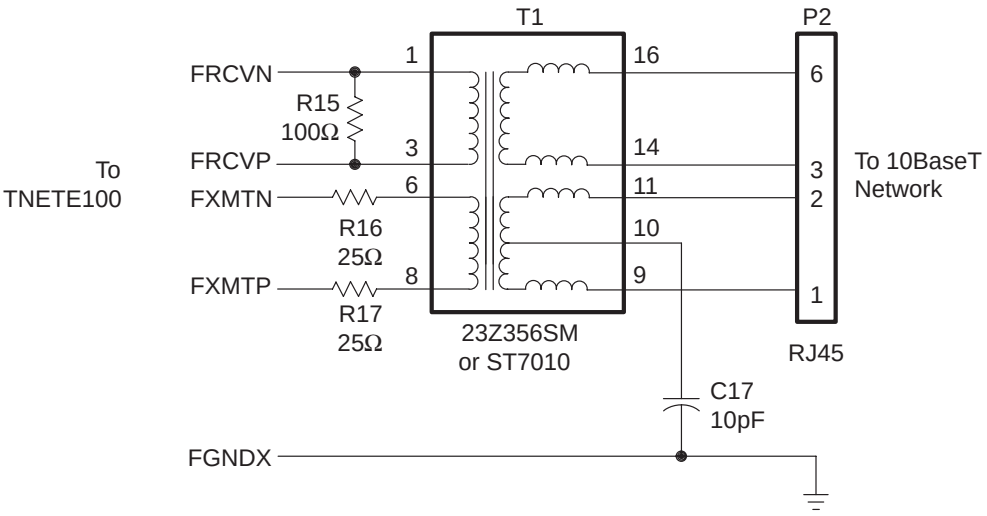

Figure 5. UTP Media Interface

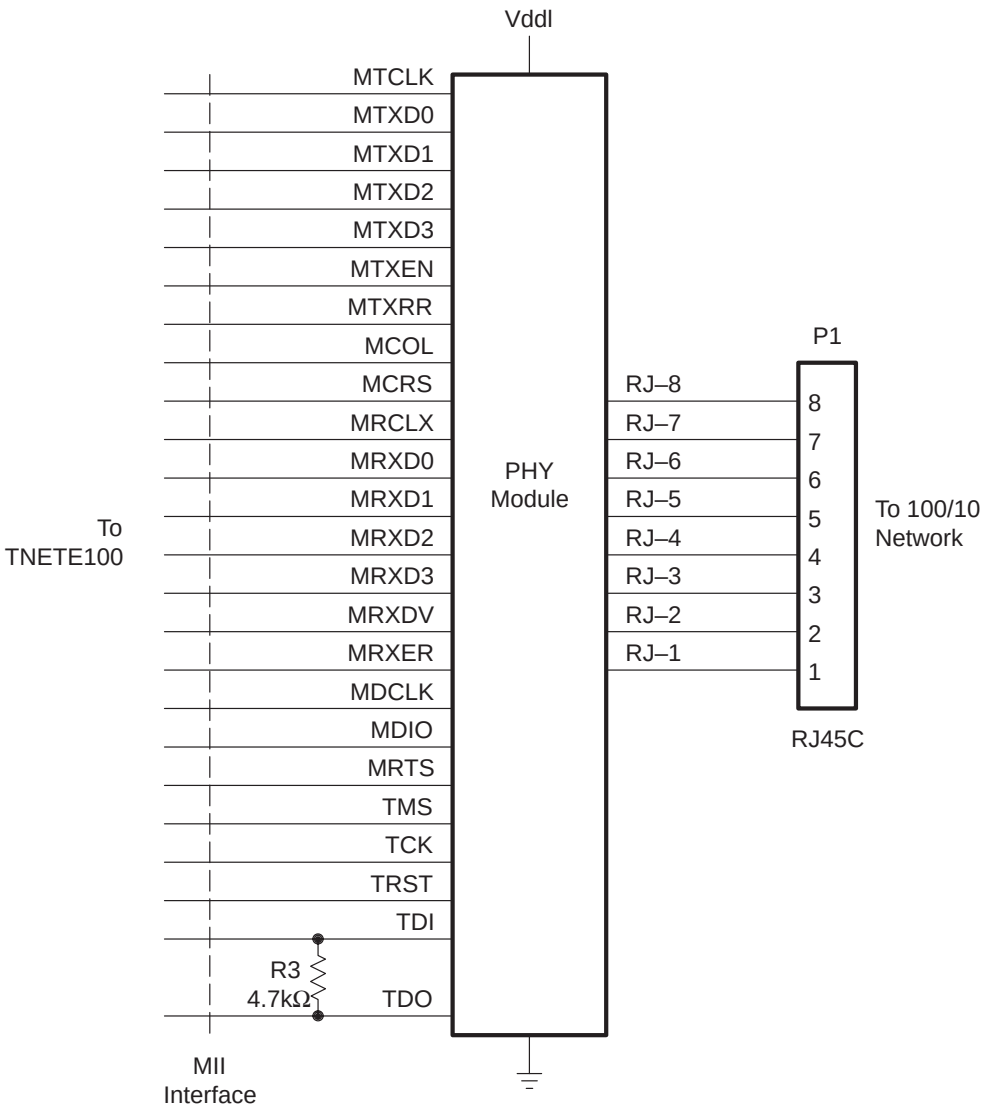

Figure 6. Media Interface Circuitry to 100/10-Mbps Network Using a 100-Mbps PHY Module

Table 2. 100VG, RJ45 UTP Cabling Pinout

RJ45 CONNECTOR PIN CONNECTOR SHIELD†	USAGE/CHASSIS
1	TP0+
2	TP0–
3	TP1+
4	TP2+
5	TP2–
6	TP1–
7	TP3+
8	TP3–

† If shield is implemented

Table 3. 10Base-T, RJ45 UTP Cabling Pinout

RJ45 CONNECTOR PIN CONNECTOR SHIELD†	USAGE CHASSIS
1	Tx+
2	Tx–
3	Rx+
4	N/C
5	N/C
6	Rx–
7	N/C
8	N/C

† If shield is implemented

Circuit Layout Guidelines

Signal Routing and Termination

Table 4 shows the grouping of the TNETE100 signals. Design tips (if any) applicable to each of these signals follow the listing in this table. Note that signals are classified in six major categories. Every attempt must be made to keep wiring runs as short as possible and within a general area bounded by these signal groupings. (Signal routing between groupings and other functions or modules must, of course, violate this rule; care should be taken not to traverse a third grouping when routing between any two.) Naturally, wherever passive components are associated with signals to or from the TNETE100, these components should be located as closely as practical to the device pins. This is especially true for power supply bypass capacitors.

Table 4. TLAN Signal Classifications

SIGNAL GROUPING	SIGNAL NAME (PIN)
PCI Interface	PAD0-31(51,50,49,47,46,45,43,42,39,38,36,35,33,32,30,29,15,13,12,11,9,8, 7,5,1,144,143,141,140,138,137,135), PCLK (131), PC/BE3-0 (2,16,28,41), PDEVSEL (21), PFRAME (17), PGNT (132), PIDSEL (4), PINTA (128), PIRDY (19), PTRDY (20), PPAR (27), PPERR (24), PREQ (134), PRST (129), PSERR (25) and PSTOP (23) and PCLKRUN (53)
100base MII Interface	MCOL (80), MCRS (81), MDCLK (91), MDIO (93), MRCLK (82), MRST (95) MRXD0-3 (83,85,86,87), MRXDV (89), MRXER (90), MTCLK (71), MTXD0-3 (72,73,74,76), MTXER (78) and MXTEN (77)
10Base-T PHY Interface	ACOLN (111), ACOLP (109), ARCVN (108), ARCVP (106), AXMTP (99), AXMTN (100), FATEST (118), FIREF (116), FONLY (120), FRCVN (105), FRCVP (103), FXTL1-2 (113,114), FXMTP (97) and FXMTN (98)
Serial EEPROM Interface	EDCLK (68) and EDIO (69)
EPROM/LED Interface	EAD7 – EAD0 (54,55,56,57,59,60,61,62), EALE (65), EOE (64) and EXLE (66)
Test Ports	TCLK (124), TDI (126), TDO (125), TMS (123) and TRST (121)

PCI Interface

Reliable operation of the self-contained, glueless TNETE PCI interface primarily depends on industry-standard board design practice. The PCI design specification must be followed carefully for all PCI-compliant designs, and this application is no exception. In the context of board design, the impedance of the signal traces is particularly important to help ensure proper signaling levels. At operating frequencies greater than 30 MHz, these run impedances must be held between 60 and 100 ohms. Another constraint on the design of these trace geometries is matching the TNETE CMOS outputs to the PCI bus. CMOS output drivers typically have impedances that range upward to 120 ohms, which is above the 100-ohm limit for the PCI bus. It is best practice to set the trace's stripline impedance as closely as design tolerances allow to 100 ohms. If the printed circuit board house has a 10% tolerance, then the trace stripline impedance should be set at 90 ohms, so that the high end of the PCI specification is not violated.

Test Ports

The test ports are compliant with the requirements of the IEEE Standard 1149.1-1990, ~Test Access Port and Boundary-Scan Architecture" (JTAG).

Power and Ground Distribution

The choice of whether to use ground and power configuration requires the engineer to make a few fundamental considerations. To maintain the required trace impedances, the ground foil must be the first inner layer (layer number 2) underneath the stripline wiring for signal and critical wiring runs. Application testing has proven that a solid ground plane as shown in Figure 7 is a better alternative than attempting to segment grounds according to internal function.

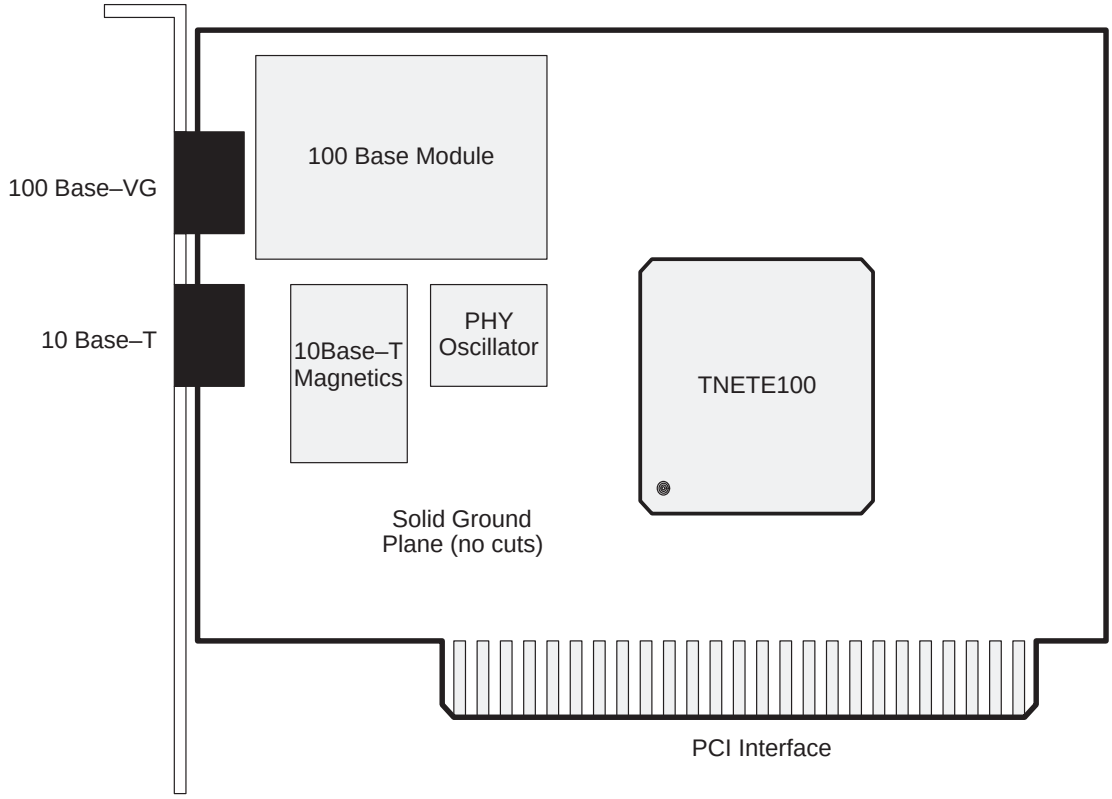

Figure 7. Ground Layout Guidelines

Further, the analog PHY functions must have a higher quality filtered power supply than all other functions on the board to achieve the lowest noise, jitter-free environment for errorless data communications at high data transfer rates. This implies isolation of the V_{DD} paths within the major three power domains described in Table 5.

The PCI adapter solution can operate with both 3-V and 5-V PCI bus configurations. To achieve this flexibility, all of the PCI interface buffers are tied to a separate interface power (VIO) region that includes the PCI connector and wiring paths. Simply stated, when the PCI connector is plugged into a 3-V PCI slot, the VIO section of the plane becomes 3 V, but when it is plugged into a 5-V slot, it becomes 5 V.

Table 5. V_{DD} and V_{SS} Pins of TLAN

Supply Grouping	Signal Name (Pin)
PCI Interface Power (3 V or 5 V)	V_{DDI} (6,14,34,48,122,136,142)
10Base-T PHY Power (filtered 5 V)†	V_{DDR} (104,107),V_{DDVCO} (117), V_{DDOSC} (115) and V_{DDT} (96)
Logic Power (5 V only)	V_{DDL} (22,37,58,70,79,84,94,130)
All common grounds	V_{SSI} (3,10,26,31,40,52,67,88,127,139), V_{SSL} (18,44,63,75,92,133), V_{SST} (101), V_{SSR} (102,110), V_{SSVCO} (119) and V_{SSOSC} (112)

† Although V_{DDOSC}(115) and V_{DDT}(96) are supplies to the analog section, it is recommended that they be connected to the logic supply rather than to the analog supply to help minimize noise in the analog power supply.

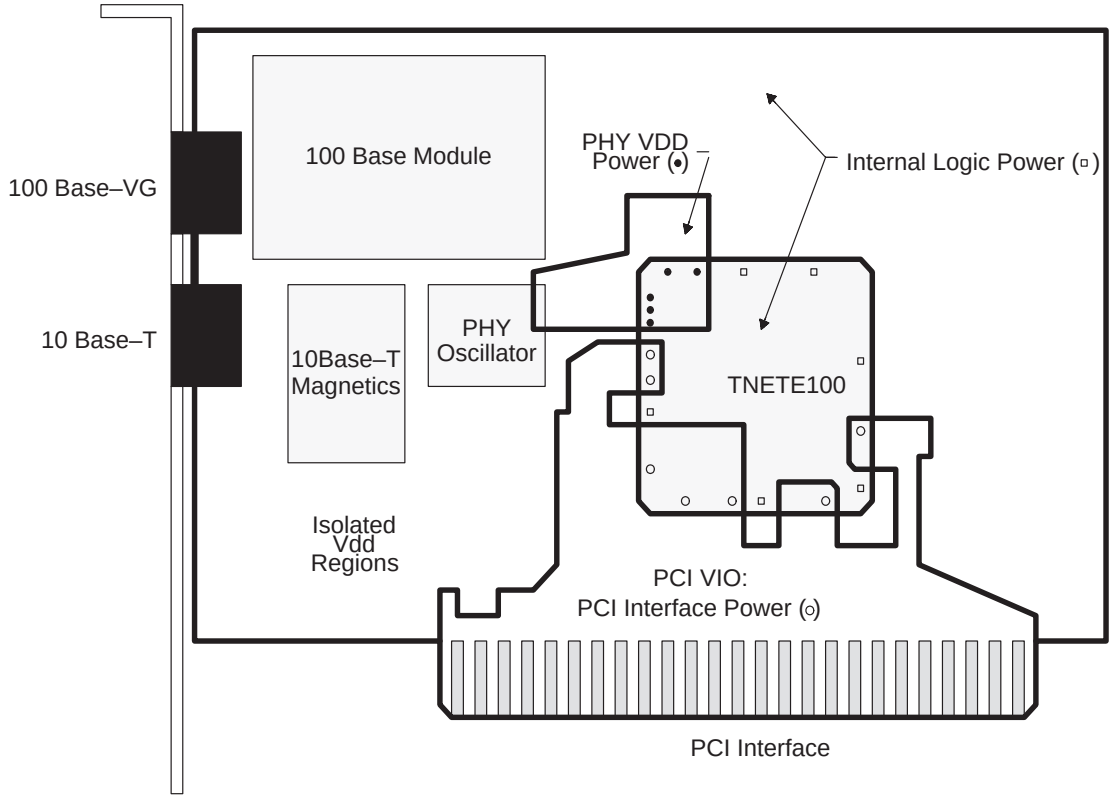

Figure 8. Power Layout Guidelines

Four-layer boards, where the two inner layers are for power and ground and the two outer layers are for signals (ground side) and random logic (V_{DD} side), have been successfully implemented at the test and development facilities. When designing the V_{DD} layer,segmented regions with notches and swirls similar to that shown in Figure 8 can be used for each of the power supply regions described in Table 5. These cuts should include rounded or 45° corners to prevent electrical reflections of high frequency current, and mechanical undermining of the foil itself. The layout shown in Figure 8 is a representation (not exact) of these cuts. The actual positions of the cuts and swirls are made to include V_{DD} appropriate for the power supply region. The regions with the notches and swirls, are the PCI VIO and PHY V_{DD}. The region with

the largest cutout is VIO. VIO goes from the VIO pins of the PCI bus to the VIO pins on the TLAN. The pads that are being avoided on the left and right side are the V_{DD} pins of the main logic power that are neither PCI nor PHY related.

Given that the initial deployment of TNETE silicon is in the 144 QFP package, and that future silicon plans to be packaged in the thinner, small area TQFP, TI recommends that a board layout accommodate both of the TNETE package styles in a dual-footprint configuration. Such a dual-footprint configuration is shown in Figure 9.

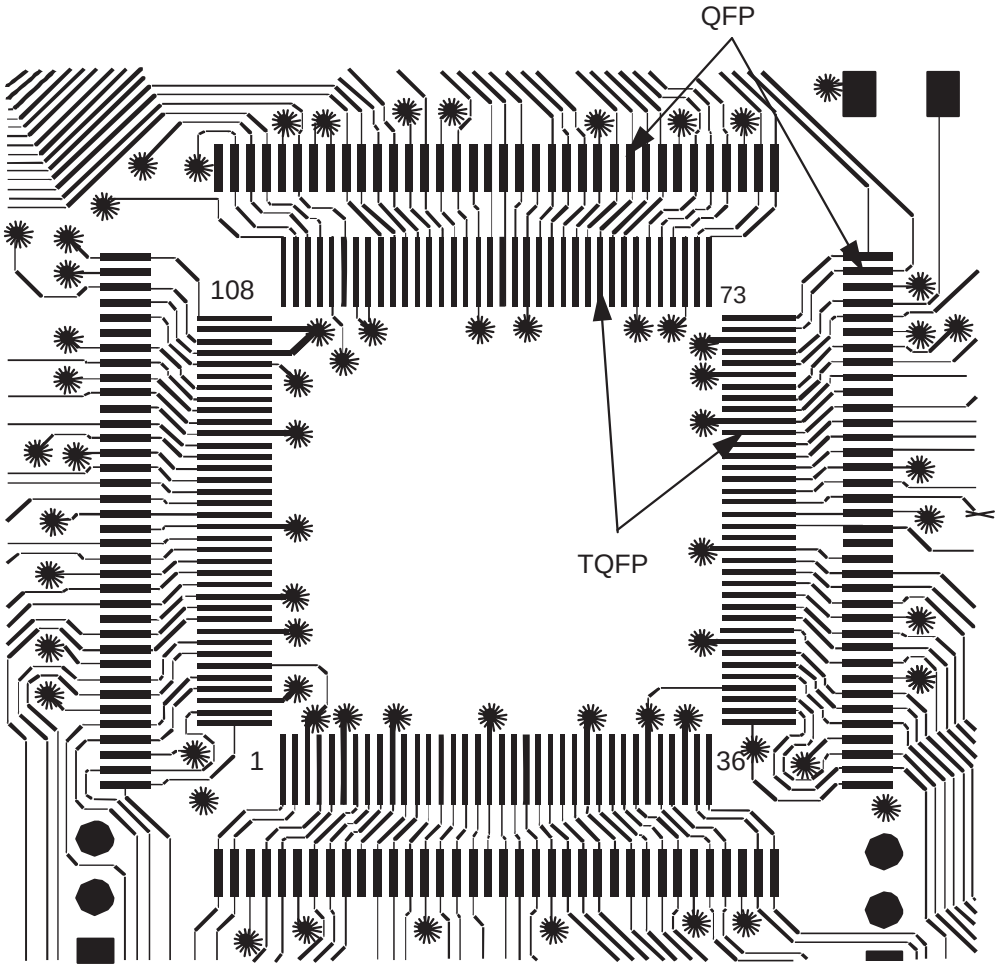

Figure 9. Dual-Footprint Arrangement for QFP and TQFP Package Styles

Decoupling

Figure 10 shows typical supply voltage and ground filtering components for the TNETE solution and summarizes the component values. It is expected that the 22 uF tantalum capacitors are planned to be used close to the point of entry of the power supply, and that the remainder of the decoupling can be achieved by the 0.1 uF BX ceramic capacitors distributed around the device. The quantity and types of decoupling capacitors are chosen to maintain a solid V_{DD} bus that is uniformly distributed around the periphery of the TNETE device and that provides a progressively lower impedance to increasing frequency. All of the V_{DD} and V_{SS} pins of the TNETE should be connected directly to the appropriate internal plane, and the decoupling capacitors should also be connected to these internal planes. Each V_{DD} and V_{SS} terminal and each decoupling capacitor pin should use a separate via to reach the internal plane. They share vias with nonpower connections such as pullups, but an engineer should aviod sharing of vias between separate bypass capacitors.

In the PHY V_{DD} region, there is a filter inductor to further buffer conducted noise on the V_{DD} supply from sensitive analog PLL circuits and receivers. This is the cap/bead structure (L1) shown in Figure 10 for the PHY V_{DD}.

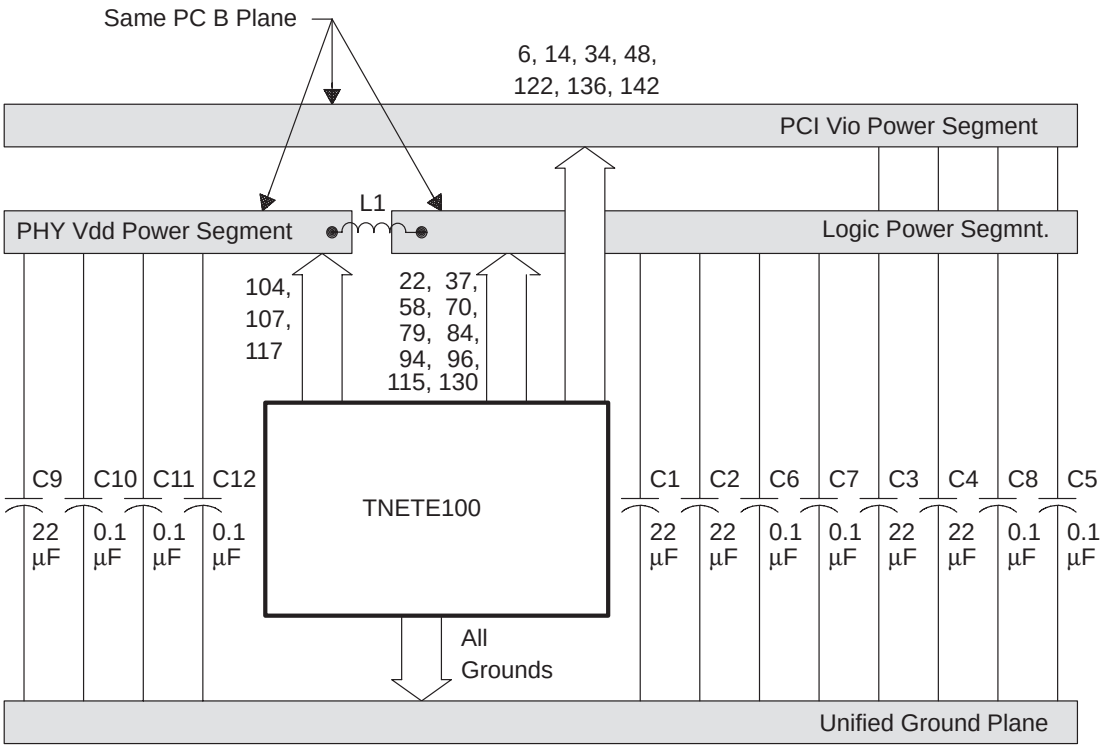

Figure 10. Supply Voltage and Ground Filtering Components

Table 6 shows typical component values for the diagram in Figure 10.

Table 6. Typical Component Values for Figure 10.

Symbol(S)	Function	Value	Type
L1	Power Supply Filtering		HF70ACB453215
C1, C2, C3, C4, C9	Power supply bypass capacitors (low frequency)	22 μF	Tantalum
C5, C6, C7, C8, C10, C11, C12	Power supply bypass capacitors (mid frequency)	0.1 μF	BX/X7R