System Layout Guidelines for Using the TNETE2101 10/100 Mbit/s Ethernet Physical Layer Device

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Abstract

The goal of these guidelines is to provide hardware systems designers with the information and recommendations needed for achieving the highest level of cost-effective system performance when using the Texas Instruments (TI™) TNETE2101 10/100 Mbps ethernet physical layer interface (PHY) device in their networking applications.

Careful planning and special considerations are required during the schematic and layout stages of high-speed system design in order to create an operating environment which is not only stable and robust, but also emits a minimal amount of radiated energy (i.e., low EMI).

Interfacing to Twisted Pair Media

For most ethernet systems, the TNETE2101 will be interfaced to a network consisting of CAT 5 unshielded twisted pair (UTP) media through an RJ-45 connector and a 10/100 Mbps capable transformer. Below are system considerations when designing a hardware system for interfacing to a Fast ethernet network.

General Layout Considerations

- The isolation voltage of the transformer used to connect to the UTP or STP media should be rated to $\geq$ 2kV to protect the system circuitry from static voltages accidentally applied across the connectors or cables.
- The 10/100 transformer should be placed as close as possible to the RJ-45 connector.
- All traces, which run from the transformer to the RJ-45 connector, should be matched in length and made as short as practically possible. The individual signal lines within differential signal pairs (e.g., AXMTP/AXMTN and ARCVP/ARCVN) should always be routed closely together.
- One should avoid allowing transmit and receive signals to cross by routing them, when possible, on board layers which are on opposite sides of the Printed Circuit Board (PCB).
- The use of vias, particularly on critical traces, should be avoided or at least kept to a minimum.

Ground and Power Plane Layout Considerations

For PCB layouts used to implement systems incorporating the TNETE2101 device, it is recommended that a board with at least 4 layers be used. For a 4-layer implementation, it is recommended that the power and ground planes be placed as the two inner most planes, with the ground plane being located closest to the component side of the board. In order to achieve the highest performance possible, it is further recommended that the ground plane for multiple physical layer devices located on the same board should be separated from each other by moats or gaps to isolate any noise that might be generated by an adjacent device. As shown in Figure 1, the gaps between a physical layer device's ground plane and any adjacent device(s) is a minimum of 0.1 inches (2.5 mm) wide. In addition, as shown in Figure 1, no ground plane exists under the transformer. To prevent the coupling of any noise from the RJ-45 connector(s), they should sit upon a dedicated chassis ground plane. It is recommended that this isolated chassis plane be implemented both in the upper signal level and in the inner ground plane. Special attention is taken with gaps in the chassis plane so LED connections can pass through.

In order to avoid having high frequency noise being injected onto active signals via the global ground plane, the ground plane for the PHY and other devices should be completely separated from the connectors (RJ-45) and transformers by a gap of 0.20-0.40 inches (5.1-10.2 mm) wide. Most standard single channel magnetic devices are at least 0.24 inches (6.10 mm) wide and most four channel (quad) magnetic devices are approximately 0.48 inches (12.2 mm) wide, so their packages can comfortably bridge this gap. If, however, the package of the magnetic device you want to use is somewhat narrower than this, scale the gap so that the magnetic device can comfortably bridge this gap with sufficient overlap.

As shown in Figure 2, the power plane for the TNETE2101 should be designed to isolate the sensitive analog portions of the device from other parts of the system. In particular, isolated analog power planes should be used in order to minimize clock jitter and transmit distortion. For the TNETE2101, we recommend creating *two* (2) separate analog power planes. One analog power plane should be used for connection to the AXMTP/AXMTN input pair and the VDDA power input for the Xmt circuit connections (pin #84). The other analog power plane should be used for connection to ARCVP/ARCVN circuit, the ACPLL, and other VDDA power pins.

The gap between power planes should also be at least 0.1 inches (2.5 mm) wide. A separate chassis ground section should be included on the top two board layers (Signal layer #1 and GND) only. Provisions for routing a connection between the chassis ground and the input for the power supplies should be made so that the chassis ground section can be capacitively coupled to the system during electromagnetic interference (EMI) testing.

Signal Line Routing Considerations

All differential or complimentary signal lines, such as ARCVP and ARCVN, should be routed as pairs in parallel. These signals should always be routed on the same side of the board, and should have a separation not to exceed 0.20 inches (5.1 mm) between them. The MII signals (e.g., MRXD<0-3>, MRXER, etc.) are also fairly sensitive and should be routed as directly from source to destination as possible. The use of vias, particularly on certain signal lines such as ARCVP/ACRVN, AXMTP/AXMTN, MTCLK and MRCLK, should be avoided.

Digital logic signals such as MTXD<0-3>, MRCLK, or MTCLK should be kept away from the differential transmitter or receiver pair signals and the reference clock input.

For a four-layer PCB implementation with components mounted on the top side of the board, we recommend the following layer assignment:

Top of Board:

1) Signal Layer#1
2) Ground Layer (GND)
3) Power Layer (DVDD, AVDD, XMT_VDD)
4) Signal Layer #2

Bottom of Board

Power Supply Decoupling

It is recommended that ferrite beads as shown in Figure 3 should be used to decouple the analog and digital power planes for the board. In addition to the ferrite beads, additional bypass capacitors are needed between each power supply pin and its associated ground. For the majority of the power supply pins on the TNETE2101, the recommended bypass capacitor is a 0.1 μF ceramic capacitor. For filtering and decoupling of the major power supply planes, we recommend the use of a 22 μF tantalum capacitor in parallel with a 0.22 μF ceramic capacitor. For ferrite beads, we recommend the TDK ZBF503D-00, Phillips BDW-3.4/7/6-452, or an equivalent ferrite bead with impedance at 250 MHz of at least 100 Ω.

Component Placement

Decoupling capacitors should be mounted as close as physically possible to their respective device pins. Figure 4 shows an example of good traces routing for those device pins which require decoupling components. The trace should route directly from the pin to the pad for one of the terminals of the capacitor. From the capacitor terminal pad the trace routs to a via which connects directly to the power or ground plane. This layout scheme places the capacitor directly in the path of any noise on the power or ground plane. In addition, it adds a small amount of inductance in series, which helps to add further filtering behavior. For best transmit and receive behavior, the UTP cable termination resistors located on the chip side of the magnetics should be placed as close as possible to their respective AXMTP/AXMTN and ARCVP/ARCVN pins on the TNETE2101. In addition, the bias resistors connected to pins ATXREF and AIREF are very important, as they are a potential source for coupling noise into the device. As demonstrated in Figure 5, make sure that the traces for these components are as short as possible and that no high-speed signals pass near them.

Figure 1. Ground Plane Structure to Minimize Noise Injection

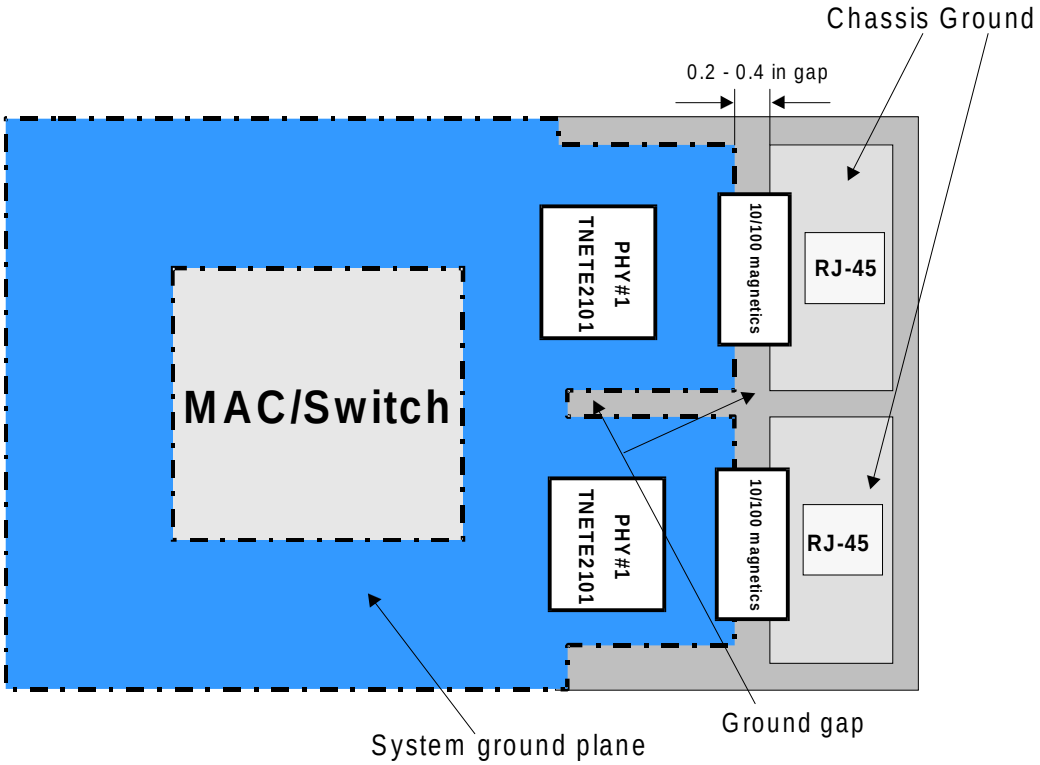


Figure 2. Power Plane Structure; DVDD, AVDD#1, Xmt_VDD#1, AVDD#2, and Xmt_VDD#2

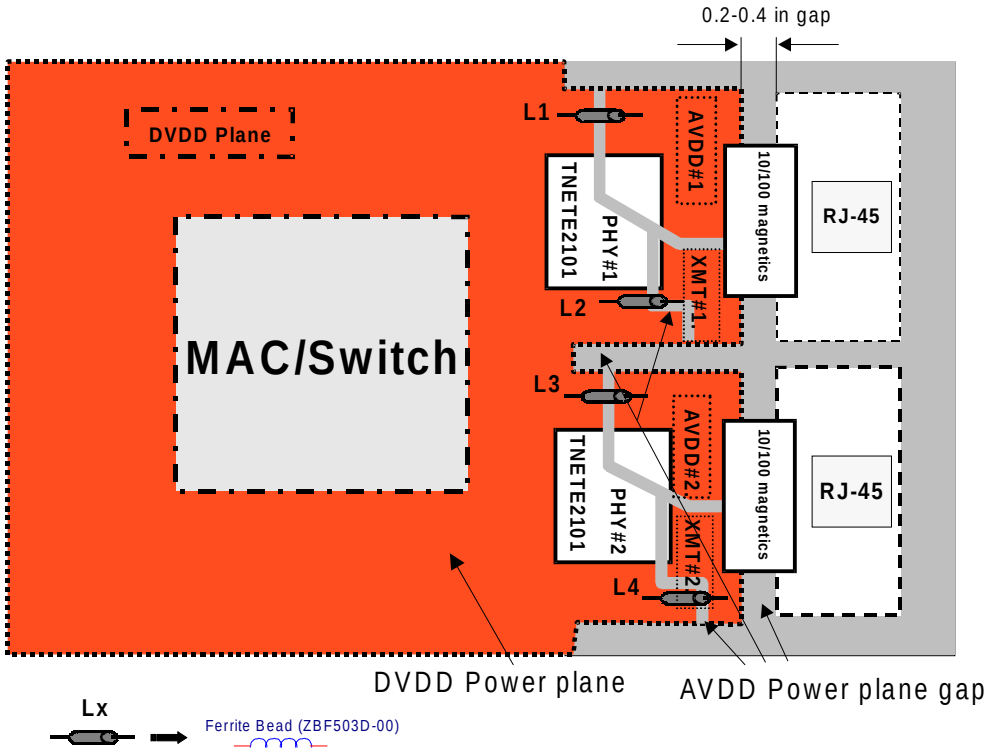


Figure 3. Power Plane Decoupling and Filtering

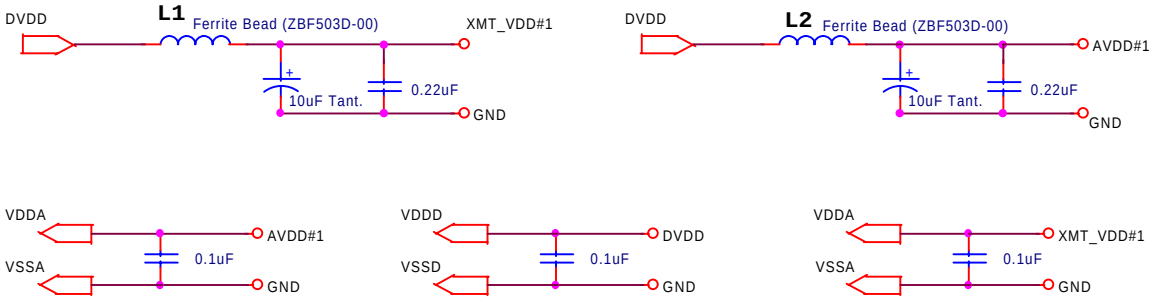


Figure 4. Suggested Trace Routing for Device Level Power Decoupling

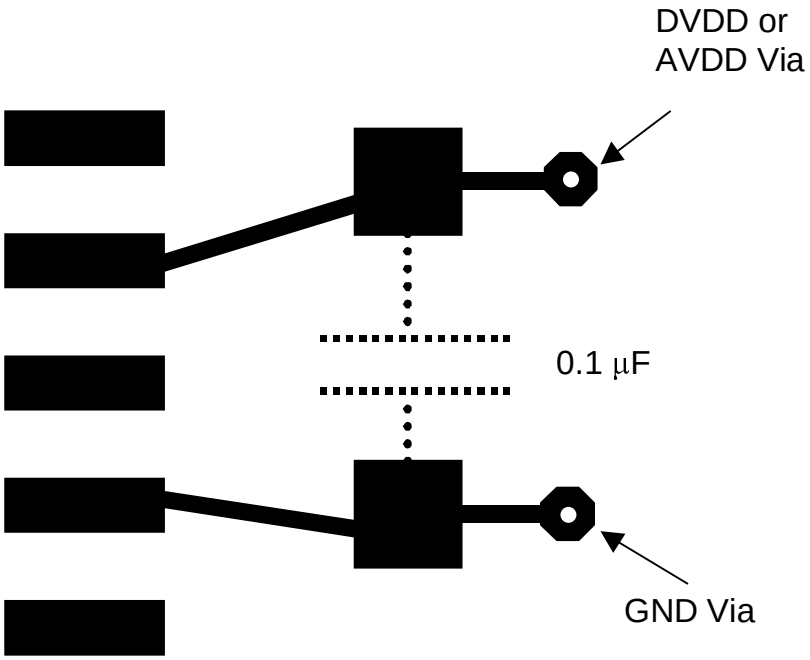


Figure 5. Example of Suggested Trace Routing for Biasing Resistors

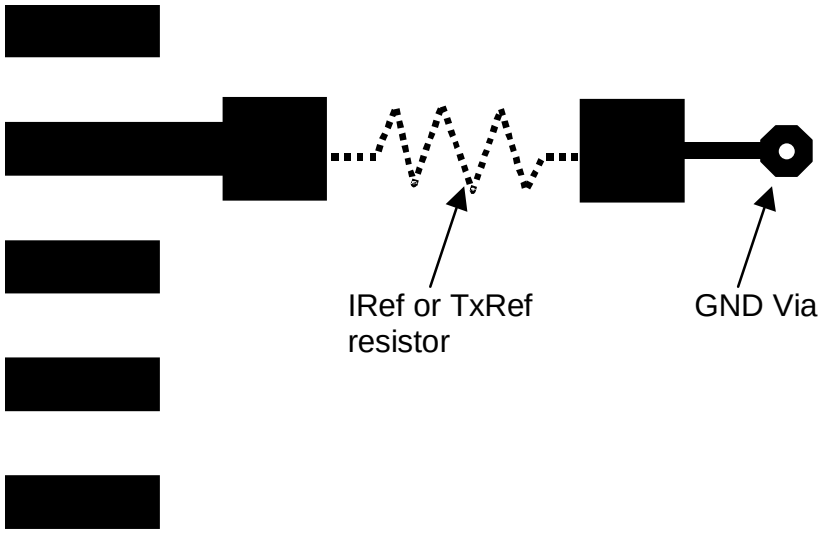
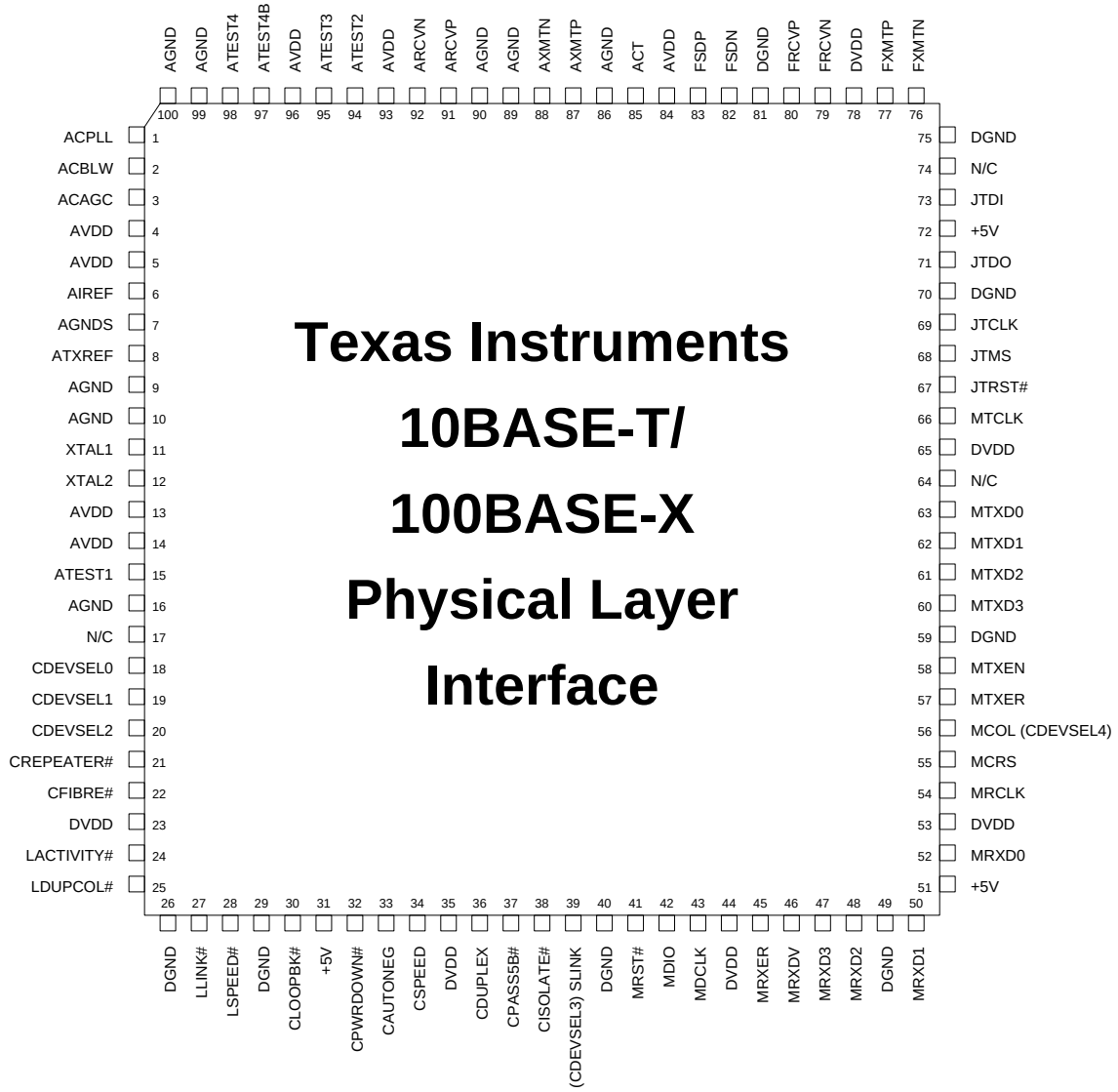


Figure 6. Pin Out Diagram for the TNETE2101



Appendix A. Product Support on the World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.