Application Report
SPWA009A

System Considerations Using Three TNETE2008 OctalPHY Devices with the TNETX3270 ThunderSWITCH

Worldwide Broadband Access Group
LAN Products

Abstract

The Texas Instruments (TI™) TNETX3270 ThunderSWITCH™ 24/3 is a high-speed Ethernet multiport switching device allowing network system designers to deliver switching products that satisfy corporate desktop environments. The TI TNETE2008 OctalPHY is a physical-layer (PHY) interface device for up to eight 10BASE-T networks using a multiplexed medium-access controller interface compatible with the TNETX3270 or equivalent.

This application report describes a printed circuit board (PCB) layout using the TNETX3270 device and three TNETE2008 interface devices. The PCB layout reflects the special considerations required to create a stable operating environment and minimize radiated energy.

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Introduction

A PCB layout using the TNETX3270 device and three TNETE2008 devices requires special considerations to create a stable operating environment and minimal radiated energy.

Ground Plane Layout

Figure 1 shows a recommended ground plane layout. Use the “20h rule” to isolate the physical layer devices from the circulating currents between the switching fabric and the adjacent physical layer sections. The “20h rule” says that adjacent buses should be separated by at least 20 times the distance from the routing layer to its reference plane. Do **NOT** place any splits or slots in the ground plane, except to separate the system and chassis ground areas.

The gap under the isolation transformers, the chassis ground split, is 0.4 inch. This spacing should be acceptable under most standard four-channel magnetic devices that have a package body width of approximately 0.48 inch. If a thinner device is used, scale the gap so that the body bridges the open space between the ground planes with little overlap to the planes.

Power Plane Layout

Figure 2 shows a recommended power plane layout that isolates the analog sections of the TNETE2008 devices.

These areas must be kept quiet because the receive and phase locked loop (PLL) circuit sections are referenced to this plane. Noise here can create jitter in the clock and receivers. The transmitters are also referenced here since they must have a clean power to prevent transmit distortion.

Signal Plane Layout

The RXz+ and RXz- tracks should route from the TNETE2008 to the terminations and then on to the magnetics.

The TXz+ and TXz- track lengths between the TNETE2008 and the magnetics should be as short as possible to minimize radiation. At the same time, the pairs should be spread out to reduce cross talk as much as possible while maintaining the same length.

The layers of a four layer board should be stacked as follows:

1) Signal layer (see Figure 3)
2) Ground layer (see Figure 4)
3) Power layer (see Figure 5)
4) Signal layer (see Figure 6)

Figure 3 through Figure 6 show a layout developed by Texas Instruments for system compliance testing as well as EMC scans.

Analog Power Connections and Decoupling

Figure 7 shows the decoupling components and the pins they are mounted near. To improve power supply noise decoupling, all decoupling capacitors should be connected near the related power supply pins and then the capacitors connected to the power planes with a short track.

Figure 8 shows a structure to place the pin decoupling on the individual pins in the analog VDD sections. Notice that the capacitor on XMTVDD, pin 38, is referenced to the GND plane and not to an individual component pin. It should also be noted that all XMTGND pins need an individual GND plane connection and should not have shared vias.

The trace should route from the pin pad to the capacitor and then on to the power plane. This places the capacitor in the path of any noise and will add a small amount of inductance in series with the power source. Both of these effects are desired.

The chassis ground section is included on each power plane and routed to the power input so that the chassis can be capacitively coupled to the system ground return during electromagnetic interference testing. This has been shown on some occasions to provide a path for noise to leave the cable interface without being radiated into the area of measured concern.

Other Design Suggestions

1) Use only 3.3V oscillators. Do not use a 5V oscillator with a output level shifter. 5V oscillators tend to radiate during EMC testing more than the lower drive clocks. Also, the level shifter is another source of noise.

2) Keep the 83MHz source close to the TNETX3270 with minimal trace lengths.

3) Prevent the clocks from changing layers.

4) Isolate the clock VDDs from the power plane with a ferrite bead. Include a bulk cap and small decoupler on the oscillator side of the bead.

5) Add group bulk decoupling in the SDRAM area of the PCB. This section is noisy and may radiate during EMC testing.

6) No signal should cross a gap in either the power or ground plane. A gap forces the return path to form a loop and radiated noise will result.

7) JTAG signals should not be routed parallel to any clock signal. The JTAG traces route to the entire PCB and any clock noise coupled onto the JTAG lines will be distributed across the board. If JTAG is not used, tie these lines to their default conditions. (i.e., JRST=0, JTMS=1, JTDI=1, JTCLK=1, JTDO=NC)

Figure 1. Recommended Ground Plane Layout

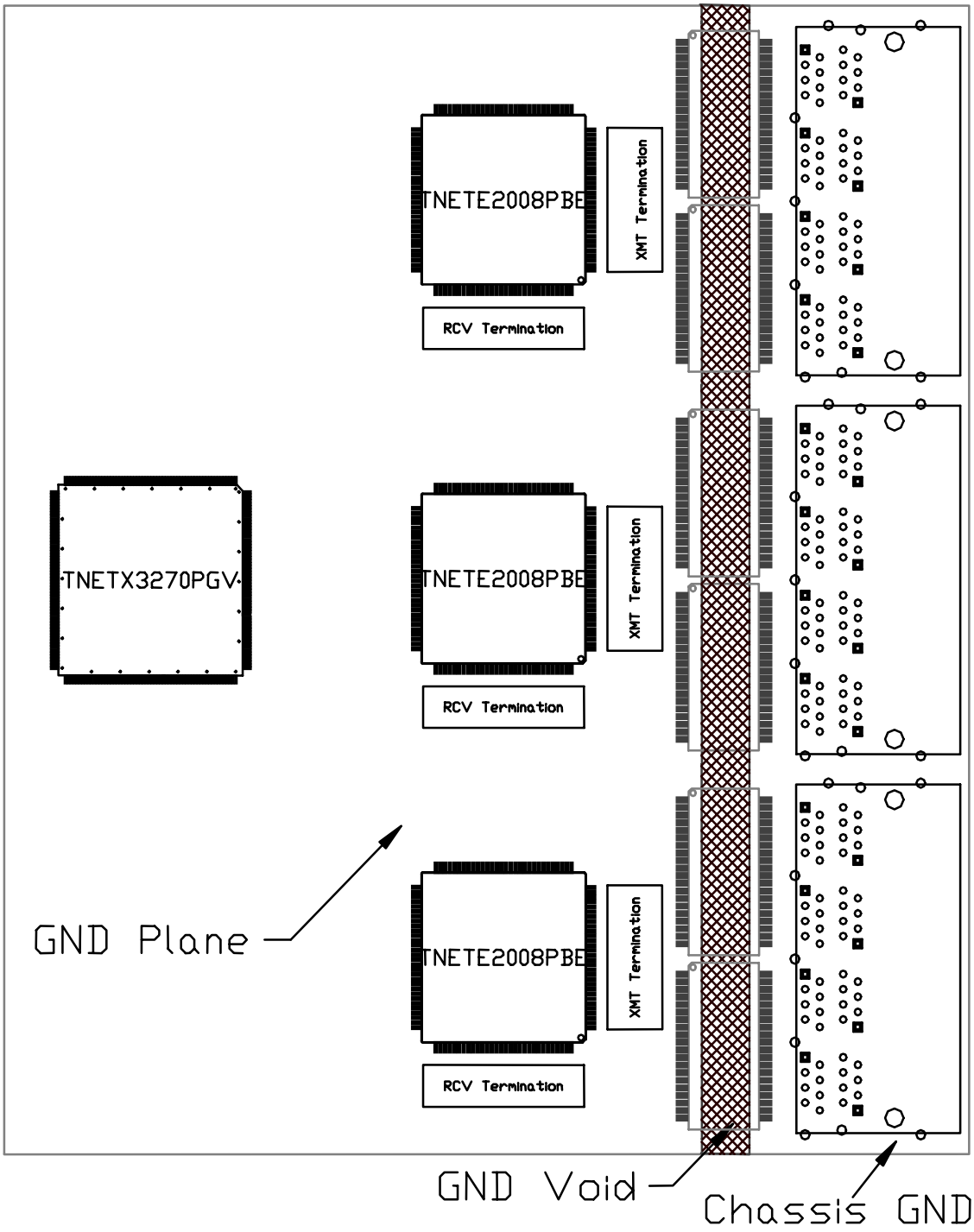


Figure 2. Recommended VDD Plane Layout

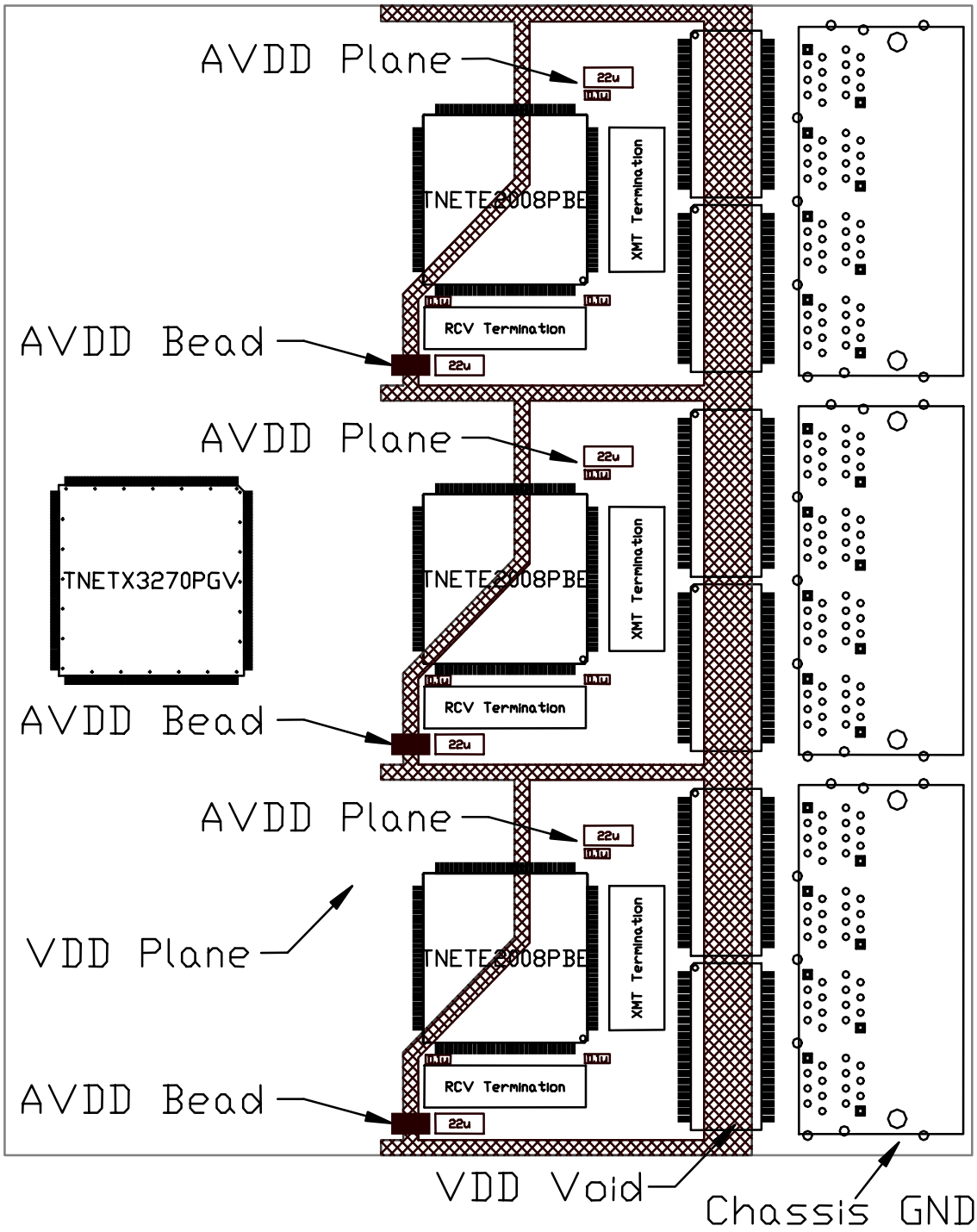


Figure 3. First Signal Layer for Four Layer Board

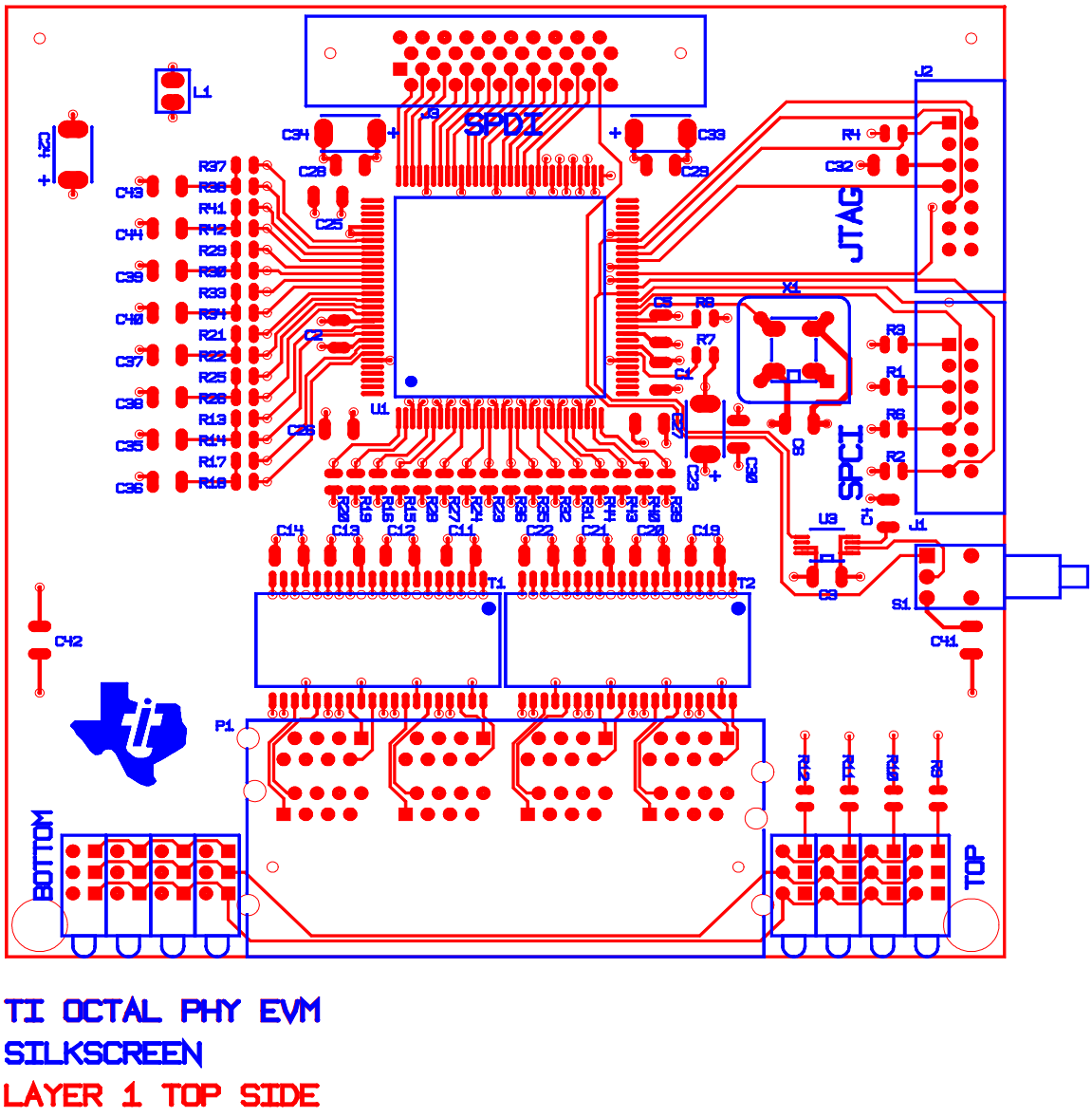


Figure 4. Ground Layer for Four Layer Board

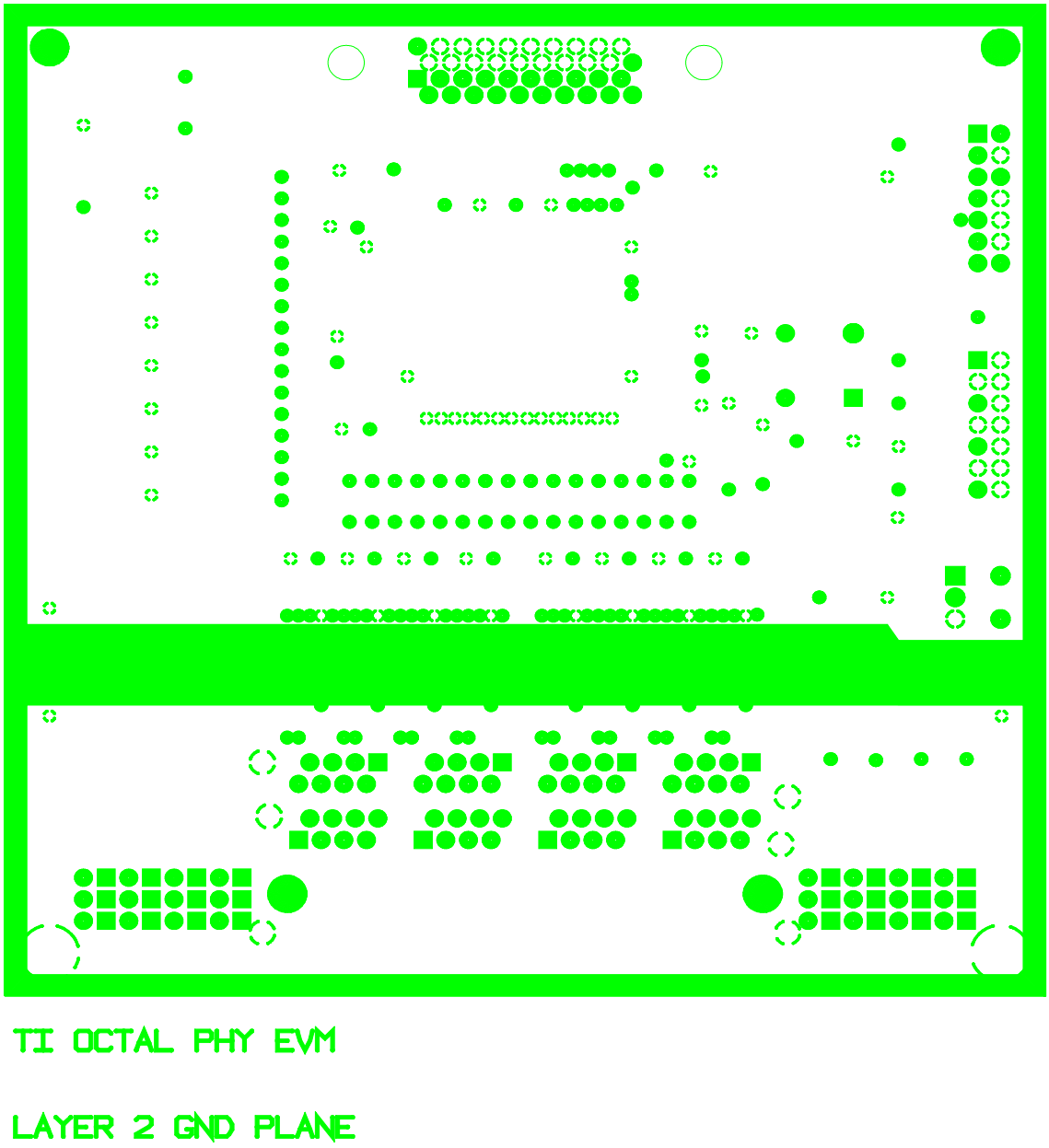


Figure 5. Power Layer for Four Layer Board

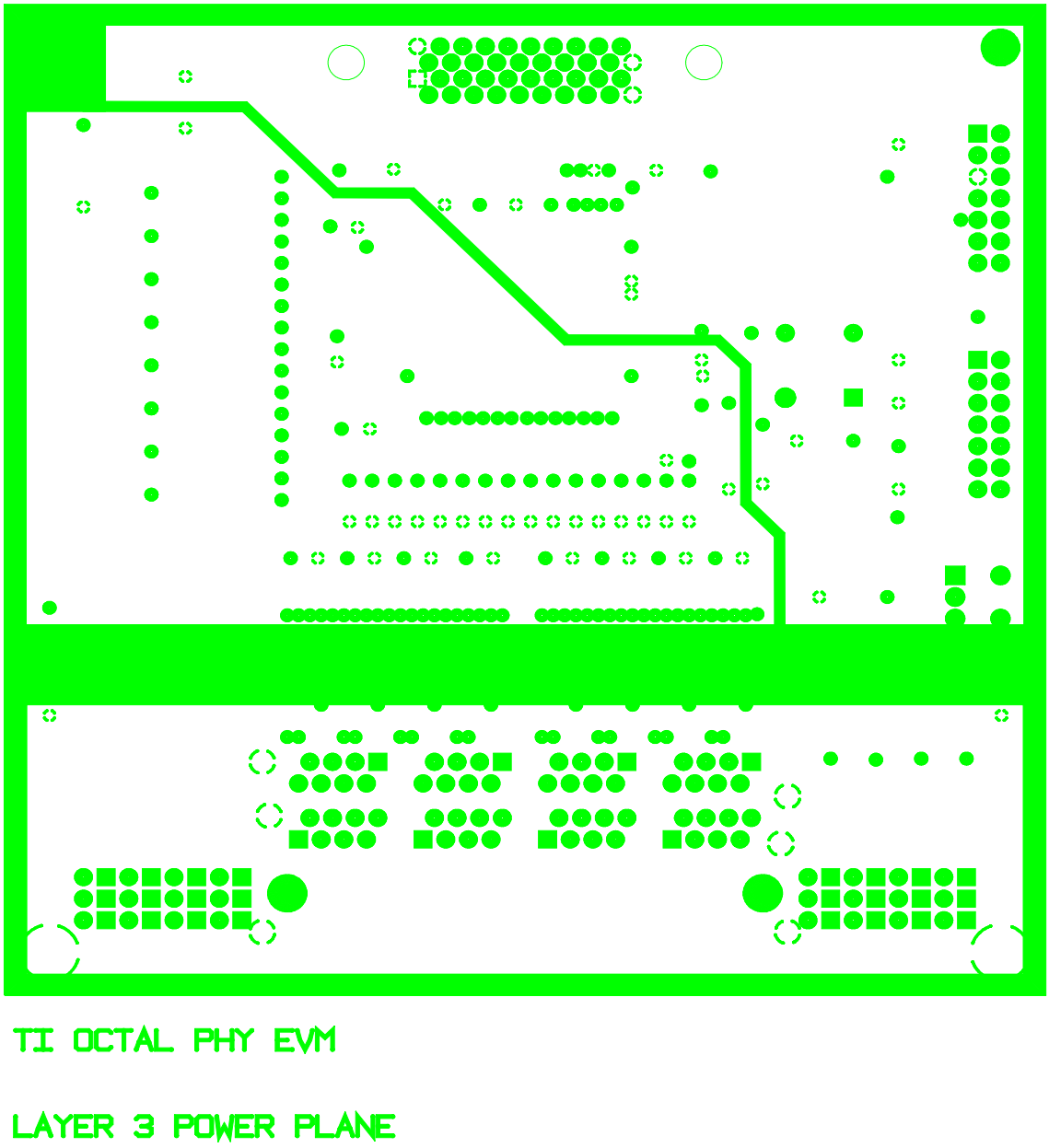


Figure 6. Second Signal Layer for Four Layer Board

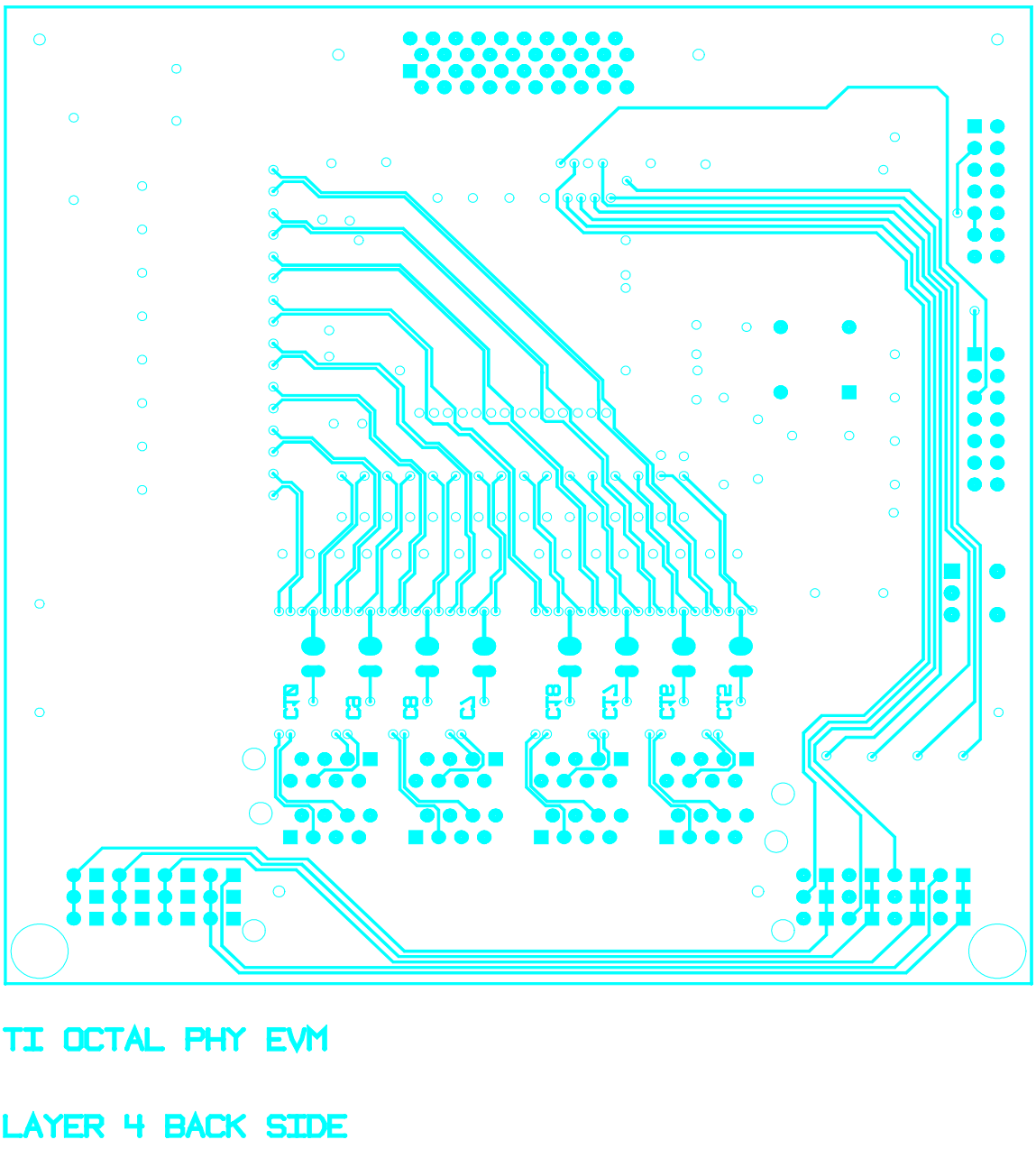


Figure 7. Analog Power Connections

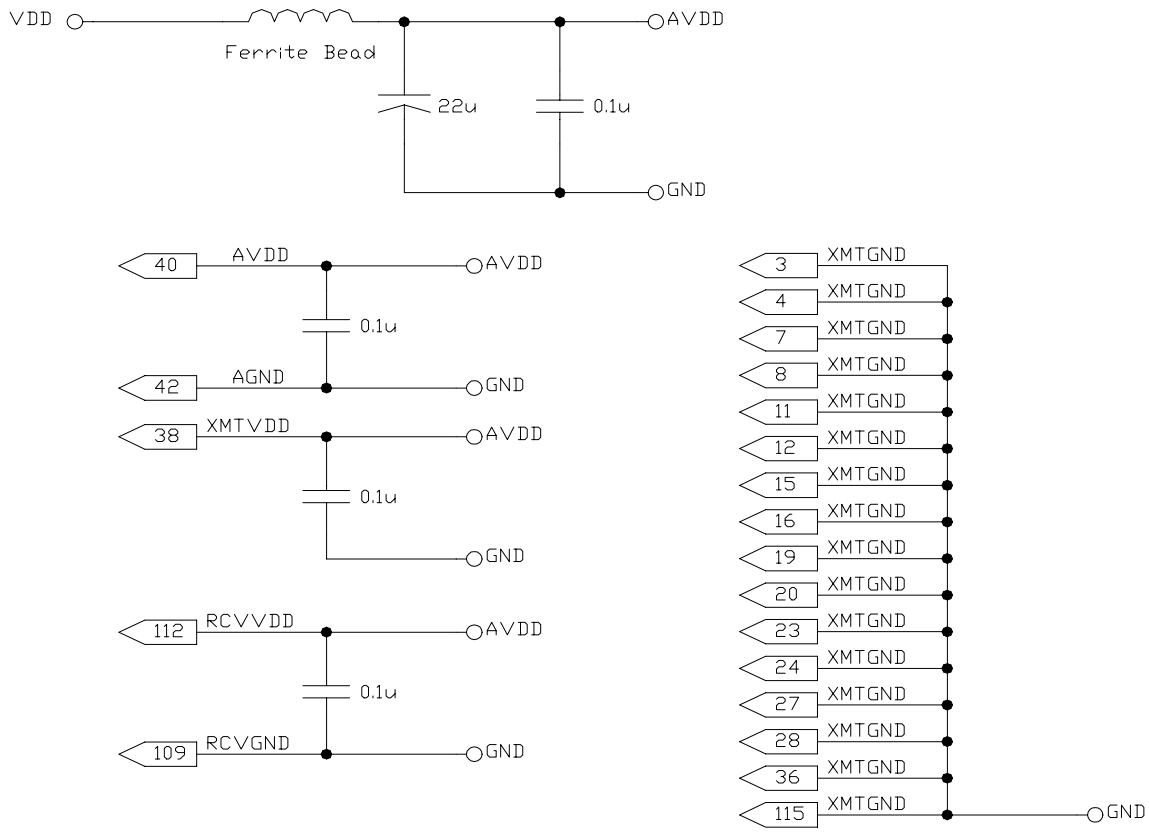
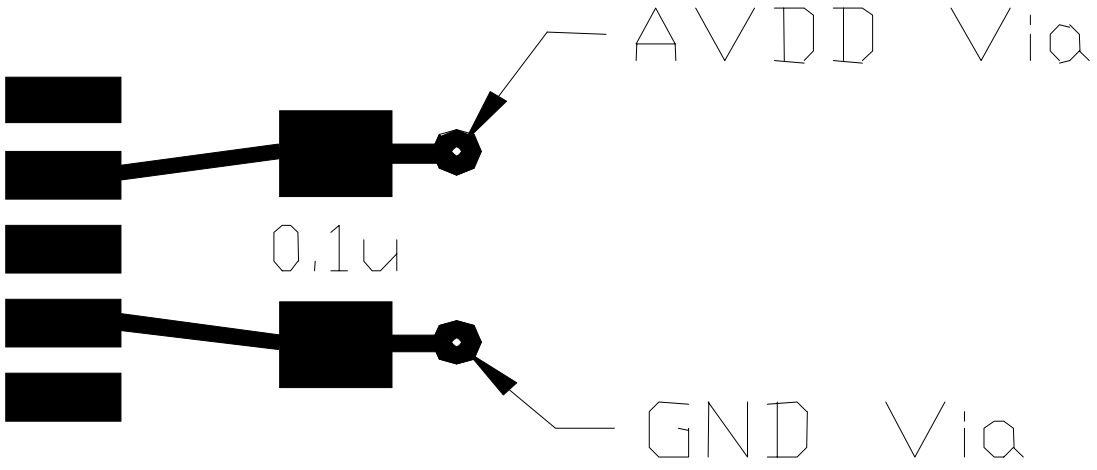


Figure 8. Analog Power Decoupling



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