Implementing the Spanning Tree Algorithm Using TNETX15VE and TNETX3150

APPLICATION REPORT: (SDNA010A)

Networking Business Unit May 1997



IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

Ab	ostrac	ct		7
1.	Intro	oductio	on	8
	1.1	Produ	ct Support	9
		1.1.1	Related Documentation	9
		1.1.2	World Wide Web Support	9
		1.1.3	Email Support	9
2.	Con	nfigurin	g the Network	10
		-	U Messages	
	2.2	Algorit	hm Operation	12
	2.3	Elimin	ating Packet Looping	13
		2.3.1	Configuring a LAN	
		2.3.2	Determining LAN Root Switch	
		2.3.3	Selecting Switch Root Ports	
		2.3.4	Defining Designated Switch	18
3.	Ass	igning	Port States	20
4.	TNE			
4.	TNE 4.1	ETX315	0 Hardware Requirements ed State	21
4.	4.1	TX315 Disabl	0 Hardware Requirements	21 21
4.	4.1	TX315 Disabl	0 Hardware Requirements ed State ng State	21 21 22
4.	4.1	TX315 Disabl Blocki	0 Hardware Requirements ed State ng State	21 21 22 22
4.	4.1	TX315 Disabl Blockii 4.2.1 4.2.2	0 Hardware Requirements ed State ng State Disable Learning	21 21 22 22 23
4.	4.1 4.2 4.3	TX315 Disabl Blockin 4.2.1 4.2.2 4.2.3 Listeni	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State	21 22 22 22 23 23 24 25
4.	4.1 4.2 4.3 4.4	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State ng State	21 22 22 23 23 24 25 25
4.	4.1 4.2 4.3 4.4 4.5	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni Forwa	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State rding State	21 22 22 22 23 23 24 25 25 25 26
4.	4.1 4.2 4.3 4.4	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni Forwa	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State ng State	21 22 22 22 23 23 24 25 25 25 26
4 .	4.1 4.2 4.3 4.4 4.5 4.6	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni Forwa Recon	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State ng State rding State figuring Ports Spanning Tree Algorithm in the Cascade Mode	21 22 22 23 23 24 25 25 26 26 27 28
	4.1 4.2 4.3 4.4 4.5 4.6 Usin 5.1	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni Forwa Recon	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State ng State rding State figuring Ports Spanning Tree Algorithm in the Cascade Mode	21 22 22 22 23 24 25 25 25 26 27 28 28
	4.1 4.2 4.3 4.4 4.5 4.6 Usin 5.1	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni Forwa Recon	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State ng State rding State figuring Ports Spanning Tree Algorithm in the Cascade Mode	21 22 22 22 23 24 25 25 25 26 27 28 28
	4.1 4.2 4.3 4.4 4.5 4.6 Usin 5.1 5.2	TX315 Disabl Blockii 4.2.1 4.2.2 4.2.3 Listeni Learni Forwa Recon ng the \$ Receiv Transr	0 Hardware Requirements ed State ng State Disable Learning Discard Received Frames Disable Frame Forwarding ing State ng State rding State figuring Ports Spanning Tree Algorithm in the Cascade Mode	21 22 22 23 23 24 25 25 25 26 27 28 28 29

Contents

Figures

Figure 1. Initial Power Up Configuration of the LAN	15
Figure 2. Configuring the LAN Root Switch	17
Figure 3. Loop Free Configuration for LAN	19
Figure 4. Simplified Development Platform Flat View	21
Figure 5. Development Platform Cascade Mode Configuration	28
Figure 6. Using VLANs to Determine Destination Port	29
Figure 7. Interfacing an Ethernet controller to a ThunderSWITCH 10 Mbit Port	32
Figure 8. Interfacing an Ethernet controller to a ThunderSWITCH 100 Mbit Port	32

Tables

Table 1.	Port States and Capabilities	20
Table 2.	TNETX15VE NLRNPorts Register, 0x04-0x05	22
Table 3.	TNETX15VE RxBlock Register, 0xF6-0xF7	23
Table 4.	TNETX15VE AddPort Register, 0x3E-0x3F	23
Table 5.	TNETX15VE TxBlock Register, 0xF4-0xF5	24
Table 6.	TNETX15VE Tx Routing Code Register, 0xF8	24
Table 7.	TNETX15VE Disable Learning Register, 0x04-0x05	25
Table 8.	TNETX15VE Receive Block (RxBlock) Register, 0xF6-0xF7	25
Table 9.	TNETX15VE Forward Block (TxBlock) Register, 0xF4-0xF5	26
Table 10	. TNETX15VE Learning Disable Register, 0x04-0x05	26
Table 11	. TNETX15VE Receive Block (RxBlock) Register, 0xF6-0xF7	26
Table 12	. TNETX15VE Forwarding Block (TxBlock) Register, 0xF4-0xF5	26
Table 13	. TNETX15VE DelPort Register, 0x4F	27
Table 14	. TNETX15VE AddPorts DIO Command, 0x3E-0x3F	30
Table 15	. TNETX15VE VLANmask Register, 0x50-0x57	31

Implementing the Spanning Tree Algorithm Using TNETX15VE and TNETX3150

Abstract

The Spanning Tree Algorithm is an intelligent algorithm that is used to eliminate packet looping in Local Area Networks (LAN). This document provides a detailed discussion of the Spanning Tree Algorithm. Topics include Configuration Bridge Protocol Data Unit (CBPDU) messages, requirements, operation, and port states; VLAN-Engine Address-Lookup Device (TNETX15VE) and ThunderSWITCH[™] (TNETX3150) configuration.

1. Introduction

The Spanning Tree Algorithm (IEEE 802.1D) is a program that resides in all managed network switches. It was developed by the IEEE standards body as a solution to packet looping. It configures the LAN by transmitting and evaluating the contents of Bridge Protocol Data Units (BPDU).

Initially, all switches broadcast BPDUs out all ports. The receiving switches then update the BPDUs and broadcast them. This process continues until all switches contain the same network configuration. The algorithm then assigns port functions and states to eliminate packet looping.

In a switch without the Spanning Tree Algorithm, the forwarding and learning process assumes the topology of the extended LAN is a tree, or there is only one path between any two nodes separated by a switch. When a switch receives a broadcast packet, it will automatically broadcast the packet to all its ports, except the port it received it on. In turn, the next receiving switch will forward the packet to all its ports, except the port it received the packet on. The packet may eventually be forwarded to the originating LAN segment. The switches will continue to forward the packet, thus creating an infinite loop. Packet looping continues until there is a break in the loop, such as a turned off switch. If loops exist (multiple paths), then packets may be duplicated or travel through the LAN endlessly. With potentially hundreds of nodes on a segment, packet looping will cause a network crash.

1.1

1.2 Product Support

1.2.1 Related Documentation

Following is a list of specific product names, part numbers, and their documentation's literature number.

- □ Configuring theTNETX3150 ThunderSWITCH for the Cascade Mode Application Report, Literature number SDNA009.
- □ *ThunderSWITCH (TNETX3150) Data Sheet*, Literature number SPWS027C.
- □ *VLAN-Engine Address-Lookup Device (TNETX15VE) Data Sheet*, Literature number SPWS028.
- Desktop ThunderSWITCH (TNETX3100) 10-PORT 10-/100-MBIT/S ETHERNET SWITCH Data Sheet, Literature number SPWS031.
- □ ISO/IEC 10038 [ANSI/IEEE Std. 802.1D] for Media access control (MAC) bridges

1.2.2 World Wide Web Support

Our world wide web site at **www.ti.com**. contains the most up to date product information, revisions, and additions. New users must register with TI&ME before they can access the data sheet archive. TI&ME allows users to build custom information pages and receive automatic new product updates via email.

1.2.3 Email Support

For technical issues or clarification on switching products, please send a detailed email to **networks@ti.com**. Questions receive prompt attention and are usually answered within one business day.

2. Configuring the Network

The Spanning Tree Algorithm resides in all LAN switches. At power up or reset, the algorithm broadcasts CBPDU messages out all switch ports. The algorithm uses the contents of received CBPDU messages to configure the LAN switches. The algorithm continues to run as long as the switch is powered up.

2.1 CBPDU Messages

At power up, the Spanning Tree Algorithm assumes it is the root switch. The Spanning Tree Algorithm then transmits CBPDU messages out all its ports to the unique Spanning Tree Algorithm destination address . The CBPDU messages contain the following switch information:

- Unique Spanning Tree Algorithm destination address (01-80-C2-00-00-10 h)
- Switch identifier
- □ Switch priority
- Port number
- Path cost
- D Port identifier

Each switch must recognize the unique Spanning Tree Algorithm destination address (all bridges multicast address). This unique destination address is used to communicate spanning tree packets between switches.

The switch identifier is determined by the combination of the switch MAC address and a two byte switch priority field. The MAC address is assigned by the company that designed the switch.

The switch priority field is assigned by the network administrator. If two switches have the same switch priority, then the lower MAC address is used to determine the root switch.

Port numbers are assigned by the Spanning Tree Algorithm. The lower the port speed, the lower the port priority.

Path cost is computed by the Spanning Tree Algorithm. The path cost is determined by the number of switches the CBPDU has to travel through to reach the root switch. The closer the switch is to the root switch, the lower the path cost.

The port identifier is comprised of the port number and the port priority. Each port is assigned a unique port identifier.

2.2

2.3 Algorithm Operation

The algorithm uses the unique Spanning Tree Algorithm destination address, switch priority, switch identifier, port priority, path cost, and port identifier to configure the network. The algorithm operates in the following manner.

- 1) The LAN root switch/bridge is selected.
- 2) Switch root ports are selected.
- 3) A designated switch path to the root for each segment in the LAN is selected.
- 4) Root ports and designated switches are enabled.

First, while all ports are blocking normal traffic, a root switch is determined. The algorithm selects the switch with the highest switch priority as the root switch. If the switch priorities are equal, then the switch with the lowest switch identifier (MAC address plus priority field) is chosen to be the root switch.

Next, the algorithm selects a root port for each switch, except for the root switch. The root port is the port with the lowest path cost to the root switch.

The algorithm then selects a designated switch for each LAN segment. The designated switch incurs the lowest path cost when forwarding traffic from that LAN segment to the root switch. A port of the designated switch is then selected. This port is referred to as the designated port and is used by the designated switch to connect to the LAN.

Finally, the algorithm places all root ports and designated ports in the forwarding state. The remaining ports are placed in the blocking state.

2.4

2.5 Eliminating Packet Looping

The Spanning Tree Algorithm evaluates and configures the LAN to eliminate packet looping. The Spanning Tree Algorithm resides in all managed LAN switches.

2.5.1 Configuring a LAN

At power-up or reset, the algorithm begins to broadcast Configuration switch Protocol Data Unit (CBPDU) messages out of all switch ports.

When a switch receives a superior CBPDU that contains a higher switch priority, lower path cost, or higher port priority, it stores the CBPDU information including the port it was received on. If the CBPDU is received at the port that the switch recognizes as the root port, the switch transmits an updated CBPDU to all the LANs for which it recognizes as the designated switch.

When a switch receives a inferior CBPDU at a port it considers to be a designated port, it transmits its own information to the attached LANs.

The algorithm uses the information contained in the CBPDUs to determine its position in the network and the configuration of the LAN.

2.5.1.1 Example Spanning Tree Algorithm Sequence of Events

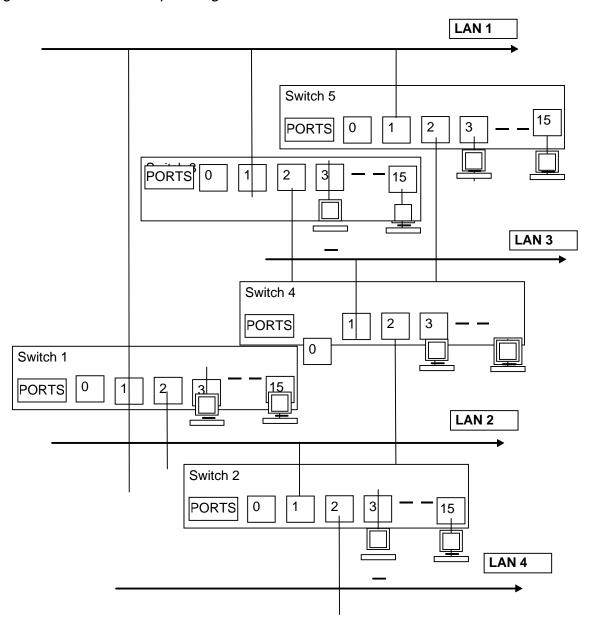
The following is a simplified sequence of events when configuring a LAN. Figure 1 shows the configuration of a typical LAN before running the Spanning Tree Algorithm.

- 1) Switch 1 broadcasts CBPDU messages from all ports.
- 2) Switches 2, 3, 4, and 5 receive CBPDU messages.
- 3) The receiving switches note the port that the CBPDUs were received on, then analyze and store the CBPDU contents.
- 4) The receiving switches update the CBPDU contents with their own routing information and broadcast the updated CBPDUs out of all their ports, except the port the original CBPDU was received on.
- 5) The CBPDU is updated as it passes from switch to switch, creating a routing record that travels with the CBPDU.
- Each switch updates and broadcasts all CBPDU messages received, unless it receives a CBPDU that it originated. In this case the CBPDU information is recorded, but not broadcast.

7) Ultimately each switch contains the network configuration.

The Spanning Tree Algorithm configures the LAN in 30 seconds or less. The algorithm configures the LAN by selecting a LAN root switch, switch root ports, a dedicated switch for each LAN segment, and assigns port states (see Figure 3).

Figure 1. Initial Power Up Configuration of the LAN



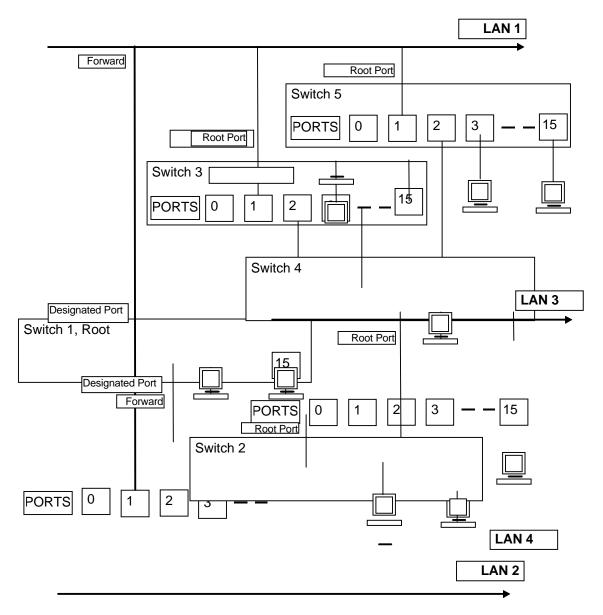
2.5.2 Determining LAN Root Switch

After exchanging CBPDUs, all switches contain the same information. The algorithm then evaluates the CBPDU data to determine the LAN root switch.

Switch 1 has the lowest switch ID and switch 5 has the highest switch ID. All the switches have the same priority, and all the ports have the same priority and path cost (see Figure 2). Because switch 1 has the lowest switch ID and all other factors are the same, switch 1 is selected as the root switch. Since the root switch is the designated switch for all LANs to which it is attached, switch 1 is also the designated switch for LANs 1 and 2.

The algorithm places all the root switch ports in the forwarding state. Topology messages originate from all ports of the root switch, they are received by the root port on each designated switch, and are propagated out the designated port for other switches.

Figure 2. Configuring the LAN Root Switch



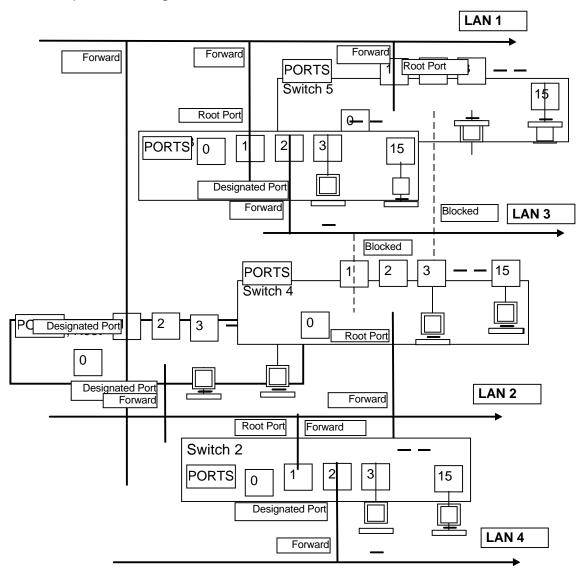
2.5.3 Selecting Switch Root Ports

2.5.4 Defining Designated Switch

The Spanning Tree Algorithm requires that each LAN has a designated switch. If a LAN is attached to a single switch, then by default, that switch becomes the designated switch. Because (see Figure 3) switch 2 is the only switch attached to LAN 4 it is, by default, the designated switch for LAN 4. All the ports on switch 2 that go directly to desktop PCs (or shared hubs with no switches) are treated the same. Since switch 2 is the only switch connected to these single port LAN segments, it becomes the designated switch for these desktop PCs. Its ports will be put into the forwarding state as per normal Spanning Tree Algorithm operation.

A designated switch, for LANs attached to more than one switch, must be selected. In Figure 3, LAN 3 is attached to switch 3, switch 4 and switch 5, the algorithm compares the path cost of these switches to the root. In this case, the path costs are the same. Since switch 3 has the lowest switch ID, switch 3 is selected as the designated switch for LAN 3. Since switch 3 is connected to LAN 3 via port 2, port 2 becomes the designated port for LAN 3 and is placed in the forwarding state. The algorithm then places switch 5, port 2 and switch 4, port 1 in the blocked state.

Figure 3. Loop Free Configuration for LAN



3. Assigning Port States

The Spanning Tree Algorithm evaluates CBPDU messages and assigns port states to eliminate packet looping. The algorithm configures the port states by writing to the VLAN Engine Address Lookup Device and ThunderSWITCH internal registers. The five port states are:

- Disabled
- Blocking
- Listening
- □ Learning
- □ Forwarding

The port states and their capabilities are listed in Table 1. Only root ports and designated ports are put into the forwarding state. Other ports, such as port 1 of switch 4 and port 2 of switch 5 are put into blocking state as shown in Figure 3.

When a port is in the forwarding state, it performs learning, filtering, and forwarding functions. When in the blocking state, it performs none of these functions. Thus by putting some ports in forwarding, and others in blocking state, the Spanning Tree Algorithm prevents packet looping on the LAN.

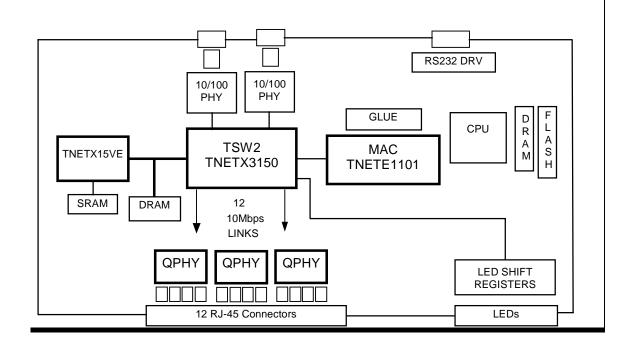
Table 1. Port States and Capabilities

Port States	Enable Learning	Enable Frame Forwarding	Forward Received Frames	Receive BPDUs	Enable Filtering	Forward BPDUs
Disabled	No	No	No	No	No	No
Blocking	No	No	No	Yes	No	Yes
Listening	No	No	No	Yes	No	Yes
Learning	Yes	No	No	Yes	No	Yes
Forwarding	Yes	Yes	Yes	Yes	Yes	Yes

4. TNETX3150 Hardware Requirements

As shown in Figure 4, to support Spanning Tree, an external MAC device such as the ThunderLAN[™] (TNETE1101) is required to receive the BPDUs. The onboard CPU runs the Spanning Tree Algorithm.





4.1 Disabled State

A port can be disabled by the Spanning Tree Algorithm or the network administrator. A disabled port is ignored by the Spanning Tree Algorithm and protocol.

All ThunderSWITCH ports can be disabled by writing a 1 to its port control register bit-7. The Spanning Tree Algorithm will then go into the disabled state for that port. When a ThunderSWITCH port is disabled, it ignores received frames and frames destined for the port. Since no frames will be received by this port, the TNETX15VE will not be able to learn any addresses on this port.

4.2

4.3 Blocking State

At start-up, all ports are placed in the blocking state. The Spanning Tree Algorithm then determines if they should go to the forwarding state. A port in the blocking state is ignored by the algorithm and protocol in the computation of the active topology.

This state is entered following initialization of the switch or after the network administrator enables the port after it has been disabled. The blocking state may also be entered from the listening, learning, or forwarding states through the operation of the spanning tree protocol. In the blocking state the ports capabilities to enable learning, enable frame forwarding, forward received frames, enable filtering, and forwarding BPDUs are all disabled.

To enter the blocking state in the Spanning Tree Algorithm from the disabled state:

- 1) Write a 1 to that port's bit, in the TNETX15VE NLRNPorts register at DIO address 0x4-0x5, to disable learning.
- Write a 1 to that port's bit, in the TNETX15VE RxBlock register at DIO address 0xF6-0xF7, to disable forwarding received frames. These frames are then discarded.
- 3) Write a 1 to that port's bit, in the TNETX15VE TxBlock register at DIO address 0xF4-0xF5, to disable frame forwarding to ports in the blocking state. These frames are then discarded.
- 4) Write a 1 to the TNETX3150 port control register enable bit 6.

4.3.1 Disable Learning

To disable learning of addresses for a port in the blocking state, use the TNETX15VE Learning Disable (NLRNPorts) register, located at DIO address 0x04-05. This register contains a bit map for the ports that corresponds with the TNETX3150 ports. To disable learning of addresses for any port write a 1 to the bit position that corresponds with the port. Table 2 shows the register set to disable learning on all 15 ports.

Reserved Bit 15	NLRNPorts Bits 14 - 0
0	111 1111 1111 1111

4.3.2

4.3.3 Discard Received Frames

To discard received frames on a port in the blocking state, use the TNETX15VE Receive Block (RxBlock) register, located at DIO address 0xF6-0xF7. The RxBlock register contains a bit map that corresponds with the TNETX3150 ports. Received frames can be discarded for any port by writing a 1 to the bit position that corresponds with the port number. Table 3 shows the RxBlock register set to discard all packets received.

To receive BPDUs in the blocking state, program the unique Spanning Tree Algorithm destination address (all bridges multicast address) into the TNETX15VE lookup table, with an add operation, and set the NBLCK bit to 1 for this address. This allows the port to receive any frames with this destination address. To prevent receiving other frames while in this state, the NBLCK bits must be set to 0 for other addresses that maybe associated with this port.

When an address's NBLCK bit is set, another feature is activated. This feature copies the source address, and source port to the TNETX15VE internal NBLCK Rx FIFO. The Find command can then be used to read the source MAC address and the TNETX3150 source port that received the packet.

The TNETX15VE AddPort register is shown in Table 4. The NBLCK bit is set, hence packets destined to this address will be forwarded even if the RxBlock bit is set on the receiving port. The destination port is determined from the Portflag, in this case the destination is TNETX3150 port 14.

Table 3. TNETX15VE RxBlock Register, 0xF6-0xF7

RES Bit 15	RxBlock Bits 14-0
0	111 1111 1111 1111

Table 4. TNETX15VE AddPort Register, 0x3E-0x3F

NBLCK Bit 15	Portflag Bits 14-0
1	100 0000 0000 0000

4.3.4

4.3.5 Disable Frame Forwarding

To disable forwarding frames destined to a port in the blocking state, use the TNETX15VE Packet Forwarding/Block (TxBlock) register, located at DIO address 0xF4-F5h. The TxBlock register contains a bit map that corresponds to the TNETX3150 ports. Frames destined for these ports can be blocked by writing a 1 to the bit position that corresponds with the port number.

The register example in Table 5 shows that frame forwarding is disabled for all ports,.

Table 5. TNETX15VE TxBlock Register, 0xF4-0xF5

RES Bit 15	TxBlock Bits 14-0	
0	111 1111 1111 1111	

The Spanning Tree Bridge Protocol Data Units (BPDU) can be forwarded through a TxBlocked port by using the TNETX15VE 8-bit Tx Routing Code (CPU_Tx) register, (see Table 6) located at DIO address 0xF8h. The 4 MSBs indicate the local port for the CPU. The 4 LSBs, the Tx Routing Code, indicates the destination port. The Tx Routing Code is used to forward BPDU messages from the CPU. The Tx Routing Code register configuration shown in Table 6 attaches the CPU to TNETX3150 port 14. The Tx Routing Code is used by TNETX15VE to forward BPDUs from the CPU out on the specified port, in this case port 2, even if the port's TxBlock bit is set.

The Tx Routing Code is a one packet bypass, it is reset for each packet. that must travel around the TxBlock blocking mechanism.

Table 6. TNETX15VE Tx Routing Code Register, 0xF8

CPU Port Bits 7- 4	Tx Routing Code Bits 3-0
1110	0010

4.4

4.5 Listening State

This state is entered from the blocking state when the Spanning Tree Algorithm and spanning tree protocol determine that the port can take part in frame relay. A port in this state is preparing to take part in the frame relay process, but frame relay is temporarily disabled to prevent looping.

In terms of the TNETX15VE and TNETX3150 configuration, the listening state is identical to the blocking state. In the Spanning Tree Algorithm, this state is entered when it's determined that this port should take part in frame relay.

To prevent packet looping in the listening state, learning MAC addresses, forwarding processes, and frame reception must be disabled. The NLRNPorts, forwarding block (TxBlock) bits, and receive block (RxBlock) bits in the TNETX15VE registers respectively, are used to disable these functions.

4.6 Learning State

This state is entered from the listening state through the operation of the Spanning Tree Algorithm and spanning tree protocol, upon the expiry of a protocol timer (see the IEEE 802.1D standard for recommended timer values). A port in this state is preparing to take part in the frame relay process, but frame relay is temporarily disabled to prevent looping.

In the learning state, the port's MAC address learning function is enabled by the TNETX15VE disable learning register. The appropriate NLRNPorts bit is set to 0 to enable learning. The example shown in Table 7 enables learning on all ports except port 3, which is blocked.

Table 7. TNETX15VE Disable Learning Register, 0x04-0x05

RES Bit 15	NLRNPorts Bits 14-0
0	000 0000 0000 1000

To prevent packet looping in the learning state, disable port frame reception and forwarding with the Receive Blocking (RxBlock) and Forward Blocking (TxBlock) TNETX15VE registers (see Tables 8 and 9).

Table 8. TNETX15VE Receive Block (RxBlock) Register, 0xF6-0xF7

RES Bit 15	RxBlock Bits 14-0
0	111 1111 1111 1111

Table 9. TNETX1	5VE Forward Block	: (TxBlock) Red	lister. 0xF4-0xF5
-----------------	-------------------	-----------------	-------------------

RES Bit 15	TxBlock Bits 14-0
0	111 1111 1111 1111

4.7 Forwarding State

This state is entered from the Learning State through the operation of the Spanning Tree Algorithm and Spanning Tree Protocol, on the expiry of a protocol timer (see the IEEE 802.1D standard for recommended timer values).

A port in the forwarding state takes part in normal frame relay. Learning remains enabled in the forwarding state (see Table 10).

Table 10. TNETX15VE Learning Disable Register, 0x04-0x05

RES Bit 15	NLRNPorts Bits 14-0
0	000 0000 0000 1000

The MAC address learning function remains enabled as per the Learning State. Frame forwarding and reception is enabled for each port by setting the corresponding port bit to 0 in the Receive Block (RxBlock) and Forwarding Block (TxBlock) registers, respectively. Table 11 shows receive block enabled for all ports except port 3. Port 3 is set to 1, or blocked. Table 12 shows forwarding block enabled for all ports except port 3.

Table 11. TNETX15VE Receive Block (RxBlock) Register, 0xF6-0xF7

RES Bit 15	RxBlock Bits 14-0
0	000 0000 0000 1000

Table 12. TNETX15VE Forwarding Block (TxBlock) Register, 0xF4-0xF5

RES Bit 15	TxBlock Bits 14-0
0	000 0000 0000 1000

4.8 Reconfiguring Ports

When a topology change occurs in the LAN, the forwarding database for some ports is purged. The TNETX15VE provides a DelPort (delete port) feature which can be used to delete all addresses on a particular port. The DelPort register (see Table 13) is located at DIO address 0x4F. The DelPort register specifies the port that will have its addresses deleted when the DELP bit (bit 3) in the adddelcontrol register, 0x2C, is set.

NOTE:

This does not delete multicast addresses that include this port or secured unicast address on this port.

Table 13. TNETX15VE DelPort Register, 0x4F

Reserved Bits 7-4	DelPort Bits 3-0
0000	0000

5. Using the Spanning Tree Algorithm in the Cascade Mode

To increase port density, two TNETX3150 devices can be used in cascade mode (see *Configuring the TNETX3150 ThunderSWITCH for the Cascade Mode* Application Report, Literature number SDNA009). In this mode, there are some special considerations that must be addressed before implementing the Spanning Tree Algorithm (see Figure 5).

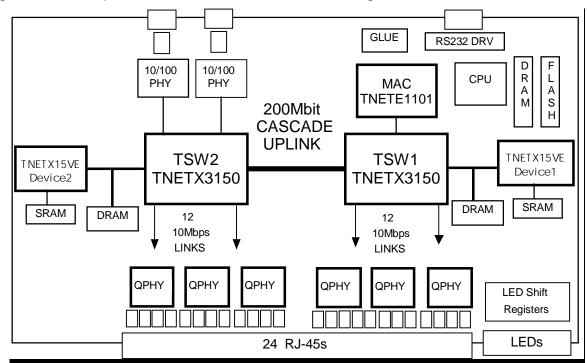


Figure 5. Development Platform Cascade Mode Configuration

5.1 Receiving BPDUs

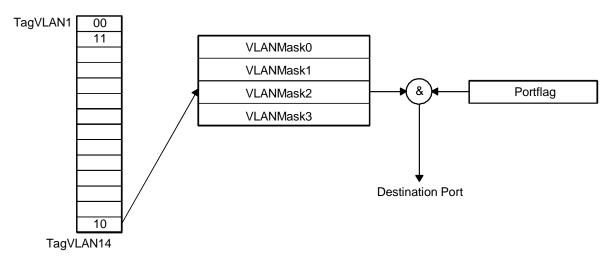
In the cascade configuration the TNETX15VE Device 2s lookup table should be programmed with the Spanning Tree Multicast MAC address, and the Portflag set to direct all BPDUs to port 0, the cascade port. This forwards BPDUs that are received on TNETX3150 TSW2 ports to TNETX3150 TSW1. The TNETX15VE Device1 will then direct the BPDU packet to the local MAC device. This will allow the CPU to process the BPDU as per the Spanning Tree Algorithm.

5.2 Transmitting BPDUs

To transmit BPDUs to ports connected to TNETX3150 TSW1, the CPU Port and Tx Routing Code are used as previously described. However, it is not possible to use this feature to transmit BPDUs to the ports on TNETX3150 TSW2 since the destination port information cannot be provided by the cascade interface. To get around this problem, reserve one of the four TNETX15VE VLAN registers.

The TNETX3150 supports packet pre-tagging on the cascade port to indicate the source port for the packet. When transmitting a BPDU from the CPU, the TX Routing Code can be used to direct the packet to the cascade port. The packet will be pre-tagged by the TNETX3150 to indicate that the source port was Port 14 (this is the port that the MAC is connected to). Then the TNETX15VE Device 2 can use the pre-tag as an offset into the TagVLAN array registers (see Figure 6).

Figure 6. Using VLANs to Determine Destination Port



The TagVLAN array for Port 14 will indicate which VLAN ID is associated with this port, and which VLANMask should be used to determine the destination port. The Portflag associated with the Spanning Tree MAC address can be programmed to all 1s (see Table 14). In this case, the bit mask in VLANMask will determine the destination port. The CPU has to modify Devices 2's VLANMask to select a different destination port, before the packet is launched.

NBLCK Bit 15	VLANflag Bits 14-0
1	111 1111 1111 1111

The TNETX15VE contains four VLANmask registers, located at 0x50h-0x54h. These registers determine which ports belong to which VLAN (see Table 15).

Table 15. TNETX15VE VLANmask Register, 0x50-0x57

RES Bit 15	VLANMask 2 Bits 14-0
0	100 0000 0000 0000

6. MAC Interface Schematics

Figure 7 contains a block diagram showing the connections needed to interface an Ethernet controller to a ThunderSWITCH 10 Mbit port.

Figure 7. Interfacing an Ethernet controller to a ThunderSWITCH 10 Mbit Port

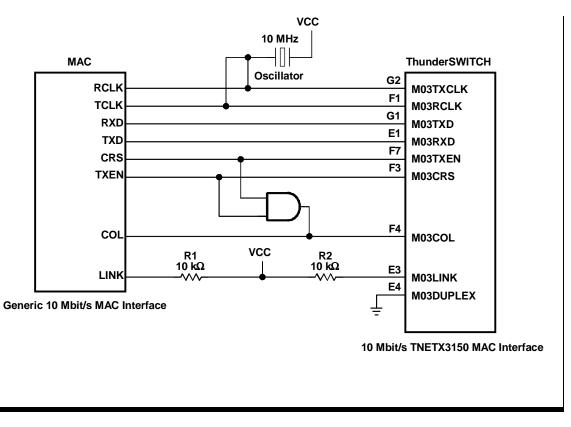
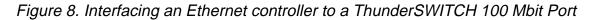
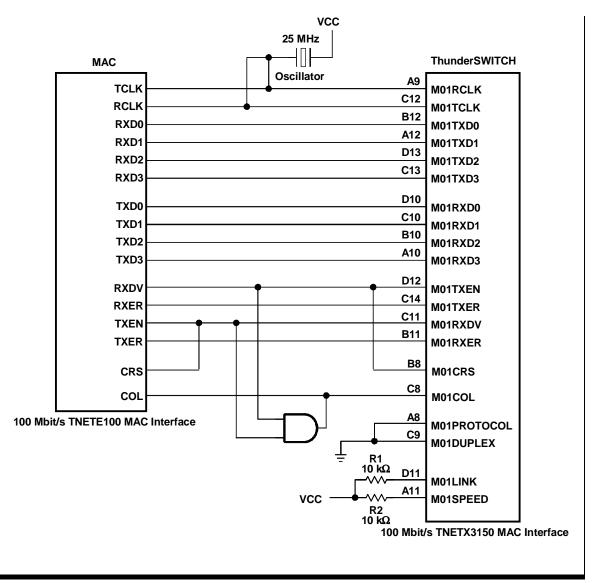


Figure 8 contains a block diagram showing the connections needed to interface an Ethernet controller to a ThunderSWITCH 100 Mbit port.





7. Terms

BPDU (Bridge Protocol Data Units)

	Message the spanning Tree Algorithm uses to communicate information between switches.
Broadcast	
Diououst	Data packet that will be sent to all nodes on a network. Broadcasts are identified by a broadcast address.
Broadcast address	
	Special address reserved for sending a message to all stations. Generally, a broadcast address is a MAC destination address of all ones.
Designated Port	
	The designated port is the port on a designated switch that is attached to the LAN segment for which that switch is the designated switch.
Designated Switch	
Designated Switch	This is a switch that is attached to each LAN segment in the network with the lowest path cost to the root switch. If all the switches attached to the LAN segment have the same path cost, then the switch with the lowest switch identifier becomes the designated switch. The designated switch communicates network topology information to all the other switches that are connected to the same physical LAN via the designated port.
Destination address	
	Address of a network device that is receiving data.
Frame	
	Logical grouping of information sent as a data link layer unit over a transmission medium. Often refers to the header and trailer, used for synchronization and error control, that surround the user data contained in the unit. The terms datagram, message, packet, and segment are also used to describe logical information groupings at various layers of the OSI reference model and in various technology circles.
Full duplex	
	Capability for simultaneous data transmission between a sending station and a receiving station.
Half duplex	
	Capability for data transmission in only one direction at a time between a sending station and a receiving station.

LAN	Least area patwork. Link aread low array data patwork asympton
	Local-area network. High-speed, low-error data network covering a relatively small geographic area (up to a few thousand meters). LANs connect workstations, peripherals, terminals, and other devices in a single building or other geographically limited areas.
MAC address	
	Standardized data link layer address that is required for every port or device that connects to a LAN. Other devices in the network use these addresses to locate specific ports in the network and to create and update routing tables and data structures. MAC addresses are 6 bytes long and are defined by the IEEE. They are assigned by the company that designs the switch.
Multicast	Single packets copied by the network and sent to a specific subset
	of network addresses. These addresses are specified in the destination address field.
Packet	
	Logical grouping of information that includes a header containing control information and (usually) user data. Packets are most often used to refer to network layer units of data. The terms datagram, frame, message, and segment are also used to describe logical information groupings at various layers of the OSI reference model and in various technology circles.
Path Cost	The path east is determined by the number of switches the CRDNI
	The path cost is determined by the number of switches the CBPDU travels through to reach the root switch. The closer the switch to the root switch, the lower the path cost. Path cost is computed by the Spanning Tree Algorithm. The computation is based on information provided in the BPDU messages received from the root switch.
Port Identifier	
	This is a unique number that is fixed in software as part of the spanning tree in each switch. It is used to identify the switch port. It consists of an adjustable priority field and a fixed port number.
Port States	
	Blocking and Forwarding are two steady states that are possible on each port of a switch. Forwarding means the switch has the ability to forward packets out of the port, and blocking means any packet will be blocked.
Root Switch	This is the switch with the lowest switch identifier. All parts on the
	This is the switch with the lowest switch identifier. All ports on the root switch are in the forwarding state. Topology messages originate from all ports of the root switch, they are received by the root port on each designated switch, and are propagated out the designated port for other switches.

RMON	Remote Monitoring. MIB agent specification described in RFC 1271 that defines functions for the remote monitoring of networked devices. The RMON specification provides numerous monitoring, problem detection, and reporting capabilities.
Root Port	
	The Spanning Tree Algorithm selects a root port for each switch, except for the root switch. The root port is the port with the lowest path cost to the root switch.
SNMP	
	Simple Network Management Protocol. Network management protocol used almost exclusively in TCP/IP networks. SNMP provides a means to monitor and control network devices, and to manage configurations, statistics collection, performance, and security.
Spanning-Tree Protocol	
	Bridge protocol that utilizes the spanning-tree algorithm, enabling a learning bridge to dynamically work around loops in a network topology by creating a spanning tree. Bridges exchange BPDU messages with other bridges to detect loops, and then remove the loops by shutting down selected bridge interfaces. Refers to both the IEEE 802.1 Spanning-Tree Protocol standard and the earlier Digital Equipment Corporation Spanning-Tree Protocol upon which it is based. The IEEE version supports bridge domains and allows the bridge to construct a loop-free topology across an LAN. The IEEE version is generally preferred over the Digital version. Sometimes abbreviated STP.
Switch Identifier	
	The switch identifier is determined by the combination of switch MAC address and a two byte priority, field that is assigned by the network administrator. The priority field is used to determine the root switch. If two switches have the same priority, then the lower MAC address is used to determine the root switch.
Unicast	
	Message sent to a single network destination.
VLAN	Virtual Local Area Network. Group of devices on a LAN that are configured (using management software) so that they can communicate as if they were attached to the same wire, when in fact they are located on a number of different LAN segments. Because VLANs are based on logical instead of physical connections, they are extremely flexible.