TC237
Timing of Frame Transfer CCD Image Sensor

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Abstract

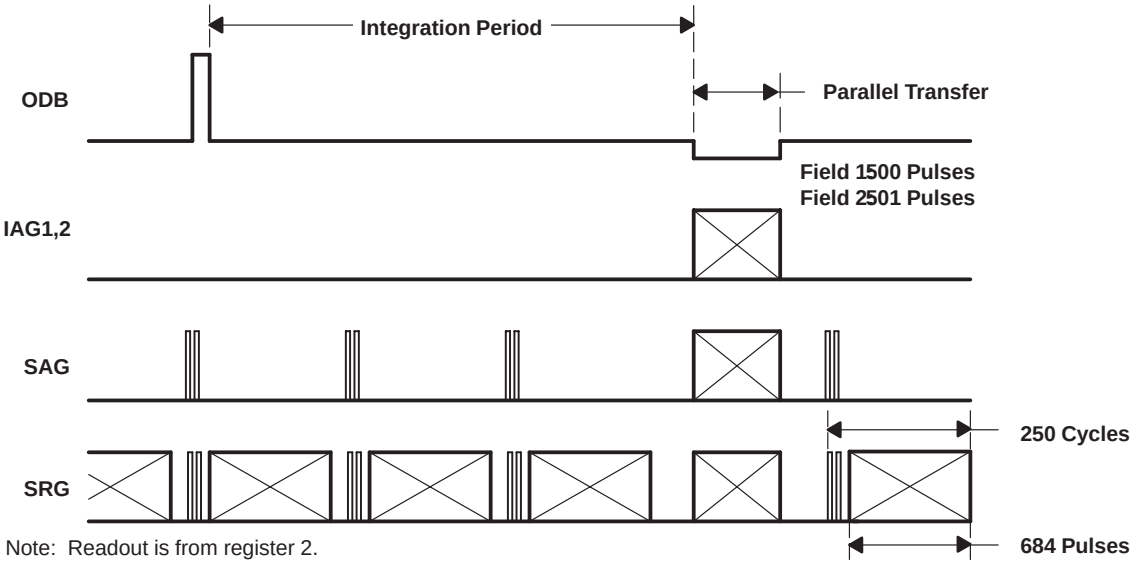
This application report describes timing design for Texas Instruments (TI™) frame transfer charge coupled device (CCD) image sensors using the TC237 CCD image sensor. This report explains timing in the integration period, the parallel transfer period, and the readout period. The timing design for the EIA RS-170 standard described here used the TC237 frame transfer CCD image sensor in a prototype EIA RS-170 camera. The scope pictures were taken with a Tektronix™ C-30 series camera on a Tektronix 2467B 400 MHz scope with a TEK™ P6137 10X probe. The probe was grounded using a lead wrapped around the probe and soldered to ground in close proximity to the signal pin.

Introduction

Texas Instruments offers several types of frame transfer CCD image sensors that can be used in a wide variety of applications. The TI frame transfer CCD image sensors feature the following topology options: from one to three serial registers, transfer gates, a multiplexer, separate reset lines, center clearing drains, and electron-hole recombination or lateral-overflow-drain antiblooming protection. Despite these differences in topology, all TI frame transfer CCD image sensors are virtual phase devices; therefore, the concepts of operation illustrated by the TC237 apply to all TI frame transfer CCD image sensors. This report gives a general explanation of CCD operation so that camera designers can customize the timing necessary for their application.

Frame Transfer CCD Timing for the TC237

The TI frame transfer CCD sensor has an image area consisting of an array of pixels, a storage area, and from one to three serial registers. The TC237 has two serial registers. The operation of the frame transfer CCD consists of an integration period, a parallel transfer period, and a readout period, which contains a line transfer and a serial readout. The timing diagrams for these periods are illustrated in Figure 1.



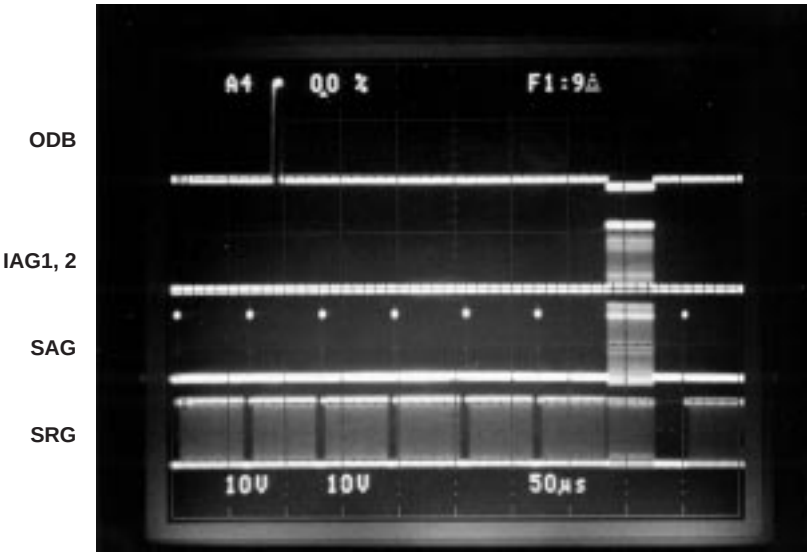


Figure 1. Timing Diagrams for the TC237

Eliminating Smear

Frame transfer devices solve the problem of smearing found in full frame devices by performing a fast parallel transfer from the image area to the storage area. The storage area is shielded from light so that no further integration of the image can occur. Frame transfer devices do have some smear associated with this parallel transfer, but it is minimized by the speed at which the transfer is performed. The percentage of smear can be calculated using the following equations:

$$\% \text{ smear} = \frac{\frac{1}{10} * t_{xfer}}{t_{int}} * 100\% \quad \textbf{(1)}$$

$$t_{xfer} = \frac{n_{IA}}{f_{xfer}} \quad \textbf{(2)}$$

where

t_{xfer} = time required to transfer an image out of the image area
t_{int} = integration time
n_{IA} = number of lines in the image area
f_{xfer} = parallel transfer frequency

The TC237 image sensor provides two methods to eliminate this small amount of smear. First, the image area can be cleared with a single pulse on the ODB pin. This eliminates any smearing effects from the previous parallel transfer resulting in unidirectional smear. Also, two lines can be combined into one in the image area. As the parallel transfer occurs, both lines accumulate smear information. Subtracting the pair of lines after they are read out of the imager eliminates the smear. This line summing operation in the image area increases the sensitivity by accumulating twice as much data in one pixel for a given integration time.

Integration Period

As light enters the CCD, the photons generate electrons which are stored in the wells of each pixel. The length of the integration period determines the number of electrons that are accumulated. The integration time can be controlled by the ODB pin. An 18-V pulse above a 17-V antiblooming level for a duration of at least 1 µs will clear all of the data in the image area. These voltage levels are listed with the substrate set at 10 V. Having the substrate at 10 V eliminates the use of negative voltages for moving charge through the sensor. The position of this pulse with respect to the parallel transfer clocks controls the integration time. See NO TAG.

Antiblooming protection is accomplished through an advanced lateral-overflow-drain antiblooming device. A voltage bias on the ODB pin controls the level of protection. The optimal setting for maximum antiblooming protection is 15−17 V. Antiblooming protection goes down and the pixel well capacity goes up as this bias is decreased. To disable the antiblooming protection, the voltage should be set below 14.5 V but not below 13 V. At 13 V, charge injection occurs.

Parallel Transfer Period

The integration period in the frame transfer image sensor is ended by a parallel transfer of the information in the image area to the storage area. This transfer period is accomplished by a series of clocks on the IAG1, IAG2, and SAG lines. Figure 2 illustrates the parallel transfer period.

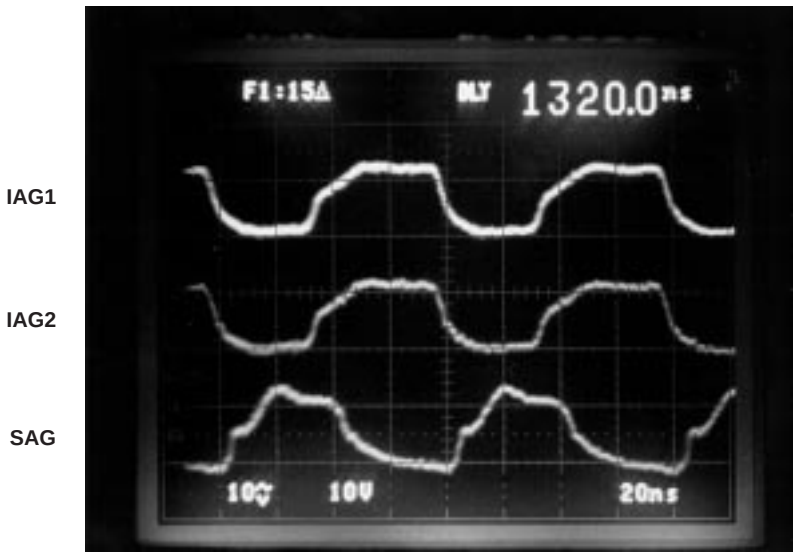


Figure 2. Parallel Transfer Period

The IAG1 line is connected to all of the odd rows, and IAG2 is connected to all of the even rows. It is important to have no phase differences between these two signals during the parallel transfer period. Any differences will cause charge to be added together. The phase difference between the IAGs and the SAG is not critical. The TC237 timing diagrams show a phase difference of 180 degrees, but the clocks can be as little as 90 degrees out of phase.

It is important to drive these clocks as fast as possible to minimize smearing effects. Using one TMC57253DSB driver, it is possible to drive these clocks at 6.25 MHz. Using two drivers in parallel, these clock signals can operate at 12.5 MHz. Using equation 1, the percentages of smear calculated for the two different clock frequencies with an integration time of 16 µs are 0.050% and 0.025% for 6.25 MHz and 12.5 MHz, respectively. These values are small, but as the integration time decreases, the parallel transfer frequency becomes more critical in minimizing smear. The two suggested circuits for the drivers are shown in Figure 3.

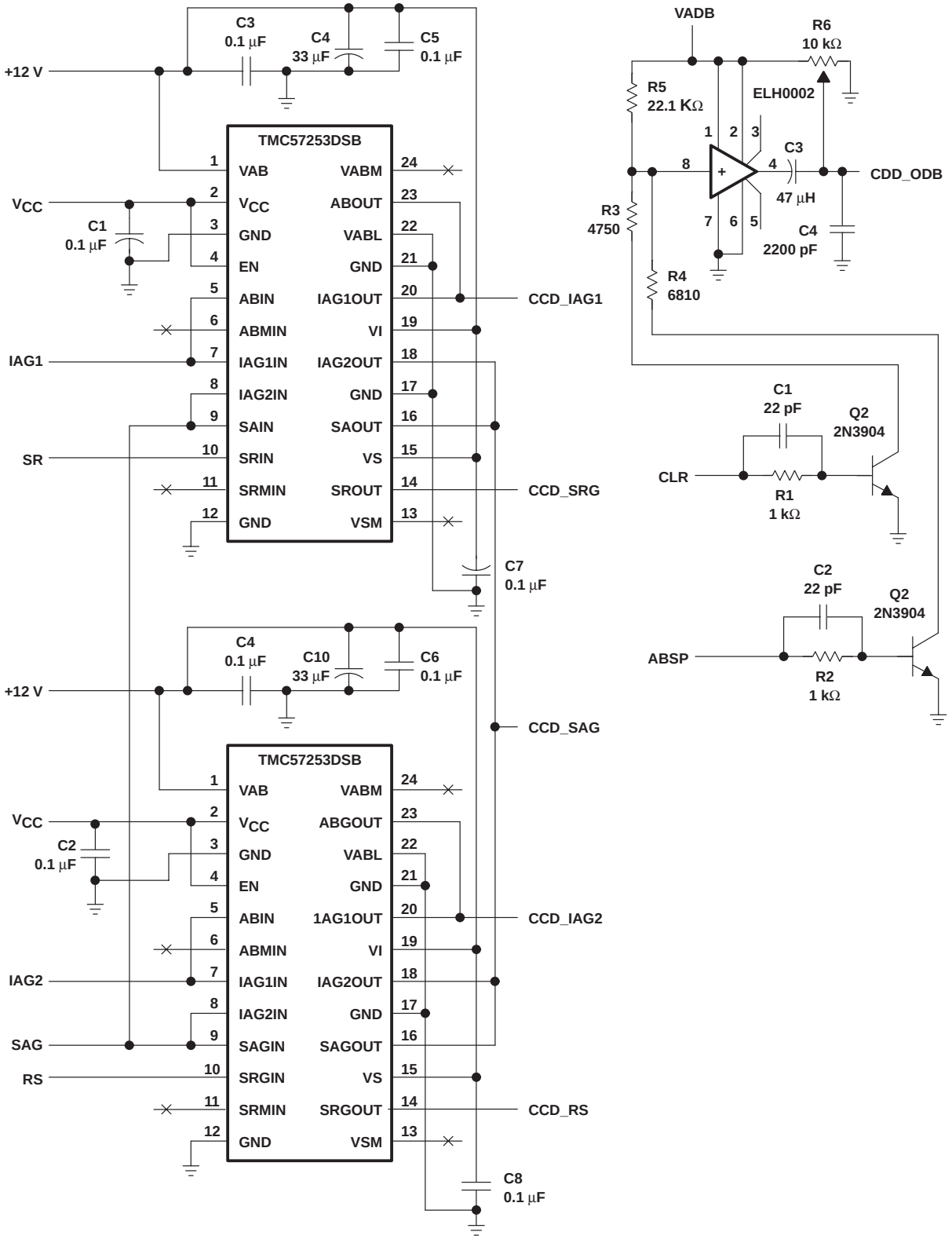


Figure 3. Suggested Driver Circuits

During the parallel transfer, it is desirable to lower the voltage bias level on ODB by 1.5 V to increase the well capacity. This prevents the differences in each pixel's well capacity from affecting the transfer of charge across it. This timing can be seen in Figure 1.

Readout Period

The readout period consists of a line transfer and a serial readout. These processes are accomplished using clock pulses.

Line Transfer

The readout period begins with a line transfer. This transfer moves charge from one row of the storage area to the row below it. The charge in the last row in the storage area is transferred to serial register 2, and charge that was in serial register 2 is transferred to serial register 1. Any charge that was in serial register 1 is transferred to the clearing drain located below the serial registers. After the pixels are read out serially, the next line transfer occurs.

A line transfer is accomplished through a clock pulse on SAG and SRG, as shown in Figure 4. The SAG and SRG clock pulses should be 180 degrees out of phase.

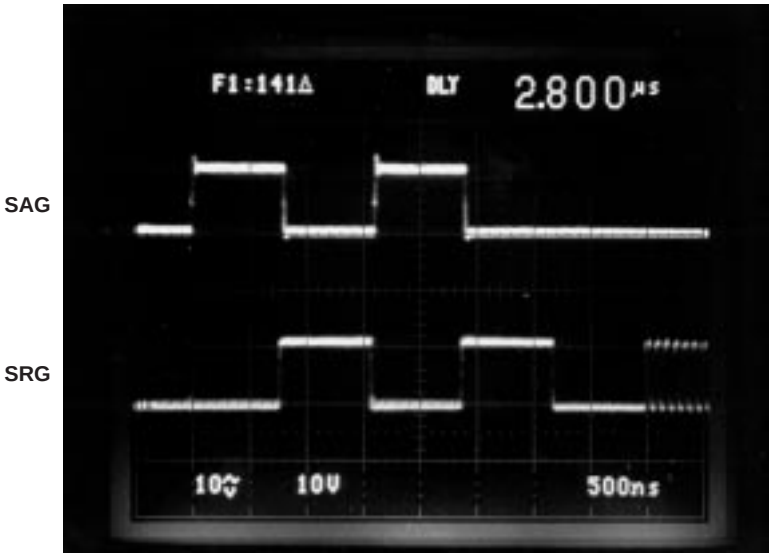
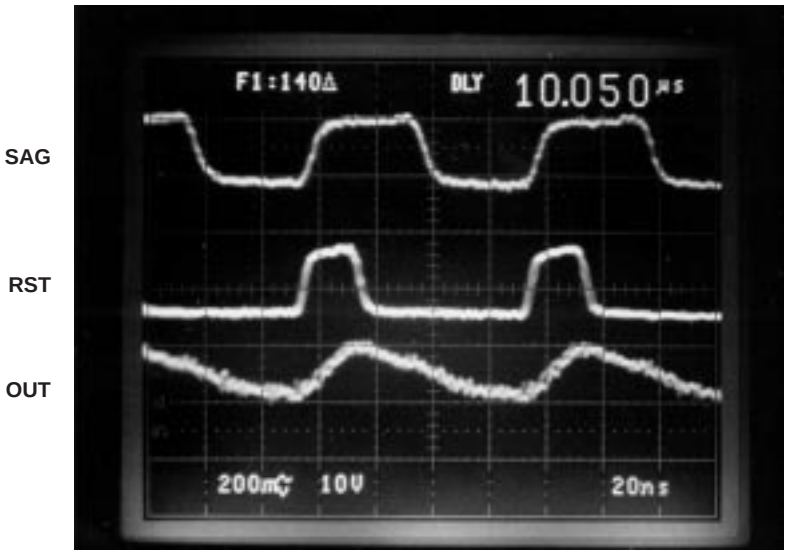


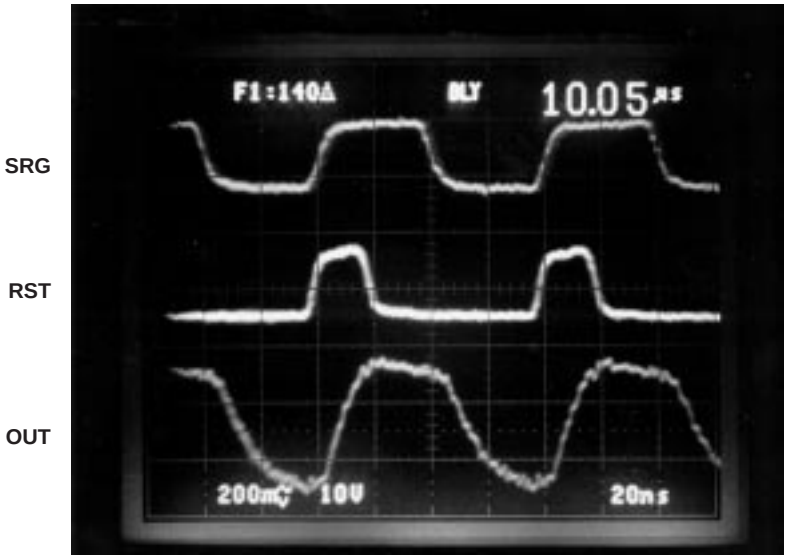
Figure 4. Line Transfer Timing

Serial Readout

Serial readout is the movement of charge from one pixel to the next in the serial registers. The charge that is in the first pixel of these registers is moved onto the detection node. The serial transfer is accomplished through clock pulses on SRG, as illustrated in Figure 5. The SRG in this figure is read out at 12.5 MHz, which conforms to RS-170 standards. The pixels can be read out at any frequency up to the maximum recommended frequency of 12.5 MHz.



(a)



(b)

Figure 5. (a) SRG and OUT2 in Dark Condition
(b) SRG and OUT2 in Saturated Condition (Single Register Readout Mode)