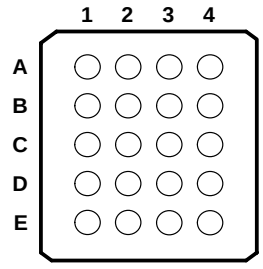
- **Integrated FETs with Low R_{DS-ON} . . . 6 Ω Max**
- **Current-Controlled Output Drives That Are Proportional to Battery Voltage to Save Power**
- **Integrated Power-Supply Switches for Power Savings During OFF State . . . 1 μA Max**
- **Applications: LCD Display for Cell Phones, PDAs, Palmtops, etc.**
- **Packaged in Space-Saving 20-Pin MicroStar Junior™ BGA Package**

GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	D1	S1	S4	D4
B	V_{IN1}	V_{OUT2}	SW	V_{IN2}
C	IN+	V_{OUT1}	V_{IN3}	GND
D	FB	NC	IN–	V_{OUT3}
E	D2	S2	D3	S3

NC – No internal connection

PIN DESCRIPTION

D1, D2, D3, D4	Drain of FETs 1, 2, 3, and 4, respectively
S1, S2, S3, S4	Source of FETs 1, 2, 3, and 4, respectively
V_{IN1}, V_{IN2}, V_{IN3}	Input of switches 1, 2, and 3, respectively
V_{OUT1}, V_{OUT2}, V_{OUT3}	Output of switches 1, 2, and 3, respectively
SW	Operates switches 1, 2, and 3 in unison Low input = switches are closed High input or Open = switches are open
IN+	Noninverting input to current-control amplifier
IN–	Inverting input to current-control amplifier
FB	Provides feedback connection to IN– of current-control amplifier
GND	Ground for I_C

description

The TLED2043 is a four-channel, white LED driver used for backlighting color LCD displays in portable equipment. The device consists of four FET outputs whose output drives are determined by a current-control op amp that automatically monitors the battery. If the battery voltage drops when compared to an externally set reference voltage, the current control op amp proportionately lowers each FET output drive to conserve battery power. Additionally, the TLED2043 has internal switches that can be programmed to connect the power supply to the device only when the LEDs are needed, offering significant power savings during periods of inactivity.

description (continued)

The TLED2043 has significant advantages over the use of discrete devices in implementing a white LED driver solution because it offers small board space, lower R_{DS-ON}, and lower overall cost. Compared to the use of charge pumps and dc-dc converters in similar applications, the TLED2043 offers the advantages of a lower solution cost and smaller board space because no inductors and/or capacitors are required. In addition, it avoids the switching noise and power-loss issues associated with such devices.

The TLED2043 is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

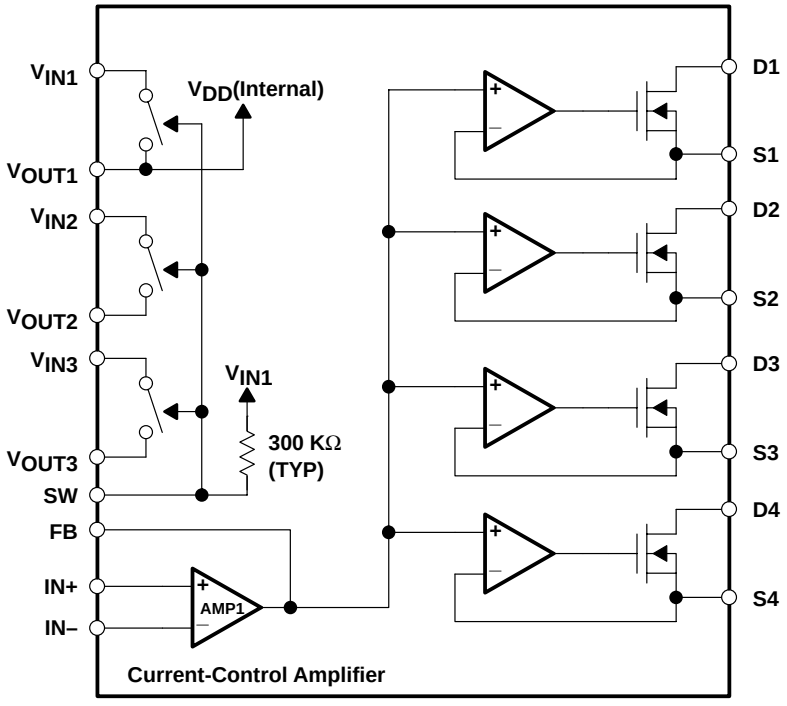
T_A	PACKAGE
	VERY LOW-PROFILE FINE-PITCH GRID ARRAY (GQN)
–40°C to 85°C	TLED2043IGQNR

The GQN package is only available taped and reeled. Add the suffix R to device type (e.g., TLED2043IGQNR).

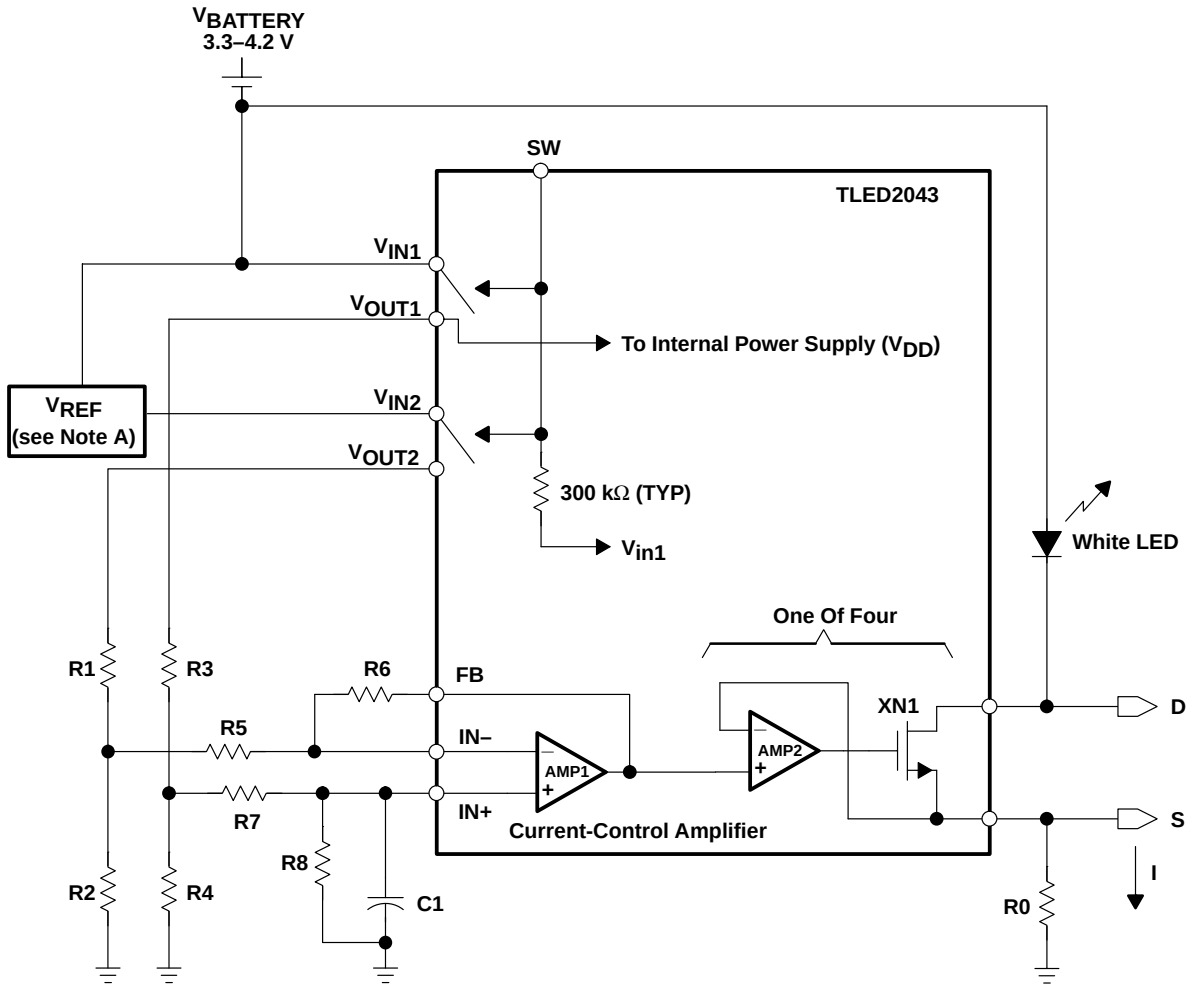
FUNCTION TABLE

SW INPUT	STATUS OF SWITCHES
H	OFF
L	ON
OPEN	OFF

functional block diagram



typical application circuit



R0 = 0.01 kΩ
R1 = 20 kΩ
R2 = 1.6 kΩ
R3 = 20 kΩ
R4 = 2.2 kΩ
R5 = 6.8 kΩ
R6 = 20 kΩ
R7 = 100 kΩ
R8 = 100 kΩ
C1 = 1 μF
V_{REF} = 2.8 V

NOTE A: V_{REF} and resistor values should be chosen for proper control of LED current, which is adjusted by the current-control amplifier to be directly proportional to the difference between $V_{BATTERY}$ and V_{REF}. A stable V_{REF} can be achieved through a low-power voltage reference or shunt regulator (such as the TLV431A), or a low-power LDO (such as the TPS770xx or TPS769xx families).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{IN1}, V_{IN2}, V_{IN3} (see Note 1) . . . . . 7 V
Supply output current: I_{OUT1}, I_{OUT2}, I_{OUT3} . . . . . 15 mA
Amplifier input voltage, V_I . . . . . V_{DD}
Output FET drain-source voltage, V_{DS} . . . . . 7 V
Output FET drain current, I_D . . . . . 50 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3) . . . . . 78°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{IN1}	Supply voltage	2.7	5.5	V
V_{IN2}		0	5.5	
V_{IN3}		0	5.5	
V_{SW}	Input voltage for SW	0	5.5	V
I_{OUT1}	Output current		3	mA
I_{OUT2}			3	
I_{OUT3}			3	
V_{DS}	FET output drain-source voltage		5.5	V
I_D	FET output drain current		50	mA
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics, T_A = 25°C (unless otherwise noted)

supply voltage switch section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT1}	Output voltage	V_{IN1} = 3.6 V, I_{OUT} = 3 mA	V_{IN}–0.1			V
V_{OUT2}		V_{IN1} = 3.6 V, I_{OUT} = 3 mA	V_{IN}–0.1			
V_{OUT3}		V_{IN1} = 3.6 V, I_{OUT} = 3 mA	V_{IN}–0.1			
V_{SW}	High input voltage range for SW OFF	V_{IN1} = 2.7 V to 5.5 V (see Note 4)	$V_{DD} \times 0.7$			V
	Low input voltage range for SW ON	V_{IN1} = 2.7 V to 5.5 V (see Note 4)			$V_{DD} \times 0.3$	
I_L	Low input current for SW	V_{IN1} = 3.6 V, V_{SW} = 0 V		20	100	µA
I_{DD}	Input current (see Figure 1)	ON state (V_{SW} = 0 V)			1	mA
		OFF state (V_{SW} = OPEN)			1	µA

NOTE 4: $V_{DD} = V_{OUT1}$

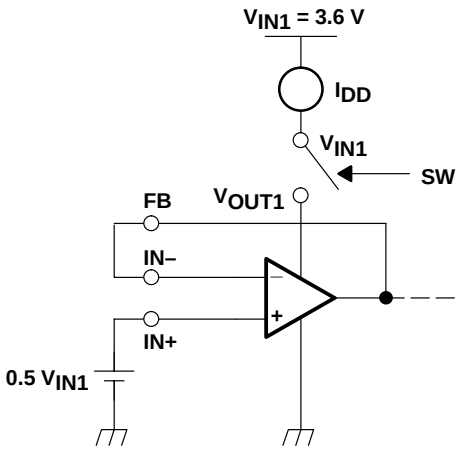
amplifier (AMP1) section, V_{IN1} = 3.6 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IN1} = 2.7 V to 5.5 V, $V_{IC} = 0.5 \times V_{IN}$ or 100 mV (see Figure 2)	T_A = 25°C		0.3	4	mV
			T_A = Full range			5	
I_{IO}	Input offset current				8		pA
I_{IB}	Input bias current				45		pA
V_{ICR}	Common-mode input voltage	V_{IN1} = 2.7 V to 5.5 V (see Figure 3)		0		V_{DD}–1.5	V
A_{VD}	Open-loop voltage gain			70			dB
B_1	Unity-gain bandwidth				630		kHz
V_{OH}	Output voltage (FB)	$R_L \geq 100$ kΩ (see Figure 4)		V_{DD}–1.5			V
V_{OL}	Output voltage (FB)	$R_L \geq 100$ kΩ (see Figure 5)				0.1	V

constant-current circuit section, AMP + FET

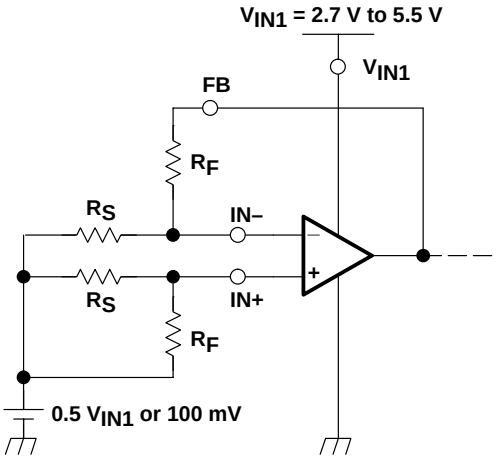
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	Drain off-state current	V_{IN1} = 3.6 V, SW: OFF ($V_{SW} = V_{DD}$ or OPEN), V_{DS} = 5.5 V		25	250	nA
r_{on}	Drain-source ON resistance	V_{IN1} = 2.7 V, IN+ = 0.1 V, I_D = 20 mA (see Figure 6)			6	Ω
V_S	Source voltage	V_{IN1} = 2.7 V to 5.5 V, FB = 200 mV, V_D = 0.5 V, R_L = 10 Ω (see Figure 7)	194	199	204	mV

PARAMETER MEASUREMENT INFORMATION



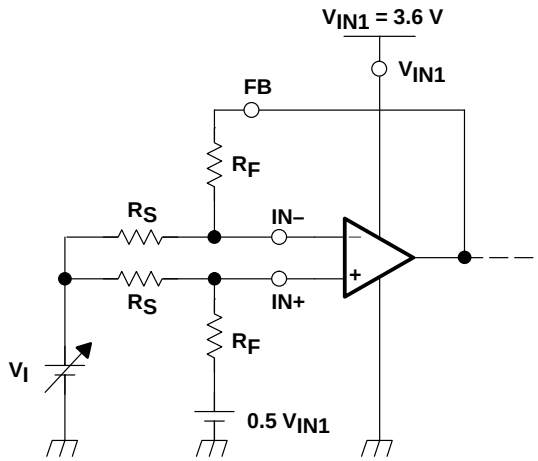
NOTE: V_{SW} = 0 V or open, all other pins open

Figure 1. I_{DD} (ON State)



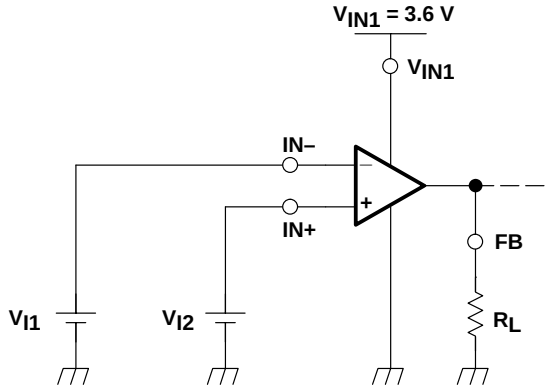
NOTE: SW = 0 V, all other pins open

Figure 2. V_{IO}



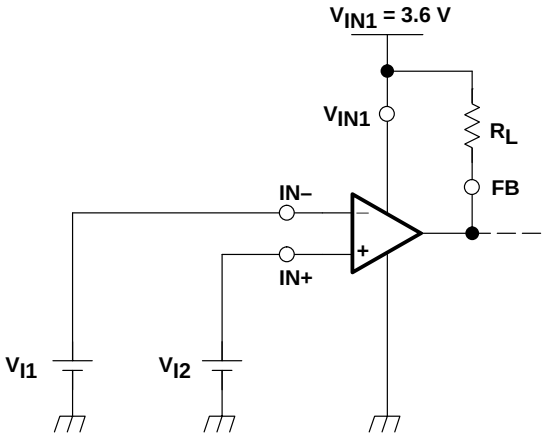
NOTE: SW = 0 V, all other pins open

Figure 3. V_{ICR}



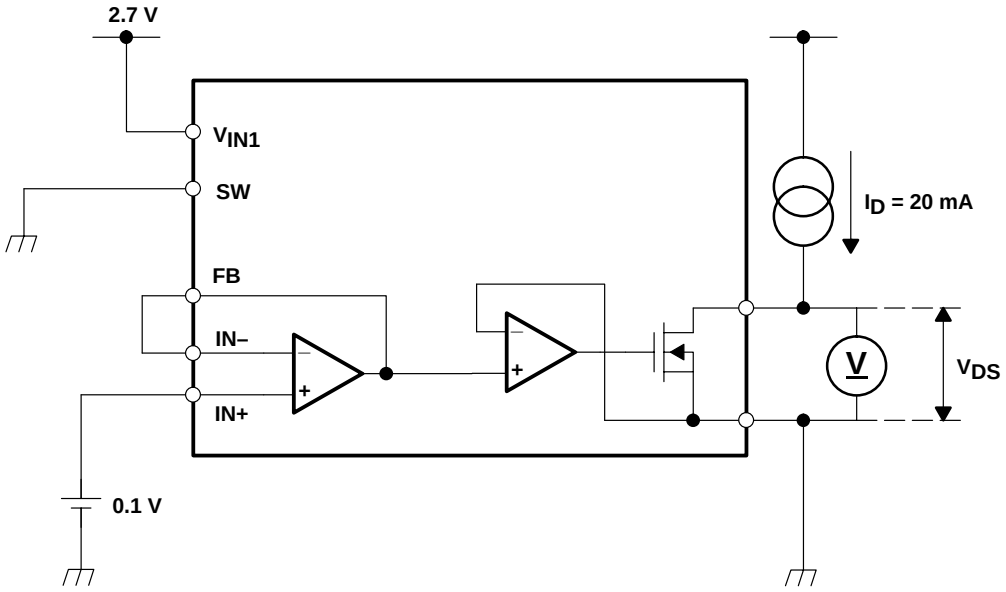
NOTE: SW = 0 V, all other pins open

Figure 4. V_{OH}



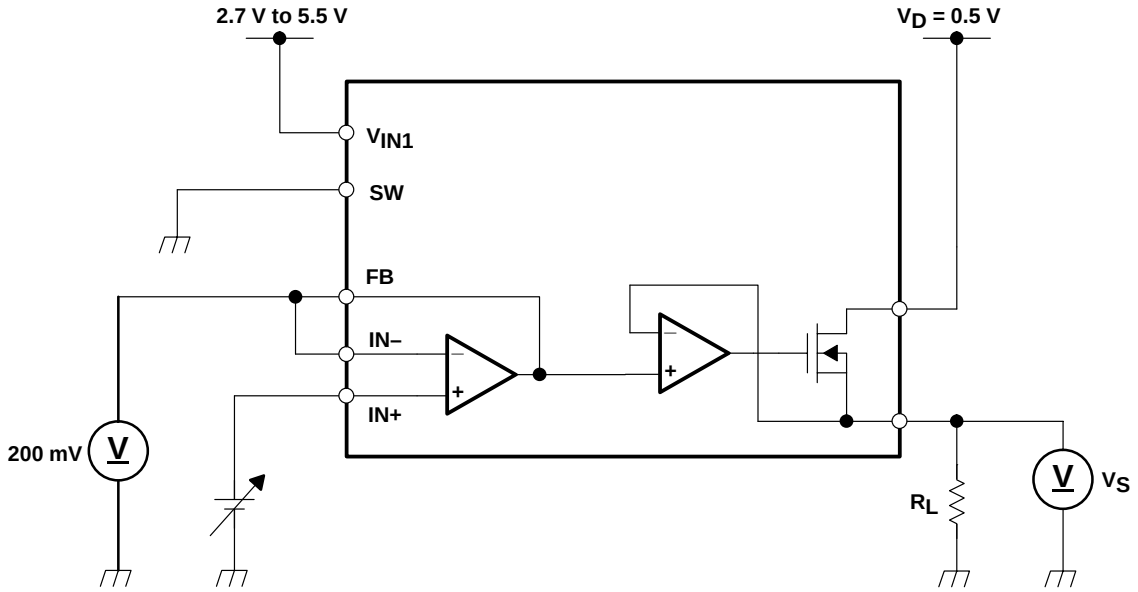
NOTE: SW = 0 V, all other pins open

Figure 5. V_{OL}



NOTE: V_{IN1} = 2.7 V, SW = 0 V, IN+ = 0.1 V, all other pins open
$r_{on} = V_{DS}/I_D$

Figure 6. r_{on}



NOTE: V_{IN1} = 2.7 V to 5.5 V, FB = 200 mV, V_D = 0.5 V, R_L = 10 Ω

Figure 7. V_S

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