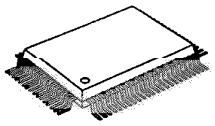
CMOS 8-Bit Microcontroller

TMP86CK74A/TMP86CM74A

TMP86CK74A/CM74A is a low power, high-speed and high-performance 8-bit single chip microcomputer, including large capacity ROM/RAM, input/output ports, multiple timer/counter, serial interface, 8-bit AD converter and VFT (Vacume Fluorescent Tube) driver.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CK74AF	24 K×8 bits	1 K×8 bits	P-QFP80-1420-0.80B	TMP86PM74AF
TMP86CM74AF	32 K×8 bits	2 K×8 bits		

P-LQFP80-1420-0.80B



TMP86CK74AF
TMP86CM74AF
TMP86PM74AF

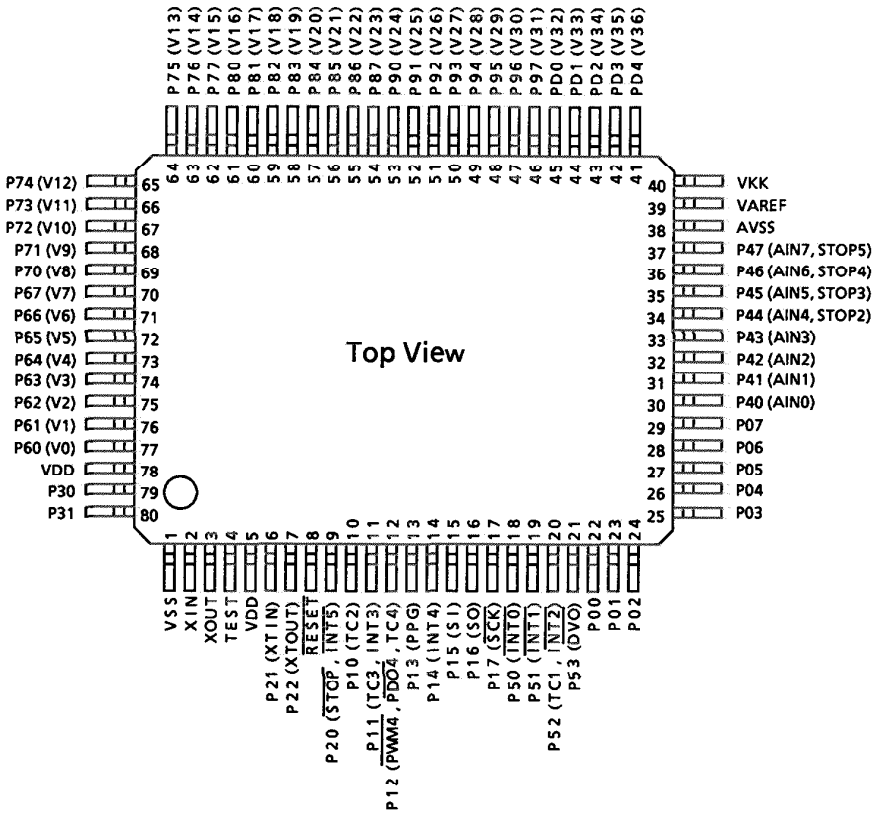
Features

- 8-bit single chip microcomputer TLCS-870/C series
- Minimum instruction execution time : 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 731 basic machine instructions : 132 types
- 17 interrupt sources (External : 6, Internal : 11)
- Input/output ports : 70 pins
- 16-bit timer counters : 2 channels
  - TC1 : Timer, Event counter, PPG (Programmable Pulse Generator) output, Pulse width measurement, External trigger timer, and Window modes
  - TC2 : Timer, Event counter, Window modes
- 8-bit timer counters : 2 channels
  - TC3 : Timer, Event counter, Capture modes (Pulse width/duty measurement).
  - TC4 : Timer, Event counter, PWM (Pulse width modulation) Output, PDO (Programmable Divider Output)

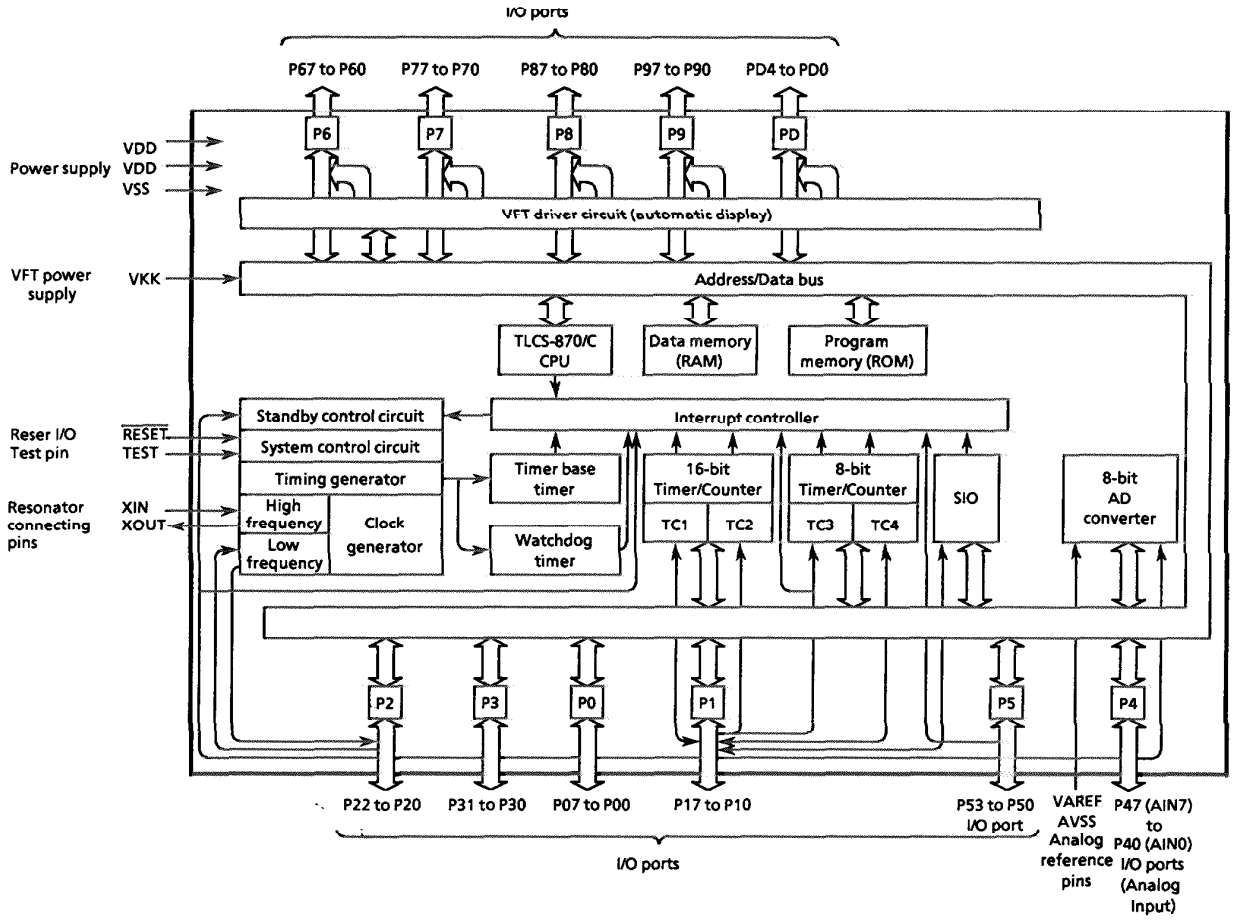
- ◆ Time base timer
- ◆ Watchdog timer
  - Interrupt source
- ◆ Divider output function
- ◆ 4 Key-on wake up pins
- ◆ Serial interface
  - 8-bit SIO : 1 channel (with 32 bytes FIFO)
- ◆ 8-bit successive approximation type AD converter
  - Analog input : 8 channels
- ◆ Vacume flouorescent tube driver (automatic display)
  - Programmable grid scan
  - High breakdown voltage ports (max 40 V × 37 bits)
- ◆ Low consumption power (9 modes)
  - STOP mode : Oscillation stop (Battery/Capacitor back-up).
  - SLOW1 mode : Low consumption power operation by low-frequency clock (High-frequency clock stop.)
  - SLOW2 mode : Low consumption power operation by low-frequency clock (High-frequency clock oscillate.)
  - IDLE0 mode : CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer.
    Release by INTTBT interrupt.
  - IDLE1 mode : CPU stops, and peripherals operate using high-frequency clock.
    Release by interrupts.
  - IDLE2 mode : CPU stops, and peripherals operate using high and low-frequency clock.
    Release by interrupts.
  - SLLEP0 mode : CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer.
    Release by INTTBT interrupt.
  - SLEEP1 mode : CPU stops, and peripherals operate using low-frequency clock.
    Release by interrupts.
  - SLEEP2 mode : CPU stops, and peripherals operate using high and low-frequency clock.
    Release by interrupts.
- ◆ Dual clock operation
  - Single/Dual-clock mode
- ◆ Wide operating voltage : 4.5 V to 5.5 V at 16 MHz/32.768 kHz
  2.7 V to 5.5 V at 8 MHz/32.768 kHz

Pin Assignments (Top View)

P-LQFP80-1420-0.80B



Block Diagram



Pin Functions

Pin Name	I/O	Function	
P00 P01 P02 P03 P04 P05 P06 P07	I/O	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	–
P10 (TC2)	I/O (Input)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control. When used as serial data input, external interrupt input, timer/counter input, the input mode is configured. When used as PWM output, PDO output, PPG output, serial data output, serial clock Output, the latch must be set to "1" and the Output mode is configured. When used as open-drain port, P1OUTCR Set to "0". When used as CMOS port, P1OUTCR set to "1".	External input for TC1
P11 (TC3/INT3)	I/O (Input, Input)		External input for TC1 External interrupt input3
P12 (PWM4/PDO4/TC4)	I/O (Output, Output, Input)		PWM output PDO output External input for TC4
P13 (PPG)	I/O (Output)		PPG output
P14 (INT4)	I/O (Input)		External interrupt input4
P15 (SI)	I/O (Input)		Serial data input
P16 (SO)	I/O (Output)		Serial data input
P17 (SCK)	I/O (I/O)		Serial clock input/output
P20 (INT5/STOP1)	I/O (Input)	3-bit input/output port. When used as input port, external interrupt input, STOP mode release signal input, the input mode is configured.	External interrupt input5 STOP mode rerease signal input
P21 (XTIN)	I/O (Input)		Low resonator connection pin (32.768 kHz). For external clock, XTIN is used and XTOUT is opened
P22 (XTOUT)	I/O (Output)		
P30 P31	I/O	2-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	–
P40 (AIN0) P41 (AIN1) P42 (AIN2) P43 (AIN3)	I/O (Input)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	AD converter analog input
P44 (AIN4/STOP2) P45 (AIN5/STOP3) P46 (AIN6/STOP4) P47 (AIN7/STOP5)	I/O (Input, Input)		AD converter analog input Key-on wake up input
P50 (INT0) P51 (INT1)	I/O (Input)	4-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	External interrupt input0 External interrupt input1
P52 (TC1/INT2)	I/O (Input, Input)		External input for TC1 External interrupt input2
P53 (DVO)	I/O (Output)		Divider output

Pin Name	I/O	Function	
P60 (V0) P61 (V1) P62 (V2) P63 (V3) P64 (V4) P65 (V5) P66 (V6) P67 (V7)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Grid output
P70 (V8) P71 (V9) P72 (V10) P73 (V11) P74 (V12) P75 (V13) P76 (V14) P77 (V15)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Grid output
P80 (V16) P81 (V17) P82 (V18) P83 (V19) P84 (V20) P85 (V21) P86 (V22) P87 (V23)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Segment output
P90 (V24) P91 (V25) P92 (V26) P93 (V27) P94 (V28) P95 (V29) P96 (V30) P97 (V31)	I/O (Output)	8-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Segment output
PD0 (V32) PD1 (V33) PD2 (V34) PD3 (V35) PD4 (V36)	I/O (Output)	5-bit programmable input/output port. Each bit of this port can be individually configured as an input or an output under software control.	Segment output
TEST	Input	Test pin for out-going test. Be tied to low.	
RESET	I/O	Reset signal input.	
XIN	Input	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
VSS	Power supply	0.0 [V] (GND)	
VDD		Power supply	
AVSS		Analog reference voltage (GND: 0.0 [V])	
VAREF		Analog reference voltage	
VKK		VFT driver power supply	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The memory of TMP86CK74A/CM74A consists of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64 Kbyte address space.Figure 1-1 shows the memory address map of TMP86CK74A/CM74A. The general-purpose registers are not assigned to the RAM address space.

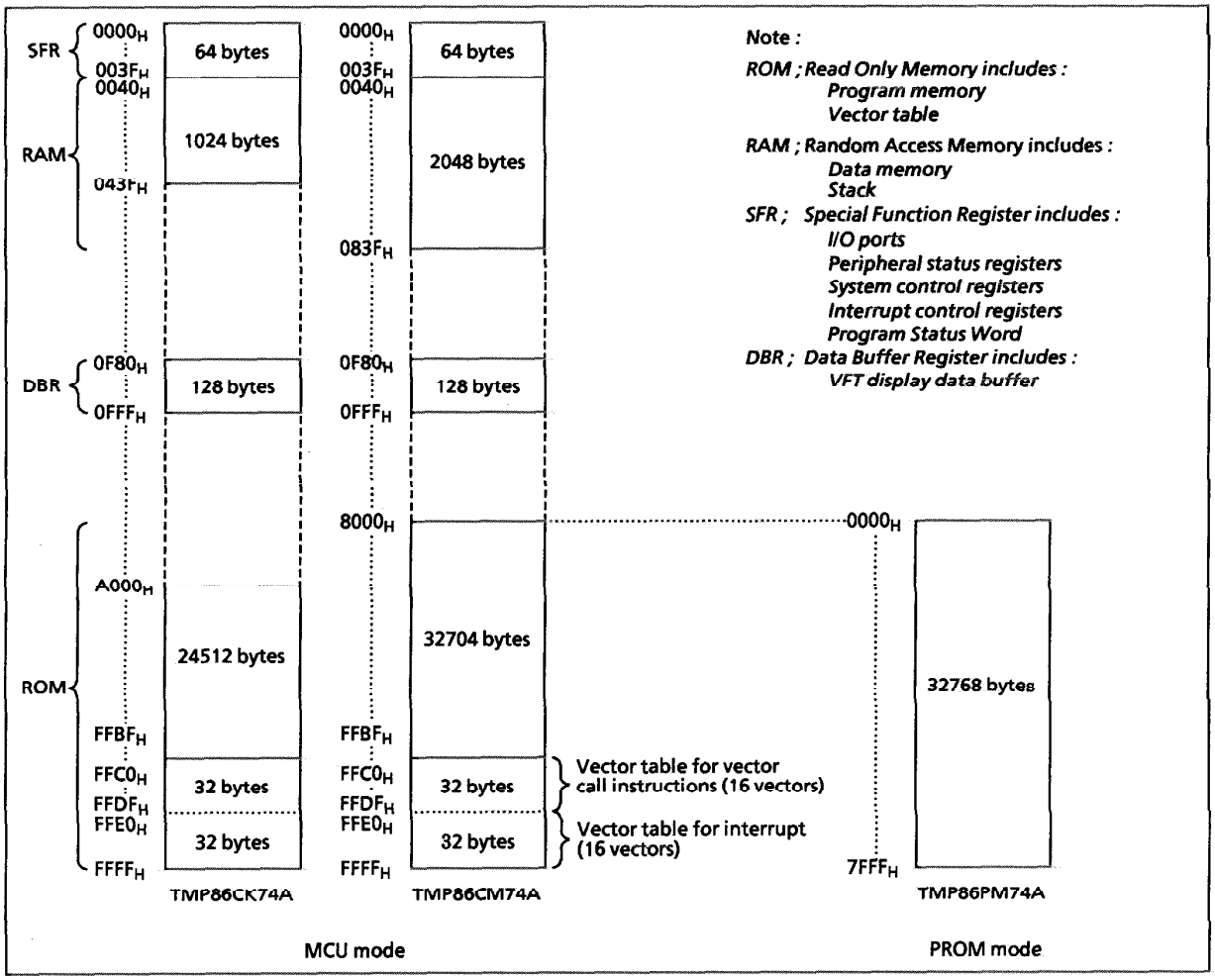


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CK74A has an 24 K×8 bits (address $A000_H$ to $FFFF_H$) of program memory, the TMP86CM74A has 32 K×8 bits (address 8000_H to $FFFF_H$) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

1.3 Data Memory (RAM)

The TMP86CK74A has 1024 bytes (0040_H to $043F_H$) of internal RAM, the TMP86CM74A has 2048 bytes (0040_H to $083F_H$) of internal RAM.
The first 192 bytes (0040_H to $00FF_H$) of the internal RAM are located in the direct area; instructions with shorten operations are available against such an area.
The data memory contents become unstable when the power supply is turned on; therefore, the data memory should be initialized by an initialization routine.

Example 1: Clears RAM to 0. (TMP86CK74A)

```
            LD    HL, 0040H     ; Sets start address.
            LD    A, H          ; Sets initial data (00H) to A register
            LD    BC, 03FFH     ; Sets number of bytes (−1)
SRAMCLR:    LD    (HL), A
            INC   HL
            DEC   BC
            JRS   F, SRAMCLR
```

Example 2: Clears RAM to 0. (TMP86CM74A)

```
            LD    HL, 0040H     ; Sets start address.
            LD    A, H          ; Sets initial data (00H) to A register
            LD    BC, 07FFH     ; Sets number of bytes (−1)
SRAMCLR:    LD    (HL), A
            INC   HL
            DEC   BC
            JRS   F, SRAMCLR
```

1.4 System Clock Controller

The system clock controller consists of a clock generator, a timing generator, and a stand-by controller.

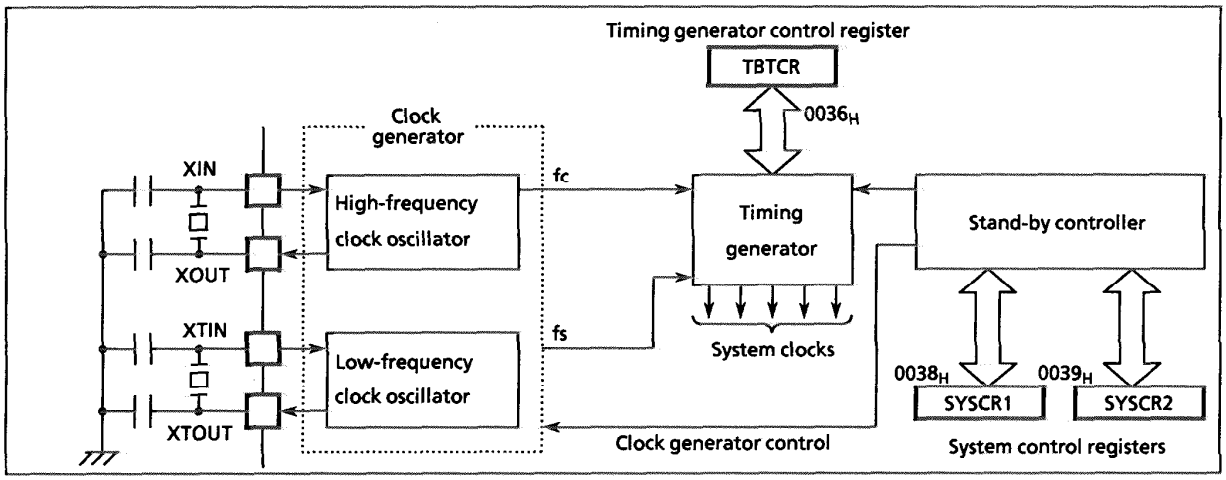


Figure 1-2. System Clock Control

1.4.1 Clock generator

The Clock generator generates the basic clock which provides the system clocks supplied to the CPU core and peripheral hardware. It contains two oscillation circuits: one for the high-frequency clock and one for the low-frequency clock. Power consumption can be reduced by switching of the standby controller to low-power operation based on the low-frequency clock.

The high-frequency (fc) and low-frequency (fs) clocks can easily be obtained by connecting a resonator between the XIN/XOUT and XTIN/XTOUT pins respectively. Clock input from an external oscillator is also possible. In this case, external clock is applied to XIN/XTIN pin with XOUT/XOUT pin not connected.

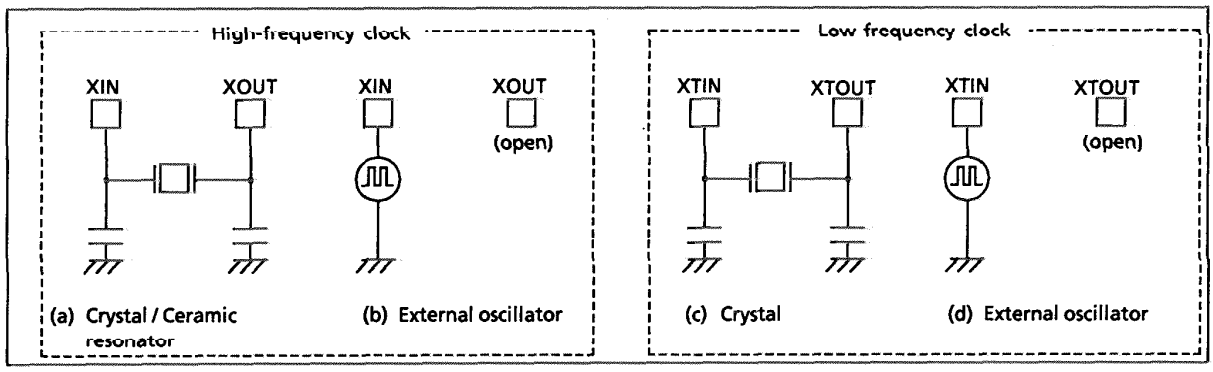


Figure 1-3. Examples of Resonator Connection

Note: The function to monitor the basic clock directly at external is not provided for hardware, however, with disabling all interrupts and watchdog timers, the oscillation frequency can be adjusted by monitoring the pulse which the fixed frequency is outputted to the port by the program.
The system to require the adjustment of the oscillation frequency should create the program for the adjustment in advance.

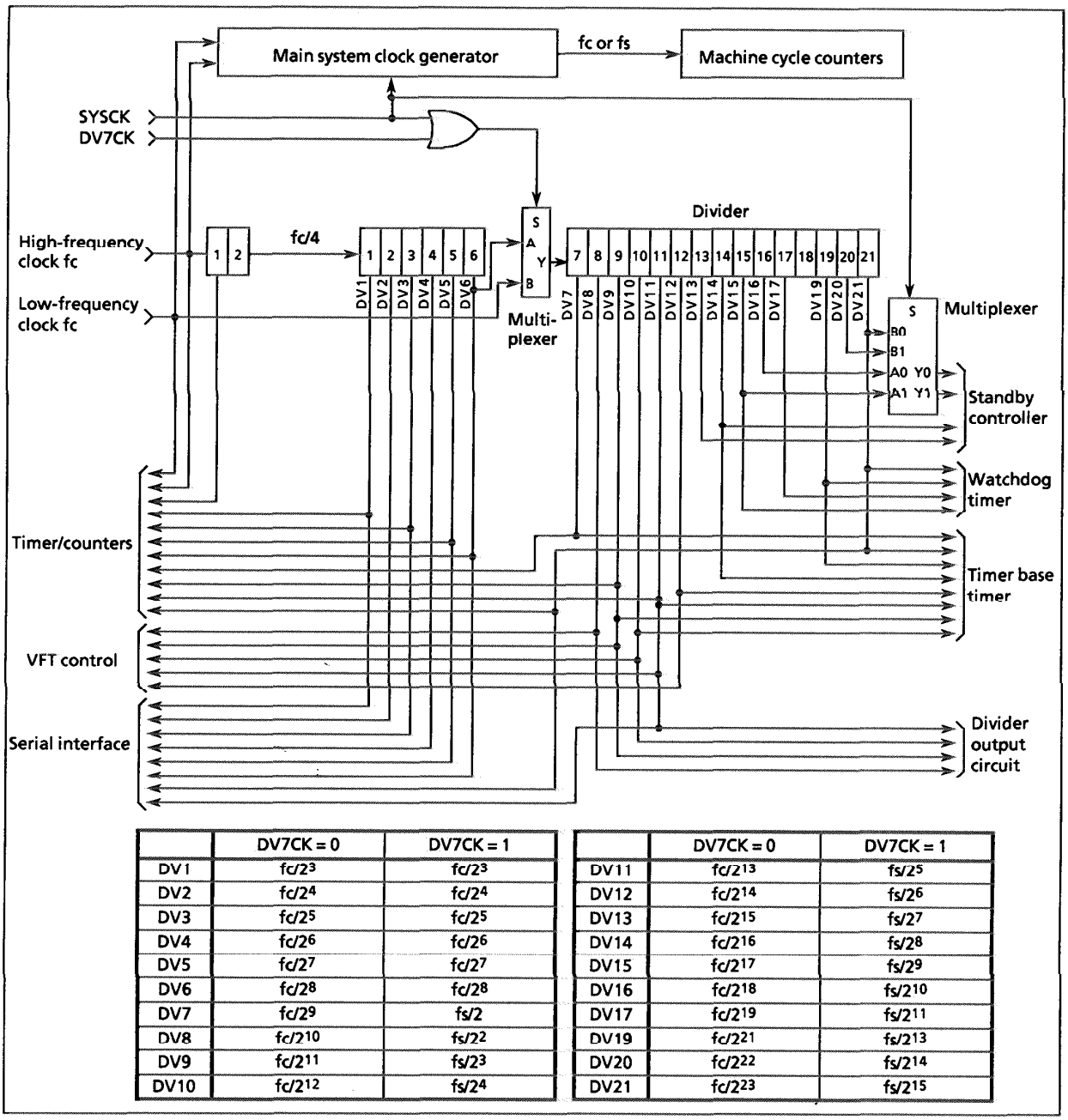
1.4.2 Timing generator

The timing generator generates the various system clocks supplied to the CPU core and peripheral hardware from the basic clock (fc or fs). The timing generator provides the following functions.

① Generation of main system clock
② Generation of divider output (DVO) pulses
③ Generation of source clocks for time base timer
④ Generation of source clocks for watchdog timer
⑤ Generation of internal source clocks for timer/counter
⑥ Generation of warm-up clocks for releasing STOP mode
⑦ Generation of source clocks for VFT driver circuit

(1) Configuration of timing generator

The timing generator consists of a 3-stage precaler, a 21-stage divider, a main system clock generator, and machine cycle counters.
An input clock to the 7th stage of the divider depend on the operating mode, DV7CK (bit4 in TBTCR), that is shown in Figure 1-5. As reset and STOP mode started/canceled, the prescaler and the divider are cleared to "0".



	DV7CK = 0	DV7CK = 1
DV1	$fc/2^3$	$fc/2^3$
DV2	$fc/2^4$	$fc/2^4$
DV3	$fc/2^5$	$fc/2^5$
DV4	$fc/2^6$	$fc/2^6$
DV5	$fc/2^7$	$fc/2^7$
DV6	$fc/2^8$	$fc/2^8$
DV7	$fc/2^9$	$fs/2$
DV8	$fc/2^{10}$	$fs/2^2$
DV9	$fc/2^{11}$	$fs/2^3$
DV10	$fc/2^{12}$	$fs/2^4$

	DV7CK = 0	DV7CK = 1
DV11	$fc/2^{13}$	$fs/2^5$
DV12	$fc/2^{14}$	$fs/2^6$
DV13	$fc/2^{15}$	$fs/2^7$
DV14	$fc/2^{16}$	$fs/2^8$
DV15	$fc/2^{17}$	$fs/2^9$
DV16	$fc/2^{18}$	$fs/2^{10}$
DV17	$fc/2^{19}$	$fs/2^{11}$
DV19	$fc/2^{21}$	$fs/2^{13}$
DV20	$fc/2^{22}$	$fs/2^{14}$
DV21	$fc/2^{23}$	$fs/2^{15}$

Figure 1-4. Configuration of Timing Generator

TBTCR (0036_H)

7	6	5	4	3	2	1	0
(DVOEN)	(DVOCK)		DV7CK	(TBTEN)	(TBTCK)		

(Initial value: 0**0 0***)

DV7CK	Selection of input to the 7th stage of the divider	0: $fc/2^8$ [Hz] 1: fs	R/W

Note 1: Do not set "1" on DV7CK when the single-clock mode.
Note 2: Do not set "1" on DV7CK while the low-frequency clock is not operated stably.
*Note 3: fc; High-frequency clock [Hz], fs; Low-frequency clock [Hz], *; Don't care*

Figure 1-5. Timing Generator Control Register

(2) Machine cycle

Instruction execution and peripheral hardware operation are synchronized with the main system clock. The minimum instruction execution unit is called an "machine cycle". There are a total of 10 different types of instructions for the TLCS-870/C Series: ranging from 1-cycle instructions which require one machine cycle for execution to 10-cycle instructions which require 10 machine cycles for execution.
A machine cycle consists of 4 states (S0 to S3), and each state consists of one main system clock.

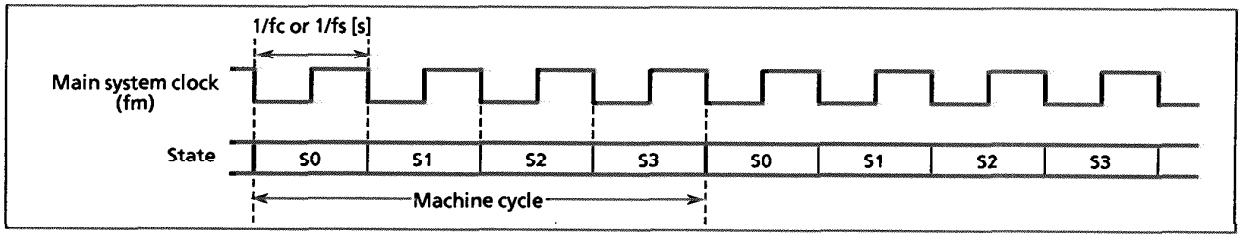


Figure 1-6. Machine Cycle

1.4.3 Standby controller

The standby controller starts and stops the oscillation circuits for the high-frequency and low-frequency clocks, and switches the main system clock. There are two operating modes: single-clock and dual-clock. These modes are controlled by the system control registers (SYSCR1 and SYSCR2).
Figure 1-7 shows the operating mode transition diagram and Figure 1-8 shows the system control registers.

(1) Single-clock mode

Only the oscillation circuit for the high-frequency clock is used, and P21 (XTIN) and P22 (XTOUT) pins are used as input/output ports. The main-system clock is obtained from the high-frequency clock. In the single-clock mode, the machine cycle time is 4/fc [s].

① NORMAL1 mode

In this mode, both the CPU core and on-chip peripherals operate using the high-frequency clock.
The TMP86CK74A/CM74A are placed in this mode after reset.

② IDLE1 mode

In this mode, the internal oscillation circuit remains active. The CPU and the watchdog timer are halted ; however on-chip peripherals remain active (operate using the high-frequency clock).
IDLE1 mode is started by the system control register 2 (SYSCR2), and IDLE1 mode is released to NORMAL1 mode by an interrupt request from the on-chip peripherals or external interrupt inputs. When the IMF (interrupt master enable flag) is "1" (interrupt enable), the execution will resume with the acceptance of the interrupt, and the operation will return to normal after the interrupt service is completed. When the IMF is "0" (interrupt disable), the execution will resume with the instruction which follows the IDLE1 mode start instruction.

③ IDLE0 mode

In this mode, all the circuit, except oscillator and the Timer-Base-Timer, stops operation.
This mode is enabled by setting "1" on bit TGHALT on the system control register 2 (SYSCR2).
When IDLE0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with TBTCR <TBTCK>, the timing generator starts feeding the clock to all peripheral circuits.

When returned from IDLE0 mode, the CPU restarts operating, entering NORMAL1 mode back again. IDLE0 mode is entered and returned regardless of how TBTCR <TBTEN> is set. When IMF = "1", EF7 (TBT interrupt individual enable flag) = "1", and TBTCR <TBTEN> = "1", interrupt processing is performed. When IDLE0 mode is entered while TBTCR <TBTEN> = "1", the INTTBT interrupt latch is set after returning to NORMAL1 mode.

(2) Dual-clock mode

Both the high-frequency and low-frequency oscillation circuits are used in this mode. P21 (XTIN) and P22 (XTOUT) pins cannot be used as input/output ports. The main system clock is obtained from the high-frequency clock in NORMAL2 and IDLE2 modes, and is obtained from the low-frequency clock in SLOW and SLEEP modes. The machine cycle time is 4/fc [s] in the NORMAL2 and IDLE2 modes, and 4/fs [s] (122 μs at fs = 32.768 kHz) in the SLOW and SLEEP modes.
The TLCS-870/C is placed in the signal-clock mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on at the start of a program.

① NORMAL2 mode

In this mode, the CPU core operates with the high-frequency clock. On-chip peripherals operate using the high-frequency clock and / or low-frequency clock.

② SLOW2 mode

In this mode, the CPU core operates with the low-frequency clock, while both the high-frequency clock and the low-frequency clock are operated. On-chip peripherals are triggered by the low-frequency clock. As the SYSCK on SYSCR2 becomes "0", the hardware changes into NORMAL2 mode. As the XEN on SYSCR2 becomes "0", the hardware changes into SLOW1 mode. Do not clear XTEN to "0" during SLOW2 mode.

③ SLOW1 mode

This mode can be used to reduce power-consumption by turning off oscillation of the high-frequency clock. The CPU core and on-chip peripherals operate using the low-frequency clock.
Switching back and forth between SLOW1 and SLOW2 modes are performed by XEN bit on the system control register 2 (SYSCR2). In SLOW1 and SLEEP mode, the input clock to the 1st stage of the divider is stopped; output from the 1st to 6th stages is also stopped.

④ IDLE2 mode

In this mode, the internal oscillation circuit remain active. The CPU and the watchdog timer are halted ; however, on-chip peripherals remain active (operate using the high-frequency clock and / or the low-frequency clock). Starting and releasing of IDLE2 mode are the same as for IDLE1 mode, except that operation returns to NORMAL2 mode.

⑤ SLEEP1 mode

In this mode, the internal oscillation circuit of the low-frequency clock remains active. The CPU, the watchdog timer, and the internal oscillation circuit of the high-frequency clock are halted ; however, on-chip peripherals remain active (operate using the low-frequency clock). Starting and releasing of SLEEP mode are the same as for IDLE1 mode, except that operation returns to SLOW mode. In SLOW and SLEEP mode, the input clock to the 1st stage of the divider is stopped; output from the 1st to 6th stages is also stopped.

⑥ SLEEP2 mode

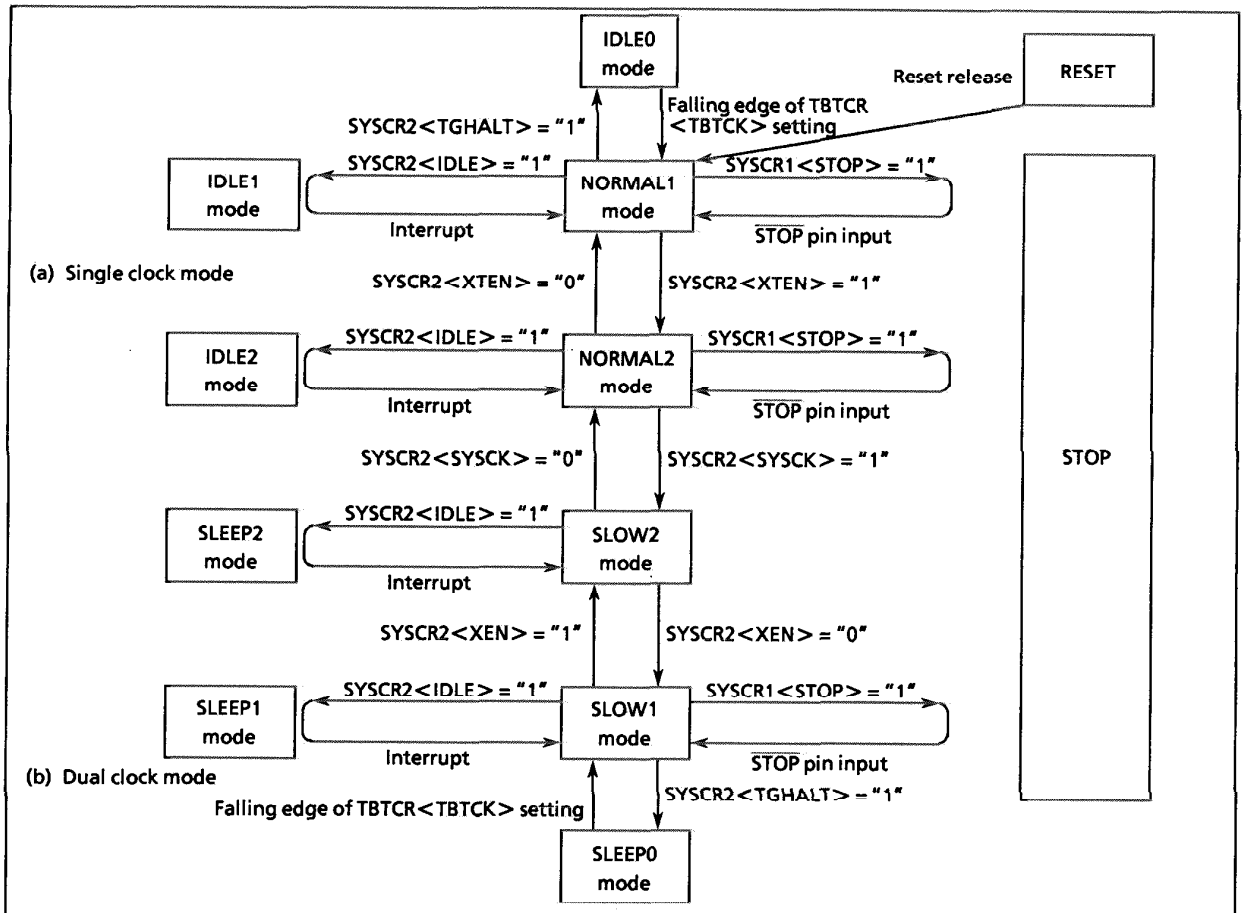
The SLEEP2 mode is the idle mode corresponding to the SLOW2 mode. The status under the SLEEP2 mode is same as that under the SLEEP1 mode, except for the oscillation circuit of the high-frequency clock.

⑦ SLEEP0 mode

In this mode, all the circuit, except oscillator and the Time-Base-Timer, stops operation.
This mode is enabled by setting "1" on bit TGHALT on the system control register2 (SYSCR2).
When SLEEP0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with TBTCR <TBTCK>, the timing generator starts feeding the clock to all peripheral circuits.
When the device exits SLEEP0 mode, the CPU restarts operating, entering SLOW1 mode back again. SLEEP0 mode is entered and returned regardless of how TBTCR <TBTEN> is set. When IMF = "1", EF7 (TBT interrupt individual enable flag) = "1", and TBTCR <TBTEN> = "1", interrupt processing is performed. When SLEEP0 mode is entered while TBTCR <TBTEN> = "1", the INTTBT interrupt latch is set after returning to SLOW1 mode.

(3) STOP mode

In this mode, the internal oscillation circuit is turned off, causing all system operations to be halted. The internal status immediately prior to the halt is held with a lowest power consumption during STOP mode.
STOP mode is started by the system control register 1 (SYSCR1), and STOP mode is released by a inputting (either level-sensitive or edge-sensitive can be programmably selected) to the $\overline{\text{STOP}}$ pin. After the warming-up period is completed, the execution resumes with the instruction which follows the STOP mode start instruction.



Note: NORMAL1 and NORMAL2 modes are generically called NORMAL ; SLOW1 and SLOW2 are called SLOW ; IDLE1, IDLE2, SLEEP1 and SLEEP2 are called IDLE.

Operating Mode		Oscillator		CPU core	TBT	Other Peripherals	Machine Cycle Time
		High-freq.	Low-freq.				
Single Clock	RESET	Oscillation	Stop	Reset	Reset	Reset	4 / fc [s]
	NORMAL1			Operate	Operate	Operate	
	IDLE1			Halt			
	IDLE0					Halt	
	STOP	Stop			Halt		—
Dual Clock	NORMAL2	Oscillation	Oscillation	Operate with High Freq.	Operate	Operate	4 / fc [s]
	IDLE2			Halt			
	SLOW2			Operate with Low Freq.			4 / fs [s]
	SLEEP2			Halt			
	SLOW1	Stop		Operate with Low Freq.			
	SLEEP1			Halt			
	SLEEP0					Halt	
	STOP		Stop		Halt		—

Figure 1-7. Operating Mode Transition Diagram

System Control Register 1

SYSCR1 (0038_H)

7	6	5	4	3	2	1	0
STOP	RELM	RETM	OUTEN	WUT			

(Initial value: 0000 00**)

STOP	STOP mode start	0: CPU core and peripherals remain active 1: CPU core and peripherals are halted (start STOP mode)		R/W
RELM	Release method for STOP mode	0: Edge-sensitive release 1: Level-sensitive release		
RETM	Operating mode after STOP mode	0: Return to NORMAL mode 1: return to SLOW mode		
OUTEN	Port output during STOP mode	0: High Impedance 1: Output Kept		
WUT	Warming-up time at releasing STOP mode		Return to NORMAL mode	Return to SLOW mode
		00	3×2^{16}/fc	3×2^{13}/fs
		01	2^{16}/fc	2^{13}/fs
		10	3×2^{14}/fc	3×2^{6}/fs
		11	2^{14}/fc	2^{6}/fs

Note 1: Always set RETM to "0" when transiting from NORMAL mode to STOP mode. Always set RETM to "1" when transiting from SLOW mode to STOP mode.

Note 2: When STOP mode is released with $\overline{\text{RESET}}$ pin input, a return is made to NORMAL1 regardless of the RETM contents.

Note 3: fc ; High-frequency clock [Hz]
fs ; Low-frequency clock [Hz]
** ; Don't care*

Note 4: Bits 1 and 0 in SYSCR1 are read as undefined data when a read instruction is executed.

Note 5: As the hardware becomes STOP mode under OUTEN = "0", input value is fixed to "0"; therefore it may cause interrupt request on account of falling edge.

Note 6: Port P20 is used as $\overline{\text{STOP}}$ pin. Therefore, when stop mode is started, OUTEN does not affect to P47, and P20 becomes Hi-Z mode.

System Control Register 2

SYSCR2 (0039_H)

7	6	5	4	3	2	1	0
XEN	XTEN	SYSCK	IDLE		TGHALT		

(Initial value: 1000 *0**)

XEN	High-frequency oscillator control	0: Turn off oscillation 1: Turn on oscillation	R/W
XTEN	Low-frequency oscillator control	0: Turn off oscillation 1: Turn on oscillation	
SYSCK	Main system clock select write) / (main system clock monitor (read)	0: High-frequency clock 1: Low-frequency clock	
IDLE	CPU and watch dog timer control (SLEEP1/2, IDLE1/2 mode)	0: CPU and watchdog timer remain active 1: CPU and watchdog timer are stopped (start SLEEP1/2 and IDLE1/2 mode)	
TGHALT	TG control (SLEEP0, IDLE0 mode)	0: TG provides source clock to all peripherals 1: TG stops source clock to peripherals except TBT (start SLEEP0 and IDLE0 mode)	

Note 1: XEN and SYSCK are automatically overwritten in accordance with the contents of RETM (bit 5 in SYSCR1) when STOP mode is released. But XTEN is not change.

RETM	Operating mode after STOP mode	XEN	SYSCK
0	NORMAL 1/2 mode	1	0
1	SLOW mode	0	1

Note 2: A reset is applied ($\overline{\text{RESET}}$ pin output goes low) if both XEN and XTEN are cleared to "0", XEN is cleared to "0" when SYSCK = "0", or XTEN is cleared to "0" when SYSCK = "1".

*Note 3: * ; Don't care*

Note 4: Bits 3, 1and 0 in SYSCR2 are always read as undefined value.

Note 5: Make it sure not to set SYSCR2<IDLE> and SYSCR2<TGHALT> to " 1 " at a same time.

Note 6: TG; Timing generator

Figure 1-8. System Control Registers

1.4.4 Operating mode control

(1) STOP mode

STOP mode is controlled by the system control register 1 and the $\overline{\text{STOP}}$ pin input.
The $\overline{\text{STOP}}$ pin is also used both as a port P20 and an $\overline{\text{INT5}}$ (external interrupt input 5) pin.
STOP mode is started by setting STOP (bit 7 in SYSCR1) to "1". During STOP mode, the following status is maintained.

① Oscillations are turned off, and all internal operations are halted.

② The data memory, registers, the program status word and port output latches are all held in the status in effect before STOP mode was entered.

③ The prescaler and the divider of the timing generator are cleared to "0".

④ The program counter holds the address 2 ahead of the instruction (e.g. [SET (SYSCR1).7]) which started STOP mode.

Releasing STOP mode includes a level-sensitive mode and an edge-sensitive mode, either of which can be selected with the RELM (bit 6 in SYSCR1).

Note: During STOP period (from start of STOP mode to end of warming-up), due to changes in the external interrupt pin signal, interrupt latches may be set to "1" and interrupts may be accepted immediately after STOP mode is released. Before starting STOP mode, therefore, disable interrupts. Also, before enabling interrupts after STOP mode is released, clear unnecessary interrupt latches.

a. Level-sensitive release mode (RELM = "1")

In this mode, STOP mode is released by setting the $\overline{\text{STOP}}$ pin high. This mode is used for capacitor back-up when the main power supply is cut off and long term battery back-up.
When the $\overline{\text{STOP}}$ pin input is high executing an instruction which starts STOP mode will not place in STOP mode but instead will immediately start the release sequence (warm-up). Thus, to start STOP mode in the level-sensitive release mode, it is necessary for the program to first confirm that the $\overline{\text{STOP}}$ pin input is low. The following two methods can be used for confirmation.

① Testing a port P20.

② Using an external interrupt input $\overline{\text{INT5}}$ ($\overline{\text{INT5}}$ is a falling edge-sensitive input).

Example 1: Starting STOP mode from NORMAL mode by testing a port P20.

```
        LD    (SYSCR1), 01010000B    ; Sets up the level-sensitive release mode
                                     ; Sets up the input mode
SSTOPH:TEST (P2DR). 0                ; Wait until the STOP pin input goes low level
        JRS   F, SSTOPH
        SET   (SYSCR1). 7            ; Starts STOP mode
```

Example 2: Starting STOP mode from NORMAL mode with an INT5 interrupt.

```
PINT5:  TEST (P2DR). 0              ; To reject noise, STOP mode does not start if
        JRS  F, SINT5                 port P20 is at high
        LD   (SYSCR1), 01010000B    ; Sets up the level-sensitive release mode.
        SET  (SYSCR1). 7            ; Starts STOP mode
SINT5:  RETI
```

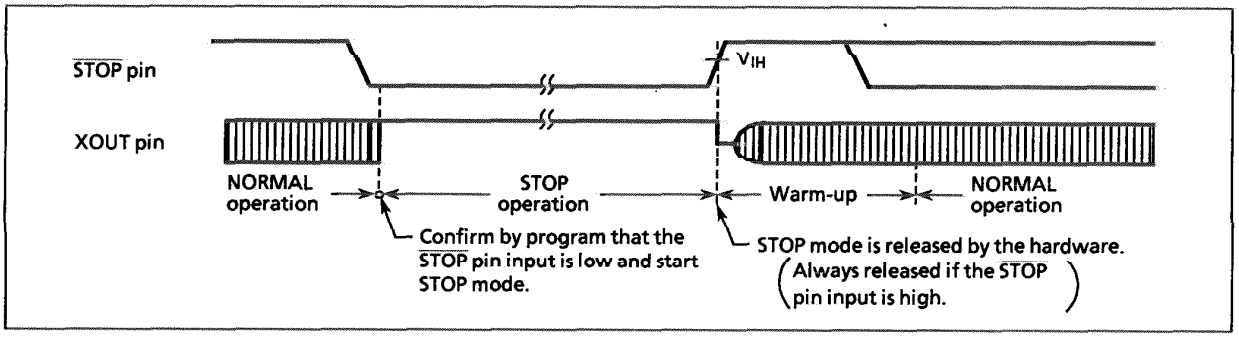


Figure 1-9. Level-sensitive release Mode

Note 1: Even if the STOP pin input is low after warming up start, the STOP mode is not restarted.
Note 2: In this case of changing to the level-sensitive mode from the edge-sensitive mode, the release mode is not switched until a rising edge of the STOP pin input is detected.

b. Edge-sensitive release mode (RELM = "0")

In this mode, STOP mode is released by a rising edge of the STOP pin input. This is used in applications where a relatively short program is executed repeatedly at periodic intervals. This periodic signal (for example, a clock from a low-power consumption oscillator) is input to the STOP pin. In the edge-sensitive release mode, STOP mode is started even when the STOP pin input is high level.

Example: Starting STOP mode from NORMAL mode

```
LD  (SYSCR1), 10010000B ; Starts after specified to the edge-sensitive release mode
```

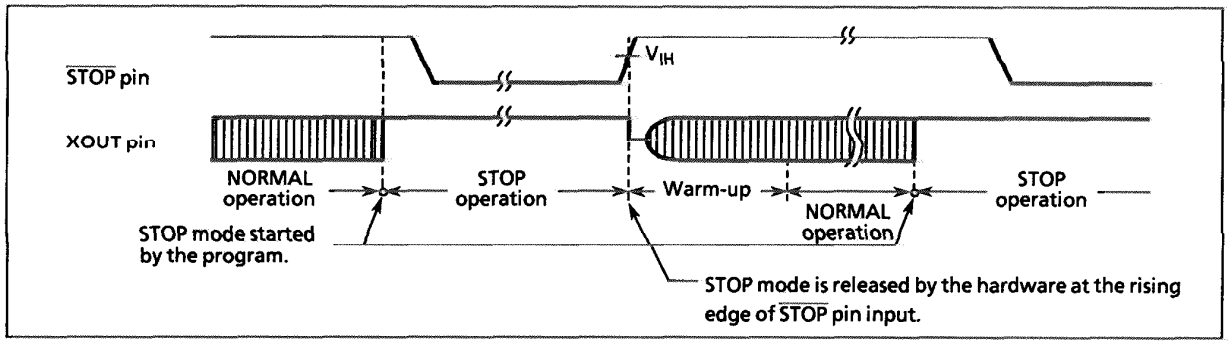


Figure 1-10. Edge-sensitive release Mode

STOP mode is released by the following sequence.

① In the dual-clock mode, when returning to NORMAL2 or SLOW2, both the high-frequency and low-frequency clock oscillators are turned on ; when returning to SLOW1 mode, only the low-frequency clock oscillator is turned on. In the signal-clock mode, only the high-frequency clock oscillator is turned on.

② A warm-up period is inserted to allow oscillation time to stabilize. During warm-up, all internal operations remain halted. Four different warm-up times can be selected with the WUT (bits 2 and 3 in SYSCR1) in accordance with the resonator characteristics.

③ When the warm-up time has elapsed, normal operation resumes with the instruction following the STOP mode start instruction. The start is made after the prescaler and the divider of the timing generator are cleared to "0".

Table 1-1. Warm-up Time Example (at fc = 16.0 MHz, fs = 32.768 kHz)

WUT	Warm-up Time [ms]	
	Return to NORMAL mode	Return to SLOW mode
00	12.288	750
01	4.096	250
10	3.072	5.85
11	1.024	1.95

Note: The warm-up time is obtained by dividing the basic clock by the divider : therefore, the warm-up time may include a certain amount of error if there is any fluctuation of the oscillation frequency when STOP mode is released. Thus, the warm-up time must be considered an approximate value.

STOP mode can also be released by inputting low level on the $\overline{\text{RESET}}$ pin, which immediately performs the normal reset operation.

Note: When STOP mode is released with a low hold voltage, the following cautions must be observed.
The power supply voltage must be at the operating voltage level before releasing STOP mode. The $\overline{\text{RESET}}$ pin input must also be "H" level, rising together with the power supply voltage. In this case, if an external time constant circuit has been connected, the $\overline{\text{RESET}}$ pin input voltage will increase at a slower pace than the power supply voltage. At this time, there is a danger that a reset may occur if input voltage level of the $\overline{\text{RESET}}$ pin drops below the non-inverting high-level input voltage (hysteresis input).

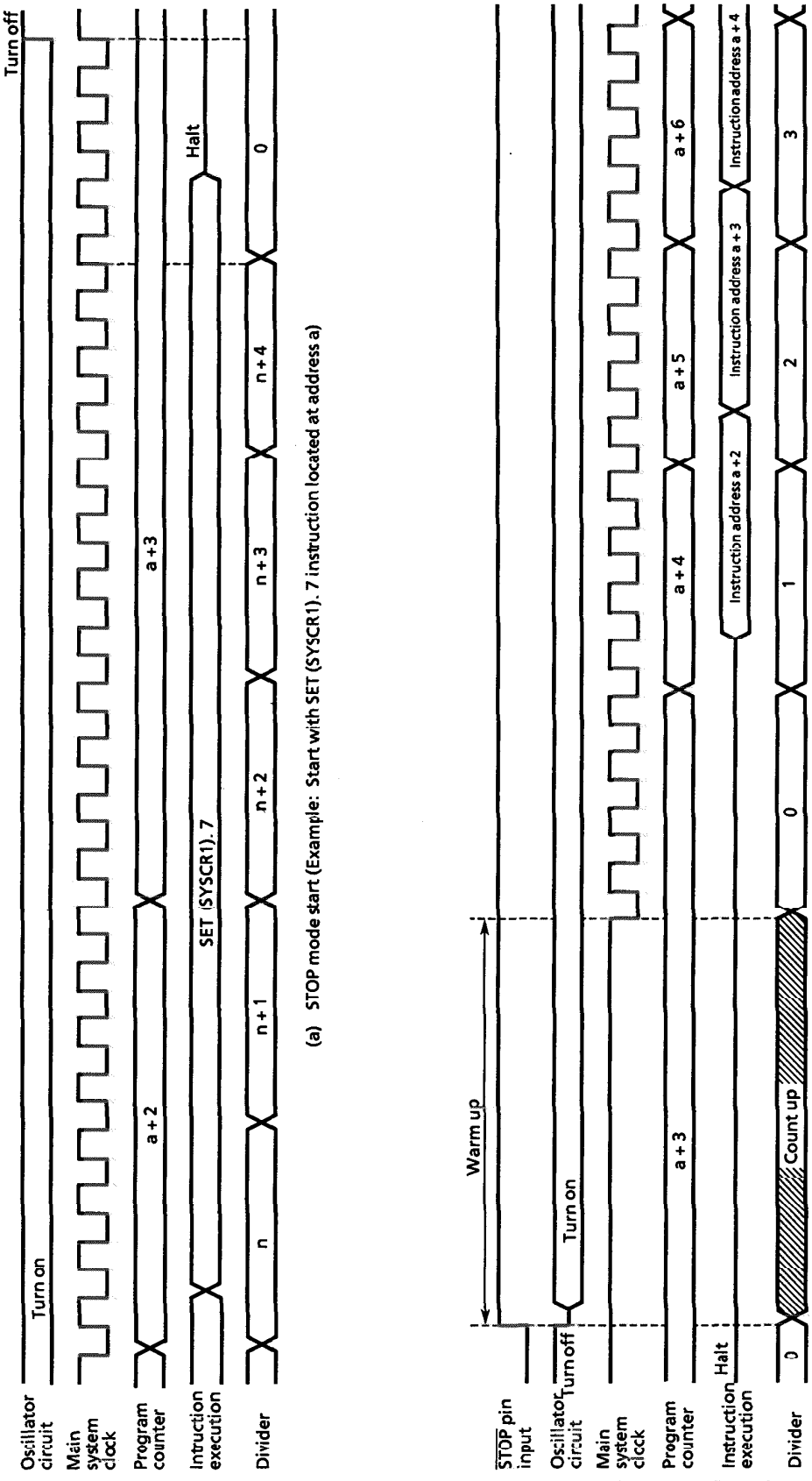


Figure 1-11. STOP Mode Start / Release

(2) IDLE mode (IDLE0, IDLE1, IDLE2, SLEEP1, SLEEP2)

IDLE mode is controlled by the system control register 2 (SYSCR2) and maskable interrupts. The following status is maintained during IDLE mode.

① Operation of the CPU and watchdog timer (WDT) is halted. On-chip peripherals continue to operate.

② The data memory, CPU registers, program status word and port output latches are all held in the status in effect before IDLE mode was entered.

③ The program counter holds the address 2 ahead of the instruction which starts IDLE mode.

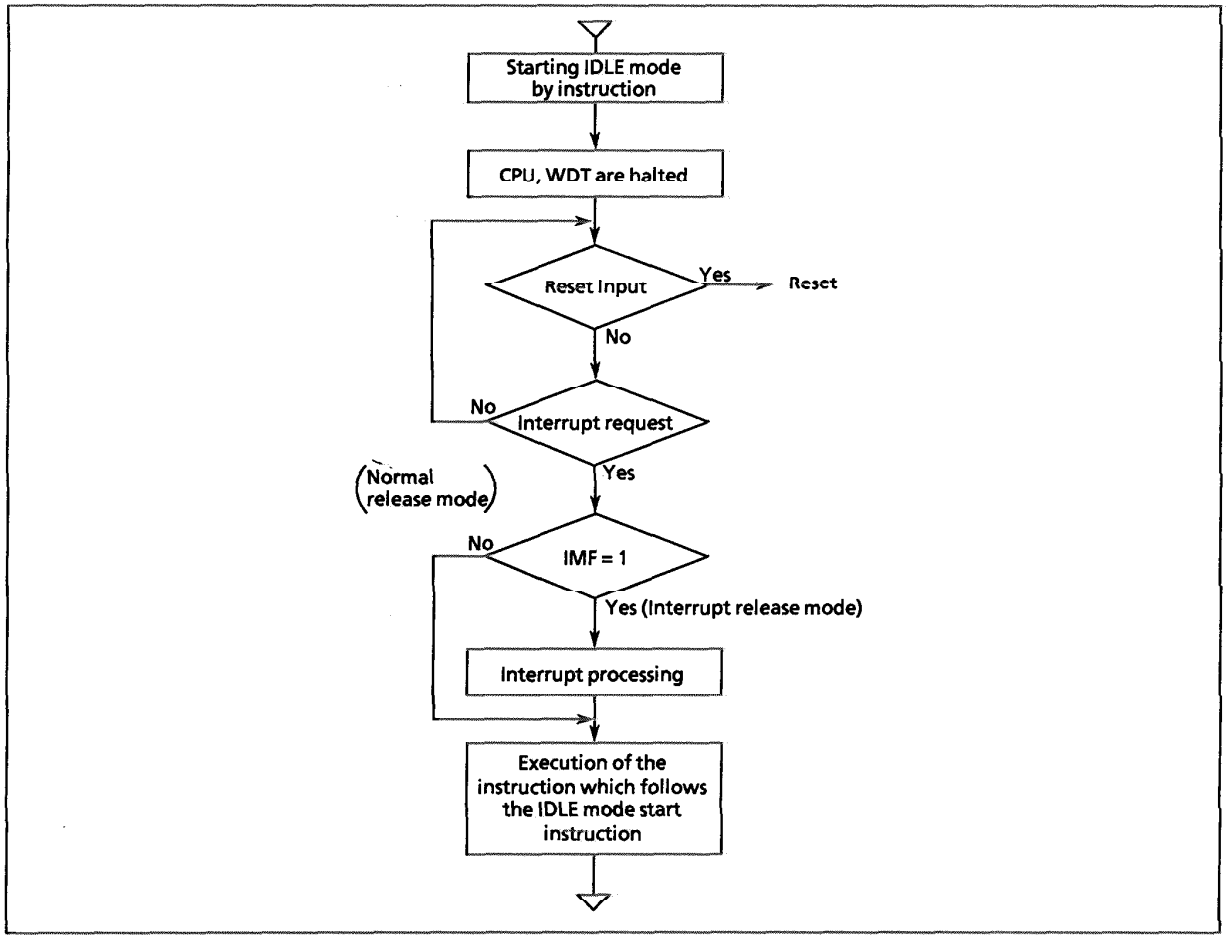


Figure 1-12. IDLE Mode

Example: Starting IDLE mode.

```
SET  (SYSCR2). 4    ;  IDLE ← 1
```

IDLE mode includes a normal release mode and an interrupt release mode. Selection is made with the interrupt master enable flag (IMF). Releasing IDLE mode returns from IDLE0/1 to NORMAL1, from IDLE2 to NORMAL2, from SLEEP0/1 to SLOW1 mode, and from SLEEP2 to SLOW2 mode.

a. Normal release mode (IMF = "0")

IDLE mode is released by any interrupt source enabled by the individual interrupt enable flag (EF). Execution resumes with the instruction following the IDLE mode start instruction . The interrupt latches (IL) of the interrupt source used for releasing must be cleared to "0" by load instructions.

b. Interrupt release mode (IMF = "1")

IDLE mode is released and interrupt processing is started by any interrupt source enabled with the individual interrupt enable flag (EF). After the interrupt is processed, the execution resumes from the instruction following the instruction which starts IDLE mode.

IDLE mode can also be released by inputting low level on the $\overline{\text{RESET}}$ pin, which immediately performs the reset operation. After reset, the TMP86CK74A/CM74A are placed in NORMAL 1 mode.

Note: When a watchdog timer interrupt is generated immediately before IDLE1 mode is started, the watchdog timer interrupt will be processed but IDLE1 mode will not be started.

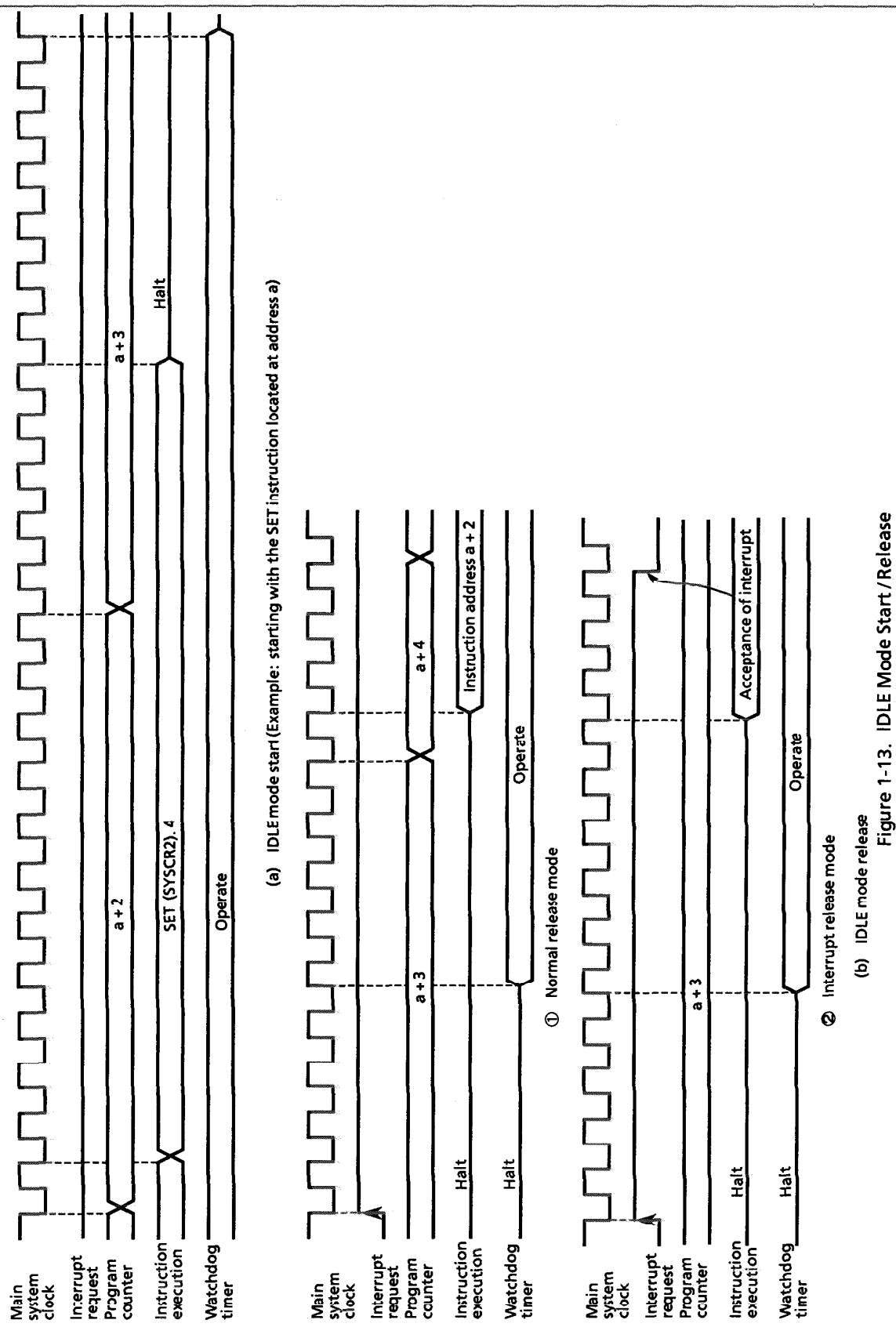


Figure 1-13. IDLE Mode Start/Release

(3) SLOW mode

SLOW mode is controlled by the system control register 2 (SYSCR2).
The following is the methods to switch the mode with the warming-up counter 2 (TC2).

a. Switching from NORMAL2 mode to SLOW1 mode

First, set SYSCK (bit 5 in SYSCR2) to switch the main system clock to the low-frequency clock for SLOW2 mode.
Next, clear XEN (bit 7 in SYSCR2) to turn off high-frequency oscillation.

Note: The high-frequency clock oscillation can be continued to return quickly to NORMAL2 mode.

When the low-frequency clock oscillation is unstable, wait until oscillation stabilizes before performing the above operations. The timer / counter 2 (TC2) can conveniently be used to confirm that low-frequency clock oscillation has stabilized.

Example1: Switching from NORMAL2 mode to SLOW1 mode.

```
SET  (SYSCR2). 5     ;  SYSCK ← 1
                        (switches the main system clock to the low-frequency
                        clock for SLOW2)
CLR  (SYSCR2). 7     ;  XEN ← 0
                        (turns off high-frequency oscillation)
```

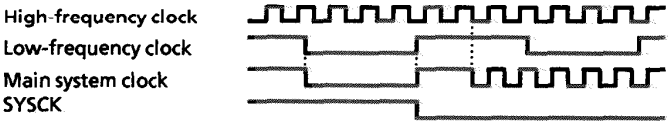
Example2: Switching to the SLOW1 mode after low-frequency clock has stabilized.

```
        LD   (TC2CR), 14H       ;  Sets mode for TC2 (16-bit TC, fs for source)
        LDW  (TC2DRL), 8000H    ;  Sets warming-up time
                                   (depend on oscillator accompanied)
        DI
        SET  (EIRH). 5          ;  Enables INTTC2
        EI
        SET  (TC2CR). 5         ;  Starts TC2
          ⋮
PINTTC2: CLR  (TC2CR). 5        ;  Stops TC2
        SET  (SYSCR2). 5        ;  SYSCK ← 1 (Switches the main system clock to the
                                   low-frequency clock)
        CLR  (SYSCR2). 7        ;  XEN ← 0 (Turns off high-frequency oscillation)
        RETI
          ⋮
VINTTC2: DW  PINTTC2            ;  INTTC2 vector table
```

b. Switching from SLOW1 mode to NORMAL2 mode

First, set XEN (bit 7 in SYSCR2) to turn on the high-frequency oscillation. When time for stabilization (warm-up) has been taken by the timer/counter 2 (TC2), clear SYSCK (bit 5 in SYSCR2) to switch the main system clock to the high-frequency clock.

Note 1: After SYSCK is cleared to "0", executing the instructions is continued by the low-frequency clock for the period synchronized with low-frequency and high-frequency clocks.



Note 2: SLOW mode can also be released by inputting low level on the RESET pin, which immediately performs the reset operation. After reset, the TMP86CK74A/CM74A are placed in NORMAL1 mode.

Example: Switching from the SLOW1 mode to the NORMAL2 mode
(fc = 16 MHz, warm-up time is 4.0 ms).

```
        SET   (SYSCR2). 7      ;  XEN ← 1 (Starts high-frequency oscillation)
        LD    (TC2CR), 10H     ;  Sets mode for TC2 (16-bit TC, fc for source)
        LD    (TC2DRH), 0F8H   ;  Sets warming-up time
        DI
        SET   (EIRH). 5        ;  Enables INTTC2
        EI
        SET   (TC2CR). 5       ;  Starts TC2
          :
PINTTC2: CLR  (TC2CR). 5       ;  Stops TC2
        CLR   (SYSCR2). 5      ;  SYSCR ← 0 (Switches the main system clock to the
                                  high-frequency clock)
        RETI
          :
VINTTC2: DW   PINTTC2          ;  INTTC2 vector table
```

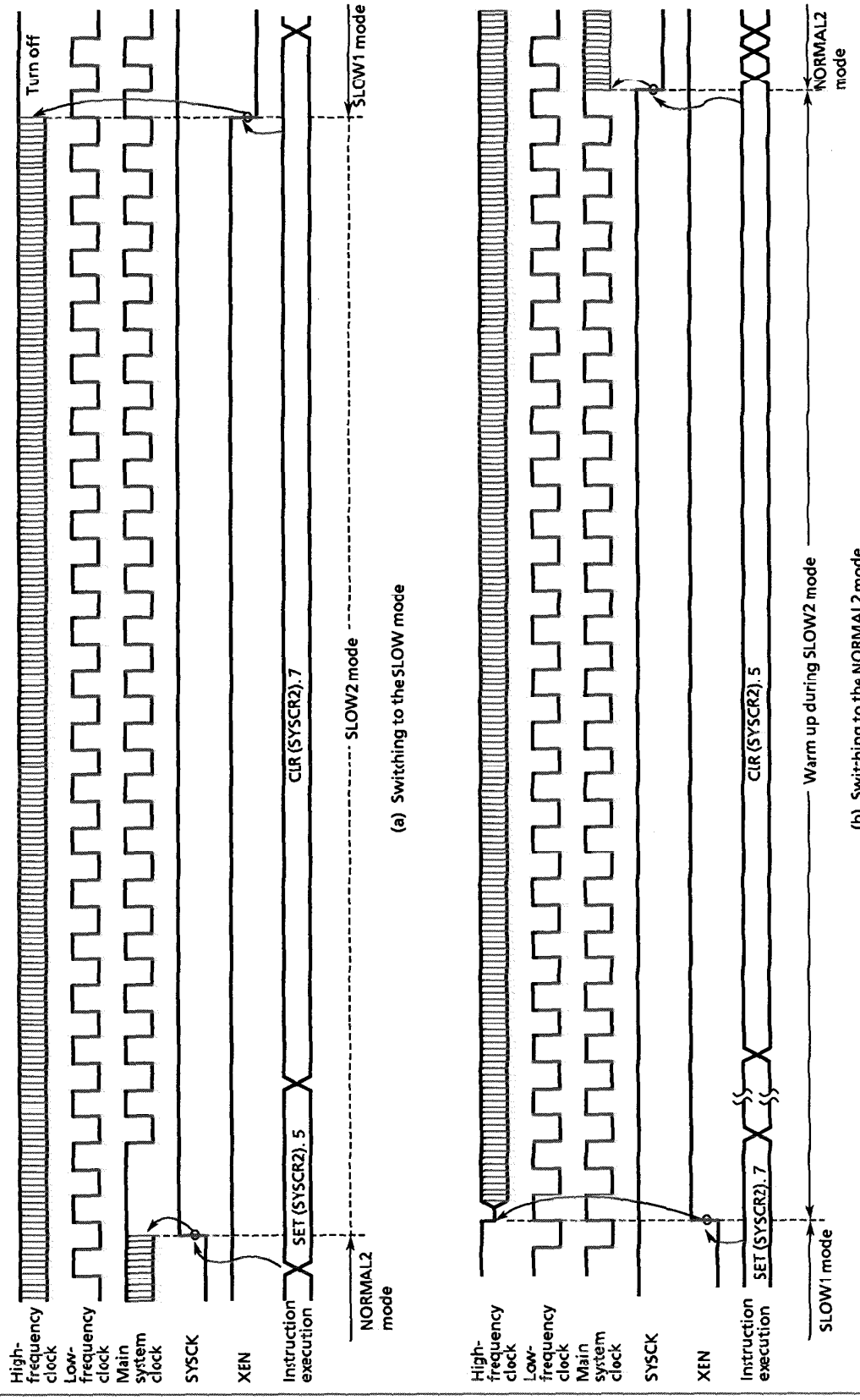


Figure 1-14. Switching between the NORMAL2 and SLOW Modes

1.5 Interrupt Control Circuit

The TMP86CK74A/CM74A have a total (Reset is exclude) of 16 interrupt sources for 17 interrupt factors; 1 of the sources are multiplexed. Multiple interrupt with priorities is available. 4 of the internal factors are non-maskable interrupts, and the rest of them are maskable interrupts.

Interrupt sources are provided with interrupt latches (IL), which hold interrupt requests, and independent vectors. The interrupt latch is set to "1" by the generation of its interrupt request which requests the CPU to accept its interrupts. Interrupts are enabled or disabled by software using the interrupt master enable flag (IMF) and interrupt enable flag (EF). If more than one interrupts are generated simultaneously, interrupts are accepted in order which is dominated by software. However, there is no priority among non-maskable interrupt factors.

Table 1-2. Interrupt Sources

Interrupt Factors		Enable Condition	Interrupt Latch	Vector Address	Priority
Internal/ External	(Reset)	Non-maskable	—	$FFFE_H$	High 1
Internal	INTSWI (Software interrupt)	Non-maskable	—	$FFFC_H$	2
Internal	INTUNDEF (Executed the undefined Instruction interrupt)	Non-maskable	—	$FFFC_H$	2
Internal	INTATRAP (Address trap interrupt)	Non-maskable	IL_2	$FFFA_H$	2
Internal	INTWDT (Watchdog timer interrupt)	Non-maskable	IL_3	$FFF8_H$	2
External	$\overline{INT0}$ (External interrupt 0)	IMF · EF_4 = 1 INT0EN = 1	IL_4	$FFF6_H$	5
Internal	INTTC1 (16-bit timer TC1 interrupt)	IMF · EF_5 = 1	IL_5	$FFF4_H$	6
External	INT1 (External interrupt 1)	IMF · EF_6 = 1	IL_6	$FFF2_H$	7
Internal	INTTBT (Time base timer interrupt)	IMF · EF_7 = 1	IL_7	$FFF0_H$	8
Internal	INTTC3 (8-bit timer TC3 interrupt)	IMF · EF_8 = 1	IL_8	$FFEE_H$	9
Internal	INTSIO (High speed SIO interrupt)	IMF · EF_9 = 1	IL_9	$FFEC_H$	10
Internal	INTTC4 (8-bit timer TC4 interrupt)	IMF · EF_{10} = 1	IL_{10}	$FFEA_H$	11
External	INT3 (External interrupt 3)	IMF · EF_{11} = 1	IL_{11}	$FFE8_H$	12
External	INT4 (External interrupt 4)	IMF · EF_{12} = 1	IL_{12}	$FFE6_H$	13
Internal	INTTC2 (16-bit timer TC2 interrupt)	IMF · EF_{13} = 1	IL_{13}	$FFE4_H$	14
External	$\overline{INT5}$ (External interrupt 5)	IMF · EF_{14} = 1	IL_{14}	$FFE2_H$	15
Internal	INTADC (AD converter interrupt)	IMF · EF_{15} = 1	IL_{15}	$FFE0_H$	Low 16
External	INT2 (External interrupt 2)				

Note 1: The interrupt factor of INTADC and INT2 shares therm interrupt source; the factor is selected on the register INTSEL.

Note 2: 2 alternatives are to bo chosen in case INTATRAP (address trap interrupt) is executed: interrupt or reset.

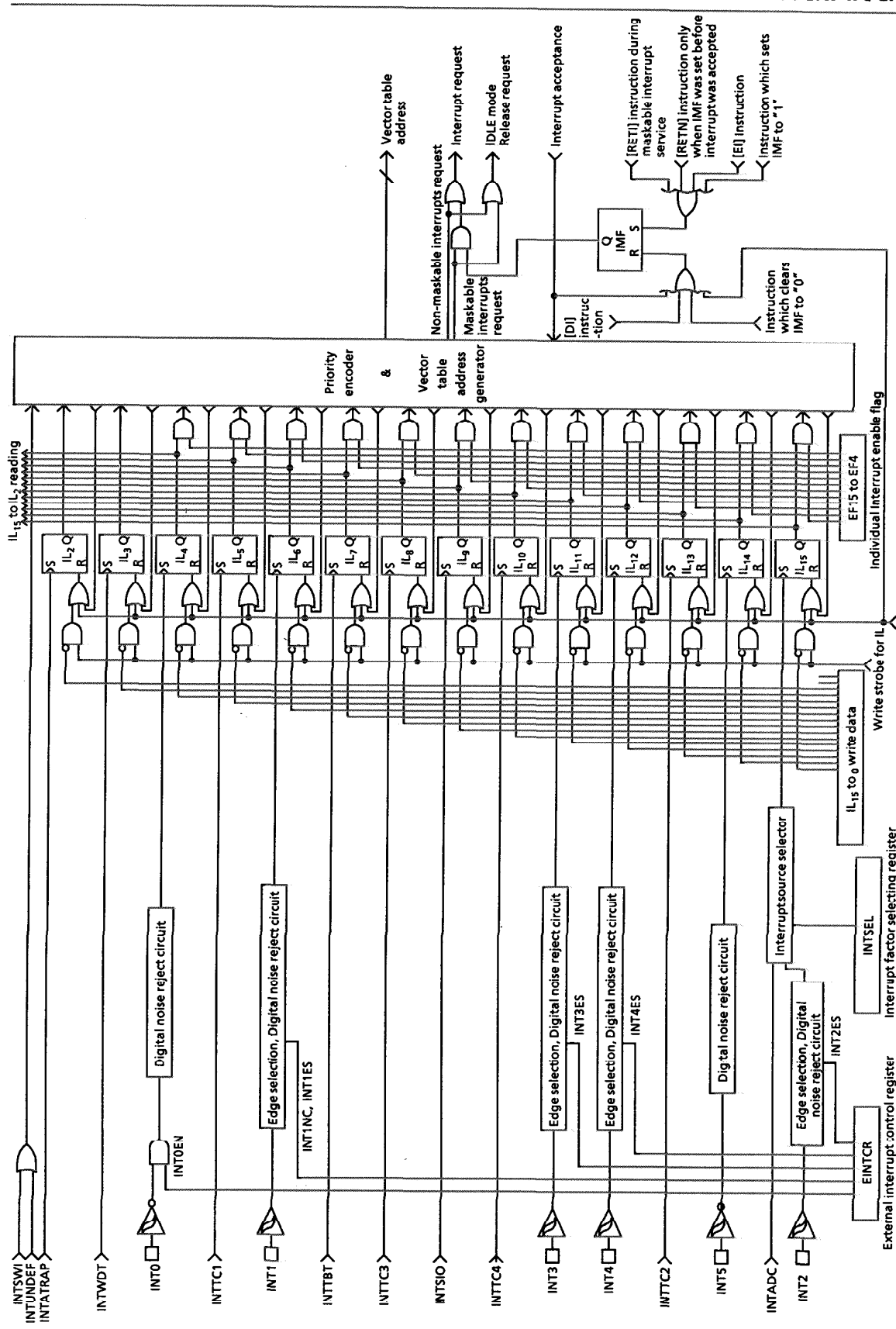


Figure 1-15. Interrupt Controller Block Diagram

(1) Interrupt Latches (IL_{15} to IL_2)

An interrupt latch is provided for each interrupt source, except for a software interrupt. When interrupt request is generated, the latch is set to "1", and the CPU is requested to accept the interrupt if its interrupt is enabled. All interrupt latches are initialized to "0" during reset.
The interrupt latches are located on address $003C_H$ and $003D_H$ in SFR area. Except for IL_3 and IL_2, each latch can be cleared to "0" individually by instruction (However, the read-modify-write instructions such as bit manipulation or operation instructions cannot be used. Interrupt request would be cleared inadequately if interrupt is requested while such instructions are executed.). Thus interrupt request can be canceled /initialized by software.
Interrupt latches are not set to "1" by an instruction. Since interrupt latches can be read, the status for interrupt requests can be monitored by software.

Example 1: Clears interrupt latches

```
DI                                  ;  IMF = "0"
LDW (ILL), 1110100000111111B        ;  IL12, IL10 to IL6 ← 0
LD  (ILH), 11111000B                ;  IL10 to IL8 ← 0
EI                                  ;  IMF = "1"
```

Example 2: Reads interrupt latches

```
LD  WA, (ILL)                       ;  W ← ILH, A ← ILL
```

Example 3: Tests an interrupt latches

```
TEST (ILL). 7                       ;  if IL7=1 then jump
JR  F, SSET
```

(2) Interrupt Enable Register (EIR)

The interrupt enable register (EIR) enables and disables the acceptance of interrupts, except for the non-maskable interrupts (software interrupt, undefined instruction interrupt, address trap interrupt and watchdog interrupt). Non-maskable interrupt is accepted regardless of the contents of the EIR.
The EIR consists of an interrupt master enable flag (IMF) and the individual interrupt enable flags (EF). These registers are located on address $003A_H$ and $003B_H$ in SFR area, and they can be read and written by an instructions (including read-modify-write instructions such as bit manipulation or operation instructions).

a) Interrupt master enable flag (IMF)

The interrupt enable register (IMF) enables and disables the acceptance of the whole maskable-interrupt. While IMF="0", all maskable interrupts are not accepted regardless of the status on each individual interrupt enable flag (EF). By setting IMF to "1", the interrupt becomes acceptable if the individuals are enabled. When an interrupt is accepted, IMF is cleared to "0" after the latest status on IMF is stacked. Thus the maskable interrupts which follow are disabled. By executing return interrupt instruction [RETI/RETN], the stacked data, which was the status before interrupt acceptance, is loaded on IMF again.
The IMF is located on bit0 in EIRL (address: $003A_H$ in SFR), and can be read and written by an instruction. The IMF is normally set and cleared by [EI] and [DI] instruction respectively. During reset, the IMF is initialized to "0", and maskable interrupts are not accepted until it is set to "1".

b) Individual interrupt enable flags (EF_{15} to EF_4)

Each of these flags enables and disables the acceptance of its maskable interrupt. Setting the corresponding bit of an individual interrupt enable flag to "1" enables acceptance of its interrupt, and setting the bit to "0" disables acceptance. The individual interrupt enable flags (EF_{15} to EF_4) are located on EIRL to EIRH (address: $003A_H$ to $003B_H$ in SFR), and can be read and written by an instruction. During reset, all the individual interrupt enable flags (EF_{15} to EF_4) are initialized to "0" and all maskable interrupts are not accepted until they are set to "1".

Example 1: Enables interrupts individually and sets IMF

```
DI                                  ; IMF ← 0
LDW (EIRL), 1110100010100000B       ; EF15 to EF13, EF11, EF7, EF5 ← 1
      :                               Note: IMF is not set.
      :
EI                                  ; IMF ← 1
```

Example 2: C compiler description example

```
unsigned int __io (3AH) EIRL        ; /* 3AH shows EIRL address */
__DI ( );
EIRL = 10100000B;
      :
__EI ( );
```

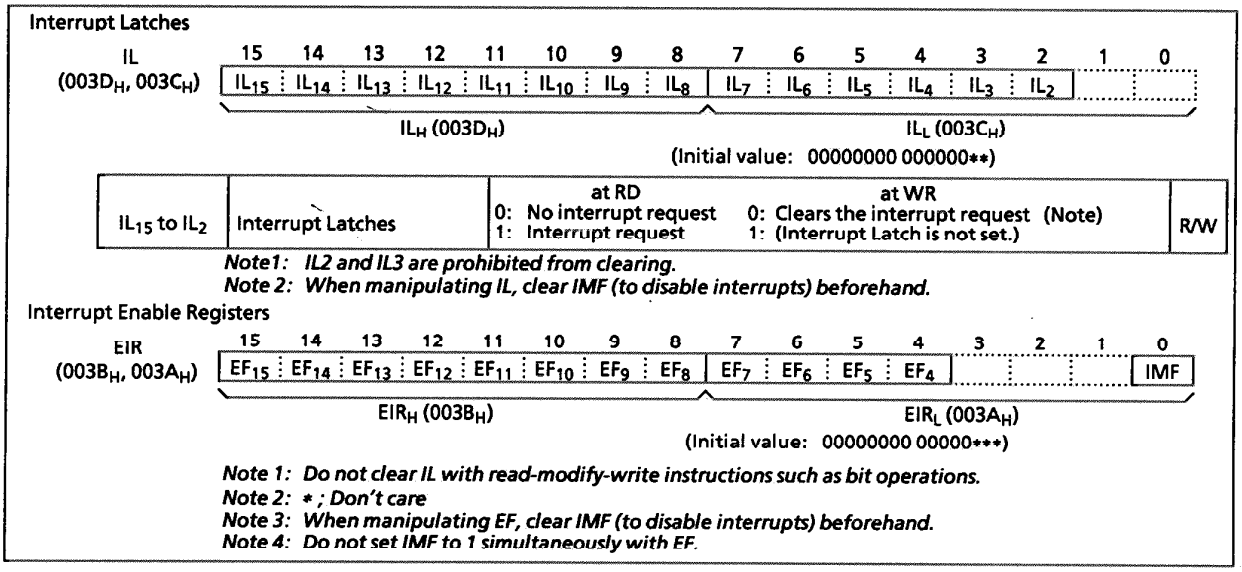


Figure 1-16. Interrupt Latch (IL), Interrupt Enable Registers (EIR)

(3) Selecting interrupt factor (INTSEL)

Each interrupt factor, that shares its interrupt source with other factors, enables its interrupt latch (IL) only if it is selected on INTSEL. The interrupt controller does not hold the interrupt request, while the factor generates the interrupt request is not selected on INTSEL. Therefore, set INTSEL appropriately befor interrup factors arises.

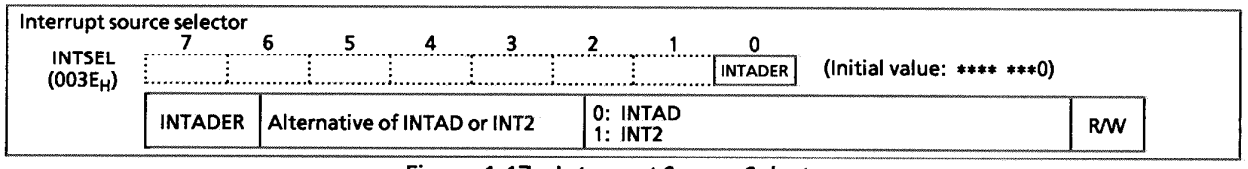


Figure 1-17. Interrupt Source Selector

1.5.1 Interrupt Sequence

An interrupt request, which raised interrupt latch, is held, until interrupt is accepted or interrupt latch is cleared to "0" by resetting or an instruction. Interrupt acceptance sequence requires 8 machine cycles (4 μs at 8.0 MHz) after the completion of the current instruction. The interrupt service task terminates upon execution of an interrupt return instruction [RETI] (for maskable interrupts) or [RETN] (for non-maskable interrupts). Figure 1-18 shows the timing chart of interrupt acceptance processing.

(1) Interrupt acceptance processing is packaged as follows.

a) The interrupt master enable flag (IMF) is cleared to "0" in order to disable the acceptance of any following interrupt.

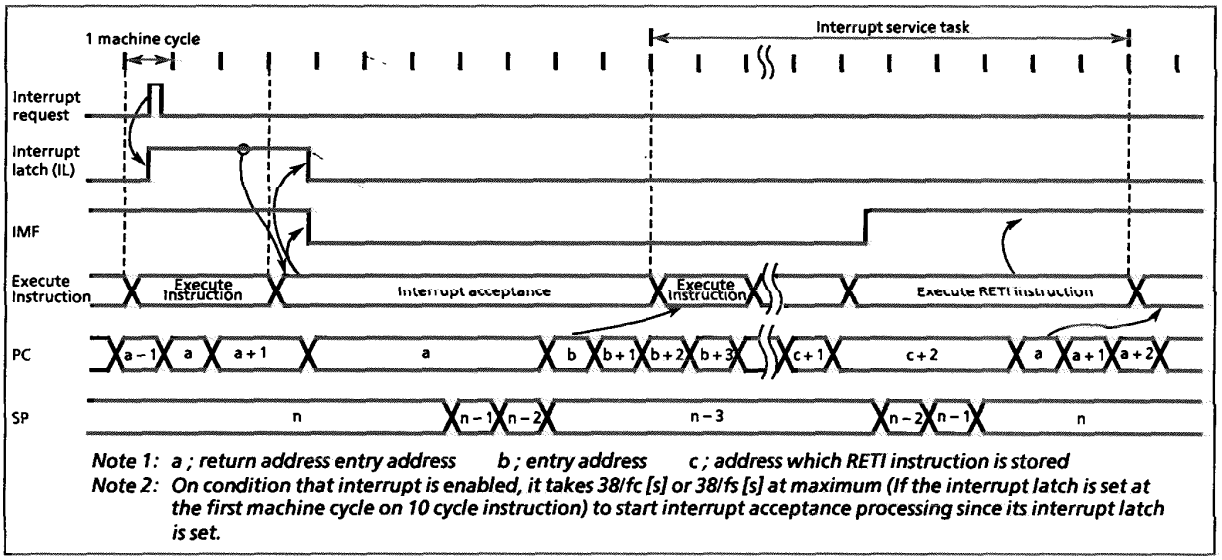
b) The interrupt latch (IL) for the interrupt source accepted is cleared to "0".

c) The contents of the program counter (PC) and the program status word, including the interrupt master enable flag (IMF), are saved (pushed) on the stack in sequence of PSW+IMF, PCH, PCL. Meanwhile, the stack pointer (SP) is decremented by 3.

d) The entry address (interrupt vector) of the corresponding interrupt service program, loaded on the vector table, is transferred to the program counter.

e) The instruction stored at the entry address of the interrupt service program is executed.

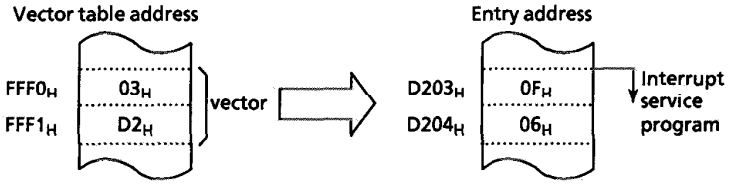
Note: When the contents of PSW are saved on the stack, the contents of IMF are also saved.



Note 1: a ; return address entry address b ; entry address c ; address which RETI instruction is stored
Note 2: On condition that interrupt is enabled, it takes 38/fc [s] or 38/fs [s] at maximum (If the interrupt latch is set at the first machine cycle on 10 cycle instruction) to start interrupt acceptance processing since its interrupt latch is set.

Figure 1-18. Timing chart of Interrupt Acceptance/Return Interrupt instruction

Example: Correspondence between vector table address for INTTBT and the entry address of the interrupt service program



A maskable interrupt is not accepted until the IMF is set to "1" even if the maskable interrupt higher than the level of current servicing interrupt is requested.
In order to utilize nested interrupt service, the IMF is set to "1" in the interrupt service program. In this case, acceptable interrupt sources are selectively enabled by the individual interrupt enable flags. To avoid overloaded nesting, clear the individual interrupt enable flag whose interrupt is currently serviced, before setting IMF to "1". As for non-maskable interrupt, keep interrupt service shorten compared with length between interrupt requests; otherwise the status cannot be recovered as non-maskable interrupt would simply nested.

(2) Saving/Restoring general -purpose registers

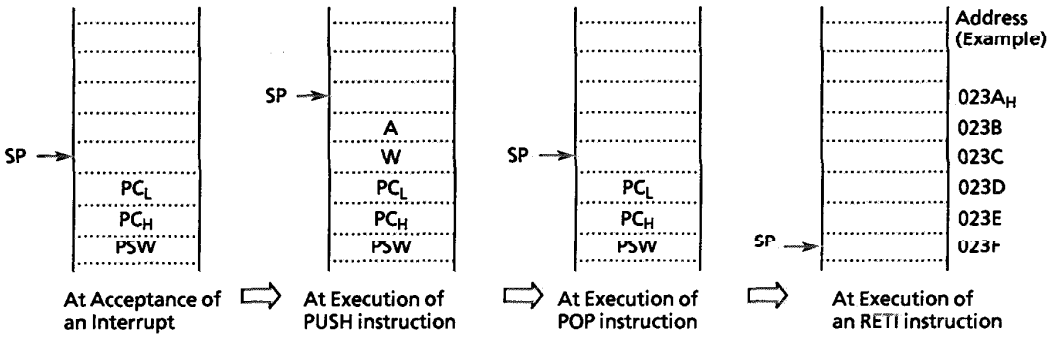
During interrupt acceptance processing, the program counter (PC) and the program status word (PSW, includes IMF) are automatically saved on the stack, but the accumulator and others are not. These registers are saved by software if necessary. When multiple interrupt services are nested, it is also necessary to avoid using the same data memory area for saving registers. The following methods are used to save/restore the general-purpose registers.

a) using PUSH and POP instructions

To save only a specific register, PUSH and POP instructions are available.

Example: save/store register using PUSH and POP instructions

```
PINTxx: PUSH   WA          ;  Save WA register
        (interrupt processing)
        POP    WA          ;  Restore WA register
        RETI               ;  RETURN
```



b) using data transfer instructions

To save only a specific register without nested interrupts, data transfer instructions are available.

Example: save/store register using data transfer instructions

```
PINTxx: LD   (GSAVA), A          ;  Save A register
        (interrupt processing)
        LD   A, (GSAVA)          ;  Restore A register
        RETI                     ;  RETURN
```

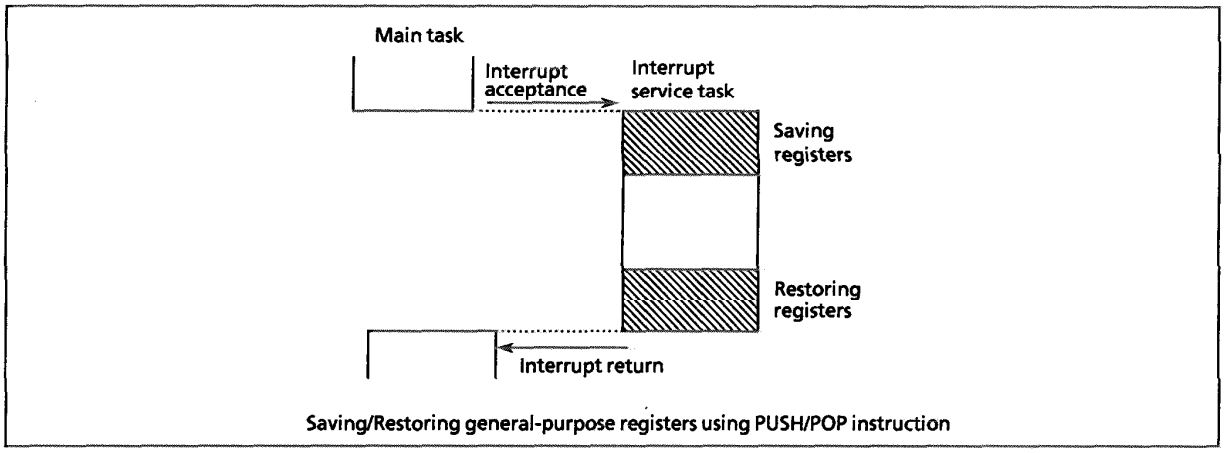


Figure 1-19. Saving/Restoring general-purpose registers under interrupt processing

(3) Interrupt return

Interrupt return instructions [RETI]/[RETN] perform as follows.

[RETI] / [RETN] Interrupt Return
① Program Counter (PC) and program status word (PSW, includes IMF) are restored from the stack.
② Stack pointer (SP) is incremented by 3.

As for Address Trap interrupt (INTATRTAP), it is required to alter stacked data for program counter (PC) to restarting address, during interrupt service program. Otherwise returning interrupt causes INTATRAP again. When interrupt acceptance processing has completed, stacked data for PC_L and PC_H are located on address (SP+1) and (SP+2) respectively.

Note: If [RETN] is executed with the above data unaltered, the program returns to the address trap area and INTATRAP occurs again.

Example 1: returning from address trap interrupt (INTATRAP) service program

```
PINTxx: POP   WA                  ;  Recover SP by 2
        LD    WA, Return Address  ;
        PUSH  WA                  ;  Alter stacked data
        (interrupt processing)
        RETN                      ;  RETURN
```

Example 2: restarting without returning interrupt
(In this case, PSW (includes IMF) before interrupt acceptance is discarded.)

```
PINTxx: INC   SP                  ;  Recover SP by 3
        INC   SP                  ;
        INC   SP                  ;
        (interrupt processing)
        LD    EIRL, data          ;  Set IMF to "1" or clear it to "0"
        JP    Restart Address     ;  Jump into restarting address
```

Note: It is recommended that stack pointer be return to rate before INTATRAP (increment 3 times), if return interrupt instruction [RETN] is not utilized during interrupt service program under INTATRAP (such as Example 2).

Interrupt requests are sampled during the final cycle of the instruction being executed. Thus, the next interrupt can be accepted immediately after the interrupt return instruction is executed.

Note: When the interrupt processing time is longer than the interrupt request generation time, the interrupt service task is performed but not the main task.

1.5.2 Software interrupt (INTSW)

Executing the [SWI] instruction generates a software interrupt and immediately starts interrupt processing (INTSW is highest prioritized interrupt).
Use the [SWI] instruction only for detection of the address error or for debugging.

① Address error detection

FF_H is read if for some cause such as noise the CPU attempts to fetch an instruction from a non-existent memory address during single chip mode. Code FF_H is the SWI instruction, so a software interrupt is generated and an address error is detected. The address error detection range can be further expanded by writing FF_H to unused areas of the program memory. Address-trap reset is generated in case that an instruction is fetched from RAM or SFR areas.

② Debugging

Debugging efficiency can be increased by placing the SWI instruction at the software break point setting address.

1.5.3 Undefined instruction interrupt (INTUNDEF)

Taking code which is not defined as authorized instruction for instruction causes INTUNDEF. INTUNDEF is generated when the CPU fetches such a code and tries to execute it. INTUNDEF is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTUNDEF interrupt process starts, soon after it is requested.

Note: The undefined instruction interrupt (INTUNDEF) forces CPU to jump into vector address, as software interrupt (SWI) does.

1.5.4 Address trap interrupt (INTATRAP)

Fetching instruction from unauthorized area for instructions (address trapped area) causes reset-output or address trap interrupt (INTATRAP). INTATRAP is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTATRAP interrupt process starts, soon after it is requested.
The address trapped area is alternative: SFR and RAM, or SFR only.

Note: The operating mode under address trapped, whether to be reset-output or interrupt processing, is selected on watchdog timer control register (WDTCR).

1.5.5 External Interrupts

The TMP86CK74A/CM74A have five external interrupt inputs. These input are equipped with digital noise reject circuits (pulse input of less than a certain time are eliminated as noise).
Edge selection is also possible with INT1 to INT4. The INT0/P50 pin can be configured as either an external interrupt input pin or an input/output, and is configured as an input port during reset.
Edge selection, noise reject control and INT0/P50 pin function selection are performed by the external interrupt control register (EINTCR).

Table 1-3. External Interrupts

Source	Pin	Secondary function pin	Enable conditions	Edge	Digital noise reject
INT0	$\overline{INT0}$	P50	IMF = 1, EF_4 = 1, INT0EN = 1	Falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 6/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulse of 3/fs [s] or more are consiered to be signals.
INT1	INT1	P51	IMF · EF_6 = 1	Falling edge or rising edge	Pulses of less than 15/fc or 63/fc [s] are eliminated as noise. Pulses of 48/fc or 192/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs[s] are eliminated as noise. Pulse of 3/fs [s] or more are consiered to be signals.
INT2	INT2	P52	IMF · EF_{15} = 1 INTAD = 1		Pulses of less than 7/fc [s] are eliminated as noise. Pulses of 24/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulse of 3/fs[s] or more are consiered to be signals.
INT3	INT3	P11/TC3	IMF · EF_{11} = 1		
INT4	INT4	P14	IMF · EF_{12} = 1	Falling edge or rising edge or falling/rising edge or "H" level	
INT5	$\overline{INT5}$	P20 / $\overline{STOP}$	IMF · EF_{14} = 1	Falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 6/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulse of 3/fs [s] or more are consiered to be signals.

Note 1: If a noiseless signal is input to the external interrupt pin in the NORMAL 1/2 or IDLE 1/2 mode, the maximum time from the edge of input signal until the IL is set is as follows :
① INT1 pin 49/fc [s] (INT1NC = 1), 193/fc [s] (INT1NC = 0)
② INT2, INT3, INT4 pins 25/fc [s]
Note 2: Even if the falling edge of $\overline{INT0}$ pin input is detected at INT0EN = 0, the interrupt latch IL_4 is not set.
Note 3: When data changed and did a change of I/O when used external interrupt ports as a normal ports, interrupt request signal occurs incorrectly. Handling of prohibition of external interrupt control register (EINTCR) is necessary.

External Interrupt Control Register

EINTCR (0037_H)

7	6	5	4	3	2	1	0	(Initial value: 0000 000*)
INT1NC	INT0EN	INT4ES		INT3ES	INT2ES	INT1ES		

INT1NC	Noise reject time select of INT1	0: Pulses of less than 63/fc [s] are eliminated as noise 1: Pulses of less than 15/fc [s] are eliminated as noise	R/W
INT0EN	P50 /$\overline{INT0}$ pin configuration	0: P50 Input/Output port 1: $\overline{INT0}$ pin (Port P50 should be set to on input mode)	
INT4ES	INT4 edge select	00: Rising edge 01: Falling edge 10: Rising/falling edge 11: "H" level	
INT3ES INT2ES INT1ES	INT3~INT1 edge select	0: Rising edge 1: Falling edge	

*Note 1: fc; High-frequency clock [Hz] *; Don't care*

Note 2: Before rewriting the External Interrupt Control Register (EINTCR), be sure to disable external interrupts by using the Interrupt Enable Register (EIR). This is so recommended because the noise canceler may not operate normally before or after rewriting the register.

Note 3: When changing the main system clocks (SYSCR2<SYSCK>), the noise canceller may not operate normally before or after operation modes change. Therefore, it is recommended that external interrupts be disabled by using the Interrupt Enable Register (EIR).

Figure 1-20. External Interrupt Control Register

1.6 Reset Circuit

The TMP86CK74A/CM74A have four types of reset generation procedures: an external reset input, an address trap reset output, a watchdog timer reset output and a system clock reset output. Table 1-4 shows on-chip hardware initialization by reset action.
The malfunction reset output circuit such as watchdog timer reset, address trap reset and system clock reset is not initialized when power is turned on. The $\overline{\text{RESET}}$ pin can output level "L" at the maximum 24/fc [s] (1.5 μs at 16.0 MHz) when power is turned on.

Table 1-4. Initializing Internal Status by Reset Action

On-chip hardware	Initial value	On-chip hardware	Initial value
Program counter (PC)	($FFFE_H$)	Prescaler and Divider of timing generator	0
Stack pointer (SP)	Not initialized		
General-purpose registers (W, A, B, C, D, E, H, L, IX, IY)	Not initialized		
Jump status flag (JF)	Not initialized	Watchdog timer	Enable
Zero flag (ZF)	Not initialized	Output latches of I/O ports	Refer to I/O port circuitry
Carry flag (CF)	Not initialized		
Half carry flag (HF)	Not initialized		
Sign flag (SF)	Not initialized		
Overflow flag (VF)	Not initialized		
Interrupt master enable flag (IMF)	0		
Interrupt individual enable flags (EF)	0	Control registers	Refer to each of control register
Interrupt latches (IL)	0		
		RAM	Not initialized

1.6.1 External Reset Input

The $\overline{\text{RESET}}$ pin contains a Schmitt trigger (hysteresis) with an internal pull-up resistor.
When the $\overline{\text{RESET}}$ pin is held at "L" level for at least 3 machine cycles (12/fc [s]) with the power supply voltage within the operating voltage range and oscillation stable, a reset is applied and the internal state is initialized.
When the $\overline{\text{RESET}}$ pin input goes high, the reset operation is released and the program execution starts at the vector address stored at addresses FFFE to $FFFF_H$.

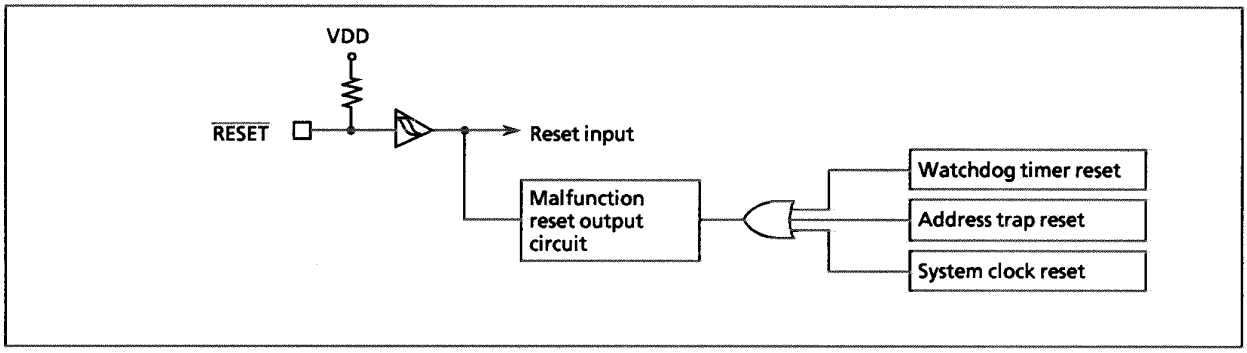
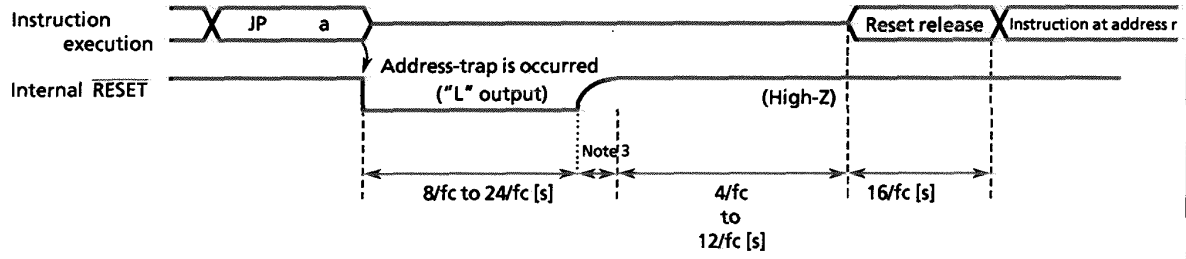


Figure 1-21. Reset Circuit

1.6.2 Address-trap-reset

If the CPU should start looping for some cause such as noise and an attempt be made to fetch an instruction from the on-chip RAM (when ATAS is set to "1") or the SFR area, address-trap-reset will be generated. Then, the $\overline{\text{RESET}}$ pin output will go low. The reset time is about 8/fc to 24/fc [s] (0.5 to 1.5 μs at 16.0 MHz).



Note 1: Address "a" is in the SFR or on-chip RAM (ATAS = 1) space.
Note 2: During reset release, reset vector "r" is read out, and an instruction at address "r" is fetched and decoded.

Figure 1-22. Address-Trap-Reset

Note: The operating mode under address trapped is alternative of reset or interrupt. The address trap area is alternative.

1.6.3 Watchdog timer reset

Refer to Section "2.5 Watchdog Timer".

1.6.4 System-clock-reset

Clearing both XEN and XTEN (bits 7 and 6 in SYSCR2) to "0", clearing XEN to "0" when SYSCK=0, or clearing XTEN to "0" when SYSCK=1 stops system clock, and causes the microcomputer to deadlock. This can be prevented by automatically generating a reset signal whenever XEN=XTEN=0, XEN=SYSCK=0, or XTEN=0 / SYSCK=1 is detected to continue the oscillation. The, the $\overline{\text{RESET}}$ pin output goes low from high-impedance. The reset time is about 8/fc to 24/fc [s] (0.5 to 1.5 μs at 16.0 MHz).

2. On-Chip Peripherals Functions

2.1 Special Function Register (SFR)

The TMP86CK74A/CM74A adopt the memory mapped I/O system, and all peripheral control and data transfers are performed through the special function register (SFR) and data buffer register (DBR). The SFR is mapped on address 0000_H to $003F_H$. DBR is mapped on address $0F80_H$ to $0FFF_H$.

Address	Read	Write
0000_H	P0DR (P0 port output latch)	
01	P1DR (P1 port output latch)	
02	P2DR (P2 port output latch)	
03	P3DR (P3 port output latch)	
04	P4DR (P4 port output latch)	
05	P5DR (P5 port output latch)	
06	P6DR (P6 port output latch)	
07	P7DR (P7 port output latch)	
08	P8DR (P8 port output latch)	
09	P9DR (P9 port output latch)	
0A	P0CR (P0 port control register)	
0B	P1OUTCR (P1 port control register)	
0C	P4CR1 (P4 port control register 1)	
0D	P5CR (P5 port control register)	
0E	ADCCR1 (AD control register 1)	
0F	ADCCR2 (AD control register 2)	
10	TC3DRA (Timer counter 3 data register A)	
11	TC3DRB (Timer Counter 3data register B)	–
12	TC3CR (Timer Counter 3 control register)	
13	TC2CR (Timer Counter 2 control register)	
14	TC4CR (Timer Counter 4 control register)	
15	P1PRD (P1 port input data)	
16	P2PRD (P2 port input data)	
17	P3PRD (P3 port input data)	
18	TC4DR (Timer Counter 4 data register)	
19	SIOCR1 (HSIO control register 1)	
1A	SIOCR2 (HSIO control register 2)	
1B	SIOSR (HSIO status register)	–
1C	SIOBUF (HSIO data buffer)	
1D	PDDR (PD port output latch)	
1E	reserved	
1F	reserved	

Address	Read	Write
0020_H	TC1DRAL (Timer Counter 1 data register A "L")	
21	TC1DRAH (Timer Counter 1 data register A "H")	
22	TC1DRBL (Timer Counter 1 data register B "L")	
23	TC1DRBH (Timer Counter 1 data register B "H")	
24	TC2DRL (Timer Counter 2 data register "L")	
25	TC2DRH (Timer Counter 2 data register "H")	
26	ADCDR2 (AD converter register 2)	
27	ADCDR1 (AD converter register 1)	
28	P4CR2 (P4 port control register 2)	
29	TC3SEL (Timer Counter 3 input control register)	
2A	VFTCR1 (VFT control register 1)	
2B	VFTCR2 (VFT control register 2)	
2C	VFTCR3 (VFT control register 3)	
2D	VFTSR (VFT status register)	–
2E	reserved	
2F	reserved	
30	reserved	
31	–	STOPCR (Key on wake up control register)
32	TC1CR (Timer Counter 1 control register)	
33	reserved	
34	–	WDTCR1 (watchdog timer control register 1)
35	–	WDTCR2 (watchdog timer control register 2)
36	TBTCR (TBT/TG/DVO control register)	
37	EINTCR (External interrupt control register)	
38	SYSCR1 (System control register 1)	
39	SYSCR2 (System control register 2)	
3A	EIR_L (The lower of interrupt enable register)	
3B	EIR_H (The upper of interrupt enable register)	
3C	IL_L (The lower of interrupt latch)	
3D	IL_H (The upper of interrupt latch)	
3E	INTSEL (Interrupt source selector)	
3F	PSW (Program status word)	

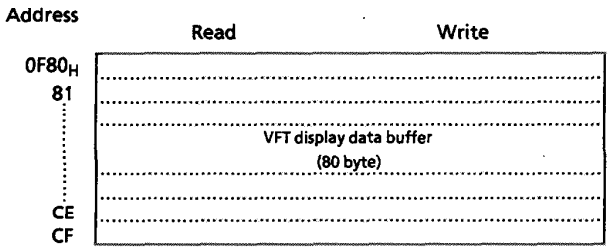
Note 1: Do not access reserved area by software

Note 2: —; Cannot be accessed

Note 3: Write only register and interrupt latches cannot use the read-modify-write instructions (bit manipulation instructions such as SET, CLR, etc. and logical operation such as AND, OR, etc.)

Figure 2-1 (a). The Special Function Register

VFT data buffer



Note 1: Do not access reserved area by software
Note 2: —; Cannot be accessed
Note 3: Write only register and interrupt latches cannot use the read-modify-write instructions (bit manipulation instructions such as SET, CLR, etc. and logical operation such as AND, OR, etc.)

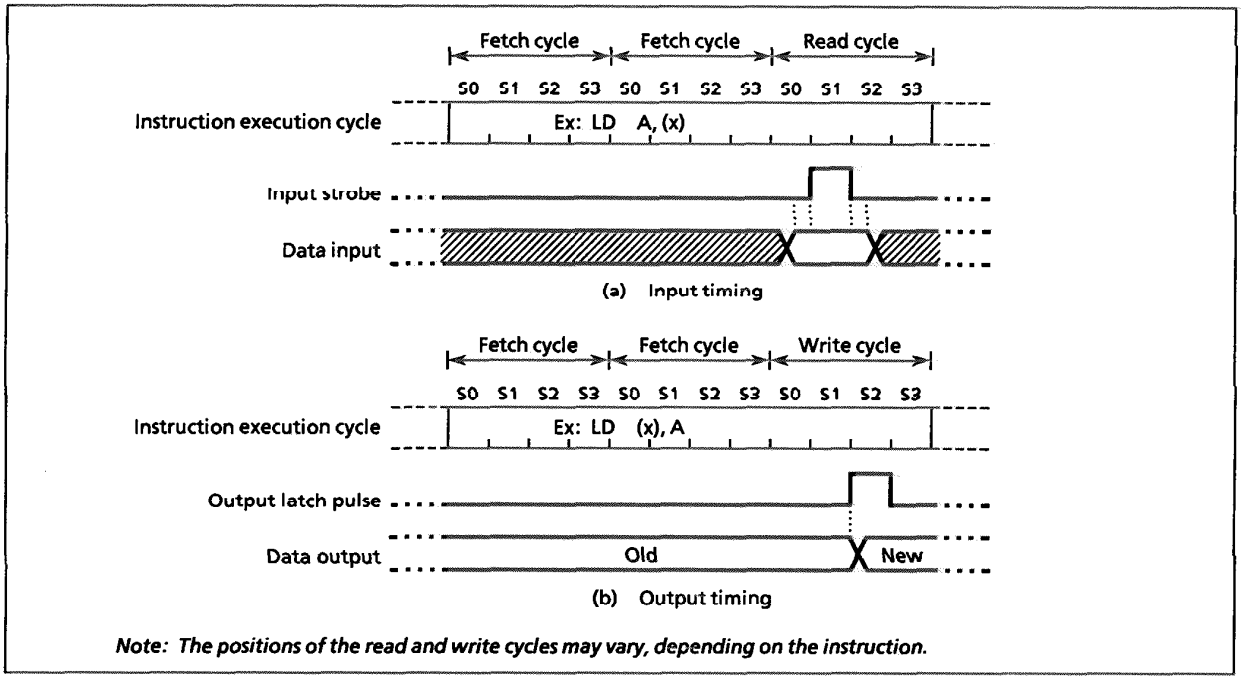
Figure 2-1 (b). The Data Buffer Register (DBR)

2.2 I/O Ports

The TMP86CK74A/CM74A have 11 parallel input/output ports (70 pins) as follows.

	Primary Functions	Secondary Functions
Port P0	8-bit I/O port	–
Port P1	8-bit I/O port	External interrupt input, timer/counter input/output, Serial interface input/output
Port P2	3-bit I/O port	Low-frequency resonator connections, external interrupt input, STOP mode release signal Input
Port P3	2-bit I/O port	–
Port P4	8-bit I/O port	Analog input, STOP mode release signal input
Port P5	4-bit I/O port	External interrupt input
Port P6	8-bit I/O port	VFT output
Port P7	8-bit I/O port	VFT output
Port P8	8-bit I/O port	VFT output
Port P9	8-bit I/O port	VFT output
Port PD	5-bit I/O port	VFT output

Each output port contains a latch, which holds the output data. All input ports do not have latches, so the external input data should be externally held until the input data is read from outside or reading should be performed several timer before processing. Figure 2-2 shows input/output timing examples.
External data is read from an I/O port in the S1 state of the read cycle during execution of the read instruction. This timing cannot be recognized from outside, so that transient input such as chattering must be processed by the program.
Output data changes in the S2 state of the write cycle during execution of the instruction which writes to an I/O port.



Note: The positions of the read and write cycles may vary, depending on the instruction.

Figure 2-2. Input / Output Timing (Example)

2.2.1 Port P0 (P07 to P00)

Port P0 is an 8-bit general-purpose input/output port which can be configured as an input or an output in one-bit unit. Each bit of the port can be configured for either input or output separately, using the P0 port input/output control register (P0CR). A reset clears the P0CR to "0", placing port P0 in input mode. A reset also initializes the P0 port output latch (P0DR) to "0".

Note: If the port is in input mode, it senses the state of an input to its pins. If some pins of the port are in input mode, and others are in output mode, the content of the output latch related to a port pin that is in input mode may be changed when a bit manipulation instruction is executed on the port.

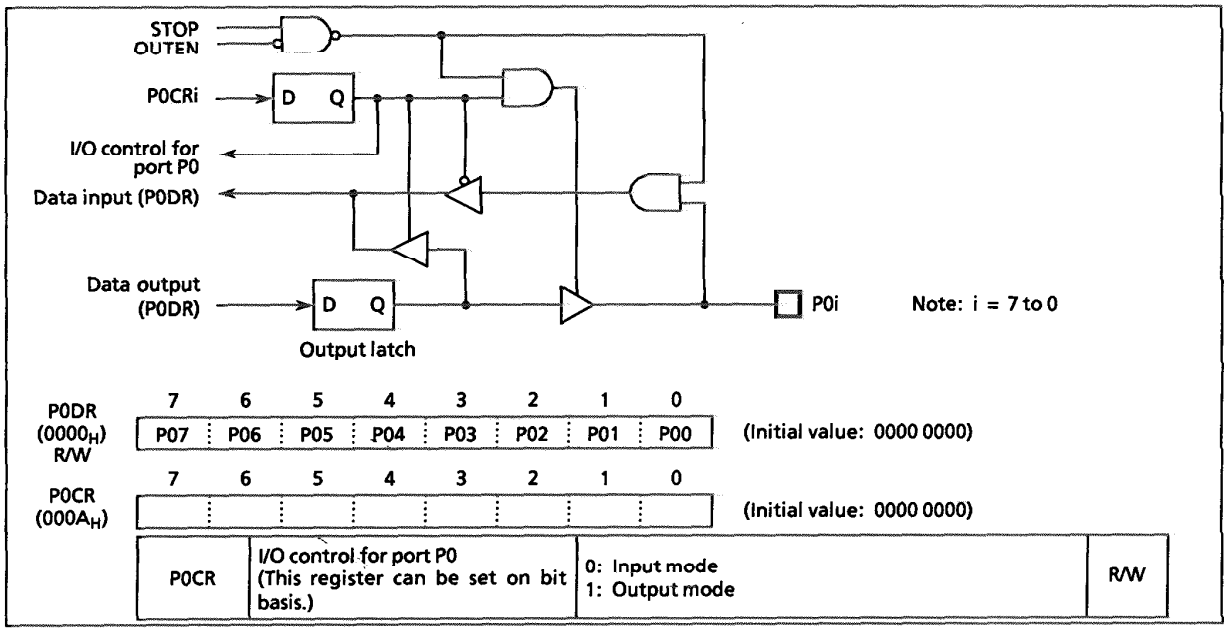


Figure 2-3. Port P0 and P0 Port Control Register

2.2.2 Port P1 (P17 to P10)

Port P1 is an 8-bit input/output port, and also used as a timer counter input/output, external interrupt input, and serial interface input/output. To use port P1 as an input port or secondary-function pins, set its output latch (P1DR) to "1". A reset sets the output latch to "1" and clears the push-pull control (P1OUTCR) to "0".

The P1OUTCR can be used to select Nch O.D. output or CMOS output for the output circuit of port P1. To use port P1 as an input port, set the P1DR to "1", and then clear the corresponding bit of the P1OUTCR to "0".

Port P1 has separate data input registers. To sense the state of the output latch, read the P1DR. To sense the state of the pins the port, read the P1PRD register.

The input waveform of a TC3 input can be inverted in terms of phase, using the TC3SEL register.

P10, P11, P12, P13, and P14 can work not only as a port but also as, respectively, the TC2, TC3/INT3, PWM4/PDO/TC4, PPG, and INT4 functions. To use the TC2, TC3, INT3, TC4, and INT4 functions, place the respective pins in input mode. To use the PWM4, PDO, and PPG functions, place the respective pins in output mode.

P15, P16, and P17 can work not only as a port but also as, respectively, the SI, SO, and SCK functions. To use these functions, place the pin corresponding to the SI function in input mode, the pin corresponding to the SO function in output mode, and the pin corresponding to the SCK function in either input or output mode.

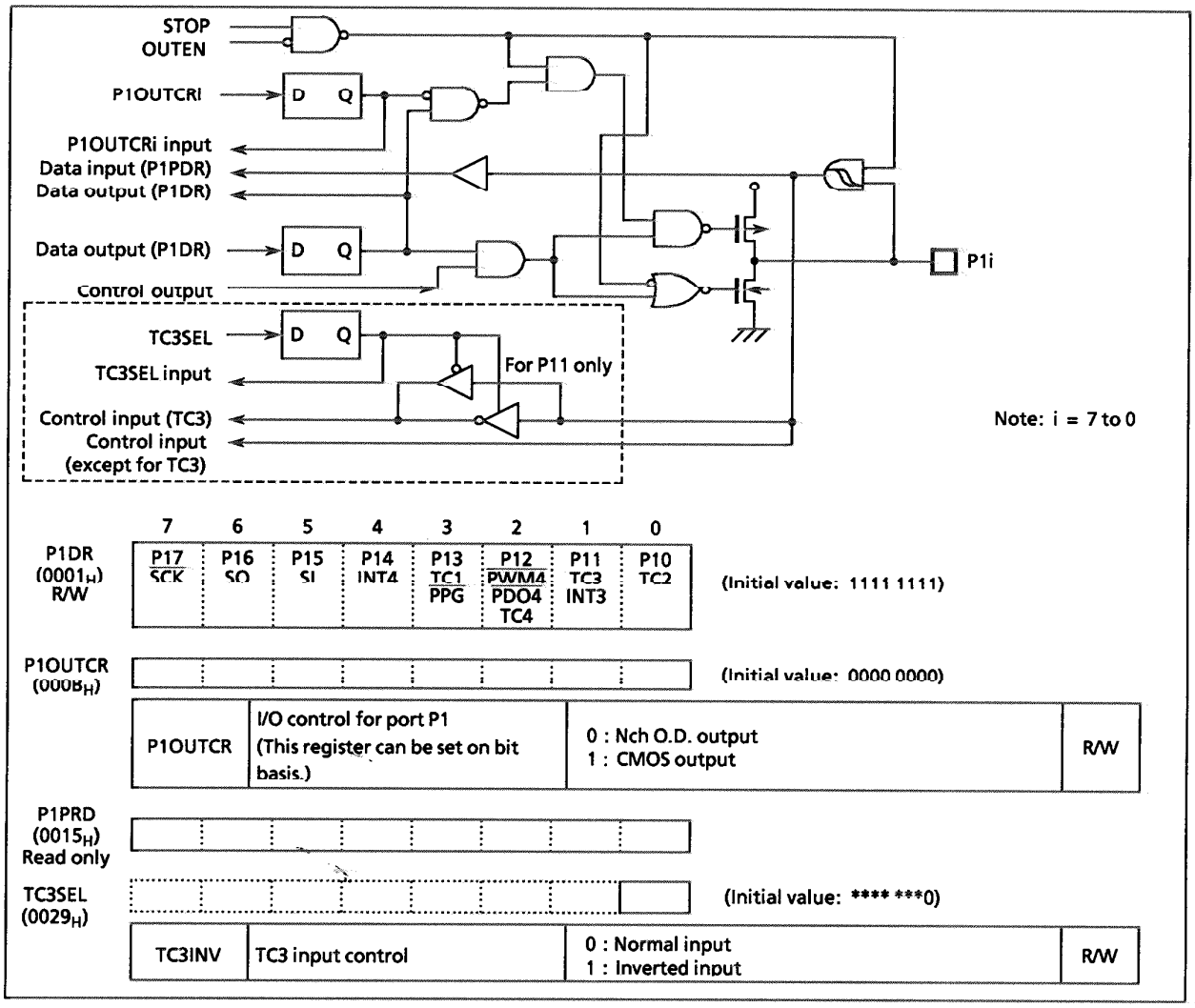


Figure 2-4. Port P1 and P1 Port Control Register

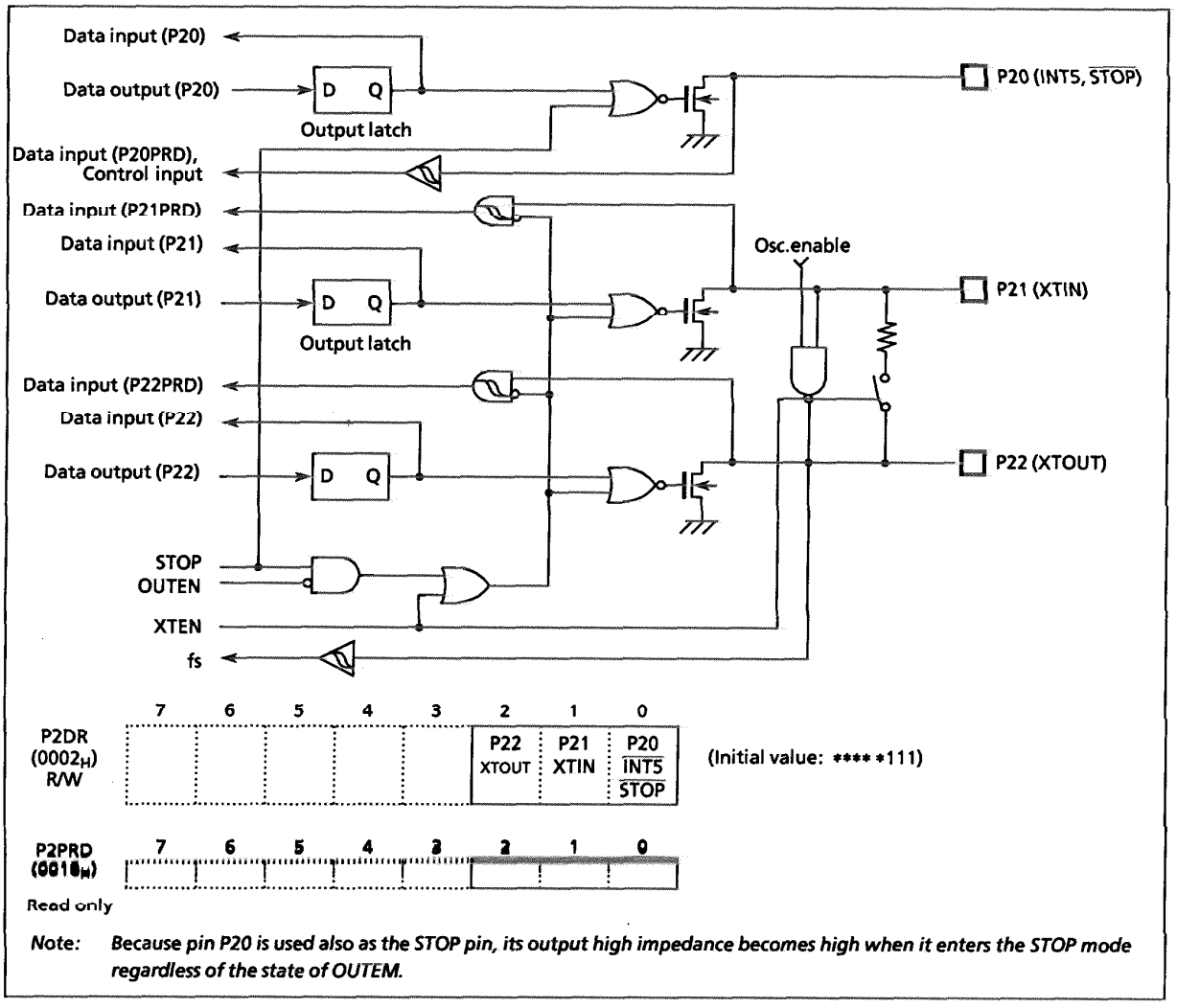
P1OUTCR	P1DR	Function
0	0	Low output
0	1	Input, O.D. output, or control input
1	0	Low output
1	1	High output or control output

2.2.3 Port P2 (P22 to P20)

Port P2 is a 3-bit input/output port. It can work not only as a port but also as external input, STOP mode release signal input, and low-frequency resonator connection pins. To use it as an input port or the secondary-function pins, set the output latch (P2DR) to "1". A reset initializes the P2DR to "1". To run the device in dual clock mode, connect a low-frequency resonator (32.768 kHz) to pins P21 (XTIN) and P22 (XOUT). When the device runs in single clock mode, P21 and P22 can be used as an ordinary input/output port. It is recommended that pin P20 be used for external interrupt input, STOP release signal input, or as an input port (if it is used as an output port, it is set with the content of the interrupt latch at the negative-going edge of the signal.)

Port P2 has separate data input registers. To sense the state of the output latch, read the P2DR. To sense the state of the pins of the port, read the P2PRD register.

If a read instruction is executed for the P2DR or P2PDR on port P2, the sensed state of bits 7 to 3 is undefined.



Note: Because pin P20 is used also as the STOP pin, its output high impedance becomes high when it enters the STOP mode regardless of the state of OUTEM.

Figure 2-5. Port P2 and P2 Port Control Register

2.2.4 Port P3 (P31 to P30)

Port P3 is a 2-bit input/output port. To use it as an input port, set the output latch (P3DR) to "1". A reset initializes the output latch to "1".

To use port P3 as an input port, set the P3DR to "1".

Port P3 has separate data input registers. To sense the state of the output latch, read the P3DR. To sense the state of the pins of the port, read the P3PRD register.

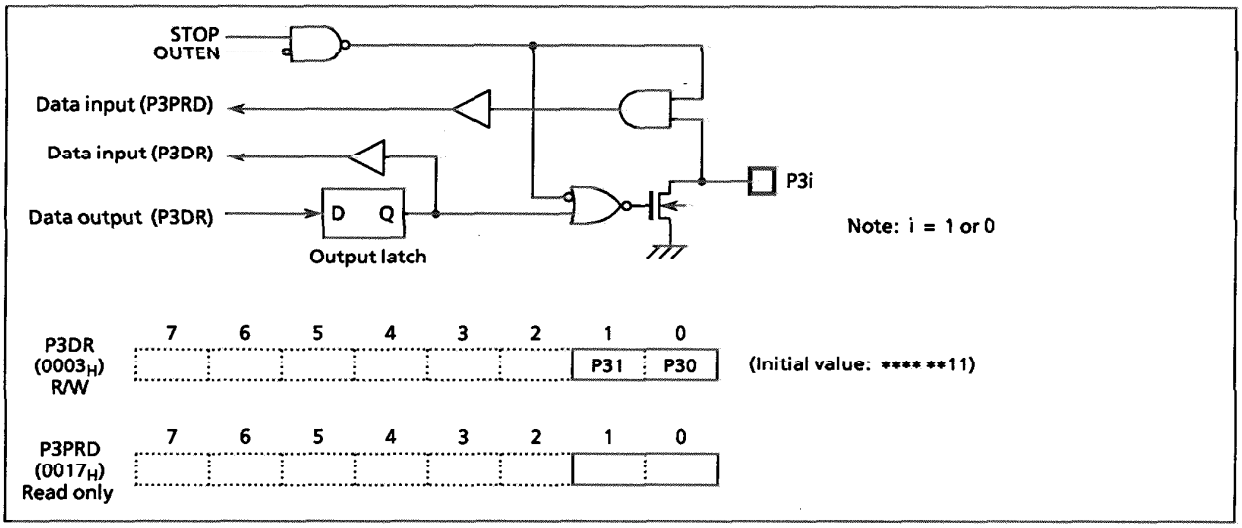
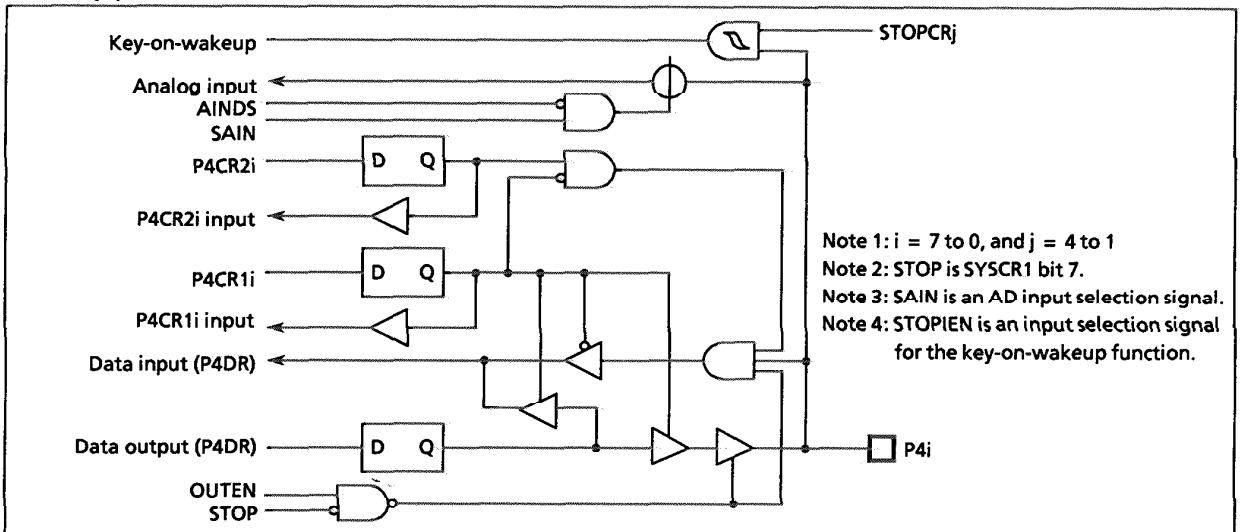


Figure 2-6. Port P3 and P3 Port Control Register

2.2.5 Port P4 (P47 to P40)

Port P4 is an 8-bit input/output port. Each bit of the port can be configured for either input or output separately, using the input/output control register (P4CR1). These pins can work not only as a port but also for analog input and key-on-wakeup input. To use each bit for output, set the corresponding bit of the P4CR1 to "1" to place them in output mode. To use them in input mode, clear the corresponding bit of the P4CR1 to "0", then set the P4CR2 to "1". To use the bits for analog input and key-on wakeup input, clear the P4CR1 and P4CR2 to "0" in the stated order (then, for analog input, clear the AINDS to "0" (ADCCR1 bit 4), and start the AD). A reset initializes the P4CR1 and P4CR2, respectively, to "0" and "1", thereby placing port P4 in input mode. A reset also clears the P4 port output latch (P4DR) to "0".



P4DR (0004_H) R/W

7	6	5	4	3	2	1	0
P47 AIN7 STOP5	P46 AIN6 STOP4	P45 AIN5 STOP3	P44 AIN4 STOP2	P43 AIN3	P42 AIN2	P41 AIN1	P40 AIN0

(Initial value: 0000 0000)

P4CR1 ($000C_H$)

7	6	5	4	3	2	1	0

(Initial value: 0000 0000)

P4CR1	I/O control for port P4 (This register can be set on bit basis.)	0 : Input mode or analog input/key-on-wakeup input 1 : Output mode	R/W

P4CR2 (0028_H)

7	6	5	4	3	2	1	0

(Initial value: 1111 1111)

P4CR2	I/O control for port P4 (This register can be set on bit basis.)	0: Analog input/key-on-wakeup input 1: Input mode	R/W

Note 1: If a port is in input mode, it senses the state of an input to its pins. If some pins of the port are in input mode, and others are in output mode, the content of the output latch related to a port pin that is in input mode may be changed when a bit manipulation instruction is executed on the port.

Note 2: For a pin used for analog input, be sure to clear the corresponding bit of the P4CR2 to "0" to protect it from through current.

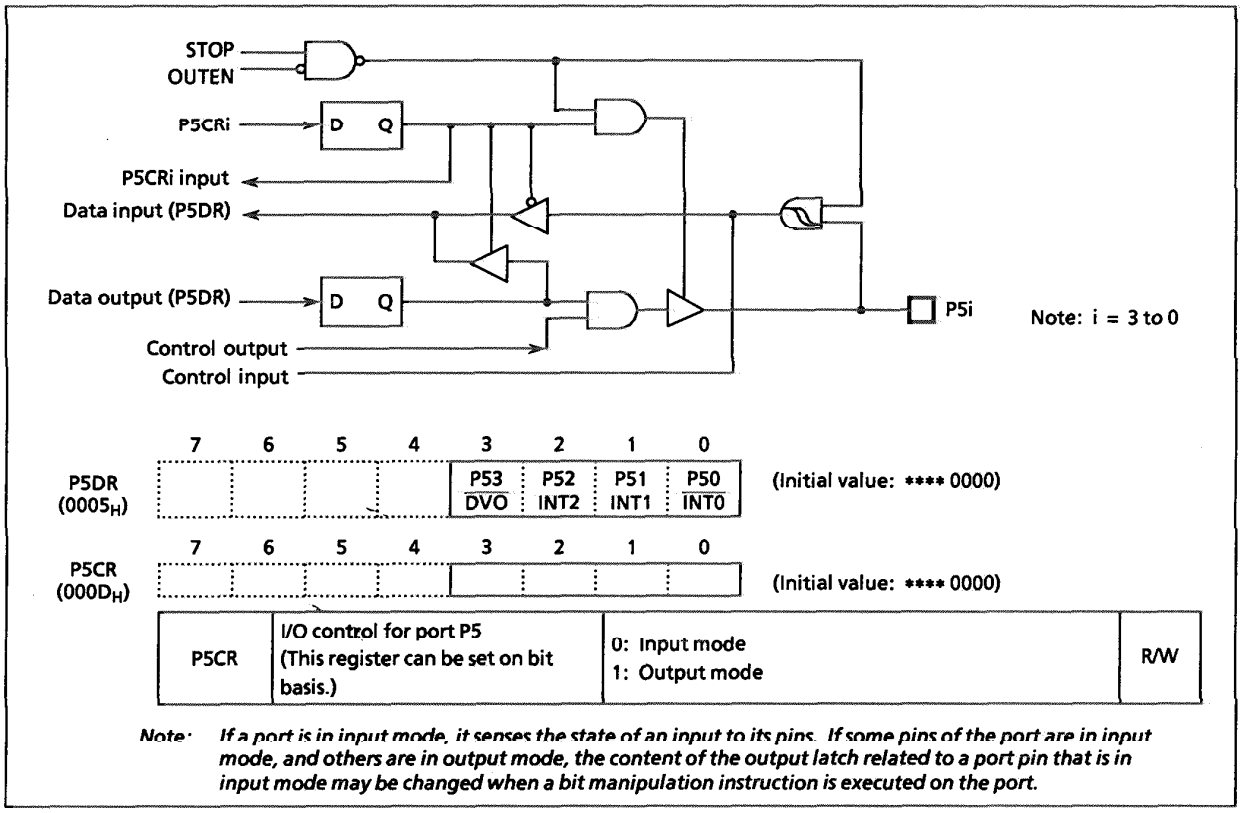
Note 3: The P4CR2 controls the input gate of pins used for analog input. In analog input mode, clear the P4CR2 to "0" to fix the input gate, thereby protecting it from through current. In input mode, set the P4CR2 to "1". When using the key-on-wakeup function, clear the P4CR2 to "0", because the inputs are received separately. If the P4CR2 is "0", read-accessing the P4CR2 yields "0".

Figure 2-7. Port P4 and P4 Port Control Register

2.2.6 Port P5 (P53 to P50)

Port P5 is a 4-bit general-purpose input/output port. Each bit of the port can be configured for either input or output separately, using the P5 port input/output control register (P5CR). A reset clears the P5CR to "0", placing port P5 in input mode. A reset also initializes the P5 port output latch (P5DR) to "0".

P50, P51, and P52 can work not only as an input/output port but also, respectively, for the INT0, INT1, and INT2 functions. To use these functions, place the corresponding pins in input mode.



Note: If a port is in input mode, it senses the state of an input to its pins. If some pins of the port are in input mode, and others are in output mode, the content of the output latch related to a port pin that is in input mode may be changed when a bit manipulation instruction is executed on the port.

Figure 2-8. Port P5 and P5 Port Control Register

2.2.7 Ports P6 (P67 to P60), P7 (P77 to P70), P8 (P87 to P80), and P9 (P97 to P90)

Ports P6, P7, P8, and P9 are 8-bit high-breakdown voltage input/output ports. They can work not only as a port but also for VFT driver output. They can drive directly a vacuum fluorescent tube (VFT). To use them as an input port or VFT driver, clear the output latch to "0".

Pins not set up for VFT driver output can be used as an input/output port. To use a pin for ordinary input/output when a VFT driver is used, clear the VFT driver output data buffer memory (DBR) for the pin to "0". A reset initializes the output latch to "0".

It is recommended that ports P6, P7, P8, and P9 be used to drive a VFT because they have a built-in pull-down resistor.

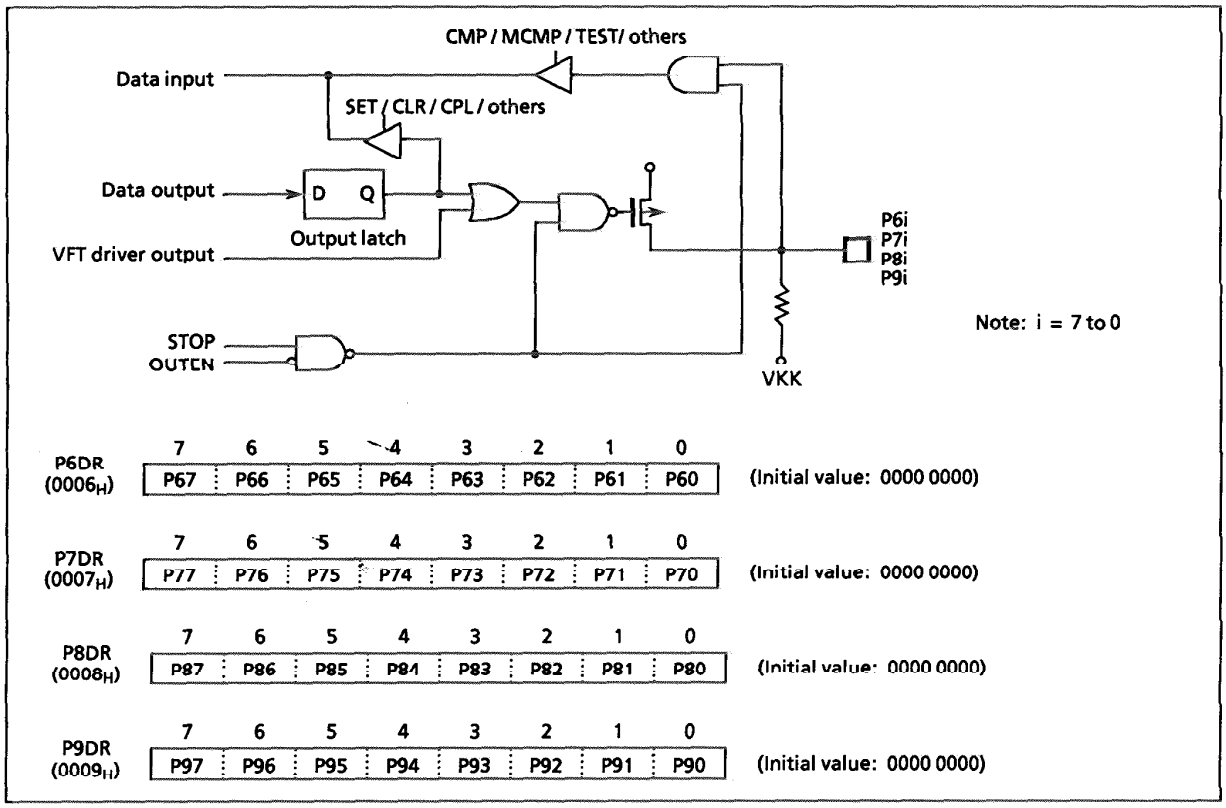


Figure 2-9. P6, P7, P8, and P9 Port Control Registers

2.2.8 Port PD (PD4 to PD0)

Port PD is a high-breakdown voltage input/output port. It can work not only as a port but also for VFT driver output. It can drive directly a VFT. Each bit of the port can be configured for a segment or input/output separately, using the VSEL (bits 4 to 0) of VFT driver control register 1 (VFTCR1). A reset clears the VSEL to "0", causing the port to work as an input/output port. To use it as an input port, clear the output latch to "0". A reset initializes the output latch to "0".

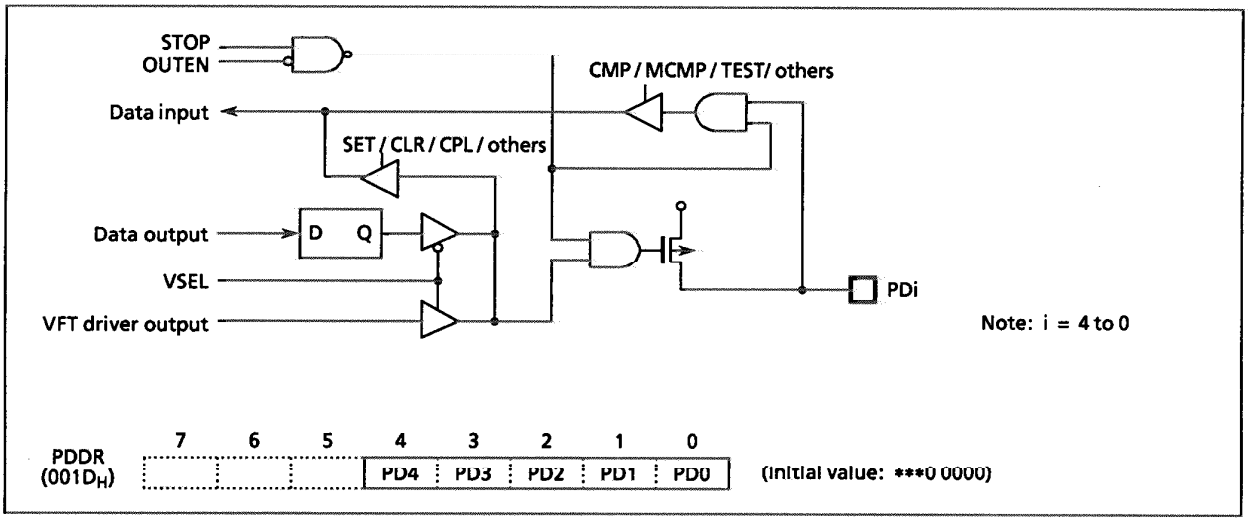


Figure 2-10. PD Port Control Register

2.3 Time Base timer (TBT)

The time base timer generates time base for key scanning, dynamic displaying, etc. It also provides a time base timer interrupt (INTTBT).

An INTTBT is generated on the first falling edge of source clock (the divider output of the timing generator) after the time base timer has been enabled. The divider is not cleared by the program; therefore, only the first interrupt may be generated ahead of the set interrupt period (Figure 2-11 (b)).

The interrupt frequency (TBTCK) must be selected with the time base timer disabled (the interrupt frequency must not be changed with the disable from the enable state). Both frequency selection and enabling can be performed simultaneously.

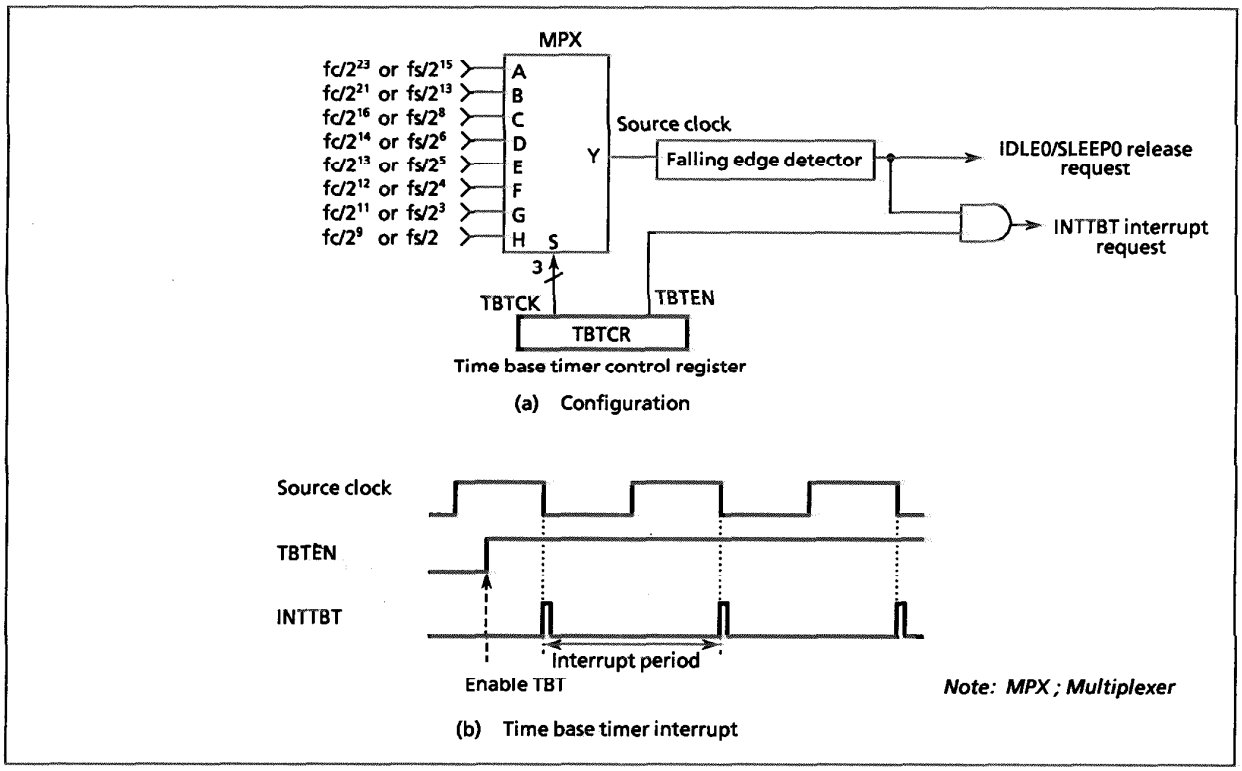


Figure 2-11. Time Base Timer

Example: Sets the time base timer frequency to fc/2^{16} [Hz] and enables an INTTBT interrupt.

```
LD    (TBTCR), 00000010B    ;  TBTCK←"010"
LD    (TBTCR), 00001010B    ;  TBTEN←"1"
SET   (EIRL). 7
```

TBTCR (0036_H)

7	6	5	4	3	2	1	0
(DVOEN)	(DVOCK)		(DV7CK)	TBTEN	TBTCK		

(Initial value: 0000 0000)

TBTEN	Time base timer enable / disable	0: Disable 1: Enable				R/W
TBTCK	Time base timer interrupt frequency select [Hz]		NORMAL1/2, IDLE1/2 mode		SLOW, SLEEP mode	
			DV7CK = 0	DV7CK = 1		
		000	$fc/2^{23}$	$fs/2^{15}$	$fs/2^{15}$	
		001	$fc/2^{21}$	$fs/2^{13}$	$fs/2^{13}$	
		010	$fc/2^{16}$	$fs/2^{8}$	$fs/2^{8}$	
		011	$fc/2^{14}$	$fs/2^{6}$	$fs/2^{6}$	
		100	$fc/2^{13}$	$fs/2^{5}$	$fs/2^{5}$	
		101	$fc/2^{12}$	$fs/2^{4}$	$fs/2^{4}$	
		110	$fc/2^{11}$	$fs/2^{3}$	$fs/2^{3}$	
		111	$fc/2^{9}$	fs/2	fs/2	

*Note: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz], * ; Don't care*

Figure 2-12. Time Base Timer Control Register

Table 2-1. Time Base Timer Interrupt Frequency (Example: fc = 16.0 MHz, fs = 32.768 kHz)

TBTCK	Time base timer interrupt frequency [Hz]		
	NORMAL1/2, IDLE1/2 mode		SLOW, SLEEP mode
	DV7CK = 0	DV7CK = 1	
000	1.91	1	1
001	7.63	4	4
010	244.14	128	128
011	976.56	512	512
100	1953.13	1024	1024
101	3906.25	2048	2048
110	7812.5	4096	4096
111	31250	16384	16384

2.4 Watchdog Timer (WDT)

The watchdog timer is a fail-safe system to rapidly detect the CPU malfunctions such as endless looping caused by noise or the like, or deadlock and resume the CPU to the normal state.
The watchdog timer signal for detecting malfunction can be selected either a reset output or a non-maskable interrupt request. However, selection is possible only once after reset. At first the reset output is selected.
When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

Note: Care must be given in system design so as to protect the Watchdog timer from disturbing noise. Otherwise the Watchdog Timer may not fully exhibit its functionality.

2.4.1 Watchdog Timer Configuration

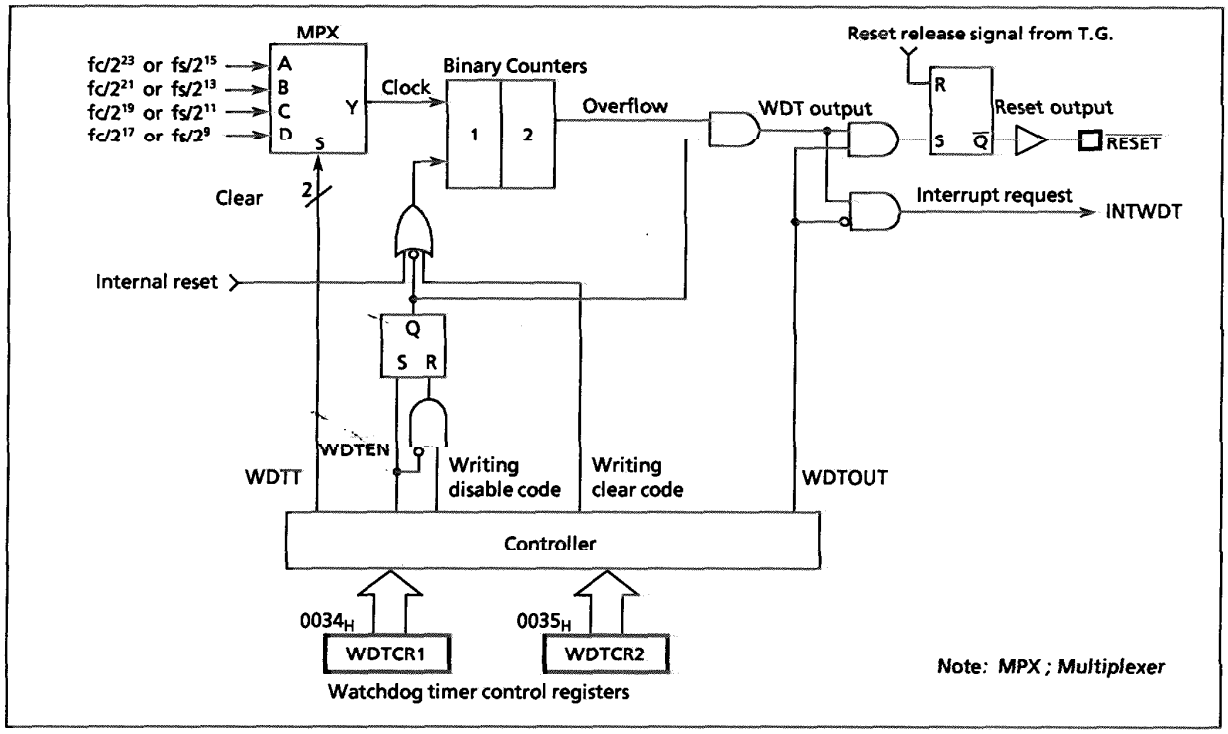


Figure 2-13. Watchdog Timer Configuration

2.4.2 Watchdog timer control

Figure 2-14 shows the watchdog timer control registers (WDTCR1, WDTCR2). The watchdog timer is automatically enabled after reset.

(1) Malfunction detection methods using the watchdog timer

The CPU malfunction is detected at follows.

① Setting the detection time, selecting output, and clearing the binary counter.

② Repeatedly clearing the binary counter within the setting detection time

> *Note: Clears the binary counter does not clear the source clock.*
> *It is recommended that the time to clear is set to 3/4 of the detecting time*

If the CPU malfunctions such as endless looping or deadlock occur for any cause, the watchdog timer output will become active at the rising of an overflow from the binary counters unless the binary counters are cleared. At this time, when WDTOUT=1 a reset is generated, which drivers the RESET pin low to reset the internal hardware and the external circuit. When WDTOUT=0, a watchdog timer interrupt (INTWDT) is generated.

The watchdog timer temporarily stops counting in STOP mode including warm-up or IDLE mode, and automatically restarts (continues counting) when the STOP / IDLE mode is released.

Example: Sets the watchdog timer detection time to 2^{21}/fc [s] and resets the CPU malfunction.

```
                LD(WDTCR2), 4EH        ;  Clears the binary counters
                LD(WDTCR1), 00001101B  ;  WDTT ← 10, WDTOUT ← 1
                LD(WDTCR2), 4EH        ;  Clears the binary counters
Within 3/4 of WDT                         (always clear immediately before and after
detection time                            changing WDTT)
                LD(WDTCR2), 4EH        ;  Clears the binary counters
Within 3/4 of WDT
detection time
                LD(WDTCR2), 4EH        ;  Clears the binary counters
```

Watchdog Timer Register 1

WDTCR1 (0034_H)

7	6	5	4	3	2	1	0
		(ATAS)	(ATOUT)	WDTEN	WDTT		WDTOUT

(Initial value: **11 1001)

			NORMAL1/2 mode		SLOW mode	
			DV7CK = 0	DV7CK = 1		
WDTEN	Watchdog timer enable/disable	0: Disable (It is necessary to write the disable code to WDTCR2) 1: Enable				Write only
WDTT	Watchdog timer detection time [s]	00	2^{25}/fc	2^{17}/fs	2^{17}/fs	
		01	2^{23}/fc	2^{15}/fs	2^{15}/fs	
		10	2^{21}/fc	2^{13}/fs	2^{13}/fs	
		11	2^{19}/fc	2^{11}/fs	2^{11}/fs	
WDTOUT	Watchdog timer output select	0: Interrupt request 1: Reset output				

Note 1: WDTOUT cannot be set to "1" by program after clearing WDTOUT to "0".
*Note 2: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz], * ; Don't care*
Note 3: WDTCR1 is a write-only register and must not be used with any of read-modify-write instructions.
Note 4: The watchdog timer must be disabled or the counter must be cleared immediately before entering to the STOP mode. When the counter is cleared, the counter must be cleared again immediately after releasing the STOP mode.
Note 5: Before rewriting WDTCR1 <WDTEN> from "1" to "0", be sure to clear the binary counter by writing "$4E_H$" to WDTCR2 immediately before writing to WDTCR1. This is necessary to prevent possible malfunction caused by rewriting the <WDTEN> bit.

Watchdog Timer Register 2

WDTCR2 (0035_H)

7	6	5	4	3	2	1	0

(Initial value: **** ****)

WDTCR2	Watchdog timer control code write register	$4E_H$: Watchdog timer binary counter clear (clear code) $B1_H$: Watchdog timer disable (disable code) $D2_H$: Enable assigning address trap area Others: Invalid	Write only

Note 1: The disable code is invalid unless written when WDTEN = 0.
*Note 2: * ; Don't care*
Note 3: The binary counter of the watchdog timer must not be cleared by the interrupt task.
Note 4: Clears the binary counter does not clear the source clock.
It is recommended that the time to clear is set to 3/4 of the detecting time

Figure 2-14. Watchdog Timer Control Registers

(2) Watchdog timer enable

The watchdog timer is enabled by setting WDTEN (bit 3 in WDTCR1) to "1". WDTEN is initialized to "1" during reset, so the watchdog timer operates immediately after reset is released.

(3) Watchdog timer disable

To disable the watchdog timer, after writing the clear code "$4E_H$" to WDTCR2, clear the WDTEN (WDTCR1 bit 3) to "0" and then write the disable code "$B1_H$" to WDTCR2. The watchdog timer is not disabled if this procedure is reversed and the disable code is written to WDTCR2 before WDTEN is cleared to "0". During disabling the watchdog timer, the binary counters are cleared to "0".

Example: Disables watchdog timer

```
DI                          ;  IMF ← 0
LD   (WDTCR2), 04EH         ;  Clears the binary counters
LDW  (WDTCR1), 0B101H       ;  WDTEN ← 0, WDTCR2 ← Disable code
EI                          ;  IMF ← 1
```

Table 2-2. Watchdog Timer Detection Time (Example: fc = 16.0 MHz, fs = 32.768 kHz)

WDTT	Watchdog timer detection time [s]		
	NORMAL1/2 mode		SLOW mode
	DV7CK = 0	DV7CK = 1	
00	2.097	4	4
01	254.288 m	1	1
10	131.072 m	250 m	250 m
11	32.768 m	62.5 m	62.5 m

2.4.3 Watchdog timer interrupt (INTWDT)

This is a pseudo non-maskable interrupt which can be accepted regardless of the contents of the EIR. If a watchdog timer interrupt or a software interrupt is already accepted, however, the new watchdog timer interrupt waits until the previous interrupt processing is completed (the end of the [RETN] instruction execution).
The stack pointer (SP) should be initialized before using the watchdog timer output as an interrupt source with WDTOUT.

Example: Watchdog timer interrupt setting up

```
LD   SP, 023FH              ;  Sets the stack pointer
LD   (WDTCR1), 00001000B    ;  WDTOUT ← 0
```

2.4.4 Watchdog timer reset

If the watchdog timer output becomes active, a reset is generated, which drivers the $\overline{\text{RESET}}$ pin (sink open drain input/output with pull-up) low to reset the internal hardware. The reset output time is about 8/fc to 24/fc [s] (0.5 to 1.5 μs at fc = 16.0 MHz).

Note: The high-frequency clock oscillator also turns on when a watchdog timer reset is generated in SLOW mode. The reset output time is 8/fc to 24/fc [s]. Therefore, the reset time may include a certain amount of error if there is any fluctuation of the oscillation frequency at starting the high-frequency clock oscillation. Thus, the reset time must be considered an approximated value.

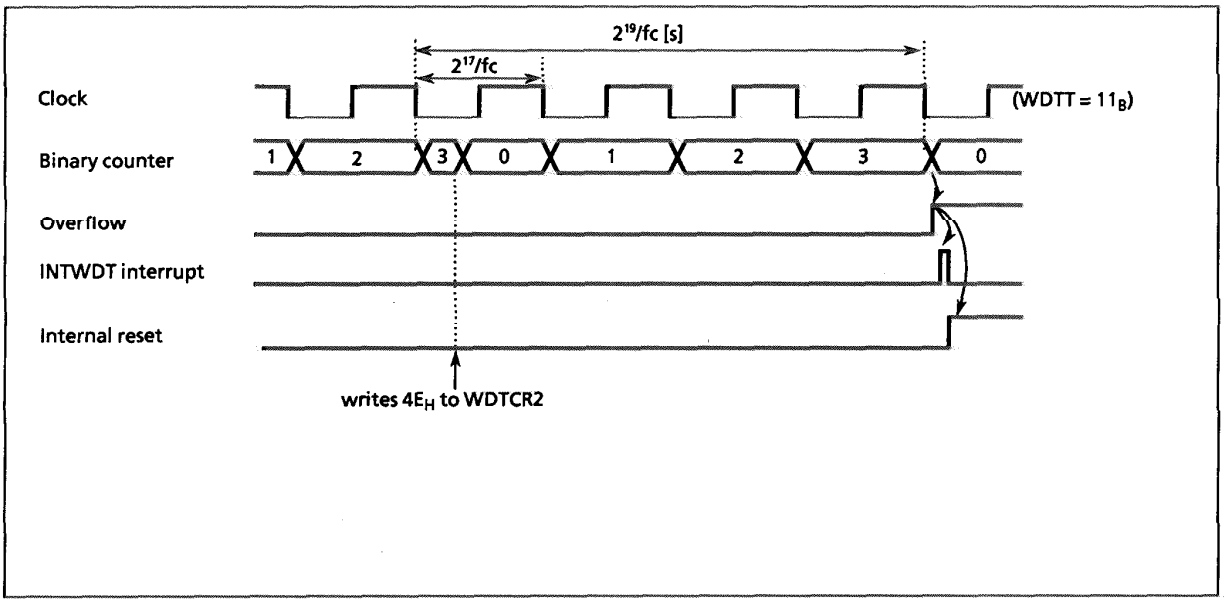


Figure 2-15. Watchdog Timer Interrupt/Reset

2.4.5 Address trap

The Watchdog Timer Control Register 1, 2 shares its addresses with the control registers in case of address trap. These control registers for address trap are shown on Figure 2-16. Whether internal RAM area should be trapped or not is selected on bit ATAS on WDTCR1. The written data becomes valid after the control code D2H is written on WDTCR2.

Watchdog Timer Control Register 1

WDTCR1 (0034_H)

7	6	5	4	3	2	1	0
		ATAS	ATOUT	WDTEN	WDTT		WDTOUT

(Initial value: **11 1001)

ATAS	Area for address trap	0: SFR and DBR area 1: SFR, RAM and DBR area (Valid if control code is written on WDTCR2)	Write only
ATOUT	Operation in case of address trap	0: Interrupt 1: Reset	

Watchdog Timer Control Register 2

WDTCR2 (0035_H)

7	6	5	4	3	2	1	0

(Initial value: **** ****)

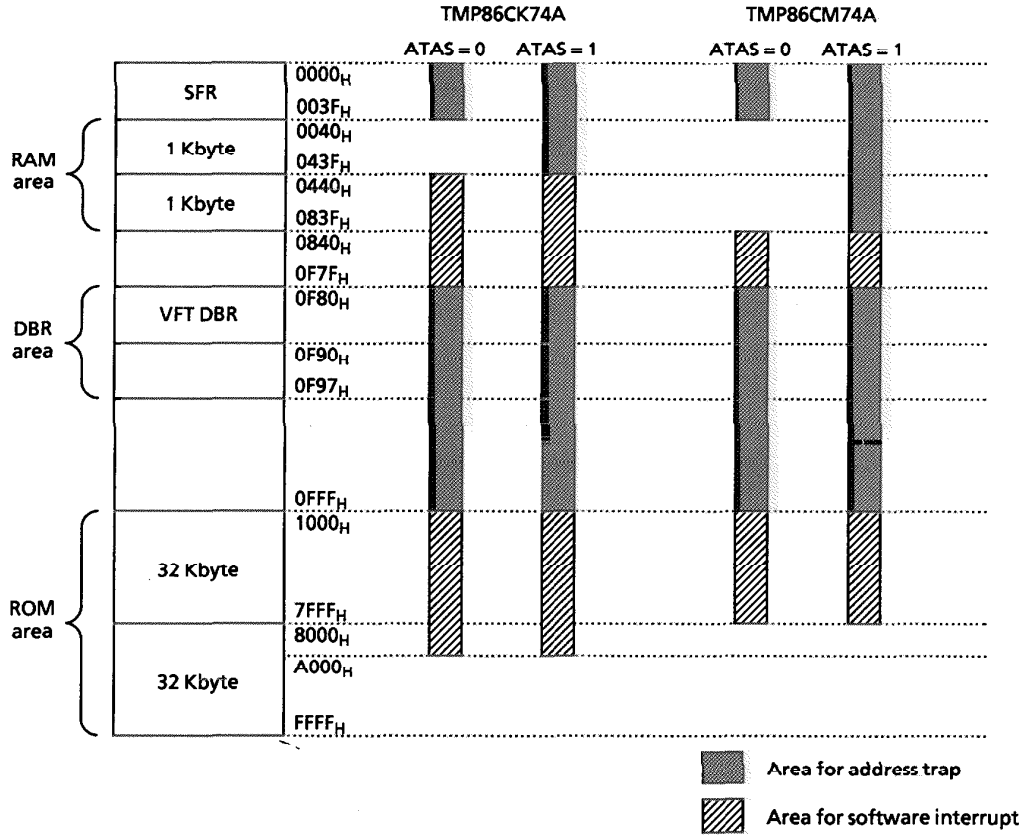
WDTCR2	Watchdog timer control code and Address trapped area control code	$D2_H$: Address trapped area valid to set (ATRAP control code) $4E_H$: Watchdog timer binary counter clear (WDT clear code) $B1_H$: Watchdog timer disable (WDT disable code) Others: Invalid	Write only

Figure 2-16. Watchdog Timer Control Registers

If the instructions are to be placed on internal RAM area, bit ATAS set "0".
The operating mode under address trapped, whether to be reset-output or interrupt processing, is selected on bit ATOUT on WDTCR1.

Example: Setting in order that the CPU normally executes instruction in internal RAM area and the address trap causes interrupt

```
LD    (WDTCR1), 0D200H
```



	TMP86CK74A		TMP86CM74A	
	ATAS = 0	ATAS = 1	ATAS = 0	ATAS = 1
Area for address trap	0000_H~$003F_H$ (SFR) $0F80_H$~$0FFF_H$ (DBR, Blank area)	0000_H~$003F_H$ (SFR) 0040_H~$043F_H$ (RAM) $0F80_H$~$0FFF_H$ (DBR, Blank area)	0000_H~$003F_H$ (SFR) $0F80_H$~$0FFF_H$ (DBR, Blank area)	0000_H~$003F_H$ (SFR) 0040_H~$083F_H$ (RAM) $0F80_H$~$0FFF_H$ (DBR, Blank area)
Area for software interrupt	0440_H~$0F7F_H$ 1000_H~$9FFF_H$	0440_H~$0F7F_H$ 1000_H~$9FFF_H$	0840_H~$0F7F_H$ 1000_H~$7FFF_H$	0840_H~$0F7F_H$ 1000_H~$7FFF_H$

2.5 Divider Output ($\overline{DVO}$)

Approximately 50% duty pulse can be output using the divider output circuit, which is useful for piezoelectric buzzer drive. Divider output is from pin P53 ($\overline{DVO}$). The P53 output latch should be set to "1".

Note: Selection of divider output frequency must be made while divider output is disabled.

TBTCR (0036_H)

7	6	5	4	3	2	1	0
DVOEN	DVOCK		(DV7CK)	(TBTEN)	(TBTCK)		

(Initial value: 0000 0000)

			NORMAL1/2 mode		SLOW, SLEEP mode	R/W
			DV7CK = 0	DV7CK = 1		
DVOEN	Divider output enable / disable	0: Disable 1: Enable				
DVOCK	Divider output ($\overline{DVO}$) frequency selection [Hz]	00	$fc/2^{13}$	$fs/2^5$	$fs/2^5$	
		01	$fc/2^{12}$	$fs/2^4$	$fs/2^4$	
		10	$fc/2^{11}$	$fs/2^3$	$fs/2^3$	
		11	$fc/2^{10}$	$fs/2^2$	$fs/2^2$	

*Note: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz], * ; Don't care*

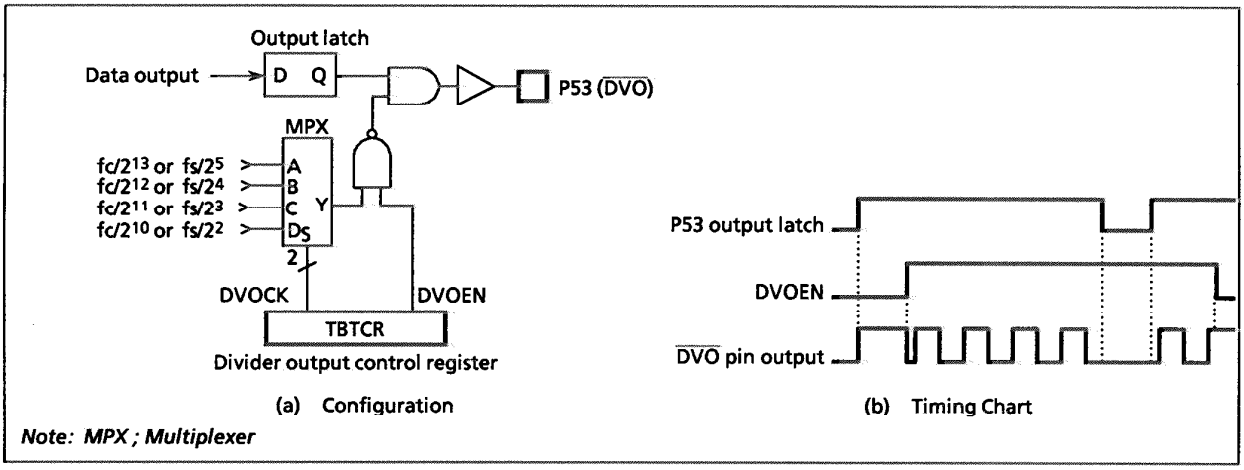
Figure 2-17. Divider Output Control Register

Example: 1.95 kHz pulse output (at fc = 16 MHz)

```
SET   (P5DR). 3            ;  P53 output latch ← "1"
SET   (P5CR). 3            ;  P53 output mode
LD    (TBTCR), 00000000B   ;  DVOCK ← "00"
LD    (TBTCR), 10000000B   ;  DVOEN ← "1"
```

Table 2-3. Divider Output Frequency (Example: at fc = 16.0 MHz, fs = 32.768 kHz)

DVOCK	Divider output frequency [Hz]		
	NORMAL1/2, IDLE1/2 mode		SLOW, SLEEP mode
	DV7CK = 0	DV7CK = 1	
00	1.953 k	1.024 k	1.024 k
01	3.906 k	2.048 k	2.048 k
10	7.813 k	4.096 k	4.096 k
11	15.625 k	8.192 k	8.192 k



Note: MPX ; Multiplexer

Figure 2-18. Divider Output

2.6 16-Bit Timer/Counter 1 (TC1)

2.6.1 Configuration

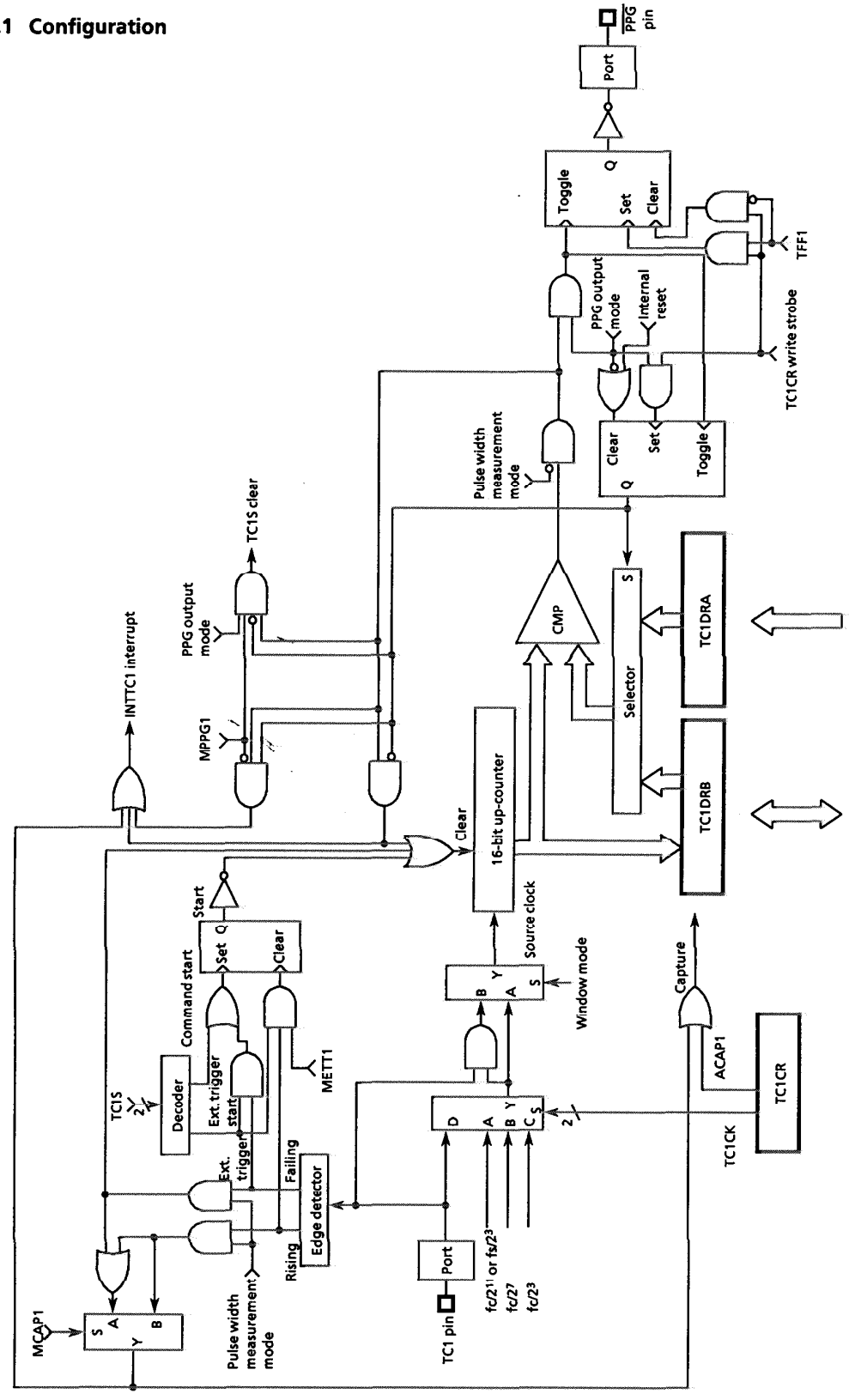


Figure 2-19. Timer/Counter 1 (TC1)

2.6.2 Control

The timer/counter 1 is controlled by a timer/counter 1 control register (TC1CR) and two 16-bit timer registers (TC1DRA and TC1DRB).

TC1DRA (00020, 00021$_H$): 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0 — TC1DRA$_H$ (00021$_H$) | TC1DRA$_L$ (00020$_H$)

TC1DRB (00022, 00023$_H$): Write only — TC1DRB$_H$ (00023$_H$) | TC1DRB$_L$ (00022$_H$)

TC1CR (00014$_H$): Read/write (Write available in only PPG output mode)

7	6	5 4	3 2	1 0
TFF1	ACAP1 MCAP1 METT1 MPPG1	TC1S	TC1CK	TC1M

(Initial value: 0000 0000)

TC1M	TC1 operating mode select	00: Timer/external trigger timer/event counter mode 01: Window mode 10: Pulse width measurement mode 11: PPG output mode								R/W
TC1CK	TC1 source clock select [Hz]		NORMAL, IDLE mode			SLOW, SLEEP mode				
			DV7CK = 0	DV7CK = 1						
		00	fc/2^{11}	fs/2^3	DV9	fs/2^3				
		01	fc/2^7	fc/2^7	DV5	–				
		10	fc/2^3	fc/2^3	DV1	–				
		11	External clock (TC1 pin input)							
TC1S	TC1 start control	00: Stop & counter clear 01: Command start 10: External trigger start at the rising edge 11: External trigger start at the falling edge	Timer	Extend	Event	Window	Pulse	PPG		
			○	○	○	○	○	○		
			○	×	×	×	×	○		
			×	○	○	○	○	○		
			×	○	○	○	○	○		
ACAP1	Auto capture control	0: Auto-capture disable	1: Auto-capture enable							
MCAP1	Pulse width measurement mode control	0: Double edge capture	1: Single edge capture							
METT1	External trigger timer mode control	0: Trigger start	1: Trigger start & stop							
MPPG1	PPG output control	0: Continuous pulse	1: Single pulse							
TFF1	Timer F/F1 control for PPG output mode	0: Clear	1: Set							

Note 1: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz]

Note 2: Writing to the lower byte of the timer registers (TC1DRA$_L$, TC1DRB$_L$), the comparison is inhibited until the upper byte (TC1DRA$_H$, TC1DRB$_H$) is written. Only the lower byte of the timer registers can not be changed. After writing to the upper byte, any match during 1 machine cycle (instruction execution cycle) is ignored.

Note 3: Set the mode, source clock, PPG control and timer F/F control when TC1 stops (TC1S = "00").

Note 4: Auto-capture can be used in only timer, event counter, and window modes.

Note 5: Values to be loaded to timer registers must satisfy the following condition.

TC1DRA > TC1DRB > 1 (PPG output mode), TC1DRA > 1 (others)

Note 6: Always write "0" to TFF1 except the PPG output mode.

Note 7: TREG1B can be written only in PPG output mode.

Note 8: When STOP mode is started, timer counter is stopped and cleared. Set TC1S to "1" after STOP mode is released for restarting timer counter.

Figure 2-20. Timer registers and TC1 Control Register

2.6.3 Function

Timer/counter 1 has five operating modes: timer, external trigger timer, event counter, window, pulse width measurement.

(1) Timer mode

In this mode, counting up is performed using the internal clock. The contents of TC1DRA are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared to "0". Counting up resumes after the counter is cleared. The current contents of up-counter can be transferred to TC1DRB by setting ACAP1 (bit 6 in TC1CR) to "1" (software capture function). (Auto-cpture function)

Table 2-4. Source Clock (internal clock) for Timer / Counter 1
(Example: at fc = 16.0 MHz, fs = 32.768 kHz)

TC1CK	NORMAL, IDLE mode			
	DV7CK = 0		DV7CK = 1	
	Resolution [μs]	Maximum time setting [s]	Resolution [μs]	Maximum time setting [s]
00	128.0	8.39	244.14	16.0
01	8.0	0.524	8.0	0.419
10	0.5	32.77 m	0.5	26.21 m

TC1CK	SLOW, SLEEP mode	
	Resolution [μs]	Maximum time setting [s]
00	244.14	16.0
01	–	–
10	–	–

Example 1: Sets the timer mode with source clock fs/2^3 [Hz] and generates an interrupt 1 later (at fc = 16.0 MHz)

```
LDW (TC1DRA), 1000H    ; Sets the timer register (1 s ÷ 2^3/fs = 1000H)
DI
SET (EIRL). 5          ; Enable INTTC1
EI
LD(TC1CR), 00000000B   ; Source clock, mode select
LD(TC1CR), 00010000B   ; Starts TC1
```

Example 2: Auto-capture

```
LD(TC1CR), 01010000B   ; ACAP1 ← 1 (Capture)
LDWA, (TC1DRB)         ; Reads the capture value
```

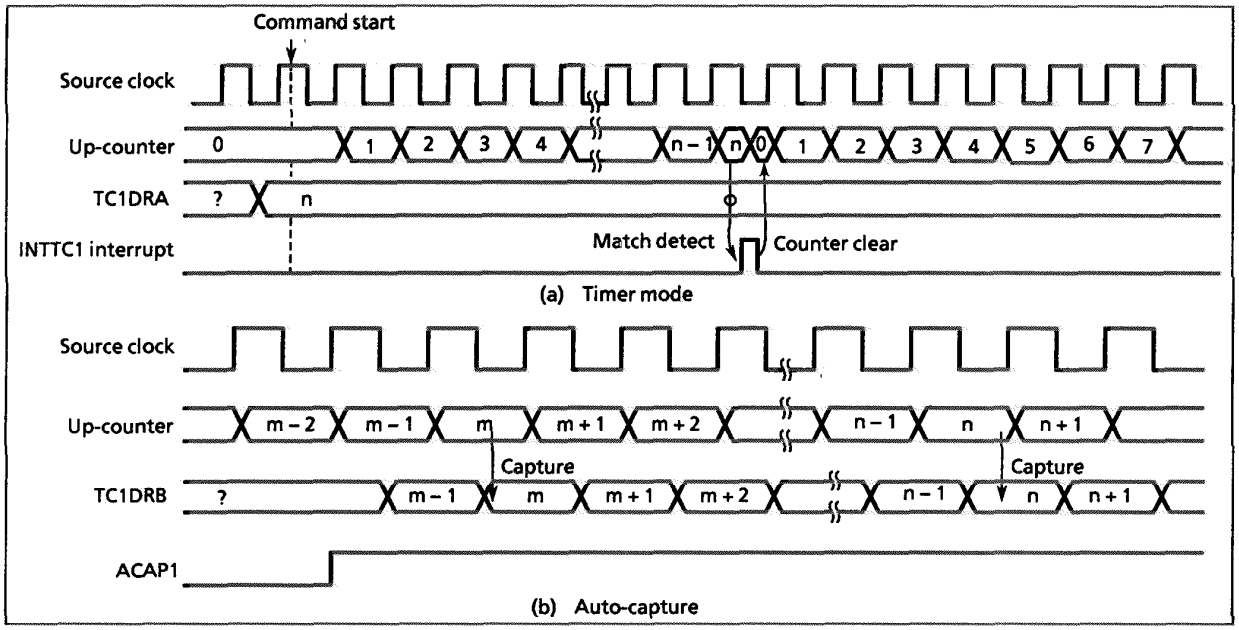


Figure 2-21. Timer Mode Timing Chart

(2) External trigger timer mode

In this mode, counting up is started by an external trigger. This trigger is the edge of the TC1 pin input. Either the rising or falling edge can be selected with TC1S. Source clock is an internal clock. The contents of TC1DRA is compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared to "0" and halted. The counter is restarted by the selected edge of the TC1 pin input.

When METT1 (bit 6 in TC1CR) is "1", inputting the edge to the reverse direction of the trigger edge to start counting clears the counter, and the counter is stopped. Inputting a constant pulse width can generate interrupts. When METT1 is "0", the reverse directive edge input is ignored. The TC1 pin input edge before a match detection is also ignored.

The TC1 pin input has the noise rejection; therefore, pulses of 4/fc [s] or less are rejected as noise. A pulse width of 12/fc [s] or more is required for edge detection in NORMAL or IDLE mode.

Example 1: Detects rising edge in TC1 pin input and generates an interrupt 100 μs later. (at fc = 16.0 MHz)

```
LDW  (TC1DRA), 00C8H     ;  100 μs ÷ 2^3/fc = C8H
DI
SET  (EIRL). 5           ;  INTTC1 interrupt enable
EI
LD   (TC1CR), 00001000B  ;  Source clock, mode select
LD   (TC1CR), 00111000B  ;  TC1 external trigger start, METT1 = 0
```

Example 2: Generates an interrupt, inputting "L" level pulse (pulse width: 4 ms or more) to the TC1 pin. (at fc = 16.0 MHz)

```
LDW  (TC1DRA), 01F4H     ;  4 ms ÷ 2^7/fc = 01F4H
DI
SET  (EIRL). 5           ;  INTTC1 interrupt enable
EI
LD   (TC1CR), 00000100B  ;  Source clock, mode select
LD   (TC1CR), 01110100B  ;  TC1 external trigger start, METT1 = 1
```

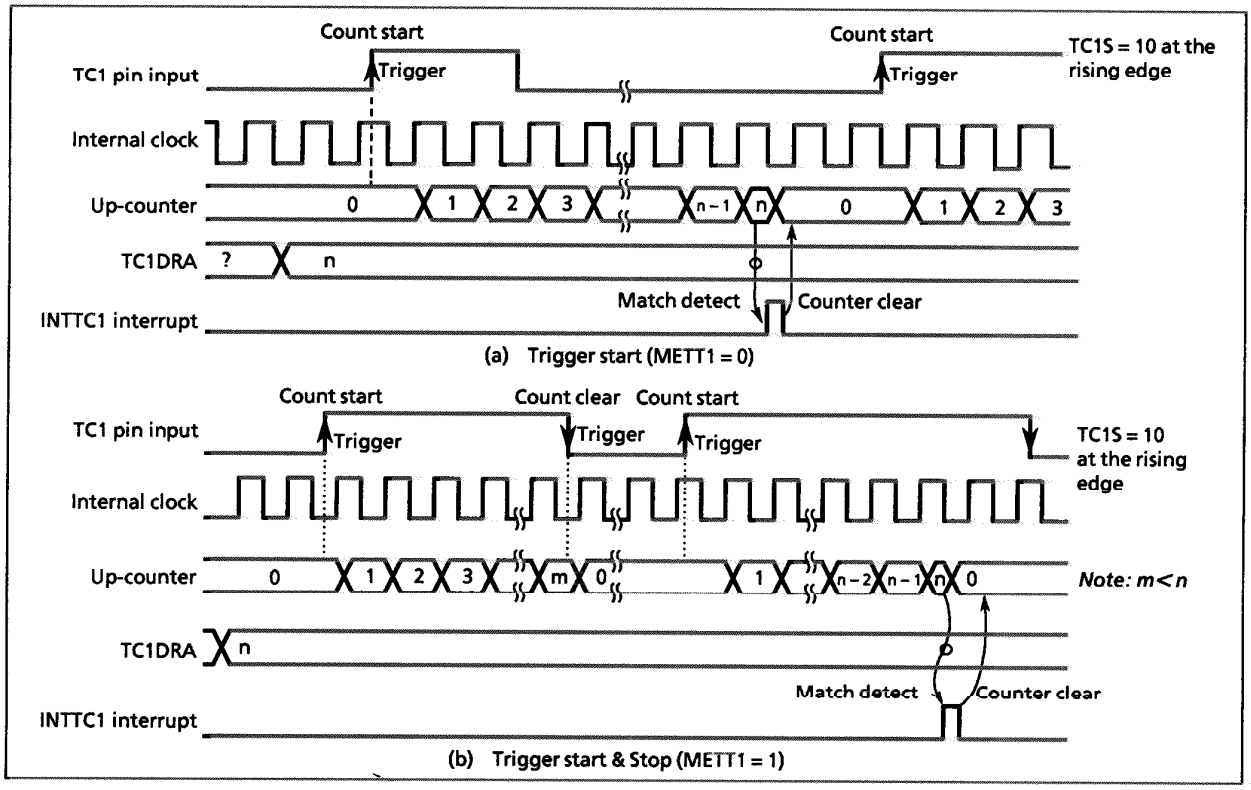


Figure 2-22. External Trigger Timer Mode Timing Chart

(3) Event counter mode

In this mode, events are counted at the edge of the TC1 pin input and bit 4 or 5 in TC1CR. Either the rising or falling edge can be selected with the external trigger. The contents of TC1DRA are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared.

Match detect is executed on other edge of count-up. A match can not be detected and INTTC1 is not generated when the pulse is still in same state.

Setting ACAP1 to "1" transfers the current contents of up-counter to TC1DRB (Auto-capture function).

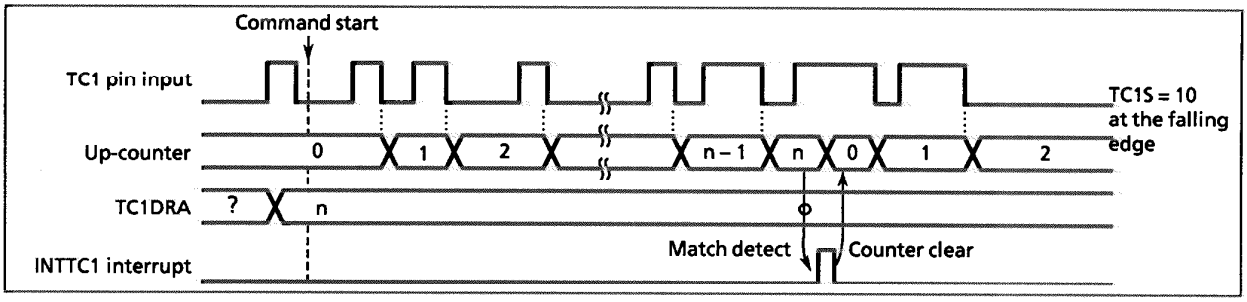


Figure 2-23. Event Counter Mode Timing Chart

Table 2-5. Source Clock (external clock) for Timer/Counter 1

	NORMAL 1/2 mode	SLOW, SLEEP mode
"H" Width	2^3/fc	2^3/fs
"L" Width	2^3/fc	2^3/fs

(4) Window mode

Counting up is performed on the rising edge of the pulse that is the logical AND-ed product of the TC1 pin input (window pulse) and an internal clock. The contents of TC1DRA are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared. Positive or negative logic for the TC1 pin input can be selected with bit4 or 5 in TC1CR.
It is necessary that the maximum applied frequency be such that the counter value can be analyzed by the program. That is ; the frequency must be considerably slower than the selected internal clock.

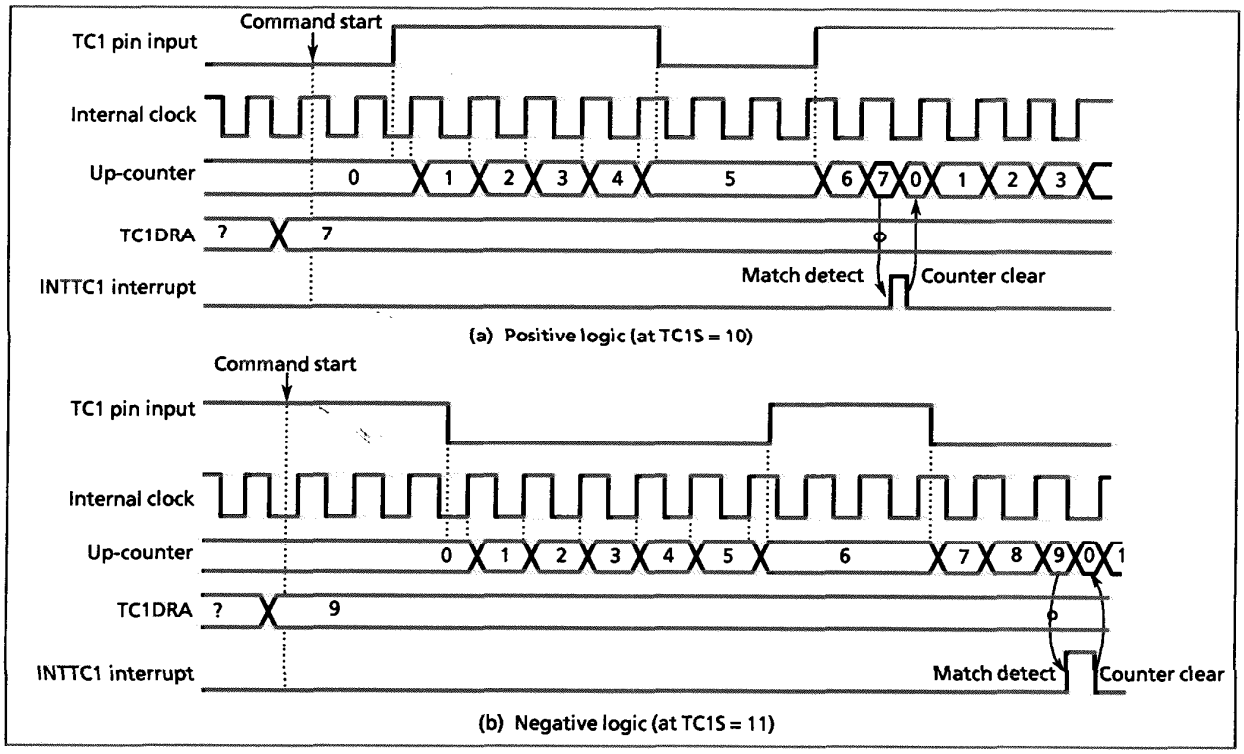


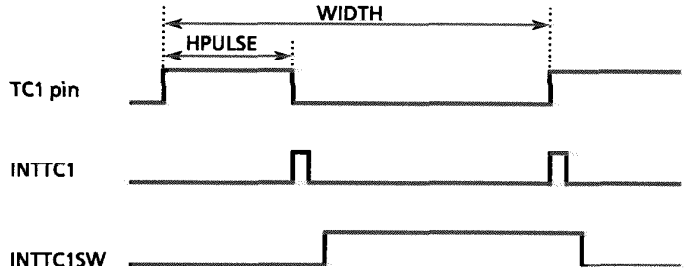
Figure 2-24. Window Mode Timing Chart

(5) Pulse width measurement mode

Counting is started by the external trigger (set to external trigger start by TC1CR). The trigger can be selected either the rising or falling edge of the TC1 pin input. the source clock is used an internal clock. On the next falling (rising) edge, the counter contents are transferred to TC1DRB and an INTTC1 interrupt is generated. The counter is cleared when the single edge capture mode is set. When double edge capture is set, the counter continues and, at the next rising (falling) edge, the counter contents are again transferred to TC1DRB. If a falling (rising) edge capture value is required, it is necessary to read out TC1DRB contents until a rising (falling) edge is detected. Falling or rising edge is selected with the external trigger (bit4 or 5 in TC1CR), and single edge or double edge is selected with MCAP1 (bit 6 in TC1CR).

Example: Duty measurement (resolution $fc/2^7$ [Hz])

```
        CLR  (INTTC1SW). 0          ;  INTTC1 service switch initial setting
        LD   (TC1CR), 00000110B     ;  Sets the TC1 mode and source clock
        DI ;                           IMF = "0"
        SET  (EIRL). 5              ;  Enables INTTC1
        EI;                            IMF = "1"
        LD   (TC1CR), 00100110B     ;  Starts TC1 with an external trigger at MCAP1 = 0
                :
PINTTC1: CPL (INTTC1SW). 0          ;  Inverts INTTC1 service switch
        JRS  F, SINTTC1
        LD   WA, (TC1DRBL)          ;  Reads TC1DRB ("H" level pulse width)
        LD   (HPULSE), WA
        RETI
SINTTC1: LD  WA, (TC1DRBL)          ;  Reads TC1DRB (Period)
        LD   (WIDTH), WA
                :                   ;  Duty calculation
        RETI
                :
VINTTC1: DW  PINTTC1
```



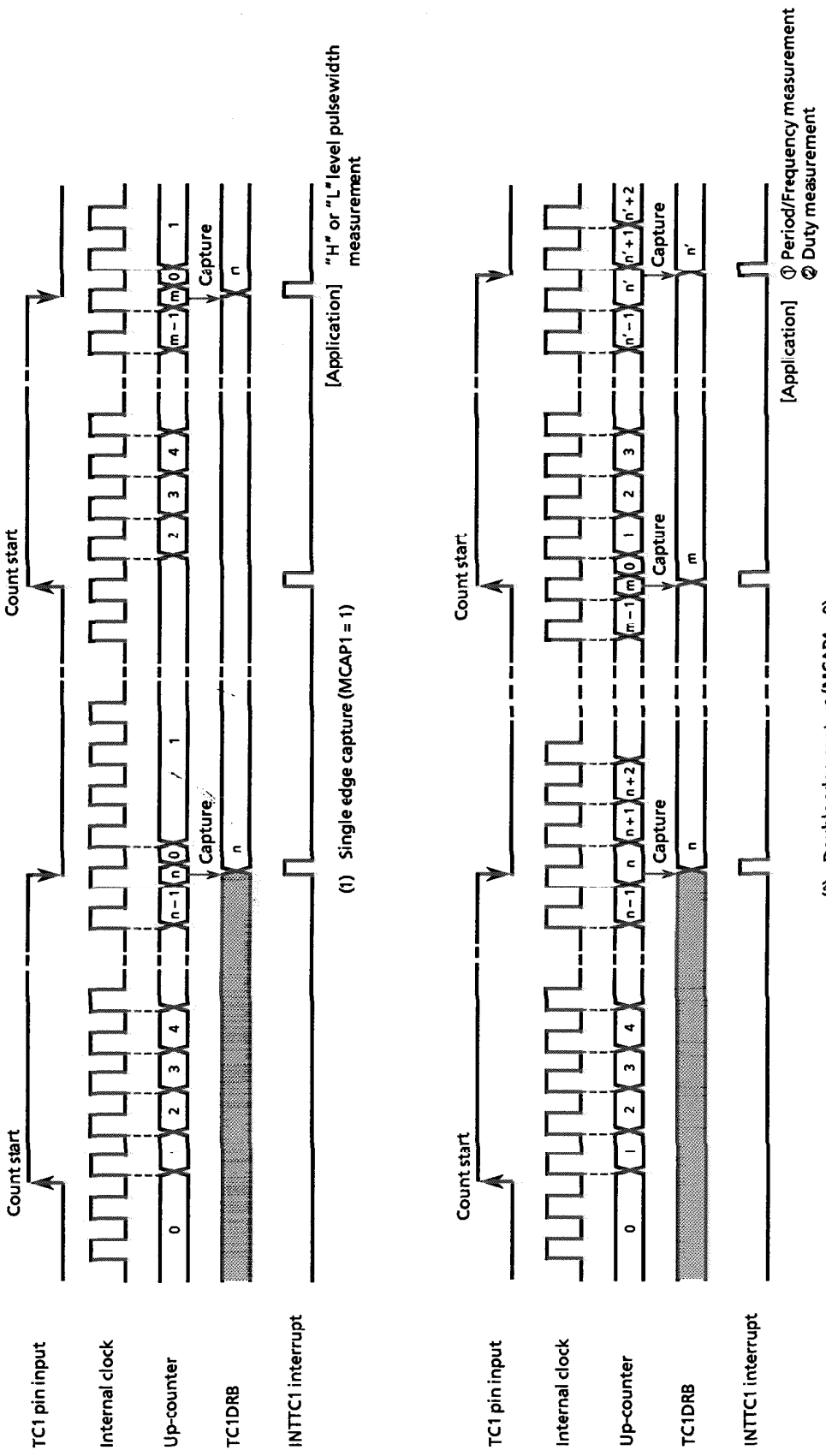


Figure 2-25. Pulse Measurement Mode Timing Chart

(6) Programmable Pulse Generate (PPG) output mode

Counting is started by an edge of the TC1 pin input (either the rising or falling edge can be selected) or by a command. The source clock is used an internal clock. First, the contents of TC1DRB are compared with the contents of the up-counter. If a match is found, timer F/F1 output is toggled. When MPPG1 = 0, an INTTC1 interrupt is generated. Next, timer F/F1 is again toggled and the counter is cleared by matching with TC1DRA. An INTTC1 interrupt is generated at this time. Timer F/F1 output is connected to the P13 ($\overline{PPG}$) pin. In the case of $\overline{PPG}$ output, set the P13 output latch to "1". Timer F/F1 is cleared to "0" during reset. The timer F/F1 value can also be set by TFF1 (bit 7 in TC1CR) and either a positive or negative logic pulse output is available. Also, writing to the TC1DRB is not possible unless the timer/counter 1 is set to the PPG output mode.

Example: Pulse output "H" level 800 μs, "L" level 200 μs (at fc = 16 MHz)

```
SET   (P1DR). 3              ;  P13 output latch ← 1
LD    (P1OUTCR), 10001000B   ;  P13 output mode
LD    (TC1CR), 10001011B     ;  Sets the PPG output mode
LDW   (TC1DRA), 07D0H        ;  Sets the period (1 ms ÷ 2^3/fc = 07D0H)
LDW   (TC1DRB), 0190H        ;  Sets "L" level pulse width
                                (200 μs ÷ 2^3/fc = 0190H)
LD    (TC1CR), 10011011B     ;  Starts
```

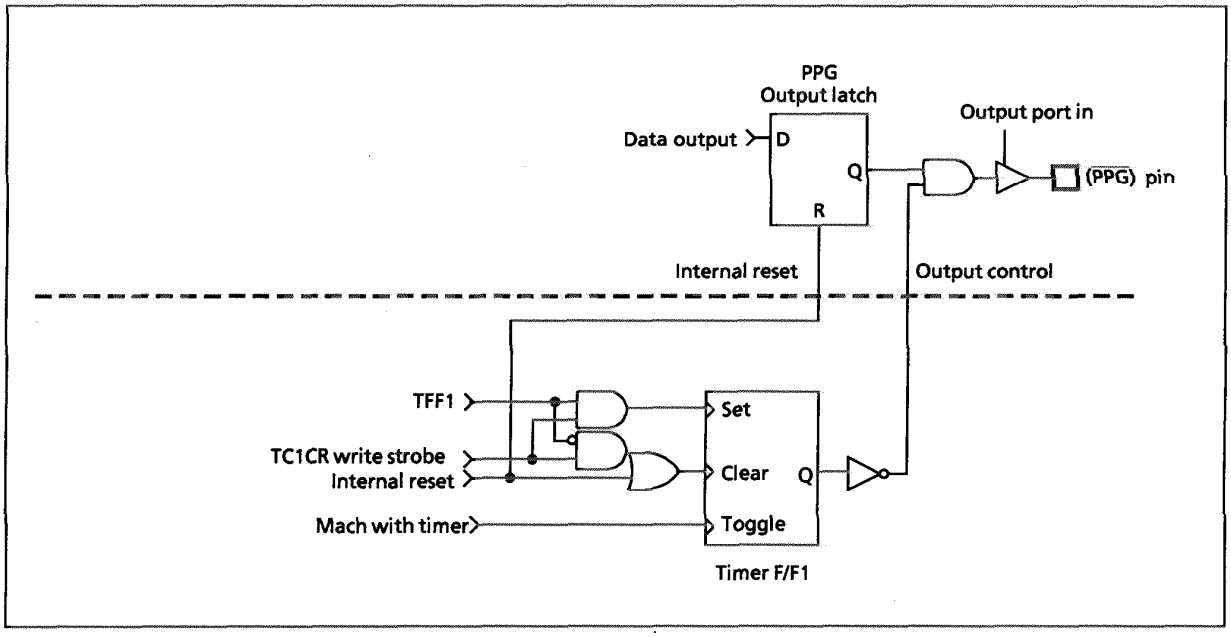


Figure 2-26. $\overline{PPG}$ Output

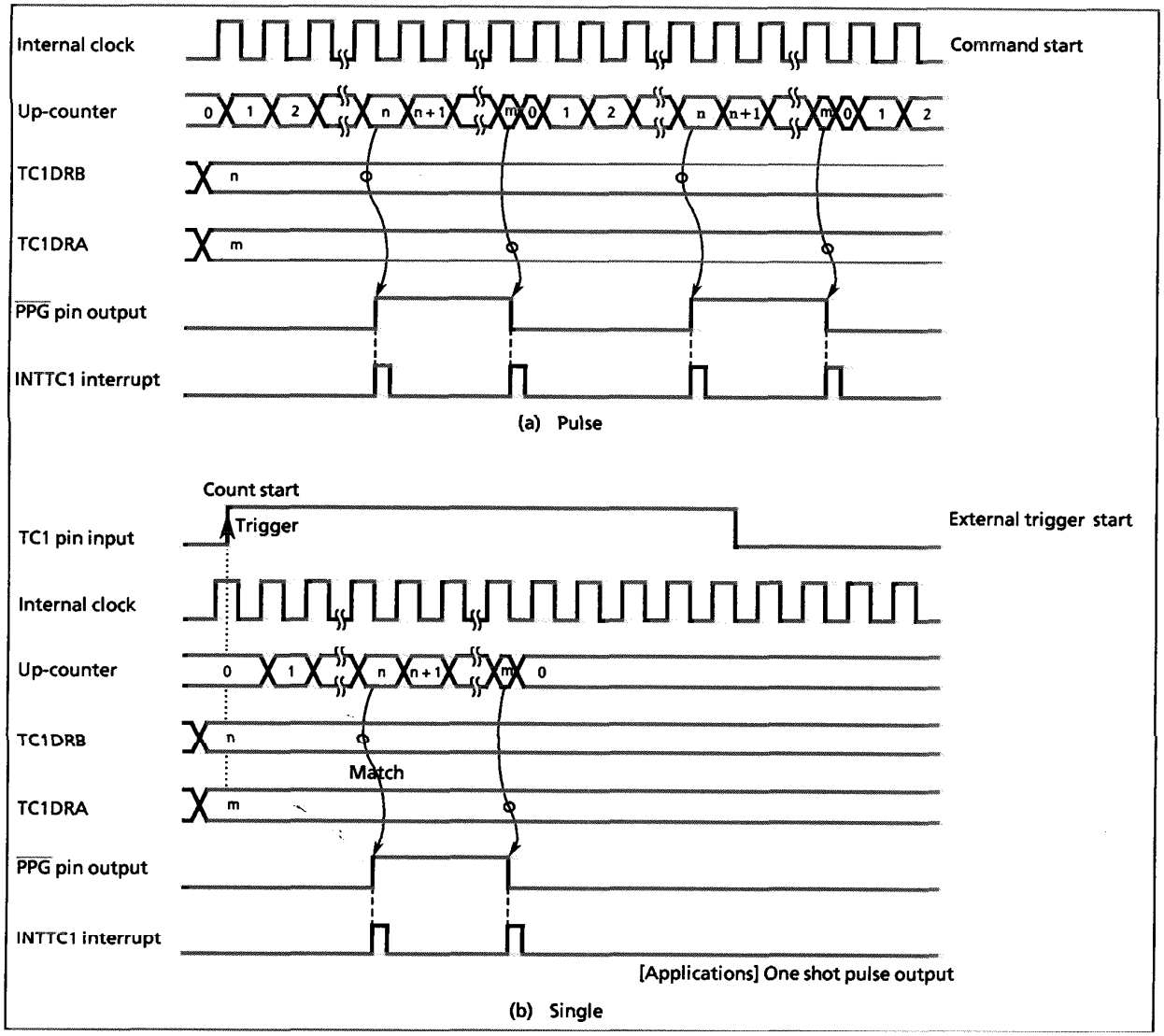


Figure 2-27. PPG Output Mode Timing Chart

2.7 16-Bit Timer/Counter 2

2.7.1 Configuration

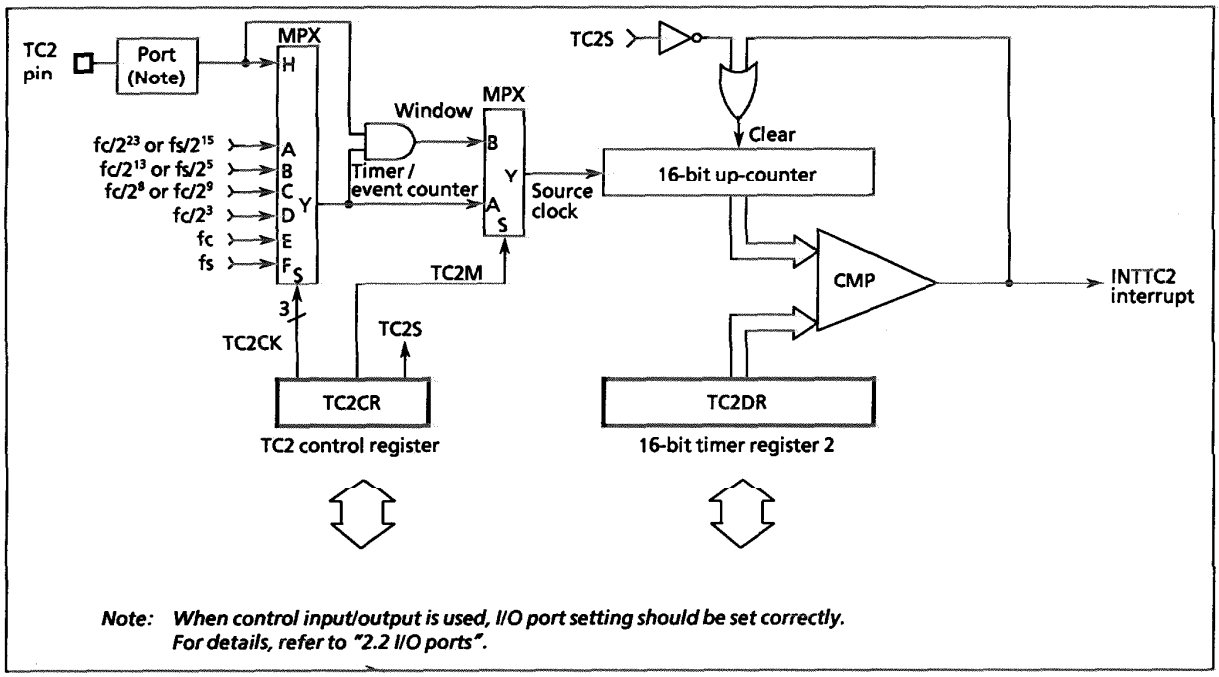


Figure 2-28. Timer/Counter 2 (TC2)

2.7.2 Control

The timer/counter 2 is controlled by a timer/counter 2 control register (TC2CR) and a 16-bit timer register 2 (TC2DR). Reset does not affect TC2DR.

TC2DR (0025, 0024$_H$) R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC2DR$_H$ (0025$_H$)								TC2DR$_L$ (0024$_H$)							

TC2CR (0013$_H$)

7	6	5	4	3	2	1	0
		TC2S	TC2CK				TC2M

(Initial value: **00 00*0)

TC2M	TC2 operating mode select	0: Timer/event counter mode 1: Window mode					R/W
TC2CK	TC2 source clock select [Hz]		NORMAL1/2, IDLE1/2 mode		Divider	SLOW1/2 mode	SLEEP1/2 mode	
			DV7CK = 0	DV7CK = 1			
		000	fc/2^{23}	fs/2^{15}	DV21	fs/2^{15}	fs/2^{15}	
		001	fc/2^{13}	fs/2^{5}	DV11	fs/2^{5}	fs/2^{5}	
		010	fc/2^{8}	fc/2^{8}	DV6	–	–	
		011	fc/2^{3}	fc/2^{3}	DV1	–	–	
		100	–	–	–	fc	–	
		101	fs	fs	–	–	–	
		110	Reserved					
		111	External clock (TC2 pin input)					
TC2S	TC2 start control	0: Stop and counter clear 1: Start					

*Note 1: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz], *; Don't care*

Note 2: When writing to the Timer Register 2 (TC2DR), always write to the lower side (TC2DR$_L$) and then the upper side (TC2DR$_H$) in that order. Writing to only the lower side (TC2DR$_L$) or the upper side (TC2DR$_H$) has no effect.

Note 3: The Timer Register 2 (TC2DR) uses the value previously set in it for coincidence detection until data is written to the upper side (TC2DR$_H$) after writing data to the lower side (TC2DR$_L$).

Note 4: Set the mode and source clock when the TC2 stops (TC2S = 0).

Note 5: Values to be loaded to the timer register must satisfy the following condition.

TC2DR > 1 (TC2DR$_{15\ to\ 11}$ > 1 at warm-up)

Note 6: "fc" can be loaded as the source clock only in the timer mode during the SLOW mode.

Note 7: If a read instruction is executed for TC2CR, read data of bits 7, 6 and 1 are unstable.

Figure 2-29. Timer Register 2 and TC2 Control Register

2.7.3 Function

The timer/counter 2 has three operating modes: timer, event counter and window modes. Also timer/counter 2 is used for warm-up when switching from SLOW mode to NORMAL2 mode.

(1) Timer mode

In this mode, the internal clock is used for counting up. The contents of TC2DR are compared with the contents of up-counter. If a match is found, a timer/counter 2 interrupt (INTTC2) is generated, and the counter is cleared. Counting up is resumed after the counter is cleared.
Also, when "fc" is selected as the source clock during SLOW mode, the lower 11 bits of TC2DR are ignored and an INTTC2 interrupt is generated by matching the upper 5 bits. Thus, in this case, only the $TC2DR_H$ setting is necessary.

Table 2-6. Source Clock (internal clock) for Timer / Counter 2 (at fc = 16.0 MHz, fs = 32.768 kHz)

TC2CK	NORMAL1/2, IDLE1/2 mode			
	DV7CK = 0		DV7CK = 1	
	Resolution	Maximum time setting	Resolution	Maximum time setting
000	524.3 s	9.54 h	1 s	18.2 h
001	512.0 μs	33.6 s	0.98 ms	1.07 min
010	16.0 μs	1.05 s	16.0 μs	1.05 s
011	0.5 μs	32.8 ms	0.5 μs	32.8 ms
100	–	–	–	–
101	30.5 μs	2.0 s	30.5 μs	2 s

TC2CK	SLOW mode		SLEEP mode	
	Resolution	Maximum time setting	Resolution	Maximum time setting
000	1 s	18.2 h	1 s	18.2 h
001	0.98 ms	1.07 min	0.98 ms	1.07 min
01*	–	–	–	–
100	62.5 ns (Note)	–	–	–
101	–	–	–	–

Note: "fc" can be used only in the timer mode. It is used for warm-up when switching from SLOW mode to NORMAL2 mode.

Example: Sets the timer mode with source clock $fc/2^3$ [Hz] and generates an interrupt every 25 ms (at fc = 16 MHz).

```
LDW (TC2DR), C350H      ; Sets TC2DR (25 ms ÷ 2^3/fc = C350H)
LD  (INTSEL), 01H       ; IL15 ← INTTC2
DI                      ; IMF = "0"
SET (EIRH). 5           ; Enables INTTC2 interrupt
EI                      ; IMF – "1"
LD  (TC2CR), 00001100B  ; TC2CK ← "011", TC2M ← "0"
LD  (TC2CR), 00101100B  ; Starts TC2
```

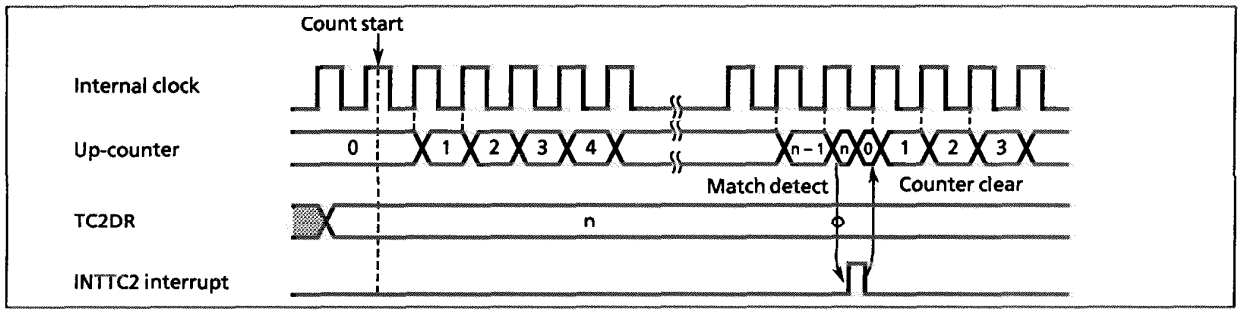


Figure 2-30. Timer Mode Timing Chart

(2) Event counter mode

In this mode, events are counted on the rising edge of the TC2 pin input. The contents of TC2DR are compared with the contents of the up-counter. If a match is found, an INTTC2 interrupt is generated, and the counter is cleared. The maximum frequency applied to the TC2 pin is shown in Table 2-6. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width. Match detect is executed on the falling edge of the TC2 pin. A match can not be detected and INTTC2 is not generated when the pulse is still in a falling state.

Example: Sets the event counter mode and generates an INTTC2 interrupt 640 counts later.

```
LDW  (TC2DR), 640          ;  Sets TC2DR
LD   (INTSEL), 01H         ;  IL15 ← INTTC2
DI                         ;  IMF = "0"
SET  (EIRH). 5             ;  Enables INTTC2 interrupt
EI                         ;  IMF = "1"
LD   (TC2CR), 00011100B    ;  TC2CK ← "111", TC2M ← "0"
LD   (TC2CR), 00111100B    ;  Starts TC2
```

Table 2-7. Timer/Counter 2 External Clock Source

Maximum applied frequency [Hz]	
NORMAL1/2, IDLE1/2 mode	SLOW, SLEEP mode
$fc/2^4$	$fs/2^4$

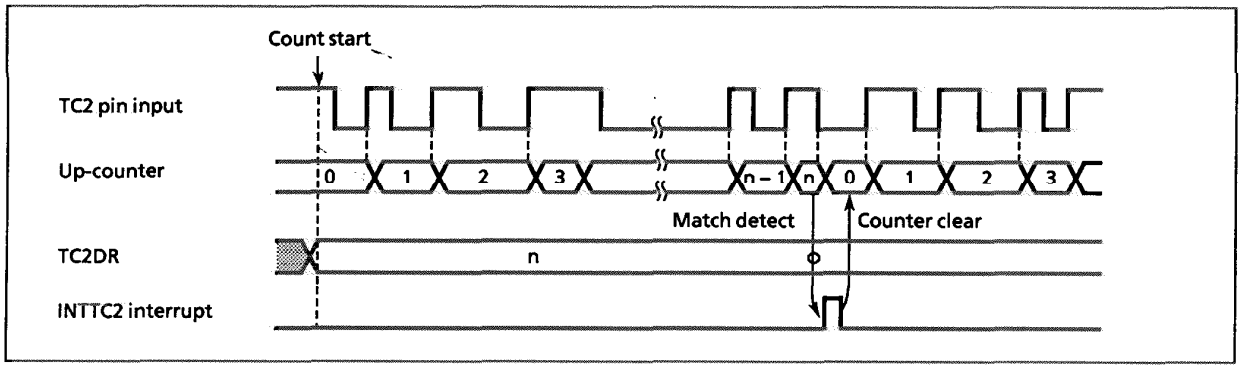


Figure 2-31. Event Counter Mode Timing Chart

(3) Window mode

In this mode, counting up performed on the rising edge of an internal clock during TC2 external pin input (window pulse) is "H" level. The contents of TC2DR are compared with the contents of up-counter. If a match found, an INTTC2 interrupt is generated, and the up-counter is cleared.
The maximum applied frequency (TC2 input) must be considerably slower than the selected internal clock.

Example: Generates an interrupt, inputting "H" level pulse width of 120 ms or more. (at fc = 16 MHz)

```
LDW  (TC2DR), 00EAH      ;  Sets TC2DR (120 ms ÷ 2^10/fc = 00EAH)
LD   (INTSEL), 01H       ;  IL15 ← INTTC2
DI                       ;  IMF = "0"
SET  (EIRH). 5           ;  Enables INTTC2 interrupt
EI                       ;  IMF = "1"
LD   (TC2CR), 00000101B  ;  TC2CK ← "001", TC1M ← "1"
LD   (TC2CR), 00100101B  ;  Starts TC2
```

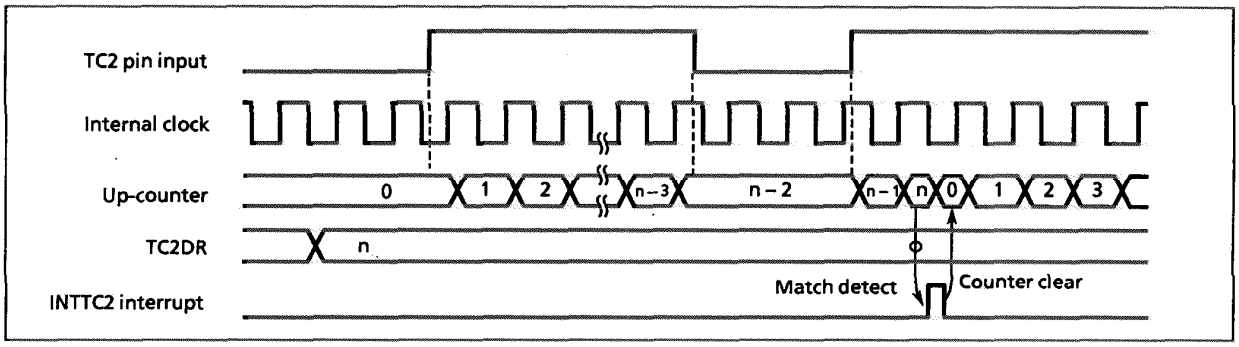
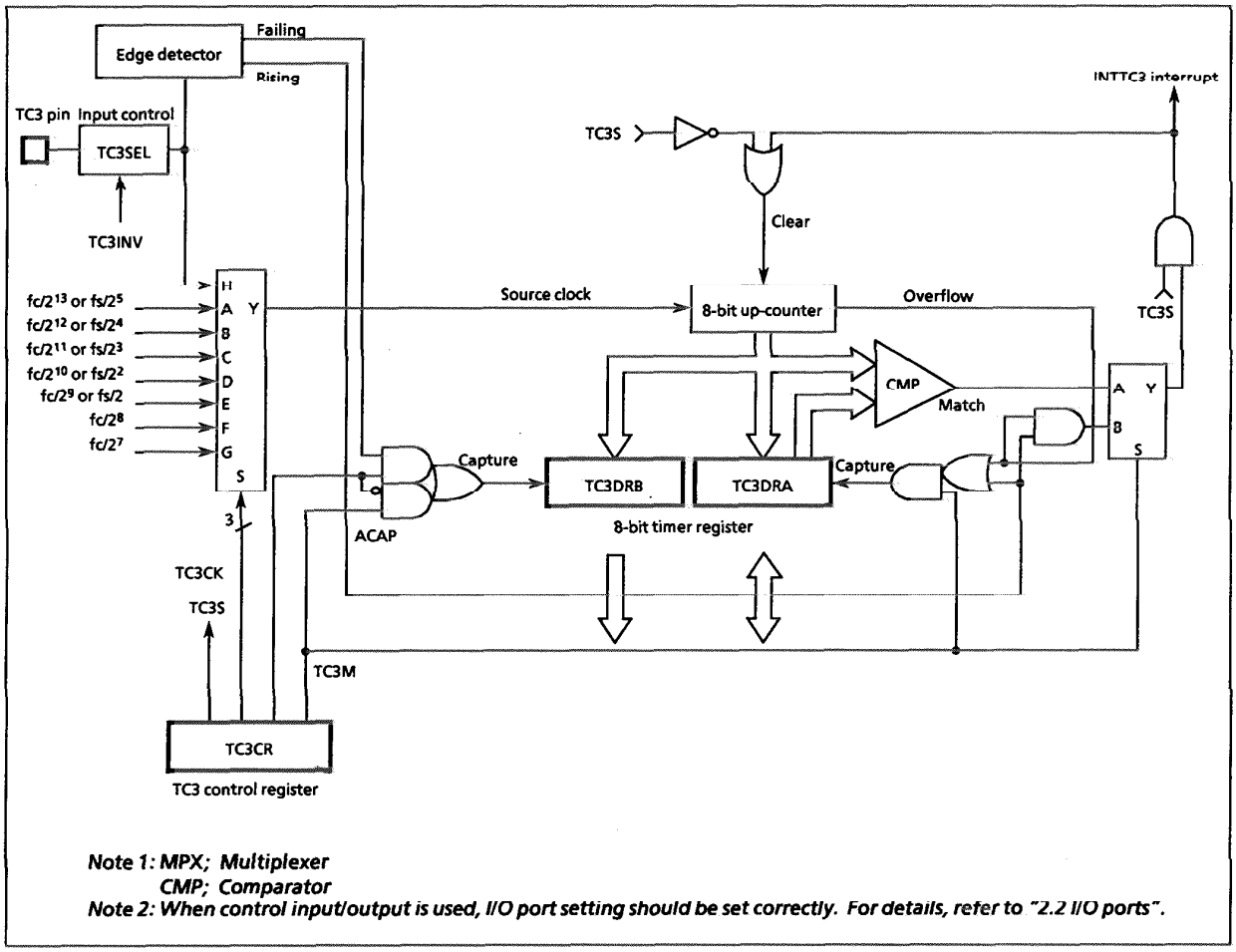


Figure 2-32. Window Mode Timing Chart

2.8 8-Bit Timer/Counter 3

2.8.1 Configuration



Note 1: MPX; Multiplexer
CMP; Comparator
Note 2: When control input/output is used, I/O port setting should be set correctly. For details, refer to "2.2 I/O ports".

Figure 2-33. Timer/Counter 3 (TC3)

2.8.2 Control

The timer/counter 3 is controlled by a timer/counter 3 control register (TC3CR) and two 8-bit timer registers (TC3DRA and TC3DRB)

TC3DRA (0010_H) R/W — 7 6 5 4 3 2 1 0 — (Initial value: 1111 1111)

TC3DRB (0011_H) Read only — (Initial value: 1111 1111)

TC3CR (0012_H) — 7 6 5 4 3 2 1 0 — ACAP | | TC3S | TC3CK | TC3M — (Initial value: *0*0 0000)

TC3M	TC3 operation mode set	0: Timer / event counter 1: Capture					R/W
TC3CK	TC3 source clock select [Hz]		NORMAL1/2, IDLE1/2 mode		Divider	SLOW1/2, SLEEP1/2 mode	
			DV7CK = 0	DV7CK = 1			
		000	$fc/2^{13}$	$fs/2^5$	DV11	$fs/2^5$	
		001	$fc/2^{12}$	$fs/2^4$	DV10	$fs/2^4$	
		010	$fc/2^{11}$	$fs/2^3$	DV9	$fs/2^3$	
		011	$fc/2^{10}$	$fs/2^2$	DV8	$fs/2^2$	
		100	$fc/2^9$	fs/2	DV7	fs/2	
		101	$fc/2^8$	$fc/2^8$	DV6	–	
		110	$fc/2^7$	$fc/2^7$	DV5	–	
		111	External clock (TC3 pin input)				
TC3S	TC3 start select	0: Stop and clear 1: Start					
ACAP	Auto-capture control	0: – 1: Software capture trigger					

*Note 1: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *: Don't care*

Note 2: Set the mode and the source clock when the TC3 stops (TC3S = 0).

Note 3: Values to be loaded into timer register 3A must satisfy the following condition.
TC3DRA > 1 (in the timer and event counter mode)

Note 4: Auto-capture can be used only in the timer and event counter mode.

Note 5: If a read instruction is executed for TC3CR, read data of bits 7 and 5 are unstable.

Note 6: During TC3 operation, do not change TC3DRA.

TC3 input control (normal/invert)

TC3SEL (0029H) — 7 6 5 4 3 2 1 0 — TC3INV — (Initial value: **** ***0)

TC3INV	TC3 input control	0: Normal 1: Invert	R/W

Note: If a read instruction is executed for TC3SEL, read data of bits 7 to 1 are unstable.

Figure 2-34. Timer Register 3 and TC3 Control Register

2.8.3 TC3 input control register

This microcomputer has the function to invert or not to invert the waveform entered from the TC3 pin. This selection is made by using TC3SEL <TC3INV>.

2.8.4 Function

The timer/counter 3 has three operating modes: timer, event counter, and capture mode.
When it is used in the capture mode, the noise rejection time of TC3 pin input can be set by remote control receive control register.

(1) Timer mode

In this mode, the internal clock is used for counting up. The contents of TC3DRA are compared with the contents of up-counter. If a match is found, a timer/counter 3 interrupt (INTTC3) is generated, and the up-counter is cleared. The current contents of up-counter are loaded into TC3DRB by setting ACAP (bit6 in TC3CR) to "1" (Auto-capture function).
The contents of up-counter can be easily confirmed by executing the read instruction (RD instruction) of TC3DRB. Loading the contents of up-counter is not synchronized with counting up. The contents of over flow (FF_H) and 00_H can not be loaded correctly. It is necessary to consider the count cycle.

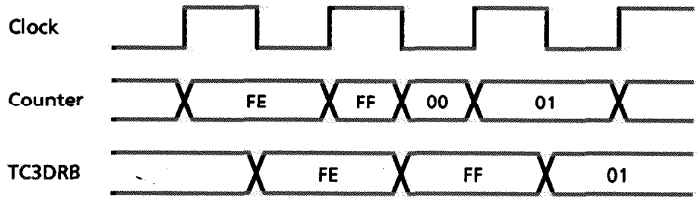


Table 2-8. Source Clock (internal clock) for Timer/Counter 3 (Example: at fc = 16.0 MHz, fs = 32.768 kHz)

TC3CK	NORMAL1/2, IDLE1/2 mode			
	DV7CK = 0		DV7CK = 1	
	Resolution [μs]	Maximum setting time [ms]	Resolution [μs]	Maximum setting time [ms]
000	512	130.6	976.56	249.0
001	256	65.3	488.28	124.5
010	128	32.6	244.14	62.3
011	64	16.3	122.07	31.1
100	32	8.2	61.01	15.6
101	16	4.1	16.0	4.1
110	8	2.0	8.0	2.0

TC3CK	SLOW, SLEEP mode	
	Resolution [μs]	Maximum setting time [ms]
000	976.56	249.0
001	488.28	124.5
010	244.14	62.3
011	122.07	31.1
100	61.01	15.6
101	–	–
110	–	–

(2) Event counter mode

In this mode, events are counted on the edge of the TC3 pin input. The input pulse at the TC3 pin can have its polarity inverted using the TC3SEL Register TC3INV bit. When TC3INV = "0", the counter counts up on the rising edge of the TC3 pin input and when its value matches the TC3DRA set value, it is cleared while at the same time generating an INTTC3 interrupt. When TC3INV = "1", the counter counts up on the falling edge of the TC3 pin input and when its value matches the TC3DRA set value, it is cleared while at the same time generating an INTTC3 interrupt.

Because detection of a match is performed on the other side of the TC3 input edge at which the counter counts up (i.e., on the falling edge when TC3INV = "0" or the rising edge when TC3INV = "1"), detection of a match is not performed until the opposite edge is encountered, nor is an INTTC3 interrupt generated.

The minimum pulse width is shown in Table 2-9. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width.

The current contents of up-counter are loaded into TC3DRB by setting ACAP (bit 6 in TC3CR) to "1" (Auto-capture funcion).

The contents of up-counter can be easily confirmed by executing the read instruction (RD instruction) of TC3DRB. Loading the contents of up-counter is not synchronized with counting up. The contents of over flow (FF_H) and 00_H can not be loaded correctly. It is necessary to consider the count cycle.

Example: Generates an interrupt every 0.5 s, inputting 50 Hz pulses to the TC3 pin.

```
LD   (TC3SEL), 00000000B   ;  TC3 normal input
LD   (TC3CR), 00001110B    ;  Set the clock mode
LD   (TC3DRA), 19H         ;  0.5 s÷1/50=25=19H
LD   (TC3CR), 00011110B    ;  Starts TC3
```

Table 2-9. Source Clock (External Clock) for Timer/Counter

	Minimum pulse width	
	NORMAL1/2, IDLE1/2 mode	SLOW, SLEEP mode
"H" width	2^2/fc	2^2/fs
"L" width	2^2/fc	2^2/fs

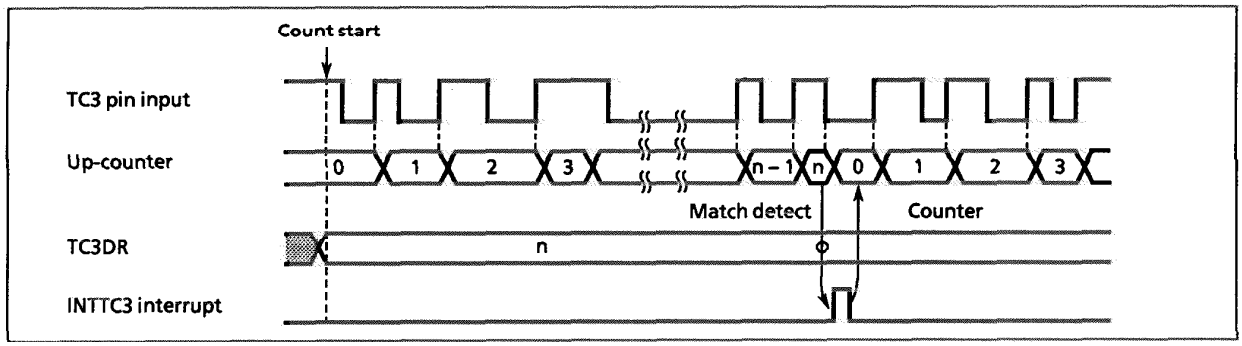


Figure 3-35. Event Counter Mode Timing Chart

(3) Capture mode

The pulse width, period and duty of the TC3 pin input are measured in this mode, which can be used in decoding the remote control signals or distinguishing AC 50/60 Hz, etc. The TC3 pin input can have its polarity changed between normal and inverse by using the TC3SEL Register.

The minimum pulse width is shown in Table 2-9. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width.

After command start, the counter operates in free-running mode with the internal clock, and the counter value is latched into TC3DRB on the falling edge of the TC3 pin input when TC3INV = "0" or on the rising edge when TC3INV = "1". In this case, the counter continues counting, with the counter value latched into TC3DRA on the opposite edge (i.e., on the rising edge when TC3INV = "0" or the falling edge when TC3INV = "1"), and the counter is cleared while at the same time generating an interrupt. If the counter overflows before the edge is detected, FF_H is set into TC3DRA, and the counter is cleared and an INTTC3 interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TC3DRA value is FF_H. Also, after an interrupt (capture to TC3DRA, or overflow detection) is generated, capture and overflow detection are halted until TC3DRA has been read out ; however, the counter continues. As reading out TC3DRA resumes capture / overflow detection, TC3DRB must be beforehand read out.

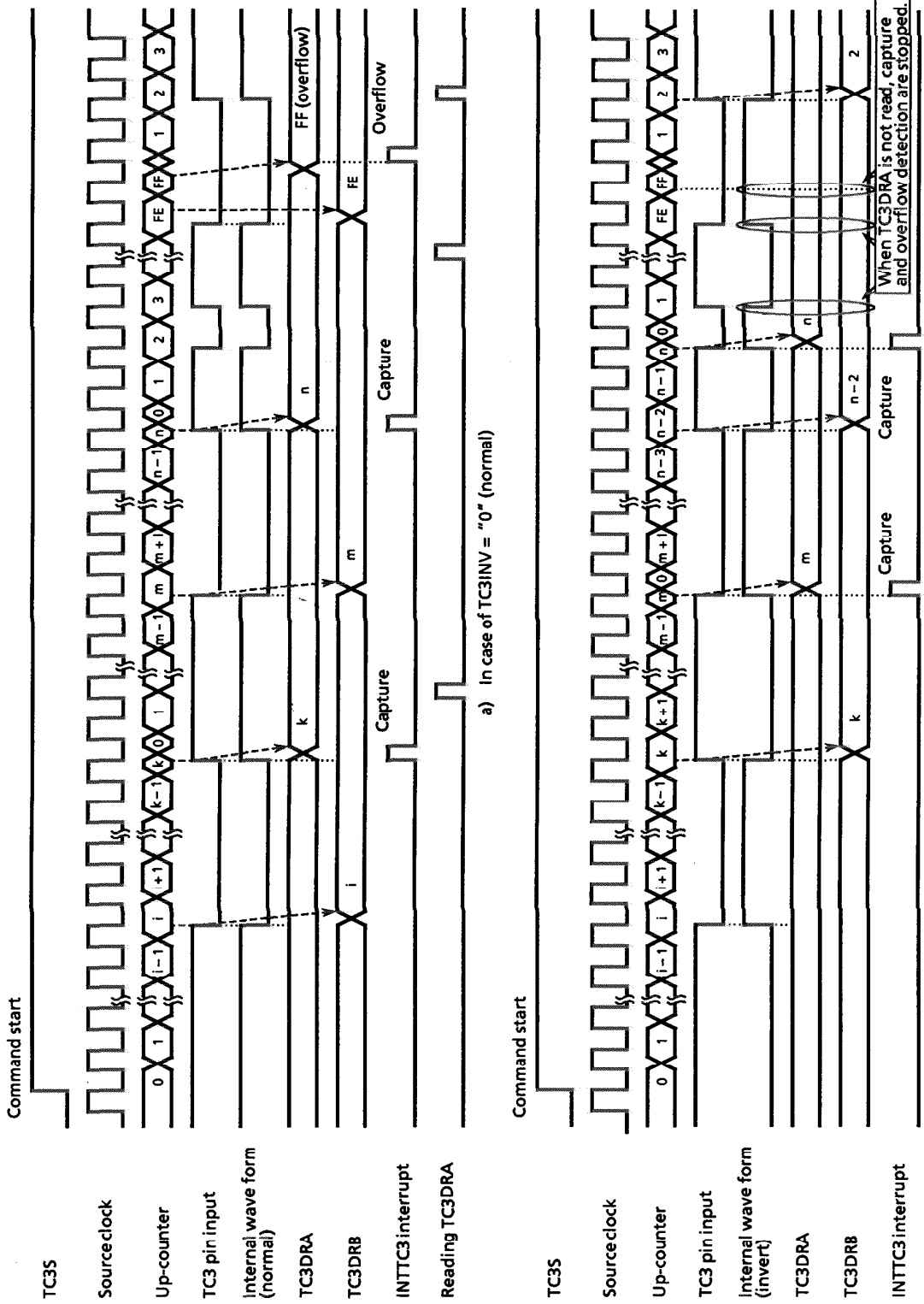
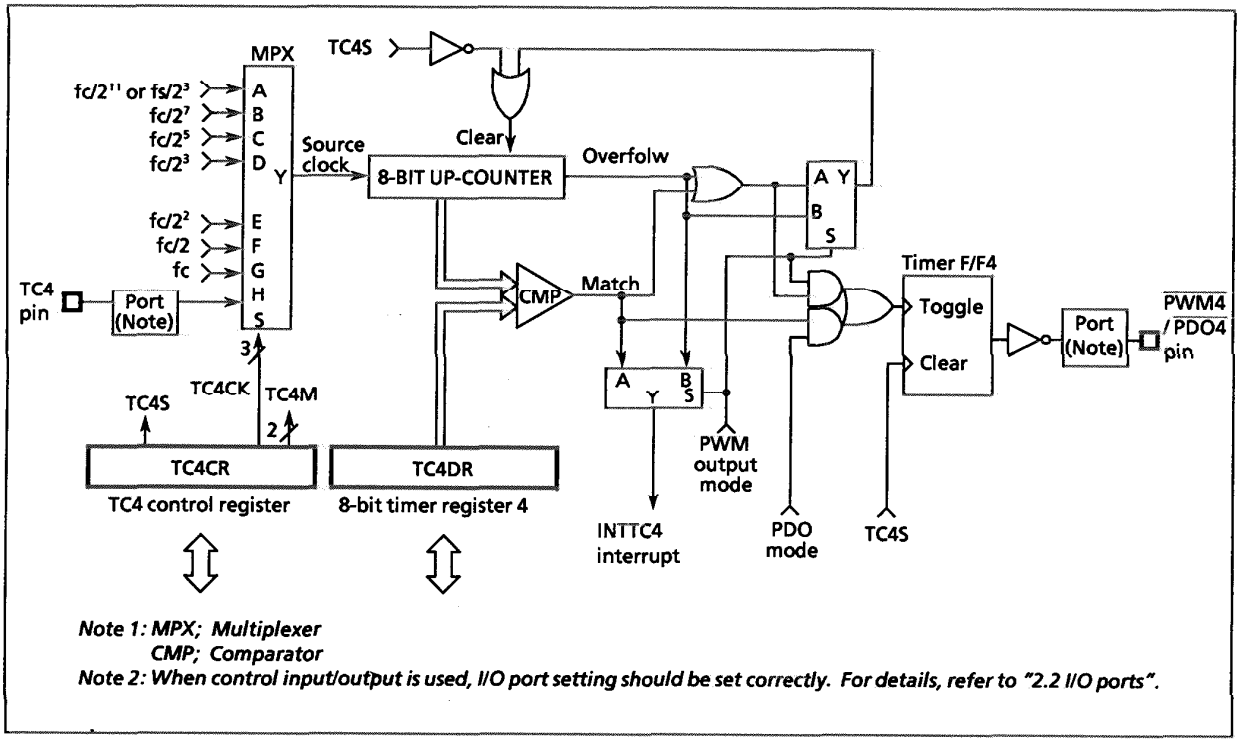


Figure 2-36. Capture mode timing chart

2.9 8-Bit Timer/Counter 4

2.9.1 Configuration



Note 1: MPX; Multiplexer
CMP; Comparator
Note 2: When control input/output is used, I/O port setting should be set correctly. For details, refer to "2.2 I/O ports".

Figure 2-37. Timer/Counter 4 (TC4)

2.9.2 Control

The timer/counter 4 is controlled by a timer/counter 4 control register (TC4CR) and an 8-bit timer register 4 (TC4DR). Reset does not affect TC4DR.

TC4DR (0018_H) R/W

7	6	5	4	3	2	1	0

(Initial value: 1111 1111)

TC4CR (0014_H)

7	6	5	4	3	2	1	0
		TC4S	TC4CK			TC4M	

(Initial value: **00 0000)

TC4S	TC4 start control	0: Stop and counter clear 1: Start				R/W
TC4CK	TC4 source clock select [Hz] (in sequence from bit 5, 3, 2)		NORMAL1/2, IDLE1/2 mode		Divider	SLOW1/2,SLEEP1/2 mode	
			DV7CK = 0	DV7CK = 1			
		000	$fc/2^{11}$	$fs/2^3$	DV9	$fs/2^3$	
		001	$fc/2^7$	$fc/2^7$	DV5	–	
		010	$fc/2^5$	$fc/2^5$	DV3	–	
		011	$fc/2^3$	$fc/2^2$	DV1	–	
		100	$fc/2^2$	$fc/2^2$	$fc/2^2$	–	
		101	fc/2	fc/2	fc/2	–	
		110	fc	fc	fc	–	
		111	External clock (TC4 pin input)				
TC4M	TC4 operating mode select	00: Timer/event counter mode 01: reserved 10: Programmable divider output (PDO) mode 11: Pulse width modulation (PWM) output mode					

*Note 1: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz], * ; Don't care*

Note 2: Values to be loaded to the timer register must satisfy the following condition.
$1 \leq TC4DR \leq 255$

Note 3: When TC4 operation is started (TC4S = "0"→"1") or TC4 operation is stopped (TC4S = "1"→"0"), do not change TC4CR<TC4M,TC4CK>. Also, during TC4 operation (TC4S = "1"→"1"), do not change TC4CR <TC4M,TC4CK>.

Note 4: Available source clocks for each operation mode is referred to the following table.

		Timer mode	Event counter mode	PDO mode	PWM mode
TC4CK	000	○	×	○	×
	001	○	×	○	×
	010	○	×	○	×
	011	○	×	×	○
	100	×	×	×	○
	101	×	×	×	○
	110	×	×	×	○
	111	×	○	×	×

Note 5: The TC4S is automatically cleared to "0" after starting STOP mode.

Note 6: If a read instruction is executed for TC4CR, read data of bits 7 and 6 are unstable.

Note 7: During TC4 operatin except PWM mode, do not change TC4DR.

Note 8: When the operating frequency exceeds 10 MHz, do not select "110" for TC4CK.

Note 9: When used as the NORMAL1 and IDLE1 modes, the TC4 source clock can not use the "fs".

Figure 2-38. Timer Register 4 and TC4 Control Register

2.9.3 Function

The timer/counter 4 has four operating modes: timer, event counter, programmable divider output, and PWM output mode.

(1) Timer mode

In this mode, the internal clock is used for counting up. The contents of TC4DR is compared with the contents of up-counter. If a match is found, an INTTC4 interrupt is generated and the up-counter is cleared to "0". Counting up resumes after the up-counter is cleared.

Table 2-10. Source Clock (internal clock) for Timer/Counter 4
(Example: at fc = 16.0 MHz, fs = 32.768 kHz)

TC4CK	NORMAL1/2, IDLE1/2 mode			
	DV7CK = 0		DV7CK = 1	
	Resolution [μs]	Maximum setting time [s]	Resolution [μs]	Maximum setting time [s]
000	128.0	32.6 m	244.14	62.2 m
001	8.0	2.0 m	8.0	2.0 m
010	2.0	510 μ	2.0	510 μ
100	0.5	128 μ	0.5	128 μ

TC4CK	SLOW, SLEEP mode	
	Resolution [μs]	Maximum setting time [s]
000	244.14	62.2 m

(2) Event counter mode

In this mode, events are counted on the rising edge of the TC4 pin input (external clock).
The contents of the TC4DR is compared with the contents of the up-counter. If a match is found, an INTTC4 interrupt is generated and the counter is cleared. Counting up resumes after the up-counter is cleared. The maximum applied frequency is shown in Table 2-11. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width.
Match detect is executed on the falling edge of the TC4 pin. A match can not be detected and INTTC4 is not generated when the pulse is still in a falling state.

Table 2-11. Timer/Counter 4 External Clock Source

	NORMAL1/2, IDLE1/2 mode
"H" width	2^3/fc
"L" width	2^3/fc

Note: The event counter mode can be used in NORMAL1, 2 and IDLE1, 2 modes.

(3) Programmable Divider Output (PDO) mode

The internal clock is used for counting up. The contents of TC4DR is compared with the contents of the up-counter. If a match is found, the timer F/F output is toggled and the counter is cleared. Timer F/F output is inverted and output to the $\overline{PDO4}$ pin. When programmable divider output is executed, P12 output latch is set to "1" and P12 is set to output mode. This mode can be used for approximate 50% duty pulse output. An INTTC4 interrupt is generated each time the $\overline{PDO4}$ output is toggled.

Example: Output a 1024 Hz pulse (at fc = 4.194304 MHz)

```
LD    (TC4CR), 0000 0110B    ;  Sets PDO mode (TC4M = 10, TC4CK = 001)
SET   (P1DR). 2              ;  P12 output latch ← 1
SET   (P1OUTCR). 2           ;  P12 output mode
LD    (TC4DR), 10H           ;  1/1024 ÷ 2^7/fc ÷ 2 = 10H
LD    (TC4CR), 00100110B     ;  Stats TC4
```

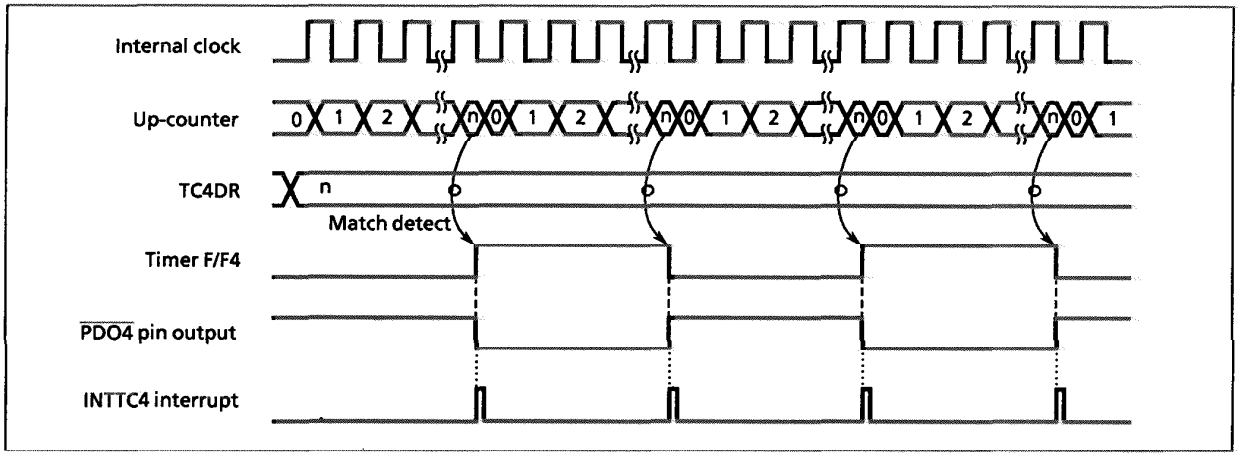


Figure 2-39. PDO Mode Timing Chart

(4) Pulse Width Modulation (PWM) output mode

PWM output with a resolution of 8 bits is possible. The internal clock is used for counting up. The contents of TC4DR is compared with the contents of up-counter. If a match is found, the timer F/F output is toggled. Counting up resumes. And, when an overflow occurs, the timer is again toggled and the counter is cleared. Timer F/F output is inverted and output to the $\overline{\text{PWM4}}$ pin. When PWM output is executed, P12 output latch is set to "1" and P12 is set to output mode. An INTTC4 interrupt is generated when an overflow occurs.

TC4DR is configured a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TC4DR is overwritten; therefore, output can be altered continuously. Also, the first time, TC4DR is shifted by setting TC4CR to "1" after data are loaded to TC4DR.

Note: The PWM output can be used in NORMAL1, 2 and IDLE 1, 2 modes.

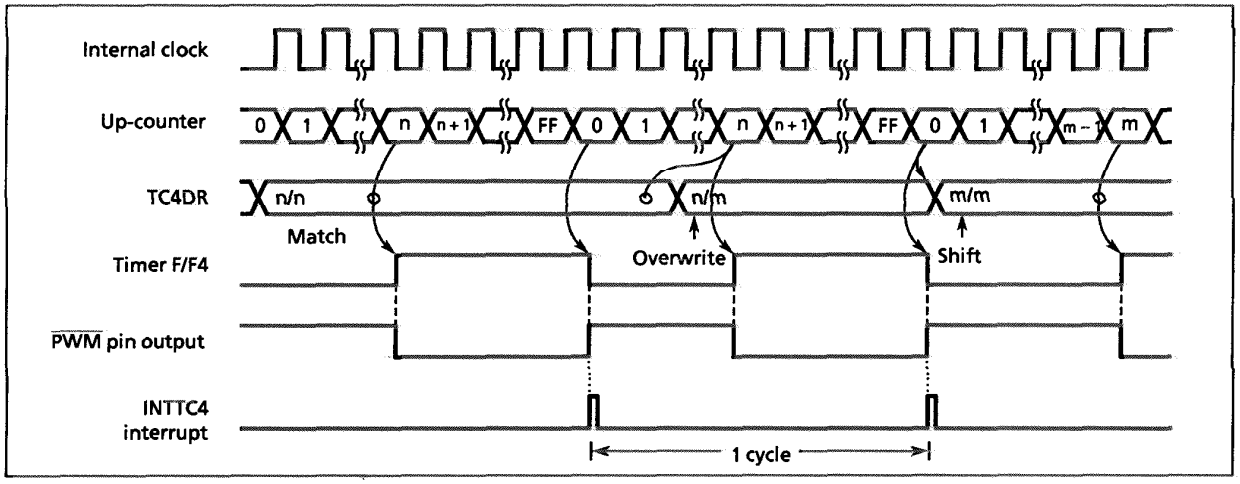


Figure 2-40. PWM Output Mode Timing Chart

Table 2-12. PWM Output Mode (Example: fc = 16 MHz)

TC4CK	NORMAL1/2, IDLE1/2 mode			
	DV7CK = 0		DV7CK = 1	
	Resolution [ns]	Repeat cycle [μs]	Resolution [ns]	Repeat cycle [μs]
000	—	—	—	—
001	—	—	—	—
010	—	—	—	—
011	500	128	500	128
100	250	64	250	64
101	125	32	125	32
110	—	—	—	—

Note: When the operating frequency exceeds 10 MHz, do not select "110" for TC4CK.

2.10 SIO (Synchronous Serial Interface)

The TMP86CK74A/CM74A contains one channel of SIO (synchronous serial interface). This serial interface connects to external devices via the SI, SO, and $\overline{SCK}$ pins. The SI, SO, and $\overline{SCK}$ pins respectively are shared with P15, P16, and P17. When using these pins for the serial interface, set the output latches of the respective P1 ports to "1".

2.10.1 Configuration

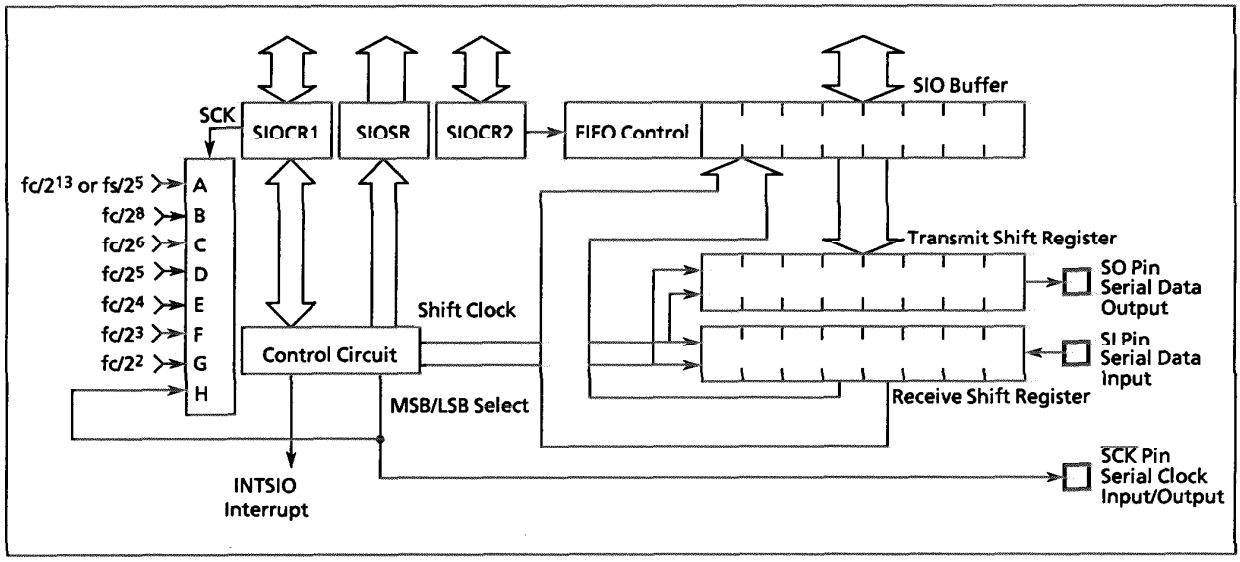


Figure 2-41. Configuration of the Serial Interface

2.10.2 Control

The SIO is controlled using Serial Interface Control Register 1 (SIO1CR1) and Serial Interface Control Register 2 (SIO1CR2). Also, a SIO Status Register (SIO1SR) is included, which may be used to know the operating status of the serial interface by reading its flags.

Serial Interface Control Register 1

SIO1CR1 (0019_H)

7	6	5	4	3	2	1	0
SIOS	SIOINH	SIOERM		SIODIR	SCK		

(Initial value: 0000 0000)

			R/W
SIOS	Indicate transfer start/stop	0: Stop 1: Start	
SIOINH	Continue/abort transfer (Note 1)	0: Continues transfer 1: Abort transfer (automatically cleared after abort)	
SIOM	Transfer mode select	00: Transmit mode 01: Receive mode 10: Transmit/receive mode 11: reserved	
SIODIR	Select direction of transfer	0: MSB (transmitted/received beginning with bit 7) 1: LSB (transmitted/received beginning with bit 0)	

SCK	Serial clock select	NORMAL1/2, IDLE1/2 mode		Source clock	SLOW1/2, SLEEP1/2 mode
		DV7CK = 0	DV7CK = 1		
000		$fc/2^{13}$	$fs/2^5$	DV11	$fs/2^5$
001		$fc/2^8$	$fc/2^8$	DV6	–
010		$fc/2^6$	$fc/2^6$	DV4	–
011		$fc/2^5$	$fc/2^5$	DV3	–
100		$fc/2^4$	$fc/2^4$	DV2	–
101		$fc/2^3$	$fc/2^3$	DV1	–
110		$fc/2^2$	$fc/2^2$	$fc/2^2$	–
111		External clock (supplied from the SCK pin)	External clock (supplied from the SCK pin)	–	–

Note 1: If SIOINH is set, the SIOS, SIOF, SEF, TXF, RXF, TXERR and RXERR are initialized.

Note 2: The SCK must select that set more the 1Mbps.

Note 3: reserved; Do not set by the program

Figure 2-42. Serial Interface Control Registers 1 and 2

Serial Interface Control Register 2

SIOCR2 ($001A_H$)

7	6	5	4	3	2	1	0	
			SIORXD					(Initial value: ***0 0000)

SIORXD	Set number of data bytes to transmit/receive	00h: 1-byte transfer 01h: 2-byte transfer 02h: 3-byte transfer 03h: 4-byte transfer ⋮ 1Fh: 32-byte transfer 20~3Fh to 0FFh: Reserved	R/W

Note 1: Make sure the SIO is idle (SIOF = "0") before setting the number of data bytes to transfer.
Note 2: The number of data bytes to transfer is used for transmit and receive operations in common.
Note 3: Always write "0" to bits 7 to 5.

Serial Interface Status Register

SIOSR ($001B_H$)

7	6	5	4	3	2	1	0	
SIOF	SEF	TXF	RXF	TXERR	RXERR			(Initial value: 0100 00**)

SIOF	Monitor operating status of serial transfer	0: Transfer terminated (Note 1) 1: Transfer in process	Read only
SEF	Shift operation status flag	0: Shift operation terminated 1: Shift operation in process	
TXF	Transmit buffer flag	0: Data exists in transfer buffer 1: No data exists in transfer buffer	
RXF	Receive buffer flag	0: No data exists in receive buffer 1: Data exists in receive buffer	
TXERR	Transmit error flag (Note 2)	0: Transmit operation performed normally 1: Error occurred when transmitting	R/W (Note 3)
RXERR	Receive error flag (Note 2)	0: Receive operation performed normally 1: Error occurred when receiving	

Note 1: This bit is reset to "0" by clearing SIOS and setting SIOINH for abort transfer or when transfer finishes.
Note 2: The TXERR and RXERR bits can be cleared by writing "0" to the register or setting SIOINH = "1". These errors cannot be cleared by setting SIOS = "0" to stop transfer.
Note 3: The TXERR and RXERR bits can only be cleared (= "0"), and cannot be set by writing "1".
Note 4: If a read instruction is executed for SIOSR, read data of bits 1 and 0 are unstable.
Note 5: The hold time for the last transmit data with respect to the transmit clock is 4/fc < T_{SODH} < 1/8fc.
Note 6: To perform one-byte transmissions successively by using a transmit interrupt, be sure to set the serial clock to "fc/2^4" or greater. This is because if the selected serial clock is "fc/2^3", operation mode change (IDLE or SLEEP) or other operations cannot be completed before generating a transmit interrupt.

Serial Interface Data Buffer

SIOBUF ($001C_H$)

7	6	5	4	3	2	1	0	
								(Initial value: **** ****)

SIOBUF	Transmit/receive data buffer	Set transmit data or store received data	R/W

Note: While transferring multiple bytes of data using the FIFO buffer, do not write to SIOBUF and read from SIOBUF.

Figure 2-43. Serial Interface Control Register 2, Status Register, and Data Buffer Register

2.10.3 Functional Description

(1) Serial clock

a. clock source

One of the following clocks can be selected using SCK (SIOCR1 Register bits 2 to 0).

① Internal clock

A clock with the frequency selected with SCK (SIOCR1 Register bits 2 to 0) (other than "111") is used as the serial clock. Output on the $\overline{SCK}$ pin goes high when transfer starts and when transfer ends.

Table 2-13. Serial Clock Rate

SCK	Clock	Baud Rate	
		fc = 16 MHz	fc = 8 MHz
000	$fc/2^{13}$	1.91 kbps	0.95 kbps
001	$fc/2^{8}$	61.04 kbps	30.51 kbps
010	$fc/2^{6}$	244.14 kbps	122.07 kbps
011	$fc/2^{5}$	488.28 kbps	244.14 kbps
100	$fc/2^{4}$	976.56 kbps	488.28 kbps
101	$fc/2^{3}$	–	976.56 kbps
110	$fc/2^{2}$	–	–
111	External	External	External

1 kbit = 1024 bit

② External clock

An external clock is selected by setting SCK (SIOCR1 Register bits 2 to 0) to "111". In this case, the clock supplied from an external source to the $\overline{SCK}$ pin is used as the serial clock.
To ensure that shift operation is performed without fail, the serial clock must have a pulse width of 4/fc or more for both high and low levels. Therefore, the maximum transfer rate is 976 kbits/s (when fc = 8 MHz).

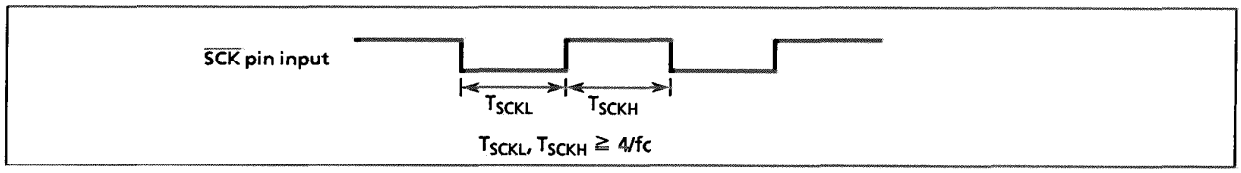


Figure 2-44. External Clock

b. Shift edges

The SIO uses leading-edge shift for transmission and trailing-edge shift for reception.

① Leading-edge shift

Data is shifted out on each leading edge of the serial clock (falling edge of the $\overline{SCK}$ pin input/output).

② Trailing-edge shift

Data is shifted in on each trailing edge of the serial clock (rising edge of the $\overline{SCK}$ pin input/output).

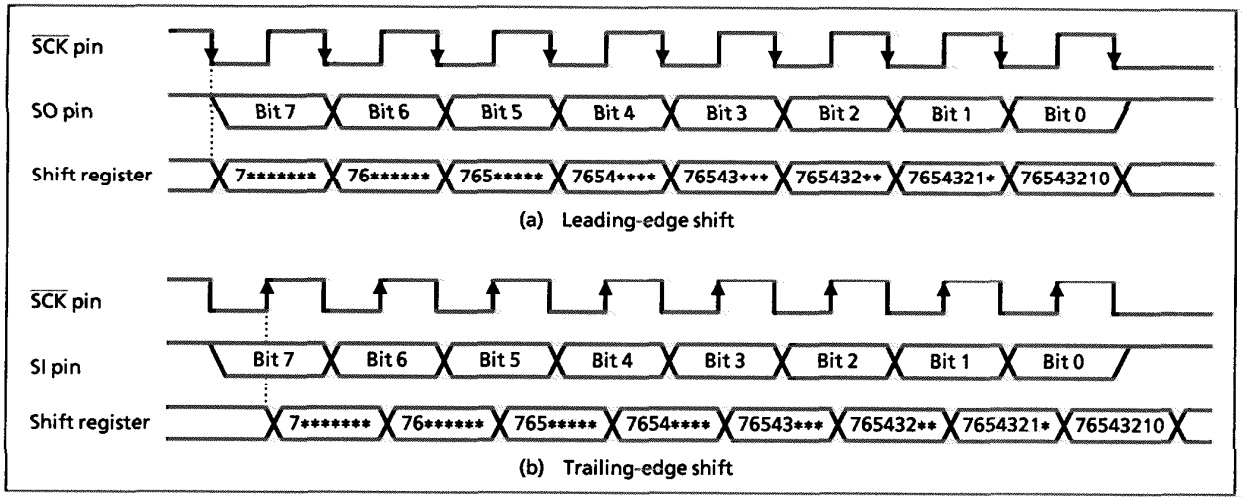


Figure 2-45. Shift Edges

(2) Transfer bit direction

The direction in which 8-bit serial data is transferred can be selected using SIODIR (SIOCR1 Register bit 3). The direction of data transfer applies in common for both transmission and reception, and cannot be set individually.

① MSB transfer

MSB transfer is assumed by setting SIOCR1<SIODIR> to "0", in which case data is transferred sequentially beginning with the most significant bit.

② LSB transfer

LSB transfer is assumed by setting SIOCR1<SIODIR> to "1", in which case data is transferred sequentially beginning with the least significant bit.

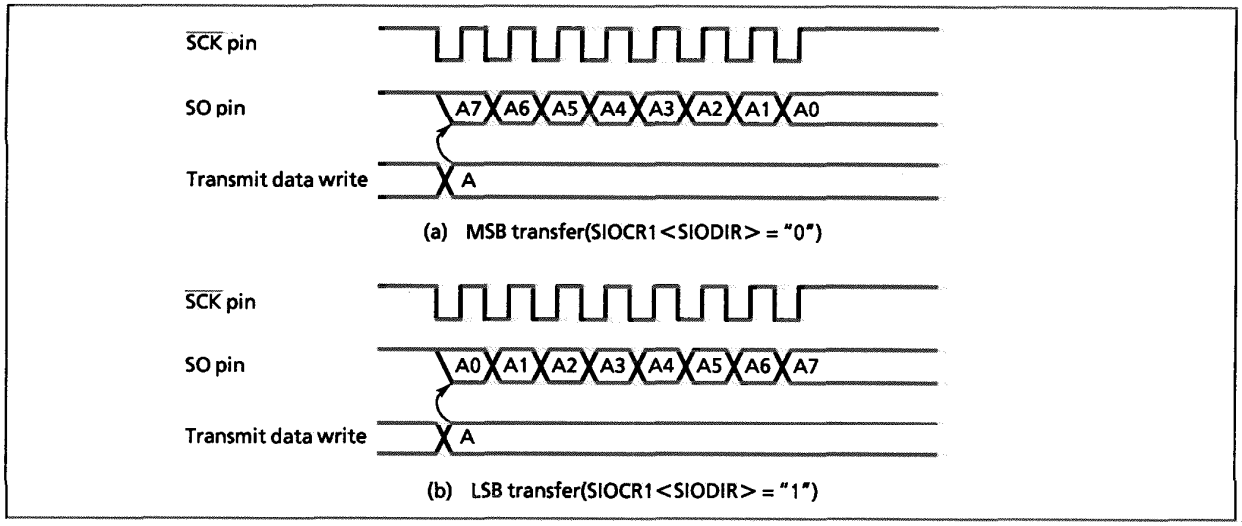


Figure 2-46. Transfer Bit Direction

(3) Transfer modes

Use SIOM (SIOCR1 Register bits 5, 4) to select transmit, receive, or transmit/receive mode.

a. Transmit mode

Transmit mode is assumed by setting SIOM (SIOCR1 Register bits 5, 4) to "00".

Starting SIO operation

① Select transmit mode (SIOCR1 Register bits 5, 4), serial clock rate (SIOCR1 Register bits 2 to 0), and the direction of transfer (SIOCR1 Register bits 3) using the SIOCR1 Register.

② Set the number of bytes to transfer in the SIORXD (SIOCR2 Register bits 4 to 0) Register.

③ Set the number of bytes of transmit data that has been set with the SIORXD (SIOCR2 Register bits 4 to 0) Register in the SIOBUF.

④ Set SIOCR1<SIOS> to "1".

- When the selected serial clock is an internal clock, the SIO immediately starts transmitting data sequentially from the MSB or LSB as selected with SIODIR (SIOCR1 Register bit 3).
- When the selected serial clock is an external clock, the SIO starts transmitting data upon external clock input, sequentially from the MSB or LSB as selected with SIODIR (SIOCR1 Register bit 3).

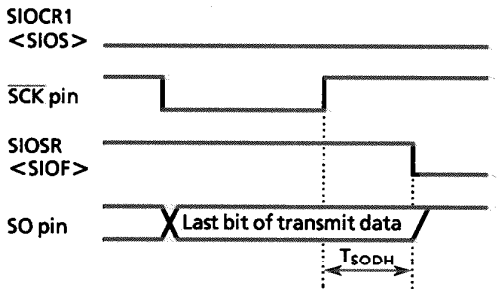
Note 1: Make sure that exactly the same number of bytes as set with the SIO1CR2 Register are written to the Buffer. If the number of data bytes written to the Buffer is larger or smaller than set with the SIOCR2 Register, the SIO may not operate correctly.

Note 2: If necessary to set transmit data back again, first set SIOCR1<SIOINH> to "1" and then write as many bytes of transmit data as set with the SIOCR2 Register to the Buffer again.

Note 3: Always be sure to write as many bytes of transmit data as set with the SIOCR2 Register to the Buffer before starting SIO operation.

Halting SIO operation

⑤ When SIOCR1<SIOS> is cleared, SIO stops. When SIOCR1<SIOS> clear, make sure the Transmit Buffer is empty (SIOSR<TXF> = "1") before clearing SIOCR1<SIOS>, or do this clearing in an INTSIO interrupt routine. However, when transferring the next data, always check to see that transfer has been completed (SIOSR<SIOF> = "0") before writing the next data to the Buffer.



(a) When automatically stopped after clearing SIOS

$16.5/fc \leqq T_{SODH} \leqq 32.5/fc$

Note: fc denotes the high-frequency clock [Hz].

Figure 2-47. Last Bit Hold Time (when Operating with Internal Clock).

- In cases when SIOINH (SIOCR Register bit 6) is set to "1",transmission stops immediately, even in the middle of transmission.

Note : The position at which the SIO generates an INTSIO interrupt is the first bit of the last byte of the data bytes set with the SIOCR2 Register.

Transmit errors

When operating with an external clock, a transmit error is assumed and the transmit error flag (SIOSR<TXERR>) is set to "1" in one of the cases described below. When a transmit error occurs, the transmit data is nullified, with all bits output at the high level.

- After setting SIOCR1<SIOS> to "1", when the $\overline{SCK}$ pin goes low before completion of writing transfer data to the Buffer
- After sending the number of data which is selected by SIOCR2, when the $\overline{SCK}$ pin goes low before completion of writing the first transfer data to the Buffer

When a transmit error is detected, be sure to forcibly terminate the SIO by setting SIOCR1 <SIOINH> to "1". When SIOCR1<SIOINH> is set to "1", and the SIOSR Register, as well as SIOCR1<SIOS>, all are initialized. (Other registers and bits are not initialized.)

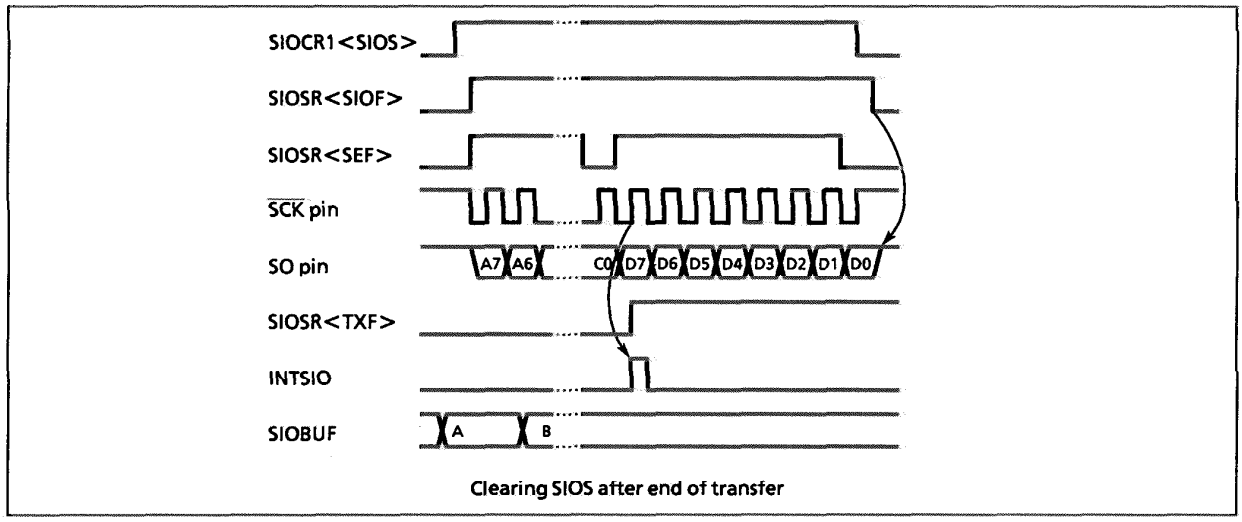


Figure 2-48. Timing at Which to Clear SIOCR1<SIOS>

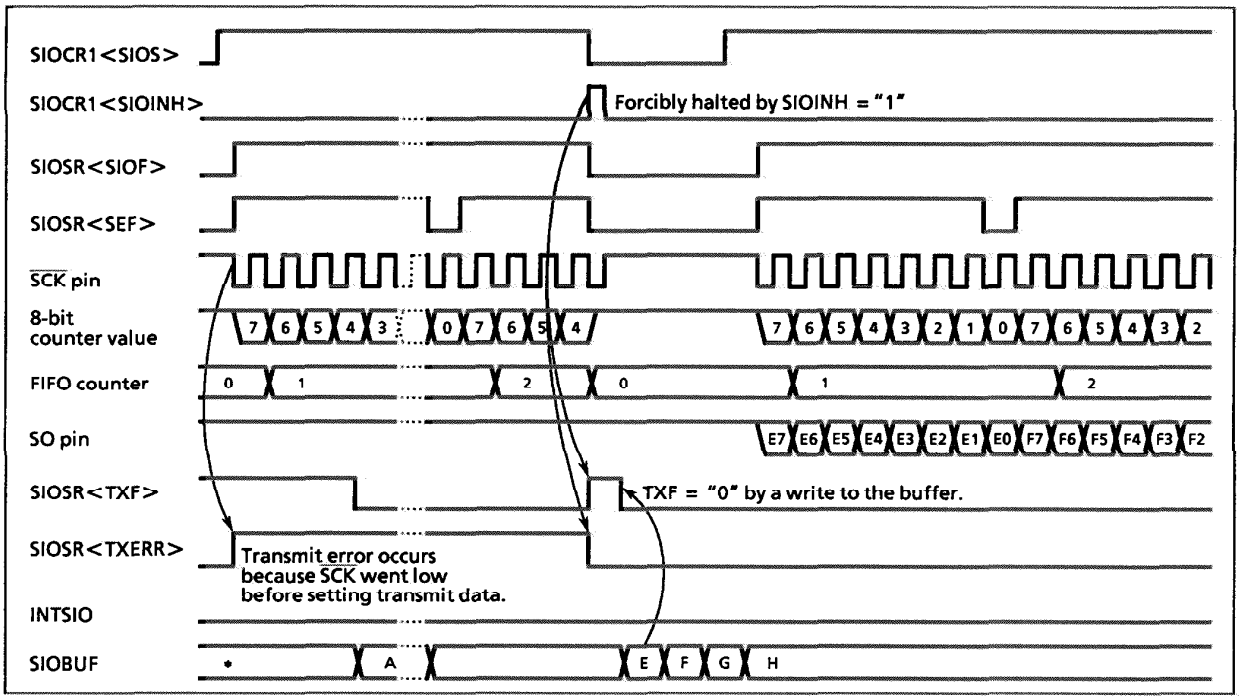


Figure 2-49. When Transmit errors occurs as soon as started operation (SIOCR2 = 03H (set to 4 bytes), using external clock)

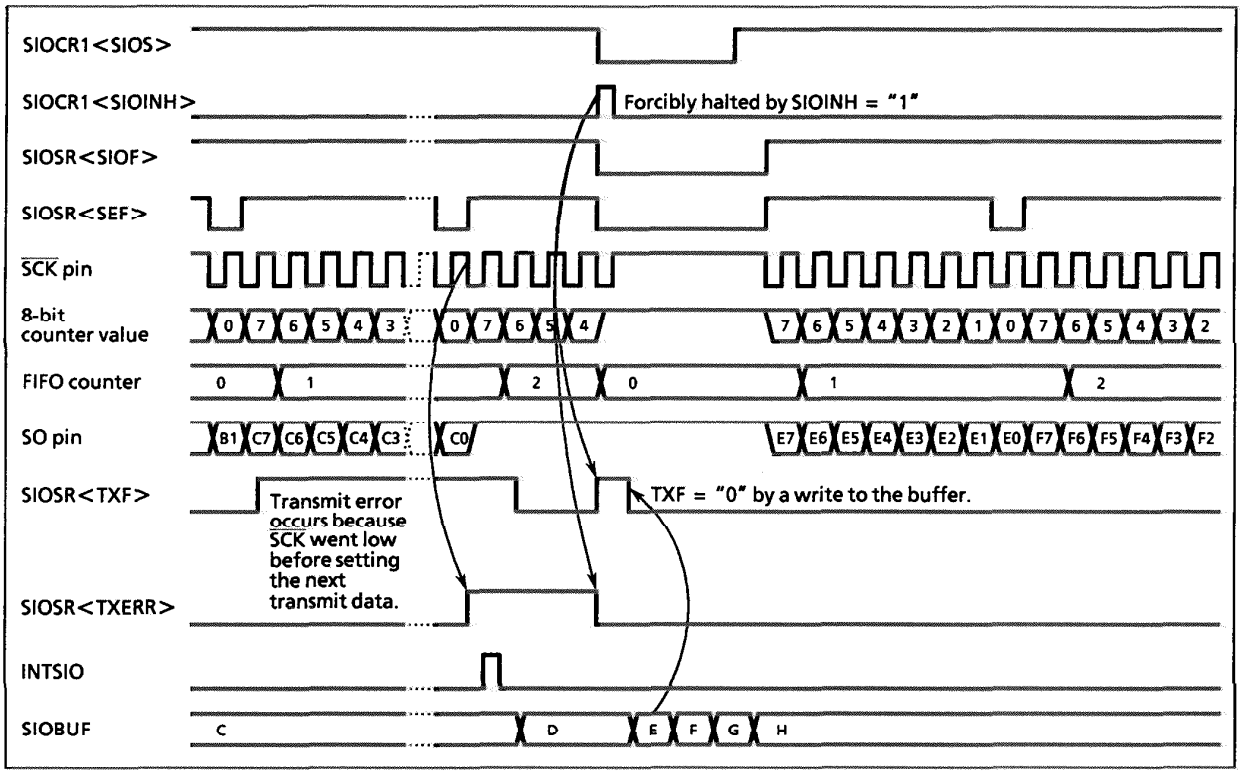


Figure 2-50. When Transmit errors occurs as soon as sending data (SIOCR2 = 03H, using external clock)

b. Receive mode

Receive mode is assumed by setting SIOM (SIOCR Register bits 5, 4) to "01".

Starting SIO operation

① Select receive mode (SIOCR1 Register bits 5, 4), serial clock rate (SIOCR1 Register bits 2 to 0), and the direction of transfer (SIOCR1 Register bit 3) using the SIOCR1 Register.

② Set the number of bytes to transfer in the SIORXD (SIOCR2 Register bit 3).

③ Set SIOS (SIOCR1 Register bit 7) to "1".

- When the selected serial clock is an internal clock, the SIO immediately starts receiving data sequentially from the MSB or LSB as selected with SIODIR (SIOCR1 Register bit 3).
- When the selected serial clock is an external clock, the SIO starts receiving data upon external clock input, sequentially from the MSB or LSB as selected with SIO1CR1<SIODIR>.

Halting SIO operation

④ When SIOCR1<SIOS> is cleared, SIO stops. When SIOCR1<SIOS> clear, make sure the Transmit Buffer is empty (SIOCR<TXF> = "1") before clearing SIOCR1<SIOS>, or do this clearing in an INTSIO interrupt routine. Note, however, when transring the next data, always check to see that transfer has been completed (SIOSR<SIOF> = "0") before writing the next data to the Buffer.

- In cases when SIOINH (SIOCR1 Register bit 6) is set to "1", reception stops immediately, even in the middle of reception.

Timing at which to read out the received data

Check to see that the Receive Buffer is full (SIOSR<RXF> = "1") before reading out the received data, or do this readout in an INTSIO interrupt routine. Note that SIOSR<RXF> is cleared to "0" when all bytes of received data as set with the SIOCR2 Register have been read out. The received data can also be read out after SIO has stopped (after SIOCR1<SIOS> cleared).

Note 1: The received data in the Buffer must always be read out as many bytes as set with the SIOCR2 Register. If more or less bytes of data than set with the SIOCR2 Register are read out from the Buffer, the SIO may not operate correctly.

Note 2: If the received data is read out before the end of reception (SIOSR<RXF> = "0"), the SIO may not operate correctly.

Note 3: The timing at which an INTSIO interrupt is generated during receive mode is when the SIO has received the last bit of the last byte of data.

Causes of receive errors

When operating with an external clock, if the SIO finished receiving the next receive data (one byte) while the Receive Buffer is full, a receive error is assumed and SIOSR<RXERR> is set to "1". When a receive error occurs, the data received after occurrence of the error is rejected, in order to protect the data already in the Receive Buffer.
When a receive error is detected, that must set SIOCR1<SIOINH> to "1" in order to forcibly terminate SIO operation. When SIOCR1<SIOINH> is set to "1", SIOCR1<SIOS> and all of the SIOSR Register bits are initialized. (Other registers and bits are not initialized.)

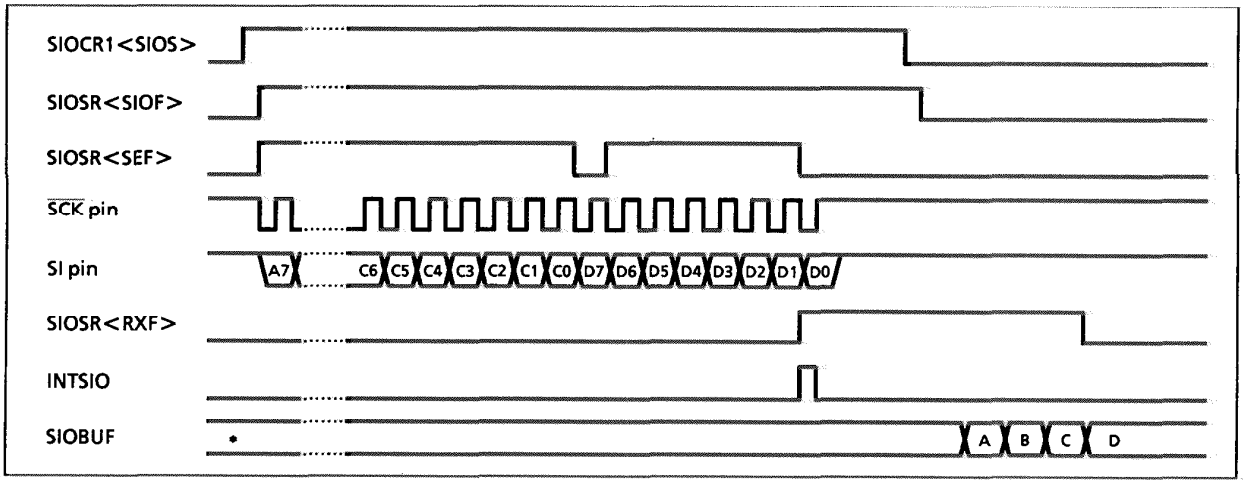


Figure 2-51. Timing at Which to Clear SIOCR1<SIOS>

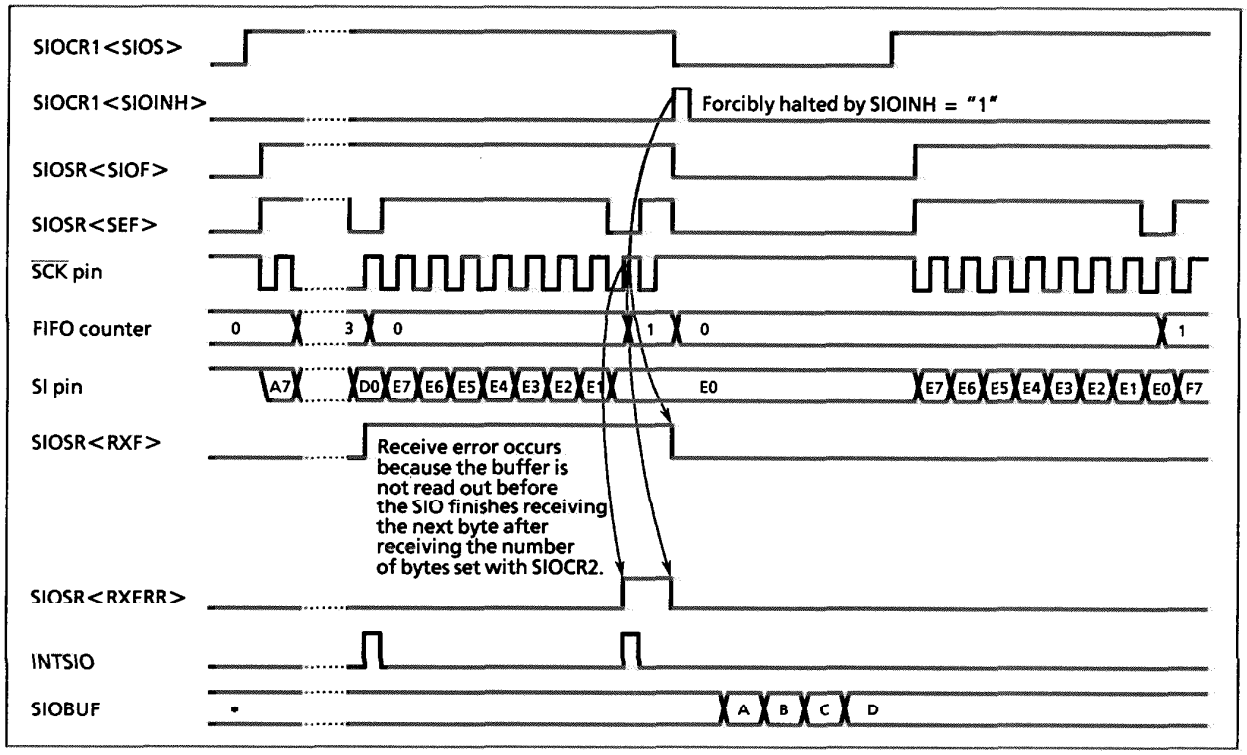


Figure 2-52. Not read our before the SIO finishes receiving the next byte (SIOCR2 = 03H (set to 4 bytes), using external clock)

c. Transmit/receive mode

Transmit/receive mode is assumed by setting SIOM (SIOCR1 Register bits 5, 4) to"10".

Starting SIO operation

① Select transmit/receive mode (SIOCR1 Register bits 5, 4), serial clock rate (SIOCR1 Register bits 2 to 0), and the direction of transfer (SIOCR1 Register bits 3) using the SIOCR1 Register.

② Set the number of bytes to transfer in the SIORXD (SIOCR2 Register bits 4 to 0).

③ Set the number of bytes of transmit data that has been set with the SIORXD (SIOCR2 Register bits 4 to 0) in the Buffer.

④ Set SIOS (SIOCR1 Register bit 7) to "1".

- When the selected serial clock is an internal clock, the SIO immediately starts transmitting/ receiving data sequentially from the MSB or LSB as selected with SIOCR1<SIODIR>.
- When the selected serial clock is an external clock, the SIO starts transmitting/receiving data upon clock input on $\overline{SCK}$ pin, sequentially from the MSB or LSB as selected with SIO1CR1 <SIODIR>.

Note: The SIOCR2 Register and the SIOCR1<SIODIR> and SIOCR1<SCK> are used for both transmission and reception in common, and cannot be set individually.

Halting SIO operation

⑤ When SIOCR1<SIOS> is cleared (SIOCR1 Register bit 7 <SIOS = "0">), SIO stops. If SIOCR1<SIOS> is cleared, make sure the Receive Buffer is full (SIOSR<RXF> = "1"), before clearing SIOCR1<SIOS>, or do this clearing in an INTSIO interrupt routine.

- In cases when SIOINH (SIOCR1 Register bit 6) is set to "1", transmission reception stops immediately, even in the middle of reception.

Timing at which to read out the received data and write transmit data

Check to see that the Receive Buffer is full (SIOSR<RXF> = "1") before reading out the received data and writing the next transmit data to the Buffer after sending/receiving the number of bytes set with the SIOCR2 Register, or do this read/write in an INTSIO interrupt routine.

Note 1: The timing at which an INTSIO interrupt is generated is when the SIO has received the last bit of the last byte of data.

Note 2: For write to and read from the Buffer, follow the sequence described below.

Before starting SIO operation: Write the number of bytes of transmit data set with the SIOCR2 Register and then set SIOCR1<SIOS>.

After SIO has stopped: Read the received data from the Buffer.

Note 3: Data must always be read out and written to the Buffer as many bytes as set with the SIOCR2 Register. If more or less bytes of data than set with the SIOCR2 Register are read out or written to the Buffer, the SIO may not operate correctly.

Note 4: RXF is cleared to "0" when all bytes of received data as set with the SIOCR2 Register have been read out. The received data can also be read out after SIO has stopped (after SIOCR1<SIOS> cleared).

Note 5: If operation in transmit/receive mode is forcibly terminated by setting SIOCR1<SIOINH> to "1", the received data is discarded.

Note 6: If necessary to set transmit data back again, first set SIOCR1<SIOINH> to "1" and then write as many bytes of transmit data as set with the SIOCR2 Register to the Buffer again.

Transmit/receive errors

When operating with an external clock, a transmission or reception error is assumed and the error flag (SIOSR<TXERR> or SIOSR<RXERR>) is set in one of the cases described below. When an error occurs, the transmit data is nullified, with all bits output at the high level.

- If after sending/receiving the number of bytes set with the SIOCR2 Register, the $\overline{\text{SCK}}$ pin goes low before the next transmit data is written to the Buffer after reading out the received data
- If while the Receive Buffer is full, the SIO finished receiving the next receive data (one byte)

When a transmission or receive error is detected, be sure to forcibly terminate the SIO by setting SIOCR1<SIOINH> to "1", even when the SIO remains idle.

Note 1: When a receive error occurs, the data received after occurrence of the error is rejected, in order to protect the data already in the Receive Buffer.

Note 2: When INTSIO interrupt in not generated, transmit error occurred with transmit/receive mode selected.

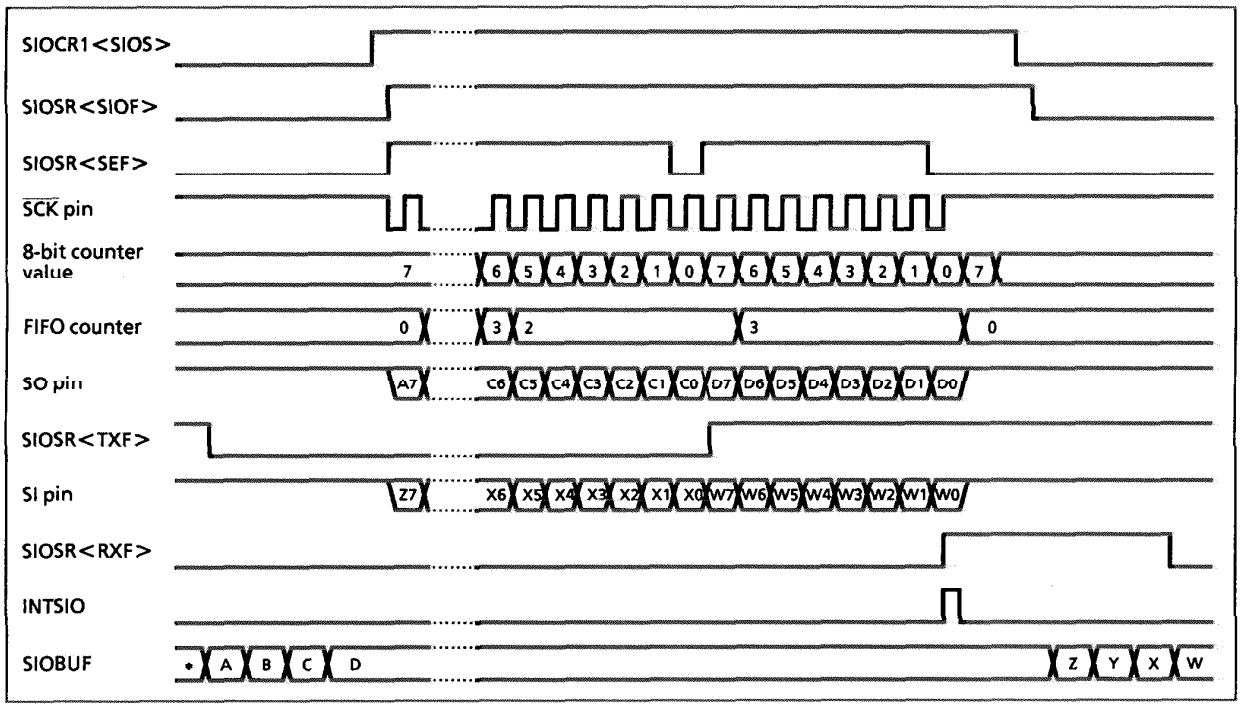


Figure 2-53. Timing at Which to Clear SIOS (transmit/receive mode using internal clock)

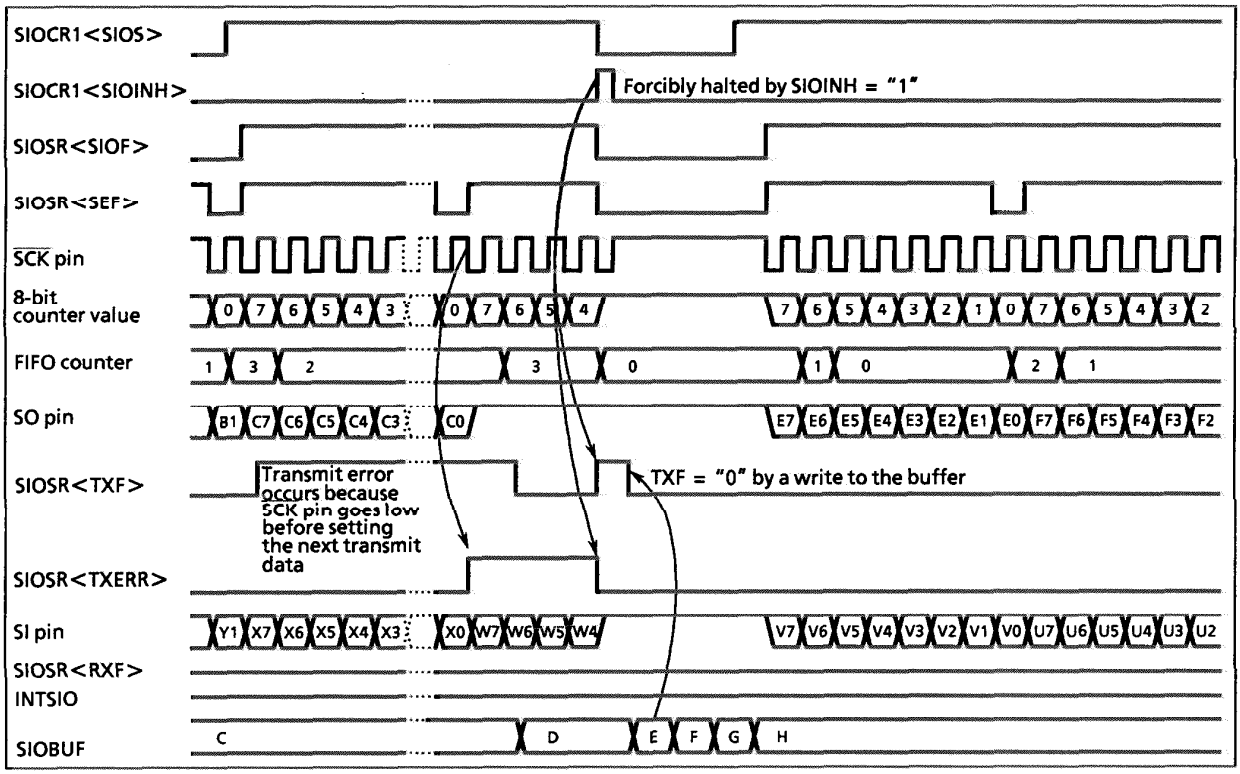


Figure 2-54. Transmit Error during Transmit/Receive Mode (SIOCR2 = 03H, using external clock)

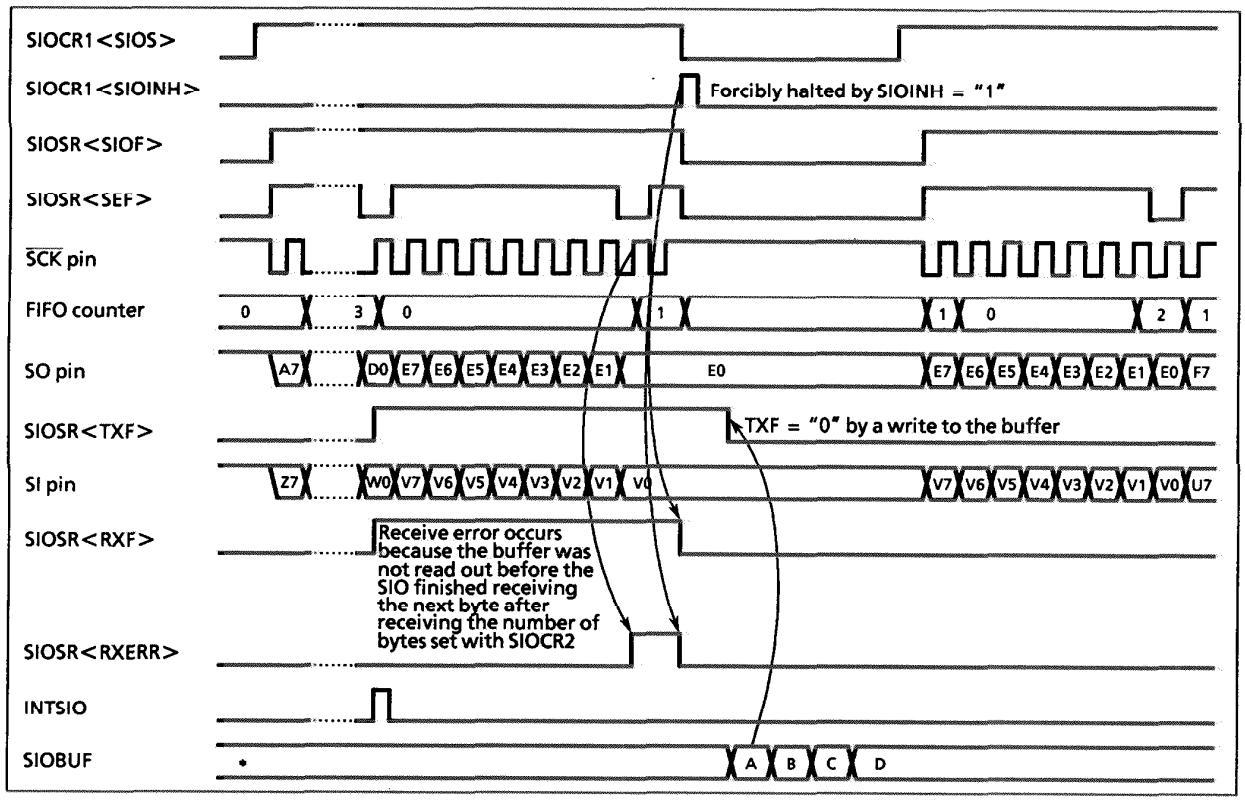


Figure 2-55. Receive Error during Transmit/Receive Mode (SIOCR2 = 03H, using external clock)

2.11 8-Bit AD Converter (ADC)

The TMP86CK74A/CM74A have an 8-bit successive approximation type AD converter.

2.11.1 Configuration

The circuit configuration of the 8-bit AD converter is shown in Figure 2-56.
It consists of control registers ADCCR1 and ADCCR2, converted value registers ADCDR1 and ADCDR2, a DA converter, a sample-and-hold circuit, a comparator, and a successive comparison circuit.

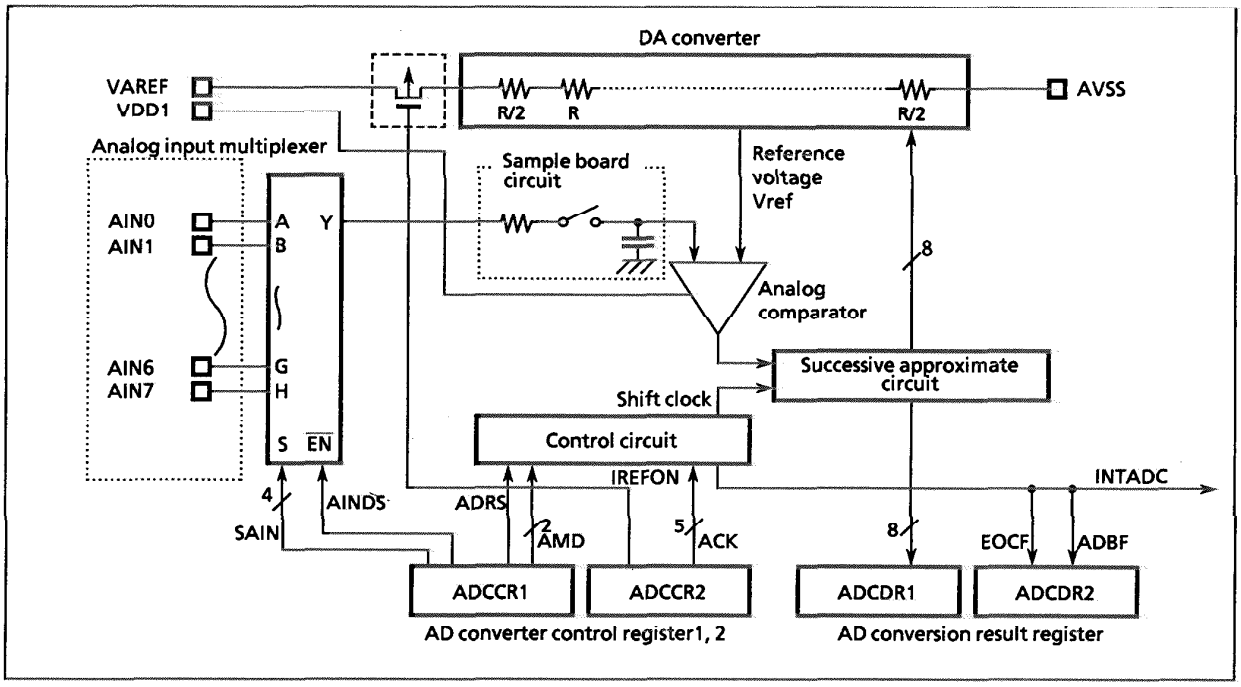


Figure 2-56. 8-Bit AD Converter (ADC)

2.11.2 Register Configuration

The AD converter consists of the following four registers:

- AD converter control register 1 (ADCCR1)
- AD converter control register 2 (ADCCR2)
- AD converted value register 1/2 (ADCDR1/ADCDR2)

(1) AD converter control register 1 (ADCCR1)
This register selects the analog channels and operation mode in which to perform AD conversion and controls the AD converter as it starts operating.

(2) AD converter control register 2 (ADCCR2)
This register selects the AD conversion time and controls the connection of the DA converter (ladder resistor network).

(3) AD converted value register1 (ADCDR1)
This register is used to store the digital value after being converted by the AD converter.

(4) AD converted value register2 (ADCDR2)
This register monitors the operating status of the AD converter.

The AD converter control register configurations are shown in Figures 2-57 and 2-58.

AD Converter Control Register 1

ADCCR1 ($000E_H$)

7	6	5	4	3	2	1	0
ADRS	AMD		AINDS	SAIN			

(Initial value: 0001 0000)

ADRS	AD conversion start	0: – 1: AD conversion restart	R/W
AMD	AD operating mode select	00: Disable 01: Software start mode 10: reserved 11: reserved	
AINDS	Analog input control	0: Analog input enable 1: Analog input disable	
SAIN	AD input channel select	0000: Selects AIN0 0100 : Selects AIN4 0001: Selects AIN1 0101 : Selects AIN5 0010: Selects AIN2 0110 : Selects AIN6 0011: Selects AIN3 0111 : Selects AIN7	

Note 1: Select analog input when AD converter stops.
Note 2: When the analog input is all use disabling, the AINDS should be set to "1".
Note 3: During conversion, do not perform output instruction to maintain a precision for all of the pins. And port near to analog input, do not input intense signaling of change.
Note 4: The ADRS is automatically cleared to "0" after starting conversion.
Note 5: Do not set ADRS (ADCCR1 bit 7) newly again during AD conversion. Before setting ADRS newly again, check EOCF (ADCDR bit 5) to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).
Note 6: After STOP or SLOW mode are started, AD converter control register 1 (ADCCR1) is all initialized. Therefore, set the ADCCR1 newly again after exiting STOP mode.

AD Converter Control Register 2

ADCCR2 ($000F_H$)

7	6	5	4	3	2	1	0
		IREFON	"1"	ACK			"0"

(Initial value: **0- 0000)

IREFON	Ladder resistor ON/OFF	Inputting current to the ladder resistor 0: ON only during AD conversion 1: Always ladder resistor ON					R/W
ACK	AD conversion time	ACK	Conversion time	fc = 16 MHz	fc = 8 MHz	fc = 4 MHz	
		000	reserved				
		001	reserved				
		010	78/fc [s]	–	–	19.5	
		011	156/fc [s]	–	19.5	39.0	
		100	312/fc [s]	19.5	39.0	78.0	
		101	624/fc [s]	39.0	78.0	156.0	
		110	1248/fc [s]	78.0	156.0	–	
		111	reserved				

Note 1: Settings for "–" in the above table are inhibited. reserved; Do not set by the program.
Note 2: Set conversion time by analog reference voltage (V_{AREF}) as follows.
V_{AREF} = 4.5 to 5.5 V (15.6 μ or more)
V_{AREF} = 2.7 to 5.5 V (31.2 μ or more)
Note 3: Always set bit 0 in ADCCR2 to "0" and set bit 4 in ADCCR2 to "1".
Note 4: When a read instruction for ADCCR2, bit 6 to 7 in ADCCR2 read in as undefined data.
Note 5: fc ; High-frequency clock [Hz]
Note 6: After STOP or SLOW mode are started, AD converter control register 2 (ADCCR2) is all initialized. Therefore, set the ADCCR2 newly again after exiting STOP mode.
Note 7: If a read instruction is executed for ADCCR2, read data of bits 7 and 6 are unstable.

Figure 2-57. AD Converter Control Register

AD Conversion Result Register

ADCDR1 (0027_H) Read only

7	6	5	4	3	2	1	0
AD07	AD06	AD05	AD04	AD03	AD02	AD01	AD00

(Initial value: 0000 0000)

ADCDR2 (0026_H)

7	6	5	4	3	2	1	0
		EOCF	ADBF				

(Initial value: **00 ****)

EOCF	AD conversion end flag	0: Under conversion or Before conversion 1: End of conversion	Read only
ADBF	AD conversion busy flag	0: During stop of AD conversion 1: During AD conversion	

Note 1: The ADCDR2<EOCF> is cleared to "0" when reading the ADCDR1. Therefore, the AD conversion result (ADCDR1) should be read after checking ADCDR2<EOCF> = "1".

Note 2: ADCDR2<ADBF> is set to "1" when AD conversion starts and cleared to "0" when the AD conversion is finished. It also is cleared upon entering standby mode (STOP or SLOW).

Note 3: If a read instruction is executed for ADCDR2, read data of bits 7, 6 and 3 to 0 are unstable.

Figure 2-58. AD Converter Result Register

2.11.3 AD Converter Operation

(1) Set up the AD converter control register 1 (ADCCR1) as follows:

- Choose the channel to AD convert using AD input channel select (SAIN).
- Specify analog input enable for analog input control (AINDS).
- Specify AMD for the AD converter control operation mode (software mode only).

(2) Set up the AD converter control register 2 (ADCCR2) as follows:

- Set the AD conversion time using AD conversion time (ACK). For details on how to set the conversion time, refer to Note 2 for AD converter control register 2.
- Choose IREFON for DA converter control.

(3) After setting up (1) and (2) above, when AD conversion start (ADRS) of AD converter control register 1 (ADCCR1) is set to "1", AD conversion starts immediately.

(4) After an elapse of the specified AD conversion time, the AD converted value is stored in AD converted value register 1 (ADCDR1) and the AD conversion finished flag (EOCF) of AD converted value register 2 (ADCDR2) is set to "1", upon which time AD conversion interrupt INTADC is generated.

(5) EOCF is cleared to "0" by a read of the conversion result. However, if reconverted before a register read, although EOCF is cleared the previous conversion result is retained until the next conversion is completed.

2.11.4 AD Converter Operation Modes

(1) Software start mode

After setting AMD (ADCCR1 bits 5, 6) to "01" (software start mode), set ADRS (ADCCR1 bit 7) to "1". AD conversion of the voltage at the analog input pin specified by SAIN (ADCCR1 bits 0 to 3) is thereby started.
After completion of the AD conversion, the conversion result is stored in AD converted value registers (ADCDR1) and at the same time EOCF (ADCDR2 bit 5) is set to 1, the AD conversion finished interrupt (INTADC) is generated.
ADRS is automatically cleared after AD conversion has started. Do not set ADRS (ADCCR1 bit 7) newly again (restart) during AD conversion. Before setting ADRS newly again, check EOCF (ADCDR2 bit 5) to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).

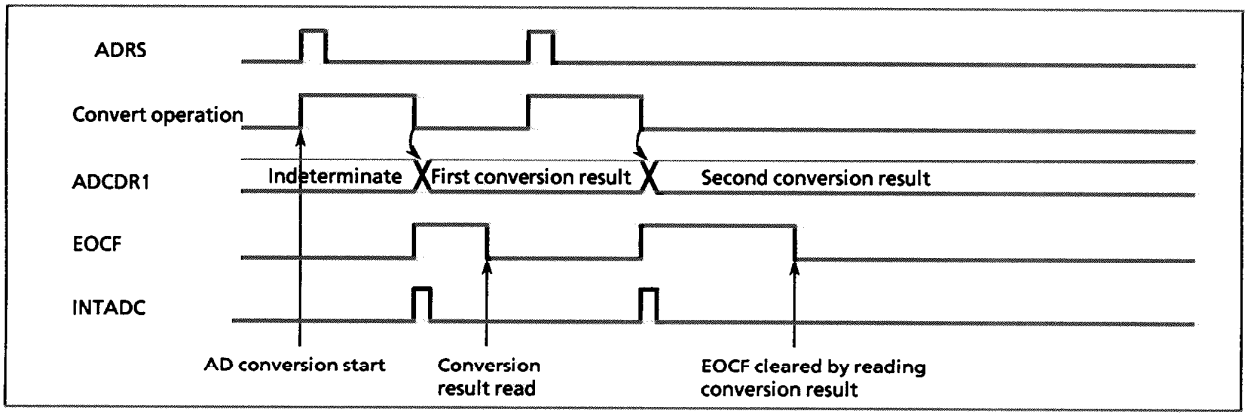


Figure 2-59. Operation in Software Start Mode

2.11.5 STOP and SLOW Modes during AD Conversion

When standby mode (STOP or SLOW mode) is entered forcibly during AD conversion, the AD convert operation is suspended and the AD converter is initialized. (ADCCR1 and ADCCR2 are initialized to initial value.) Also, the conversion result is indeterminate. (Conversion results up to the previous operation are cleared, so be sure to read the conversion results before entering standby mode.) When restored from standby mode, AD conversion is not automatically restarted, so it is necessary to restart AD conversion after setting ADCCR1 and ADCCR2. Note that since the analog reference voltage is automatically disconnected, there is no possibility of current flowing into the analog reference voltage.

2.11.6 Analog Input Voltage and AD Conversion Result

Example: After selecting the conversion time of 19.5 μs at 16 MHz and the analog input channel AIN4 pin, perform AD conversion once. After checking EOCF, read the converted value and store the 8-bit data in address $009F_H$ on RAM. The operation mode is software start mode.

```
; AIN SELECT
LD      (P4CR1), 00000000B    ; P4CR1 bit 4 = 0
LD      (P4CR2), 00000000B    ; P4CR2 bit 4 = 0
LD      (ADCCR1), 00000100B   ; Select AIN4
LD      (ADCCR2), 11011000B   ; Select conversion time (312/fc) and operation mode
; AD CONVERT START
SET     (ADCCR1). 7           ; ADRS = 1
SLOOP:  TEST    (ADCDR2). 5   ; EOCF = 1 ?
JRS     T, SLOOP
; RESULT DATA READ
LD      A, (ADCDR1)
LD      (9FH), A
```

The analog input voltage is corresponded to the 8-bit digital value converted by the AD as shown in Figure 2-60.

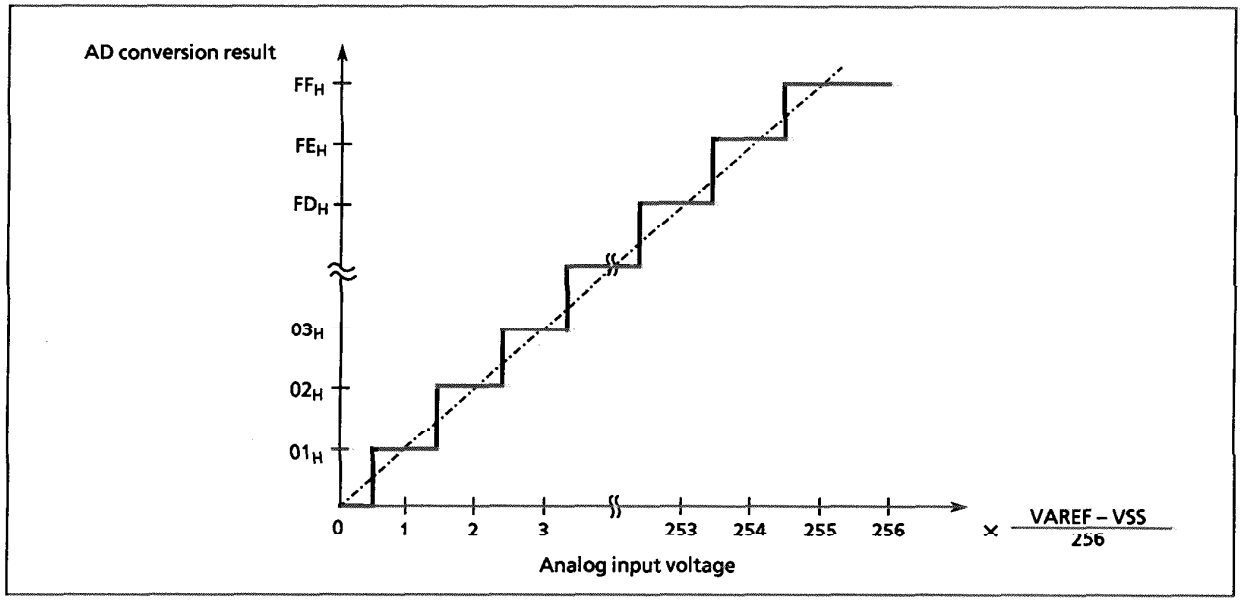


Figure 2-60. Analog Input Voltage and AD Conversion Result (typ.)

2.11.7 Precautions about AD Converter

(1) Analog input pin voltage range

Make sure the analog input pins (AIN0 to AIN7) are used at voltages within VSS below VAREF. If any voltage outside this range is applied to one of the analog input pins, the converted value on that pin becomes uncertain. The other analog input pins also are affected by that.

(2) Analog input shared pins

The analog input pins (AIN0 to AIN7) are shared with input/output ports. When using any of the analog inputs to execute AD conversion, do not execute input/output instructions for all other ports. This is necessary to prevent the accuracy of AD conversion from degrading. Not only these analog input shared pins, some other pins may also be affected by noise arising from input/output to and from adjacent pins.

(3) Noise countermeasure

The internal equivalent circuit of the analog input pins is shown in Figure 2-61. The higher the output impedance of the analog input source, more easily they are susceptible to noise. Therefore, make sure the output impedance of the signal source in your design is 5 kΩ or less. Toshiba also recommends attaching a capacitor external to the chip.

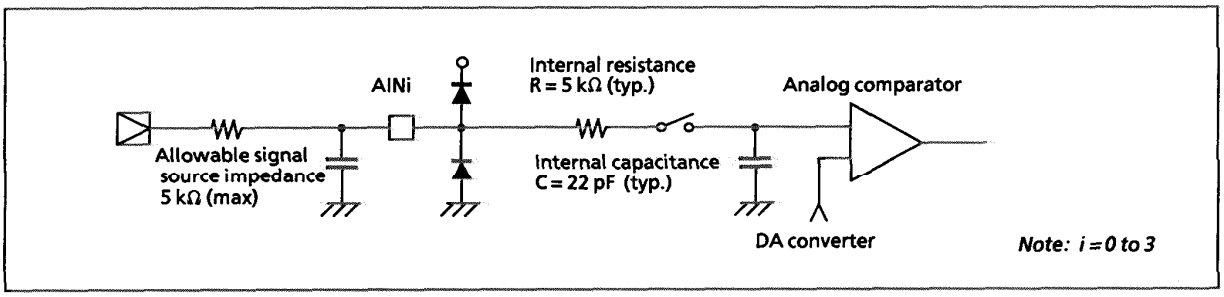


Figure 2-61. Analog Input Equivalent Circuit and Example of Input Pin Processing

2.12 Key-On Wake-Up (KWU)

In the TMP86CK74A/CM74A, the STOP mode must be released by not only P20 ($\overline{INT5}$ / $\overline{STOP}$) pin but also P44 to P47 pins.
When the STOP mode is released by P44 to P47 pins, the P20 ($\overline{INT5}$ / $\overline{STOP}$) pin needs to be used.

2.12.1 Configuration

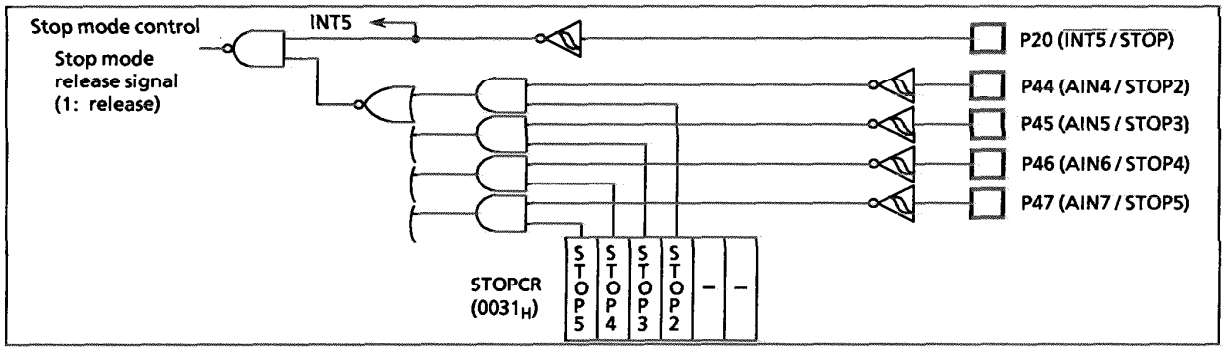


Figure 2-62. Stop Mode Control Circuit

Note: $\overline{STOP}$ pin doesn't have the control register such as STOPCR, so when STOP mode is relesed by STOPx (x ; 2 to 5), $\overline{STOP}$ pin should be fixed to low.

2.12.2 Control

P44 to P47 (STOP2 to STOP5) pin can controlled by Key-On Wake-Up control register (STOPCR). It can be configured as enable /disable in one-bit unit. When those pins are used by STOP mode release, those pins must be set input mode (P4CR, P4DR, ADCCR1).
STOP mode can be entered by setting up the System Control Register (SYSCR1), and can be exited by detecting the falling edge on STOP2 to 5 pins, which are enabled, for exiting STOP mode (Note 1). We can authentication STOP2 to 5 pins status by reading a P4 port. Be sure to check the level that all ports are high, when the STOP mode starts (Note 2).

Note 1: When the STOP mode release by edge mode (SYSCR1<RELM> = "0", prohibit input from STOP2 to STOP5 or must be set "1" level into STOP2 to STOP5 pins.

Note 2: When the $\overline{STOP}$ pin input is high or STOP2 to STOP5 pin input which is enabled by STOPCR is low, executing an instruction which starts STOP mode will not place in STOP mode but instead will immediately start the release sequence (warm-up).

Key-On Wake-Up control register

STOPCR (0031H)

7	6	5	4	3	2	1	0
STOP5	STOP4	STOP3	STOP2	–	–	–	–

(Initial value: 0000 ****)

STOP2	Stop mode released by P44 port	0: Disable 1: Enable	write-only
STOP3	Stop mode released by P45 port	0: Disable 1: Enable	
STOP4	Stop mode released by P46 port	0: Disable 1: Enable	
STOP5	Stop mode released by P47 port	0: Disable 1: Enable	

Figure 2-63. Key-On Wake-Up Control Register

2.13 Vacuum Fluorescent Tube (VFT) Driver Circuit

The 86CK74A/CM74A features built-in high-breakdown voltage output buffers for directly driving fluorescent tubes, and a display control circuit used to automatically transfer display data to the output port.

The segment and the digit, as it is the VFT drive circuit which included in the usual products, are not allocated. The segment and the digit can be freely allocated in the timing (T0 to T15) which is specified according to the display tube types and the layout.

2.13.1 Functions

(1) 37 high-breakdown voltage output buffers built-in.
- Large current output pin 16 (V0 to V15)
- Middle current output pin 21 (V16 to V36)

There is also the VKK pin used for the VFT drive power supply.

(2) The dynamic lighting system makes it possible to select 1 to 16 digits (T0 to T15) by program.

(3) Pins not used for VFT driver can be used as general-purpose ports (PD).
- Pins can be selected using the VSEL (bits 4 to 0) in VFT control register1 bit by bit.

(4) Display data (80 bytes in DBR) are automatically transferred to the VFT output pin.

(5) Brightness level can be adjusted in 7 steps using the dimmer function.

(6) Four types (fc/2^{12} to fc/2^{9}) of display time can be selected.

Table 2-14. tdisp Time

SDT1	SDT2	tdisp Time	At 16 MHz	At 8 MHz	At 4 MHz	At 2 MHz	At 1 MHz
00	0	2^{9}/fc [s]	32 μs	64 μs	128 μs	256 μs	512 μs
01		2^{10}/fc [s]	64 μs	128 μs	256 μs	512 μs	1024 μs
10		2^{11}/fc [s]	128 μs	256 μs	512 μs	1024 μs	2048 μs
11		2^{12}/fc [s]	256 μs	512 μs	1024 μs	2048 μs	4096 μs
00	1	2^{9}/fc [s]	16 μs	32 μs	64 μs	128 μs	256 μs
01		2^{9}/fc [s]	32 μs	64 μs	128 μs	256 μs	512 μs
10		2^{10}/fc [s]	64 μs	128 μs	256 μs	512 μs	1024 μs
11		2^{11}/fc [s]	128 μs	256 μs	512 μs	1024 μs	2048 μs

2.13.2 Configuration

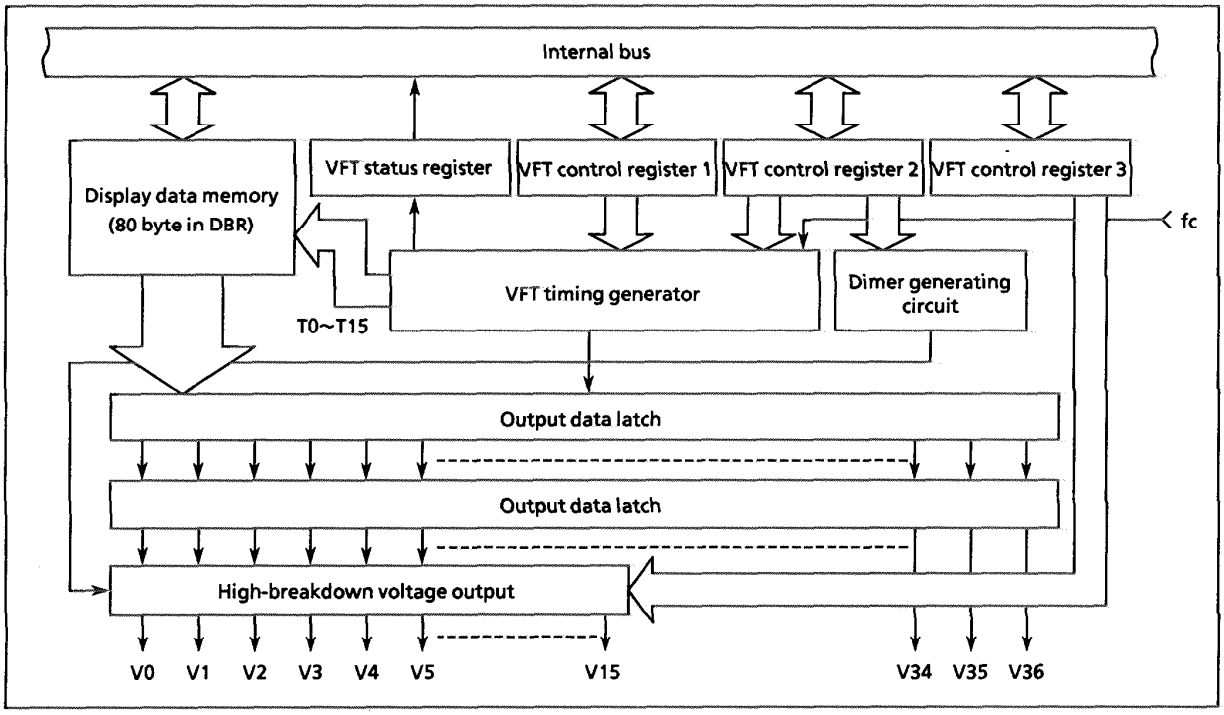


Figure 2-64. Vacuum Fluorescent Display (VFT) Circuit

2.13.3 Control

The VFT driver circuit is controlled by the VFT control registers (VFTCR1, VFTCR2, VFTCR3). Reading VFTSR determines the VFT operating status.

Switching the mode from NORMAL1/2 to SLOW or STOP puts the VFT driver circuit into blanking state (BLK is set to "1" and EXEY is cleared to "0" ; values set in the VFT control registers except BLK and EKEY are maintained), and sets segment outputs and digit outputs are cleared to "0". Thus, ports P6 to P9, and PD function as general-purpose output ports with pull-down.

VFT control register 1

VFTCR1 ($002A_H$)

7	6	5	4	3	2	1	0
BLK	SDT1			VSEL			

(initial value: 1000 0000)

BLK	VFT display control	0 : Display enable 1 : Disable		R/W
SDT1	Display time select1 (tdisp) (Display time of 1 digit)		STD2 = 0	STD1 = 0
		00	2^9/fc	2^8/fc
		01	2^{10}/fc	2^9/fc
		10	2^{11}/fc	2^{10}/fc
		11	2^{12}/fc	2^{11}/fc
VSEL	Automatic display select (When using VFT driver (automatic display), V31 to V0 are only used to output VFT.) Pins which are not selected by the output pins other than the above-mentioned pins can be used as general-purpose input/output pins. (When using as a general-purpose input/output pin, the display data which corresponds to the pin must be set to "0")	00000 : 32 (V31 to V0) 00001 : 33 (V32 to V0) 00010 : 34 (V33 to V0) 00011 : 35 (V34 to V0) 00100 : 36 (V35 to V0) 00101 : 37 (V36 to V0) Other : reserved		

Note 1 : fc ; high frequency clock
Note 2 : VFTCR1 is write-only register, which cannot use any of in read-modify-write instruction such as bit operate, etc.
Note 3 : Can not access.

VFTSR ($002D_H$)

7	6	5	4	3	2	1	0
WAIT							

WAIT	VFT operational status monitor	0 : VFT display in operation 1 : VFT display operation disabled	Read only

Note 1 : WAIT is initialized to 1 after resetting.
Note 2 : When a BLK in VFTCR is cleared to 0, WAIT flag is cleared to 0 at an end of display timing. And a VFT driving circuit is enabled at an end of next display timing.
Note 3 : During a VFT driving circuit is enabled, it is disabled just after an end of display timing (tdisp) by setting BLK in VFTCR to 1. And WAIT flag is set to 1 simultaneously.
Note 4 : When a VFT driving circuit is enabled again, it is necessary that BLK is set to 1 after confirming a WAIT is 1.

Figure 2-65. VFT Control Register 1

VFT control register 2

VFTCR2 ($002B_H$)

7	6	5	4	3	2	1	0
DIM			STA				

(initial value: 0010 0000)

DIM	Dimmer time select	000 : reserved 001 : (14/16) × tdisp (s) 010 : (12/16) × tdisp (s) 011 : (10/16) × tdisp (s) 100 : (8/16) × tdisp (s) 101 : (6/16) × tdisp (s) 110 : (4/16) × tdisp (s) 111 : (2/16) × tdisp (s)	R/W
STA	Number of state (display)	00000 : 1 display mode (T0) 00001 : 2 display mode (T1 to T0) 00010 : 3 display mode (T2 to T0) 00011 : 4 display mode (T3 to T0) 00100 : 5 display mode (T4 to T0) 00101 : 6 display mode (T5 to T0) 00110 : 7 display mode (T6 to T0) 00111 : 8 display mode (T7 to T0) 01000 : 9 display mode (T8 to T0) 01001 : 10 display mode (T9 to T0) 01010 : 11 display mode (T10 to T0) 01011 : 12 display mode (T11 to T0) 01100 : 13 display mode (T12 to T0) 01101 : 14 display mode (T13 to T0) 01110 : 15 display mode (T14 to T0) 01111 : 16 display mode (T15 to T0) Others : reserved	

Note 1 : VFTCR2 is write-only register, which cannot use any of in read-modify-write instruction such as bit operate, etc.

Note 2 : Even if a number of the display digit is set a pin which is equal to the digit dose not output. It is necessary to write data to the data buffer which corresponds to the digit according to the display timing (T0 to T15).

*Note 3 : * ; don't care*

Figure 2-66. VFT control Register 2, VFT status register

VFT control register 3

VFTCR3 ($002C_H$)

7	6	5	4	3	2	1	0
OWSEL					HVTR1	HVTR0	SDT2

(Initial value : 0000 0000)

SDT2	Display time select 2 (tdisp) (Display time of 1 digit)		SDT1 = "00"	SDT1 = "01"	SDT1 = "10"	SDT = "11"	R/W
		0	2^9/fc [s]	2^{10}/fc [s]	2^{11}/fc [s]	2^{12}/fc [s]	
		1	2^8/fc [s]	2^9/fc [s]	2^{10}/fc [s]	2^{11}/fc [s]	
HVTR0	P6~P9 Ports Tr time select	0	Tr normal mode typ 150ns (VDD = 3V, Vkk = − 35V)				
		1	Tr increment mode typ 3μs (VDD = 3V, Vkk = − 35V)				
HVTR1	PD Ports Tr time select	0	Note 1) Tr normal mode typ150ns (VDD = 3V, Vkk = − 35V)				
		1	Note 1) Tr increment mode typ 3μs (VDD = 3V, Vkk = − 35V)				
OWSEL	Output waveform select (Select grid or segment)		GRID output (Dimmer enable)	SEG output			
		00000	P60	P61~PD4			
		00001	P60~P61	P62~PD4			
		00010	P60~P62	P63~PD4			
		00011	P60~P63	P64~PD4			
		00100	P60~P64	P65~PD4			
		00101	P60~P65	P66~PD4			
		00110	P60~P66	P67~PD4			
		00111	P60~P67	P70~PD4			
		01000	P60~P70	P71~PD4			
		01001	P60~P71	P72~PD4			
		01010	P60~P72	P73~PD4			
		01011	P60~P73	P74~PD4			
		01100	P60~P74	P75~PD4			
		01101	P60~P75	P76~PD4			
		01110	P60~P76	P77~PD4			
		01111	P60~P77	P80~PD4			
		10000	reserved	reserved			
		↕	↕	↕			
		11111	reserved	reserved			

Note 1 : A rising time of Port D is measured when Port D is connected with pull-down resistor (the same value Rkk) to VKK pin.

Figure 2-67. VFT Control Register 3

Note : It is possible to reduce the VFT port noise by using Tr increment mode. When Tr increment mode is enabled, a time of Tr is increased and also Tf. Therefore, the display time and dimmer value should be decided with the stray capacitor on a PCB. Otherwise the switching timing between grid and segment is overlapped each other and a VFT display is dimmed. Please confirm a VFT display with your set.

(1) Setting of Display mode

VFT display mode is set by VFT control register 1 (VFTCR1), VFT control register 2 (VFTCR2) and VFT control register 3 (VFTCR3). VFT control register 1 (VFTCR1) sets 1 display time (tdisp) and the number of display lines (VSEL), VFT control register 2 (VFTCR2) sets dimmer timer (DIM) and state (STA) and VFT control register 3 (VFTCR3) sets Port Tr mode (HVTR0/1). (BLK of VFTCR1 must be set to "1".) The segments and the digits are not fixed, so that they can be freely allocated. However the number of states must be specified according to the number of digits of VFT which you use. Thought the layout of VFT display mode is freely allocated, the followings are recommended; usually, large current output (V0 to V15) is used for a digit, and middle current output (V16 to V36) is used for a segment.
(See Display operation in section 2.14.4 for display timing and data setting procedures.)

(2) Display data setting

Data are converted into VFT display data by instructions. The converted data stored in the display data buffer (addresses 0F80 to 0FCF in DBR) are automatically transferred to the VFT driver circuit, then transferred to the high-breakdown voltage output buffer. Thus, to change the display pattern, just change the data in the display data buffer.
Bits in the VFT segment (dot) and display data area correspond one to one. When data are set to 1, the segments corresponding to the bits light. The display data buffer is assigned to the DBR area shown in Figure 2-68. (The display data buffer can not be used as data memory)

Bit	0 to 7	0 to 7	0 to 7	0 to 7	0 to 4	Timing
	$0F80_H$	$0F90_H$	$0FA0_H$	$0FB0_H$	$0FC0_H$	T0
	$0F81_H$	$0F91_H$	$0FA1_H$	$0FB1_H$	$0FC1_H$	T1
	$0F82_H$	$0F92_H$	$0FA2_H$	$0FB2_H$	$0FC2_H$	T2
	$0F83_H$	$0F93_H$	$0FA3_H$	$0FB3_H$	$0FC3_H$	T3
	$0F84_H$	$0F94_H$	$0FA4_H$	$0FB4_H$	$0FC4_H$	T4
	$0F85_H$	$0F95_H$	$0FA5_H$	$0FB5_H$	$0FC5_H$	T5
	$0F86_H$	$0F96_H$	$0FA6_H$	$0FB6_H$	$0FC6_H$	T6
	$0F87_H$	$0F97_H$	$0FA7_H$	$0FB7_H$	$0FC7_H$	T7
	$0F88_H$	$0F98_H$	$0FA8_H$	$0FB8_H$	$0FC8_H$	T8
	$0F89_H$	$0F99_H$	$0FA9_H$	$0FB9_H$	$0FC9_H$	T9
	$0F8A_H$	$0F9A_H$	$0FAA_H$	$0FBA_H$	$0FCA_H$	T10
	$0F8B_H$	$0F9B_H$	$0FAB_H$	$0FBB_H$	$0FCB_H$	T11
	$0F8C_H$	$0F9C_H$	$0FAC_H$	$0FBC_H$	$0FCC_H$	T12
	$0F8D_H$	$0F9D_H$	$0FAD_H$	$0FBD_H$	$0FCD_H$	T13
	$0F8E_H$	$0F9E_H$	$0FAE_H$	$0FBE_H$	$0FCE_H$	T14
	$0F8F_H$	$0F9F_H$	$0FAF_H$	$0FBF_H$	$0FCF_H$	T15
Output pin	V0 to V7	V8 to V15	V16 to V23	V24 to V31	V32 to V36	

Figure 2-68. VFT Display Data Buffer Memory (DBR)

2.13.4 Display Operation

As the above-mentioned, the segment and the digit are not allocated. After setting of the display timing for the number of digits according to the using VFT and storing the segment and digit data according to the respective timings, clearing BLK in VFTCR1 to 0 starts VFT display.
Figure 2-69. shows the VFT drive pulse and Figure 2-70, 71 show the display operation.

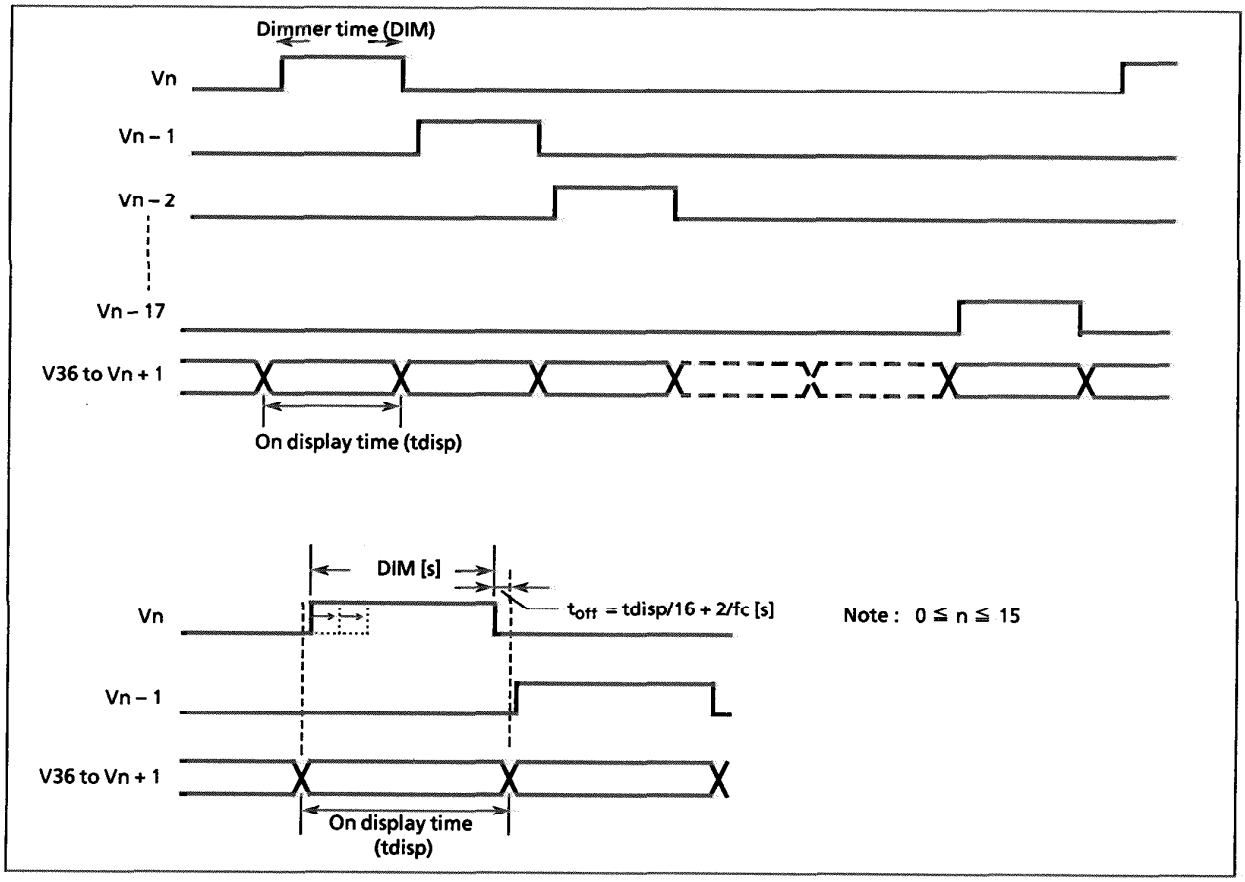


Figure 2-69. VFT Drive Wafeform and Display Timing

2.13.5 Example of Display operation

(1) For Conventional type VFT

When using the conventional type VFT, the output timing of the digits is specified to output 1 digit for 1 timing. Data must be set to output the pins which are specified to the digit in sequence. The following figure shows a data allocation of the display data buffer (DBR) and the output timing when VFT of 10 digits is used and V0 to V9 pins are allocated as the digit outputs. (When data is first written by the data buffer which corresponds to the digit pin, it is unnecessary to rewrite the data later.)

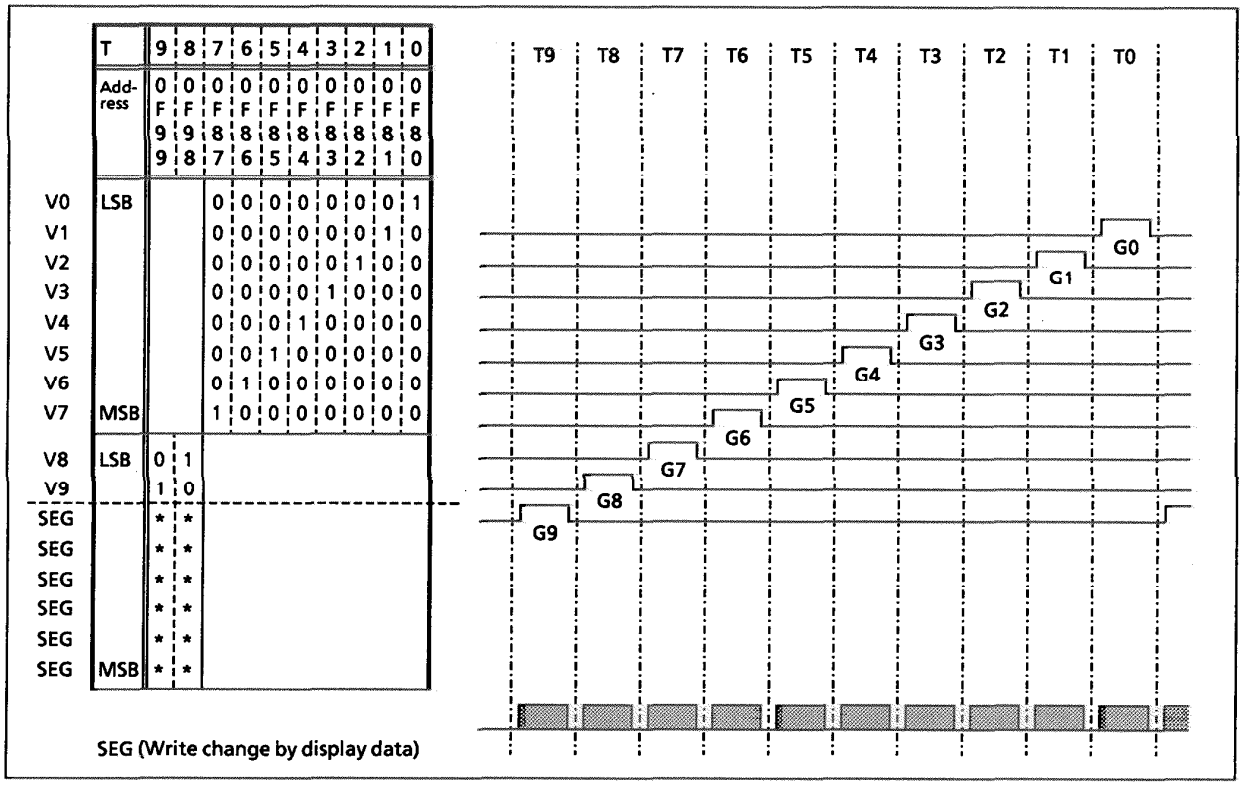


Figure 2-70. Example of Conventional type VFT driver pulse

(2) For Grid scan type VFT

When using the grid scan type VFT, two or more grids must be simultaneously selected to turn the display pattern which contains two or more grids on. Additionally, the timing and the data must be determined to set the grid scan mode as follows.

- When the display pattern which is fully set in the respective grids is turned on, only the grids which correspond as ever must be scanned in sequence to turn on the display pattern. (timing of T8 to T3 in the following figure)
- When the display pattern which contains two or more grids is turned on, two or more corresponding grids are simultaneously selected to turn on the display pattern. (timing of T2 to T0 in the following figure)

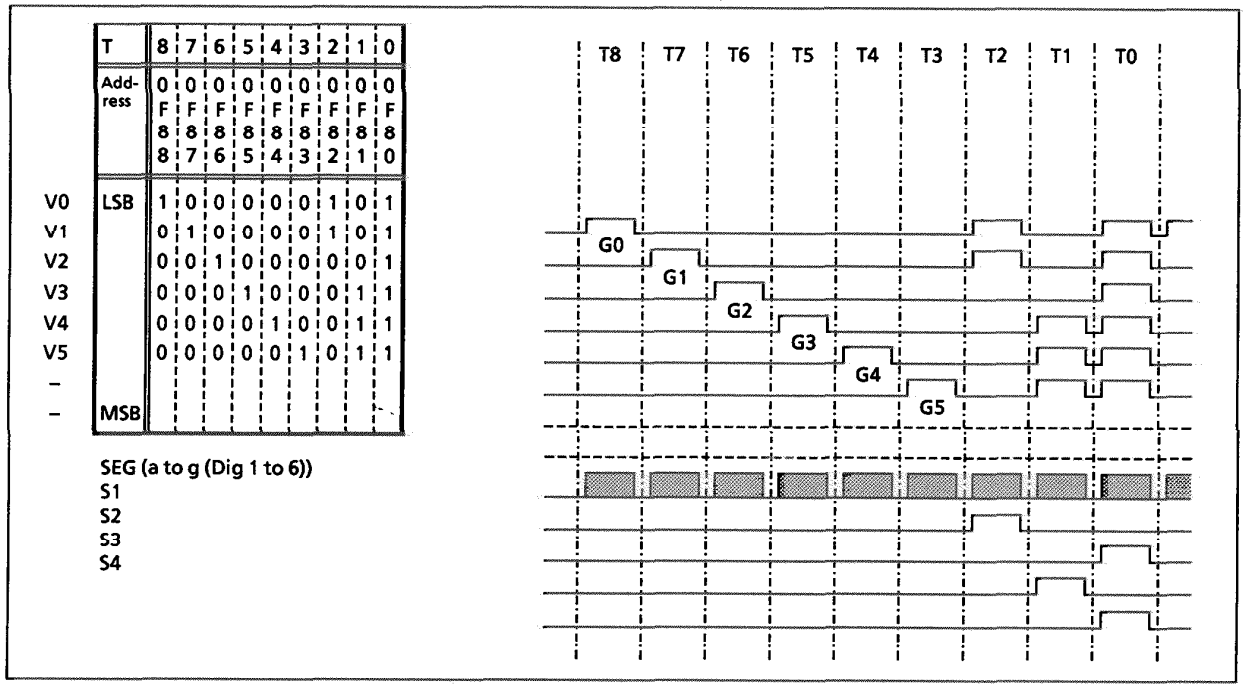


Figure 2-71. Grid Scan Type Display Vacuum Fluorescent Tube Ware

2.13.6 Port Function

(1) High-breakdown voltage buffer

To drive fluorescent display tube, clears the port output latch to "0". The port output latch is initialized to 0 at reset.
It is recommended that ports P6, P7, P8 and P9 should be used as VFT driver output. Precaution for using as general-purpose I/O pins are follows.

Note : When not using a pin which is pulled down to pin V_{KK} (RK = typ. 80 kΩ), it must be set to open. It is necessary to clear the port output latch and the data buffer memory (DBR) to "0".

① Ports P6 to P9
When a part of P6 to P9 is used as the input/output pin (VFT driver in operation), the data buffer memory (DBR) of the segment which is also used as the input/output pin must be cleared to "0".

② Port PD
VFT output and usual input/output are controlled by VSEL of VFT control register in bits. When a pin which is pulled down to pin V_{KK} is used as usual output or input, the following cautions are required.

(a) When outputting
When level "L" is output, a port which is pulled down to pin V_{KK} is pin V_{KK} voltage. Such processes as clamping with the diode as shown in figure 2-72. (a) are necessary to prevent pin V_{KK} voltage applying to the external circuit.

(b) When inputting
When the external data is input, the port output latch is cleared to "0".
The input threshold is the same as that of the other usual input/output port. However it is necessary to drive RK (typ. 80 kΩ) sufficiently because of pulled down to pin VKK.

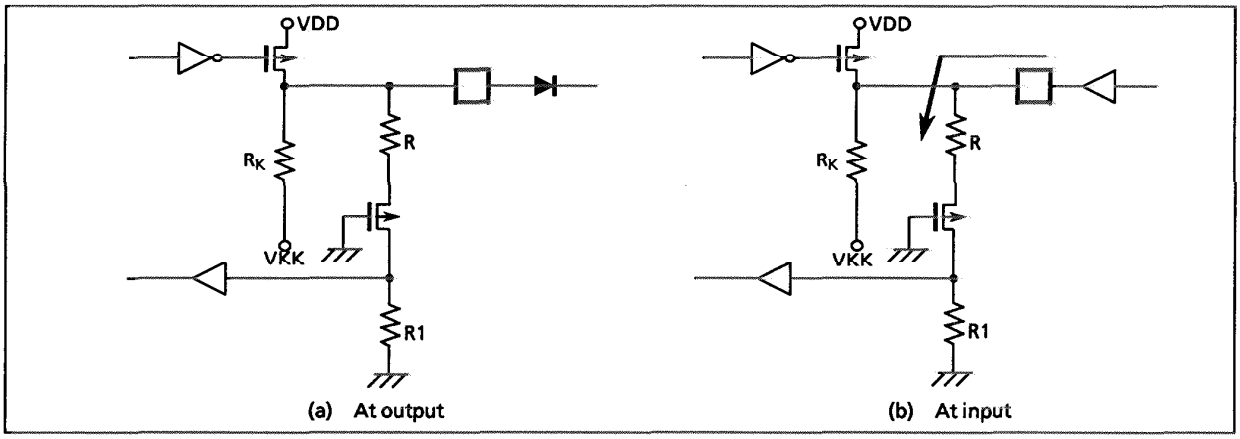
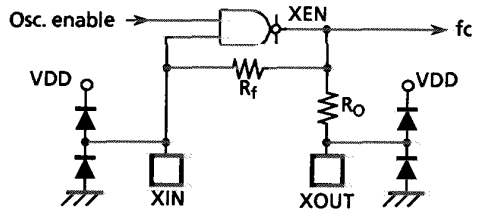
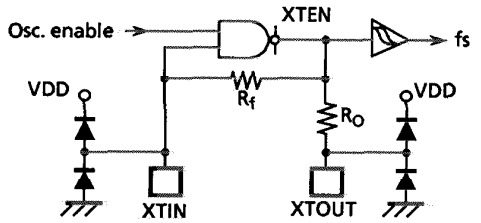
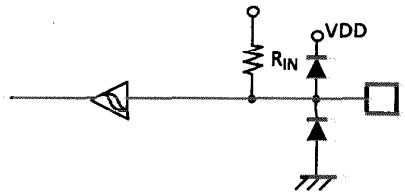
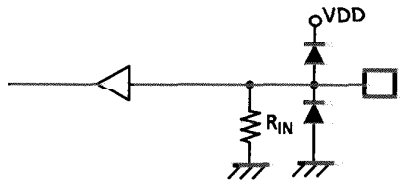


Figure 2-72. External Circuit Interface

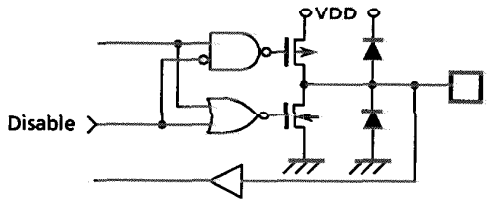
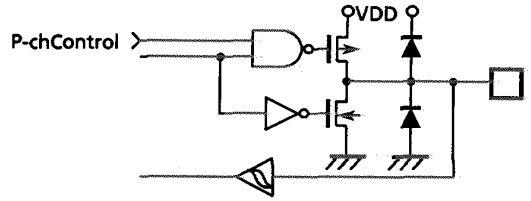
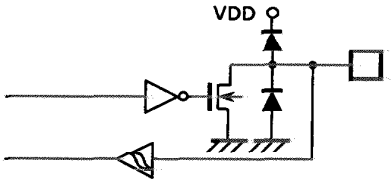
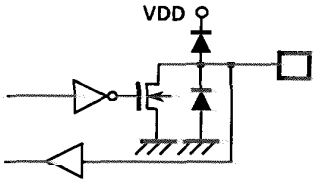
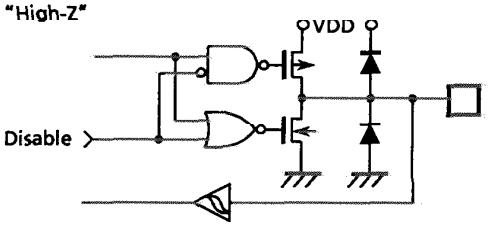
Input/Output Circuitry

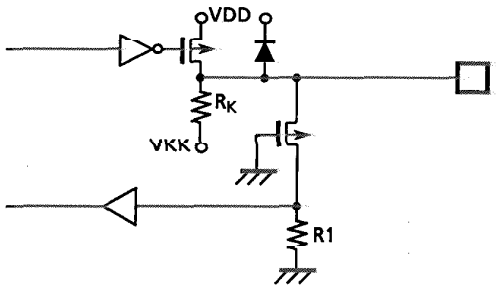
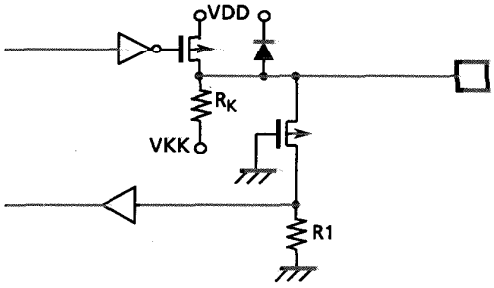
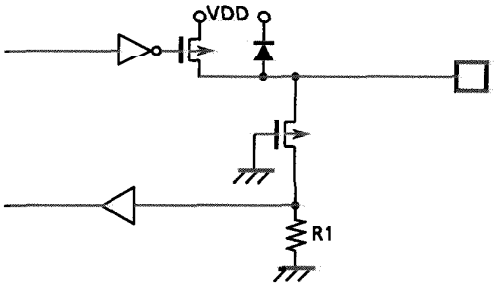
(1) Control Pins

The input/output circuitries of the TMP86CK74A/CM74A control pins are shown below.

Control Pin	I/O	Input/Output Circuitry	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency) R_f = 1.2 MΩ (typ.) R_O = 500 Ω (typ.)
XTIN XTOUT	Input Output		Resonator connecting pins (low-frequency) R_f = 6 MΩ (typ.) R_O = 220 kΩ (typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.)
TEST	Input		Pull-down resister R_{IN} = 70 kΩ (typ.)

(2) Input/Output port

Control Pin	I/O	Input/Output Circuitry	Remarks
P0 P4	I/O	Initial "High-Z" 	Tri state I/O
P1	I/O	Initial "High-Z" 	Programmable Open drain output Hysteresis input
P2	I/O	Initial "High-Z" 	Skin open drain output Hysteresis input
P3	I/O	Initial "High-Z" 	Skin open drain output Large current output
P5	I/O	Initial "High-Z" 	Tri state I/O Hysteresis input

Port	I/O	Input/Output Circuitry	Remarks
P6 P7	I/O	Initial "High-Z" 	Source open drain I/O High breakdown voltage (large current) R_K = 80 kΩ (typ.) R1 = 200 kΩ (typ.)
P8 P9	I/O	Initial "High-Z" 	Source open drain I/O High breakdown voltage (middle current) R_K = 80 kΩ (typ.) R1 = 200 kΩ (typ.)
PD	I/O	Initial "High-Z" 	Source open drain I/O High breakdown voltage (middle current) R1 = 200 kΩ (typ.)

Electrical Characteristics

Absolute Maximum Ratings (VSS = 0 V)

Parameter		Symbol	Pins	Ratings	Unit
Supply Voltage		V_{DD}		− 0.3 to 6.5	V
Program voltage		V_{PP}	TEST/VPP pin	− 0.3 to 13.0	
Input Voltage		V_{IN}		− 0.3 to V_{DD} + 0.3	
Output Voltage		V_{OUT1}		− 0.3 to V_{DD} + 0.3	
		V_{OUT2}	Source open drain port	V_{DD} − 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	IOL	I_{OUT1}	P0, P01, P2, P4, P5 ports	5	mA
		I_{OUT2}	P3 port	40	
	IOH	I_{OUT3}	P0, P1, P4, P5 ports	− 3	
		I_{OUT4}	P6, P7 ports	− 30	
		I_{OUT5}	P8, P9, PD ports	− 20	
Output Current (Total)	IOL	ΣI_{OUT1}	P0, P1, P2, P4, P5 ports	120	mA
	IOH	ΣI_{OUT4}	P6. P7. P8. P9. PD ports	− 120	
Power Dissipation [Topr = 25°C]		PD		1200	mW
Soldering Temperture (time)		Tsld		260 (10 s)	°C
Storage Temperature		Tstg		− 55 to 125	
Operating Temperature		Topr		− 30 to 70	

Note 1 : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum ratings is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products, which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2 : All VDDs should be connected externally for keeping the same voltage level.

Note 3 : Power Dissipation (PD) ; For PD, it is necessary to decrease − 14.3 mwl °C.

Recommended Operating Conditions

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fc = 8 MHz	NORMAL1, 2 modes	2.7		
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode			
Output Voltage	V_{OUT3}	Source open drain pins			V_{DD} – 38	V_{DD}	V
Input High Voltage	V_{IH1}	Except hysteresis input			$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
Input Low Voltage	V_{IL1}	Except hysteresis input			0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note : The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products, which include this device, ensure that the recommended operating conditions for the device are always adhered to.

How to calculate power consumption.

The share of VFT driver loss (VFT driver output loss + pull-down resistor (RK) loss) in power consumption Pmasx of
TMP86CK74/CM74 is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption Pd must not be exceeded.
Power consumption Pmax = operating power consumption + normal output port loss + VFT driver loss.

Where,

Operating power consumption: VDD × IDD
Normal output port loss : $\Sigma I_{OUT2} \times 0.4$
VFT driver loss : VFT driver output loss + pull-down resistor (RK) loss

Example :
When Ta = −10 to 50 °C (When using a fluorescent display tube with a conventional type which can use only one grid output at the same time.) and a fluorescent display tube with segment output = 3mA, digit output = 12mA, Vkk = −34.5V is used.
Operating conditions ; VDD = 5 V ± 10%, fc = 8 MHz, VFT dimmer time (DIM) = (14/16) × tseg,

Power consumption Pmax = (1) + (2) + (3)
Where,
(1) Operating power consumption: $V_{DD} \times I_{DD} = 5.5\ V \times 10\ mA = 55\ mW$
(2) Normal output port loss : $\Sigma I_{OUT2} \times 0.4 = 60\ mA \times 0.4\ V = 24\ mW$
(3) VFT driver loss : Segment pin = 3 mA × 2 V × number of segments X = 6 mW × X
Grid pin = 12mA × 2 V × 14/16 (DIM) × number of grids Y
= 21 mW
Rk loss = $(5.5V + 34.5V)^2 / 50\ k\Omega$ × (number of segments X + number of grids Y) = 32 mW × (X + Y)

Therefore, Pmax = 55 mW + 24 mW + 6 mW × X + 21 mW + 32 mW × (X + Y)
= 132 mW + 38 mWX···

Maximum power consumption Pd when Ta = 50 °C is determined by the following equation ;
PD = 1200 mW − (14.3 × 25) = 842.5 mW

The number of segments X that can be lit is:
PD > Pmax
842.5mW > 132 + 38 X
18.69 > X

Thus, a fluorescent display tube with less than 18 segments can be used. If a fluorescent display tube with 18 segments or more is used, either a pull-down resistor must be attached externally, or the number of segments to be lit must be kept to less than 18 by software.

DC Characteristics (V_{DD} = 5 V)

[Condition] V_{DD} = 5.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = − 30 to 70 °C
(Typ. : V_{DD} = 5.0 V, Topr = 25 °C, Vin = 5.0 V/0V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5V /0 V		–	–	± 2	μA
	I_{IN2}	Sink Open-drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input resistance	R_{IN}	RESET Pull-UP			100	220	450	kΩ
Pull-down resistance	R_K	Source Open Drain	V_{DD} = 5.5 V, V_{KK} = − 30 V		50	80	110	kΩ
Output Leakage Current	I_{LO1}	Sink Open-drain, Tri-st	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		–	–	± 2	μA
	I_{LO2}	Source Open-drain	V_{DD} = 5.5 V, V_{KK} = − 32 V		–	–	± 2	
Output High Voltage	V_{OH}	Tri-st	V_{DD} = 4.5 V, I_{OH} = − 0.7 mA		4.1	–	–	V
Output Low Voltage	V_{OL1}	Except XOUT, P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	V
Output High Current	I_{OH1}	P6, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V		− 18	− 28	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 4.5 V, V_{OH} = 2.4 V		− 9	− 14	–	
Output Low Current	I_{OL}	High-current (P3)	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	30	–	mA
Supply Current in NORMAL1, 2 modes	I_{DD}		fc = 16.0 MHz fs = 32.768 KHz	AD converter Disable (IREF off)	–	12	18	mA
			fc = 8.0 MHz fs = 32.768 KHz		–	6	9	
Supply Current in IDLE0, 1, 2 modes			fc = 16.0 MHz fs = 32.768 KHz		–	6	9	
			fc = 8.0 MHz fs = 32.768 KHz		–	3	4.5	
Supply Current in NORMAL1, 2 modes			fc = 16.0 MHz fs = 32.768 KHz	AD converter Enable	–	13	19	
			fc = 8.0 MHz fs = 32.768 KHz			7	10	
Supply Current in STOP mode			T_{opr} = to 50 °C	AD converter Disable	–	0.5	5	μA
			T_{opr} = to 70 °C				10	

Note 1 : Typical values show those at T_{opr} = 25°C, V_{DD} = 5V.
Note 2 : Input current (IIN1, IIN2) ; The current through pull-up or pull-down resistor is not included.
Note 3 : IDD does not include IREF current.

DC Characteristics (V_{DD} = 3 V)

[Condition] V_{DD} = 3.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = − 30 to 70 °C
(Typ. : V_{DD} = 3.0 V, Topr = 25 °C, Vin = 3.0 V/0V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.4	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 3.3 V, V_{IN} = 3.3 V/0 V		–	–	± 2	μA
	I_{IN2}	Sink Open-drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input resistance	R_{IN}	RESET Pull-Up			100	220	450	kΩ
Pull-down resistance	R_K	Source Open Drain	V_{DD} = 3.3 V, V_{KK} = − 30 V		45	75	105	kΩ
Output Leakage Current	I_{LO1}	Sink Open-drain, Tr-st	V_{DD} = 3.3 V, V_{OUT} = 3.3 V/0 V		–	–	± 2	μA
	I_{LO2}	Source Open-drain	V_{DD} = 3.3 V, V_{KK} = − 32 V		–	–	± 2	
Output High Voltage	V_{OH}	Tri-st	V_{DD} = 2.7 V, I_{OH} = − 0.6 mA		2.3	–	–	V
Output Low Voltage	V_{OL1}	Except XOUT, P3	V_{DD} = 2.7 V, I_{OL} = 0.9 mA		–	–	0.4	V
Output High Current	I_{OH1}	P6, P7	V_{DD} = 2.7 V, V_{OH} = 1.5 V		− 5.5	− 8	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 2.7 V, V_{OH} = 1.5 V		− 3	− 4.5	–	
Output Low Current	I_{OL}	High-current (P3)	V_{DD} = 2.7 V, V_{OL} = 1.0 V		–	6	–	mA
Supply Current in NORMAL1, 2 modes	I_{DD}		fc = 8.0 MHz fs = 32.768 KHz	AD converter Disable (IREF off)	–	3	4.5	mA
Supply Current in IDLE0, 1, 2 modes			fc = 8.0 MHz fs = 32.768 KHz		–	2	2.5	
Supply Current in NORMAL1, 2 modes			fc = 8.0 MHz fs = 32.768 KHz	AD converter Enable	–	3.5	5	
Supply Current in SLOW1, 2 modes			fs = 32.768 KHz	AD converter Disable	–	3	60	μA
Supply Current in SLEEP0, 1, 2 modes					–	15	30	
Supply Current in STOP mode			T_{opr} = to 50 °C		–	0.5	5	
			T_{opr} = to 70 °C				10	

Note 1 : Typical values show those at T_{opr} = 25°C, V_{DD} = 3V.
Note 2 : Input current (IIN1, IIN2) ; The current through pull-up or pull-down resistor is not included.
Note 3 : IDD does not include IREF current.
Note 4 : The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE0, 1, 2.

AD Characteristics

(V_{SS} = A_{VSS} = 0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = – 30 to 70℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
Analog Reerence Voltage Range	$\triangle V_{AREF}$		3.0	–	–	
Analog Input Voltage	V_{AIN}		0	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{DD} = V_{AREF} = 5.5 V, V_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = V_{AREF} = 4.5 to 5.5V, V_{SS} = 0 V	–	–	±1	LSB
Zero Point Error			–	–	±1	
Full Scale Error			–	–	±1	
Total Error			–	–	±2	

(V_{SS} = A_{VSS} = 0 V, 2.7 V ≦ V_{DD} < 4.5 V, Topr = – 30 to 70℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
Analog Reerence Voltage Range	$\triangle V_{AREF}$		1.2	–	–	
Analog Input Voltage	V_{AIN}		0	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{DD} = V_{AREF} = 4.5 V, V_{SS} = 0.0 V	–	0.5	0.8	mA
Non linearity Error		V_{DD} = V_{AREF} = 2.7 to 4.5V, V_{SS} = 0 V	–	–	±1	LSB
Zero Point Error			–	–	±1	
Full Scale Error			–	–	±1	
Total Error			–	–	±2	

Note 1 : Total errors includes all errors, except quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2 : Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".

Note 3 : Please use input voltage to AIN input pin in limit of V_{AREF} – V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4 : Analog Reference Voltage Range; $\triangle V_{AREF}$ = V_{AREF} - V_{SS}

AC Characteristics

(V_{SS} = 0 V, 4.5 V ≦ V_{DD} ≦ 5.5 V, Topr = −30 to 70℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL1,2 mode	0.25	–	4	μs
		IDLE0,1,2 mode				
		SLOW1,2 mode	117.6	–	133.3	
		SLEEP0,1,2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, 2.7 V ≦ V_{DD} ≦ 4.5 V, Topr = −30 to 70℃)

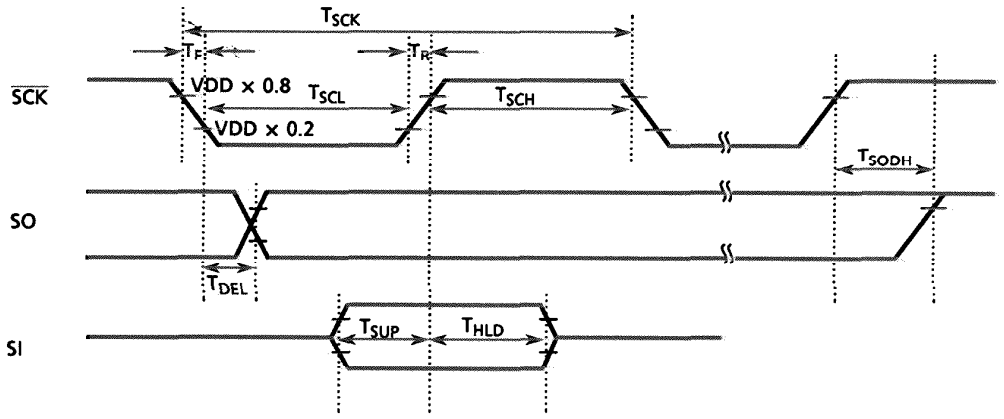
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL1,2 mode	0.5	–	8	μs
		IDLE0,1,2 mode				
		SLOW1,2 mode	117.6	–	133.3	
		SLEEP0,1,2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twcL					

HSIO AC Characteristics

(V_{SS} = 0 V, 2.7 V ≦ V_{DD} ≦ 5.5 V, Topr = −30 to 70℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
SCK output period (internal clock)	T_{SCK1}	8 MHz < fc ≦ 16 MHz V_{DD} = 4.5 V to 5.5 V	16/fc	–	–	s
SCK output low width (internal clock)	T_{SCL1}		8/fc − 100ns	–	–	
SCK output high width (internal clock)	T_{SCH1}		8/fc − 100ns	–	–	
SCK output period (internal clock)	T_{SCK2}	4 MHz < fc ≦ 8 MHz V_{DD} = 2.7 V to 5.5 V	8/fc	–	–	s
SCK output low width (internal clock)	T_{SCL2}		4/fc − 100ns	–	–	
SCK output high width (internal clock)	T_{SCH2}		4/fc − 100ns	–	–	
SCK output period (internal clock)	T_{SCK3}	fc ≦ 4 MHz V_{DD} = 2.7 V to 5.5 V	4/fc	–	–	s
SCK output low width (internal clock)	T_{SCL3}		2/fc − 100ns	–	–	
SCK output high width (internal clock)	T_{SCH3}		2/fc − 100ns	–	–	
SCK output period (external clock)	T_{SCK4}	fc ≦ 8 MHz (V_{DD} = 2.7 V to 5.5 V) fc ≦ 16 MHz (V_{DD} = 4.4 V to 5.5 V)	1000	–	–	ns
SCK output low width (external clock)	T_{SCL4}		400	–	–	
SCK output low width (external clock)	T_{SCH4}		400	–	–	
SI input setup time	T_{SUP}		200	–	–	ns
SI input hold time	T_{HLD}		200	–	–	
SO output delay time	T_{DEL}		–	–	200	
Rising time	T_R	V_{DD} = 3.0 V, CL = 50pF (Note)	–	–	100	
Falling time	T_F		–	–	100	
SO last bit hold time	T_{SODH}		16.5/fc	–	32.5/fc	

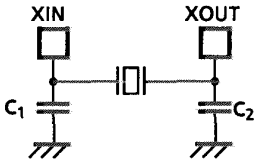
Note : CL, External Capacitance



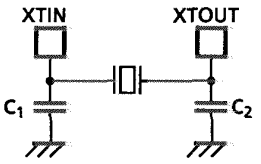
Recommended Oscillating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C_1	C_2
High-frequency Oscillation	Ceramic Resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	2.7 V to 5.5 V	MURATA CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	2.7 V to 5.5 V	SII VT-200	6 pF	6 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html

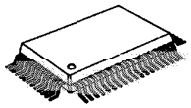
CMOS 8-Bit Microcontroller

TMP86PM74A

The TMP86PM74A is a OTP type MCU which includes 32-Kbyte One-time PROM. It is a pin compatible with a mask ROM product of the TMP86CK74A/CM74A. Writing the program to built-in PROM, the TMP86PM74A operates as the same way as the TMP86CK74A/CM74A. Using the Adapter socket, you can write and verify the data for the TMP86PM74A with a general-purpose PROM programmer same as TC571000D/AD.

Part No.	OTP	RAM	Package	Adapter Socket
TMP86PM74AF	32 K×8 bits	2 K×8 bits	P-QFP80-1420-0.80B	BM11189

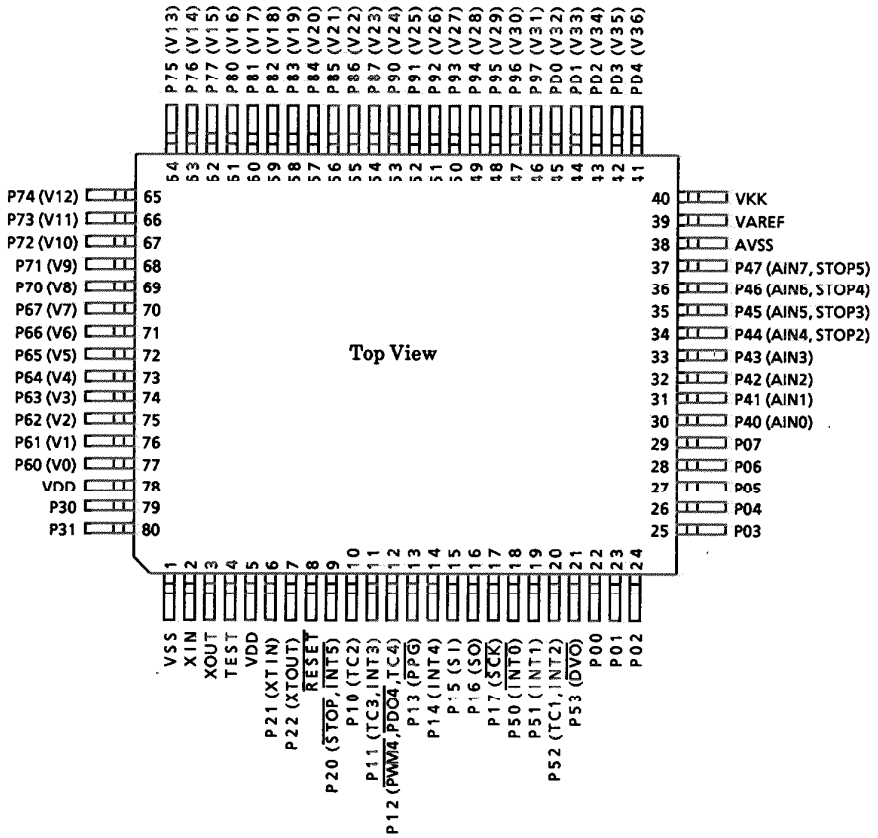
P-QFP80-1420-0.80B



TMP87PM74AF

Pin Assignments (Top View)

P-QFP80-1420-0.80B



Pin Function

The TMP86PM74A has MCU mode and PROM mode.

(1) MCU mode

In the MCU mode, the TMP86PM74A is a pin compatible with the TMP86CK74A/CM74A (Make sure to fix the TEST pin to low level).

(2) PROM mode

Pin name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16 ~ A12	Input	Input of Memory address for program	PD4 ~ PD0
A11 ~ A8			P53 ~ P50
A7 ~ A0			P47 ~ P40
D7 ~ D0	I/O	Input/Output of Memory data for program	P07 ~ P00
$\overline{CE}$	Input	Chip enable	P12
$\overline{OE}$		Output enable	P13
$\overline{PGM}$		Program control	P14
VPP	Power supply	+ 12.75 V / 5 V (Power supply of program)	TEST
VDD		+ 6.25 V / 5 V	VDD
GND		0 V	VSS
P11, P21	I/O	PROM mode setting pin. Fix to high.	
P10, P20, P22, AVSS, VAREF		PROM mode setting pin. Fix to low.	
RESET			
XIN	Input	Self oscillation with resonator (8 MHz)	
XOUT	Output		

Operation

This section describes the functions and basic operational blocks of TMP86PM74A.
The TMP86PM74A has PROM in place of the mask ROM which is included in the TMP86CK74A/CM74A.
In addition, TMP86PM74A operates as the single clock mode when releasing reset.
When using the dual clock mode, oscillate a low-frequency clock by [SET (SYSCR2). XTEN] command at the beginning of program.

1. Operating Mode

The TMP86PM74A has MCU mode and PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resister).

1.1.1 Program memory

The TMP86PM74A has a 32 Kbyte built-in one time PROM (addresses 8000 to $FFFF_H$ in the MCU mode, addresses 0000 to $7FFF_H$ in the PROM mode).
When using TMP86PM74A for evaluation of mask ROM products, the program is written in the program storing area shown in Figure 1-1.

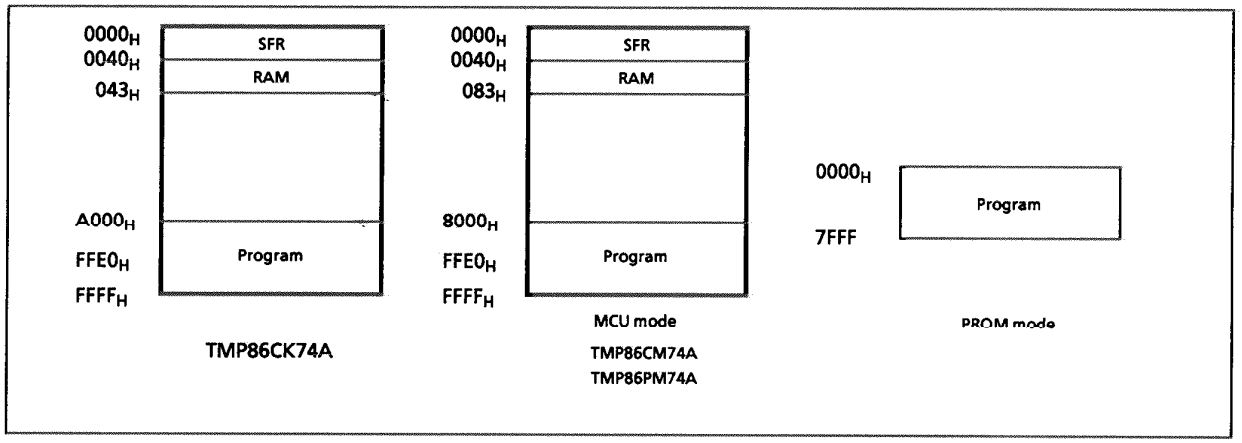


Figure 1-1. Program Memory Area

Note : The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

1.1.2 Data Memory

TMP86PM74A has a built-in 2 Kbyte Data memory (static RAM).

1.1.3 Input/Output circuitry

(1) Control pins

The control pins of the TMP86PM74A are the same as those of the TMP86CK74A/CM74A except that the TEST pin does not have a built-in pull-down resister.

(2) I/O ports

The I/O circuitries of TMP86PM74A I/O ports are the same as the those of TMP86CK74A/CM74A.

1.2 PROM Mode

The PROM mode is set by setting the $\overline{\text{RESET}}$ pin, the ports P11, P10, P22 to P20 and TEST as shown in Figure 1-2. The programming and verification for the internal PROM is achieved by using a general-purpose PROM programmer with the adapter socket.

Note: The high-speed program mode can be used. The setting is different according to the type of PROM programmer to use, refer to each description of PROM programmer.
The TMP86PM29A does not support the electric signature mode, apply the ROM type of PROM programmer to TC571000D/AD.

Always set the switch of Adapter socket to the N side when using TOSHIBA's Adapter socket.

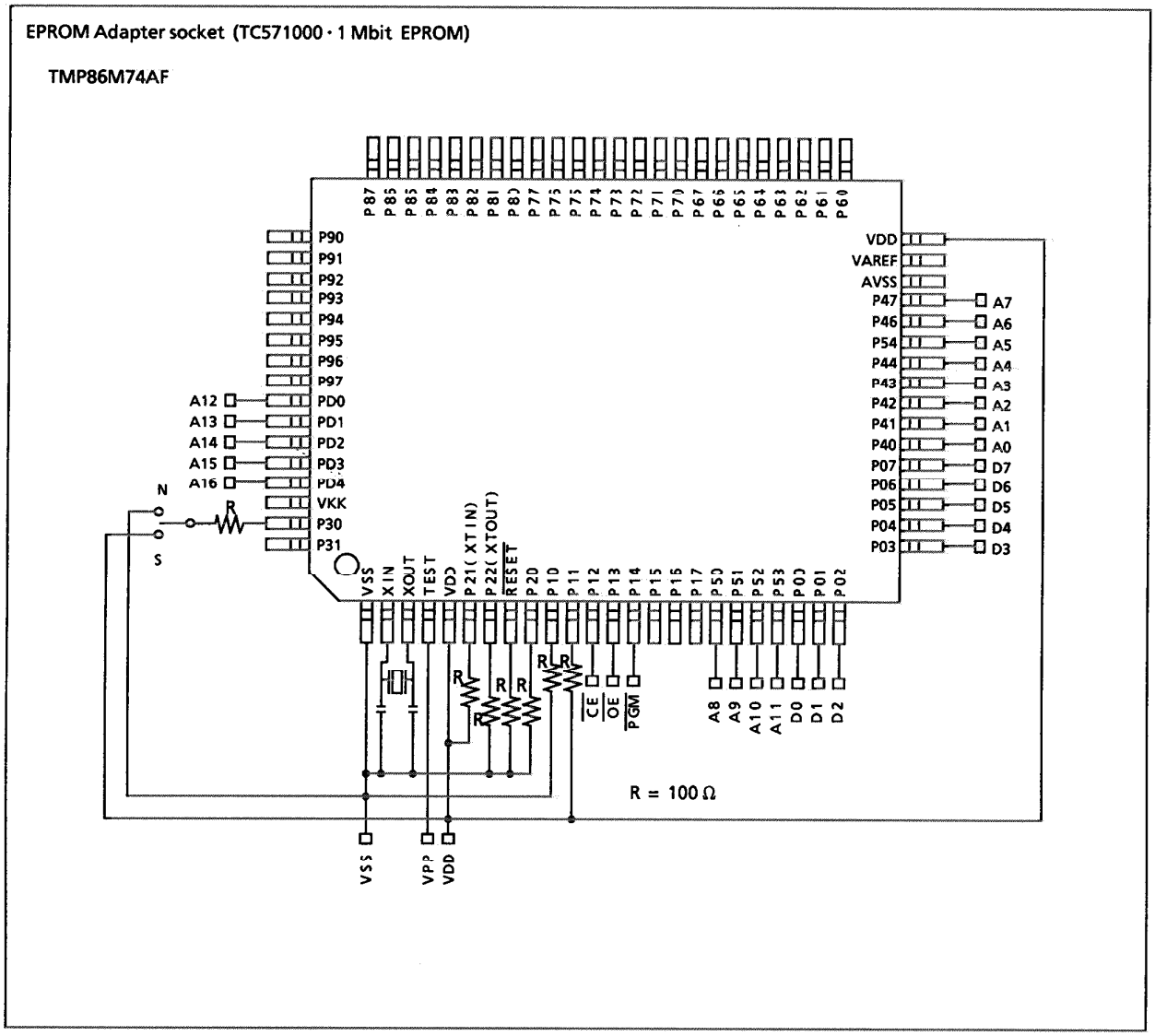


Figure 1-2. PROM Mode Setting

1.2.1 Programming flowchart (High-speed program writing)

The high-speed programming mode is set by applying 12.75 V (programming voltage) to the V_{PP} pin when the V_{CC} is 6.25 V. After the address and data are fixed, the data in the address is written by applying 0.1ms of low level program pulse to $\overline{PGM}$ pin. Then verify if the data is written.
If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{PGM}$ pin.
This programming procedure is repeated until correct data is read from the address (maximum of 25 times).
Subsequently, all data are programmed in all addresses.
When all data were written, verify all address under the condition of $V_{CC} = V_{PP} = 5$ V.

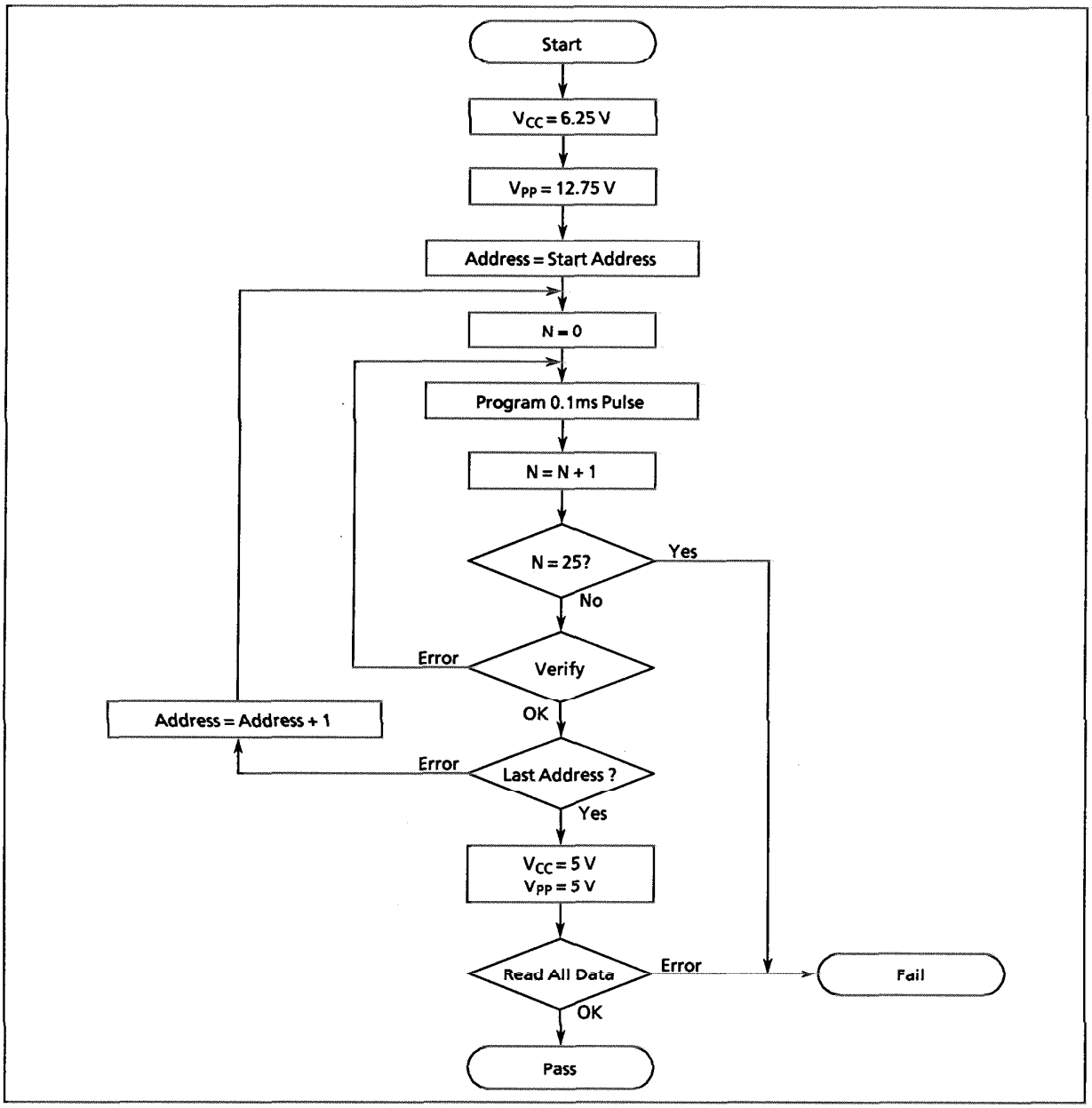


Figure 1-3. Programming Flowchart

1.2.2 Program Writing using a general-purpose PROM programmer

(1) Recommended OTP Adapter

BM11189: for TMP86PM74AF

(2) Setting of OTP Adapter

Set the switch (SW1) to N side.

(3) Setting of PROM programmer

i) Set PROM type to TC571000D/AD.
VPP: 12.75 V (high-speed program writing)

ii) Data transmission (Note 1)

The PROM of TMP86PM74A is located on different addresses; it depends on operating modes: MCU mode and PROM mode. When you write the data of ROM for mask ROM products, the data should be transferred from the address for MCU mode to that for PROM mode before writing operation is executed. For the applicable program areas of MCU mode and PROM mode are different, refer to Figure 1-1 Program Memory Area.

Example:In the block transfer (copy) mode, executed as below.

ROM capacity of 32 KB: Transferred address 8000_H to $FFFF_H$ to addresses 0000_H to $7FFF_H$

iii) Setting of the program address (Note 1)

Start address: 00000_H
End address: $07FFF_H$

(4) Writing program

Write and verify according to the above mentioned "Setting of PROM programmer."

Note 1: For the setting method, refer to each description of PROM programmer. Make sure to set the data of address area that is not in used to FF_H.

Note 2: When setting MCU to the adapter or when setting the adapter to the PROM programmer, set the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or adapter or programmer would be damaged.

Note 3: The TMP86PM74A does not support the electric signature mode. If PROM programmer uses the signature, the device would be damaged because of applying voltage of 12 ± 0.5 V to pin 9 (A9) of the address. Do not use the signature.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter		Symbol	Pins	Rating	Unit
Supply Voltage		V_{DD}		− 0.3 to 6.5	V
Program Voltage		V_{PP}	TEST/V_{PP}	− 0.3 to 13.0	
Input Voltage		V_{IN}		− 0.3 to V_{DD} + 0.3	
Output Voltage		V_{OUT1}		− 0.3 to V_{DD} + 0.3	
		V_{OUT2}	Source open drain ports	V_{DD} − 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	IOL	I_{OUT1}	P0, P1, P2, P4, P5 ports	5	mA
		I_{OUT2}	P3 port	40	
	IOH	I_{OUT3}	P0, P1, P4, P5 ports	− 3	
		I_{OUT4}	P6, P7 ports	− 30	
		I_{OUT5}	P8, P9, PD ports	− 20	
Output Current (Total)		ΣI_{OUT1}	P0, P1, P2, P3, P4, P5 ports	120	
		ΣI_{OUT2}	P6, P7, P8, P9, PD ports	− 120	°C
Power Dissipation [T_{opr} = 25°C]		PD		1200	
Soldering Temperature (time)		Tsld		260 (10 μ)	
Storage Temperature		Tstg		− 55 to 125	
Operating Temperature		Topr		− 30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = −30 to 70°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode			
Output Voltage	V_{OUT3}	Source open drain ports			V_{DD} − 38	V_{DD}	V
Input high Level	V_{IH1}	Except Hysteresis input			V_{DD} × 0.70	V_{DD}	V
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}	TTL input	$V_{DD} \leqq 4.5$ V		V_{DD} × 0.90		
Input low Level	V_{IL1}	Except Hysteresis input			0	V_{DD} × 0.30	V
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}	TTL input	$V_{DD} \leqq 4.5$ V		V_{DD} × 0.10	V_{DD}	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (1) (V_{DD} = 5 V)

[Condition] V_{DD} = 5.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = −30~70°C
(Typ.: V_{DD} = 5.0 V, Topr = 25°C, Vin = 5.0 V / 0 V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V		–	–	±2	μA
	I_{IN2}	Sink Open Drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input Resistance	R_{IN}	RESET Pull-Up			100	220	450	kΩ
Pull-down Resistance	R_K	Source Open Drain, Tri-st	V_{DD} = 5.5 V, V_{KK} = −30 V		50	80	110	kΩ
Output Leakage Current	I_{LO1}	Sink Open Drain, Tri-st	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V		–	–	±2	μA
	I_{LO2}	Source Open Drain	V_{DD} = 5.5 V, V_{KK} = −32 V		–	–	±2	
Output High Voltage	V_{OH}	Tri-st port	V_{DD} = 4.5 V, I_{OH} = −0.7 mA		4.1	–	–	V
Output Low Voltage	V_{OL1}	Except XOUT and P3 Port	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	V
Output High Current	I_{OH1}	P6, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V		−18	−28	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 4.5 V, V_{OH} = 2.4 V		−9	−14	–	
Output Low Current	I_{OL}	High Current Port (P3 port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	30	–	mA
Supply Current in NORMAL1, 2 mode	I_{DD}		fc = 16.0 MHz fs = 32.768 kHz	AD Converter Disable (IREF off)	–	12	18	mA
			fc = 8.0 MHz fs = 32.768 kHz		–	6	9	
Supply Current in IDLE0, 1, 2 mode			fc = 16.0 MHz fs = 32.768 kHz		–	6	9	
			fc = 8.0 MHz fs = 32.768 kHz		–	3	4.5	
Supply Current in NORMAL1, 2 mode			fc = 16.0 MHz fs = 32.768 kHz	AD Converter Enable	–	13	19	
			fc = 8.0 MHz fs = 32.768 kHz		–	7	10	
Supply Current in IDLE0, 1, 2 mode			Topr = to 50°C	AD Converter Disable	–	0.5	5	μA
			Topr = to 70°C		–		10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.
Note 2: Input current (I_{IN1}, I_{IN2}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.

DC Characteristics (2) (V_{DD} = 3 V)

[Condition] V_{DD} = 3.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = −30~70°C
(Typ.: V_{DD} = 3.0 V, Topr = 25°C, Vin = 3.0 V / 0 V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.4	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 3.3 V, V_{IN} = 3.3 V / 0 V		–	–	±2	μA
	I_{IN2}	Sink Open Drain, Tri-st						
	I_{IN3}	RESET, STOP						
Input Resistance	R_{IN}	RESET Pull-Up			100	220	450	kΩ
Pull-down Resistance	R_K	Source Open Drain, Tri-st	V_{DD} = 3.3 V, V_{KK} = −30 V		45	75	105	kΩ
Output Leakage Current	I_{LO1}	Sink Open Drain, Tri-st	V_{DD} = 3.3 V, V_{OUT} = 3.3 V / 0 V		–	–	±2	μA
	I_{LO2}	Source Open Drain	V_{DD} = 3.3 V, V_{KK} = −32 V		–	–	±2	
Output High Voltage	V_{OH}	Tri-st port	V_{DD} = 2.7 V, I_{OH} = −0.6 mA		2.3	–	–	V
Output Low Voltage	V_{OL1}	Except XOUT and P3 Port	V_{DD} = 2.7 V, I_{OL} = 0.9 mA		–	–	0.4	V
Output High Current	I_{OH1}	P6, P7	V_{DD} = 2.7 V, V_{OH} = 1.5 V		−5.5	−8	–	mA
	I_{OH2}	P8, P9, PD	V_{DD} = 2.7 V, V_{OH} = 1.5 V		−3	−4.5	–	
Output Low Current	I_{OL}	High Current Port (P3 port)	V_{DD} = 2.7 V, V_{OL} = 1.0 V		–	6	–	mA
Supply Current in NORMAL1, 2 mode	I_{DD}		fc = 8.0 MHz fs = 32.768 kHz	AD Converter Disable (IREF off)	–	3	4.5	mA
Supply Current in IDLE0, 1, 2 mode			fc = 8.0 MHz fs = 32.768 kHz		–	2	2.5	
Supply Current in NORMAL1, 2 mode			fc = 8.0 MHz fs = 32.768 kHz	AD Converter Enable	–	3.5	5	
Supply Current in SLOW1 mode			fs = 32.768 kHz	AD Converter Disable	–	30	60	μA
Supply Current in SLEEP0, 1 mode					–	15	30	
Supply Current in STOP mode			Topr = to 50°C		–	0.5	5	
			Topr = to 70°C				10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 3 V.
Note 2: Input current (I_{IN1}, I_{IN2}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.
Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent IDLE0, 1, 2.

AD Conversion Characteristics

(V_{SS} = 0.0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, Topr = − 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} − 1.5	−	V_{DD}	V
Analog Reference GND	A_{VSS}			V_{SS}		V
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$		3.0	−	−	V
Analog Input Voltage	V_{AIN}		V_{SS}	−	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = V_{AREF} = 5.5 V V_{SS} = AV_{SS} = 0.0 V	−	0.6	1.0	mA
Non linearity Error		V_{DD} = 4.5 to 5.0 V, V_{SS} = A_{VSS} = 0.0 V V_{VDD} = VAREF = 5.5 V	−	−	±1	LSB
Zero Point Error			−	−	±1	
Full Scale Error			−	−	±1	
Total Error			−	−	±2	

(V_{SS} = 0.0 V, 2.7 V ≤ V_{DD} < 4.5 V, Topr = − 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} − 1.5	−	V_{DD}	V
Analog Reference GND	A_{VSS}			V_{SS}		V
Analog Reference Voltage Range (Note 4)	$\triangle V_{AREF}$		2.5	−	−	V
Analog Input Voltage	V_{AIN}		V_{SS}	−	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = V_{AREF} = 4.5 V V_{SS} = A_{VSS} = 0.0 V	−	0.5	0.8	mA
Non linearity Error		V_{DD} = A_{VDD} = 2.7 V to 4.5 V V_{SS} = A_{VSS} = 0.0 V	−	−	±1	LSB
Zero Point Error			−	−	±1	
Full Scale Error			−	−	±1	
Total Error			−	−	±2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.11.2 Register Configuration".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} - V_{SS}$

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = −30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.25	−	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	−	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 16 MHz	−	31.25	−	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	−	15.26	−	μs
Low Level Clock Pulse Width	twcL					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, Topr = −30 to 70°C)

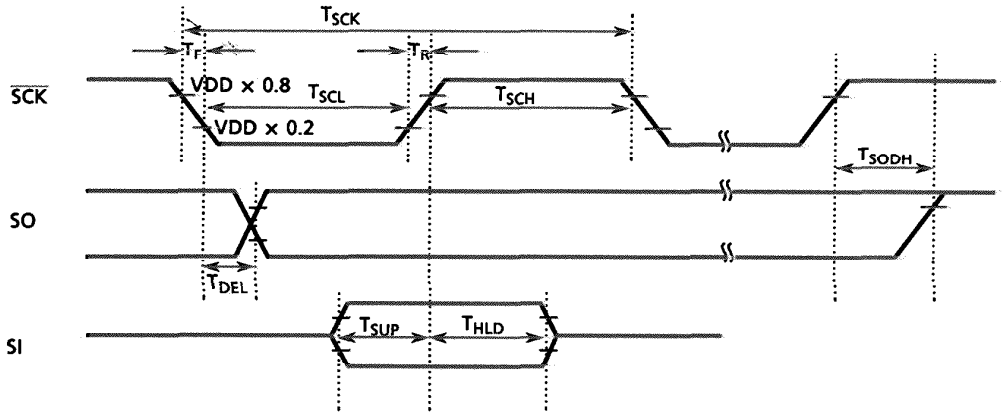
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.5	−	8	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	−	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	−	62.5	−	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	−	15.26	−	μs
Low Level Clock Pulse Width	twcL					

HSIO AC Characteristics

(V_{SS} = 0 V, 2.7 V ≦ V_{DD} ≦ 5.5 V, Topr = −30 to 70℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
SCK output period (internal clock)	T_{SCK1}	8 MHz < fc ≦ 16 MHz V_{DD} = 4.5 V to 5.5 V	16/fc	–	–	s
SCK output low width (internal clock)	T_{SCL1}		8/fc − 100ns	–	–	
SCK output high width (internal clock)	T_{SCH1}		8/fc − 100ns	–	–	
SCK output period (internal clock)	T_{SCK2}	4 MHz < fc ≦ 8 MHz V_{DD} = 2.7 V to 5.5 V	8/fc	–	–	s
SCK output low width (internal clock)	T_{SCL2}		4/fc − 100ns	–	–	
SCK output high width (internal clock)	T_{SCH2}		4/fc − 100ns	–	–	
SCK output period (internal clock)	T_{SCK3}	fc ≦ 4 MHz V_{DD} = 2.7 V to 5.5 V	4/fc	–	–	s
SCK output low width (internal clock)	T_{SCL3}		2/fc − 100ns	–	–	
SCK output high width (internal clock)	T_{SCH3}		2/fc − 100ns	–	–	
SCK output period (external clock)	T_{SCK4}	fc ≦ 8 MHz (V_{DD} = 2.7 V to 5.5 V) fc ≦ 16 MHz (V_{DD} = 4.4 V to 5.5 V)	1000	–	–	ns
SCK output low width (external clock)	T_{SCL4}		400	–	–	
SCK output low width (external clock)	T_{SCH4}		400	–	–	
SI input setup time	T_{SUP}		200	–	–	ns
SI input hold time	T_{HLD}		200	–	–	
SO output delay time	T_{DEL}		–	–	200	
Rising time	T_R	V_{DD} = 3.0 V, CL = 50pF (Note)	–	–	100	
Falling time	T_F		–	–	100	
SO last bit hold time	T_{SODH}		16.5/fc	–	32.5/fc	

Note : CL, External Capacitance

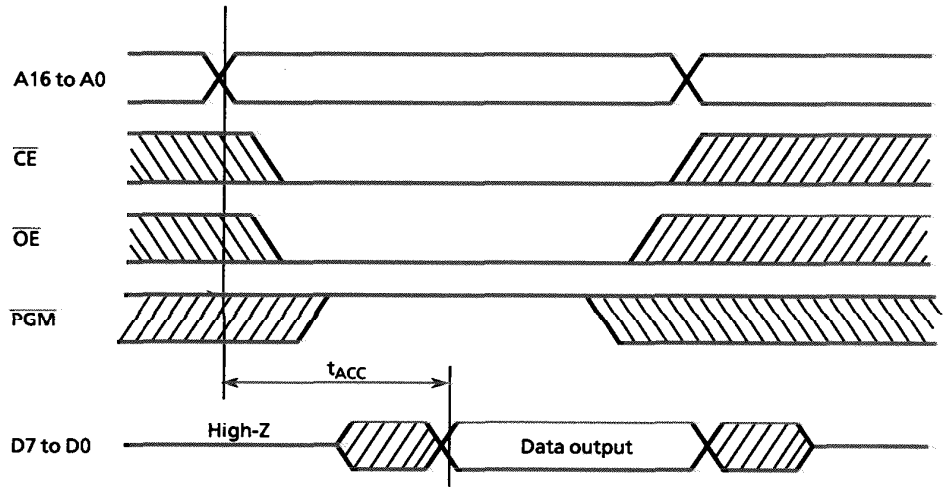


DC Characteristics, AC Characteristics (PROM Mode) (V_{SS} = 0 V, Topr = 25 ±5°C)

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH4}		2.2	–	V_{CC}	V
Low leve input voltage (TTL)	V_{IL4}		0	–	0.8	V
Power supply	V_{CC}		4.75	5.0	5.25	V
Power supply of program	V_{PP}					
Address access time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5tcyc + 300	–	ns

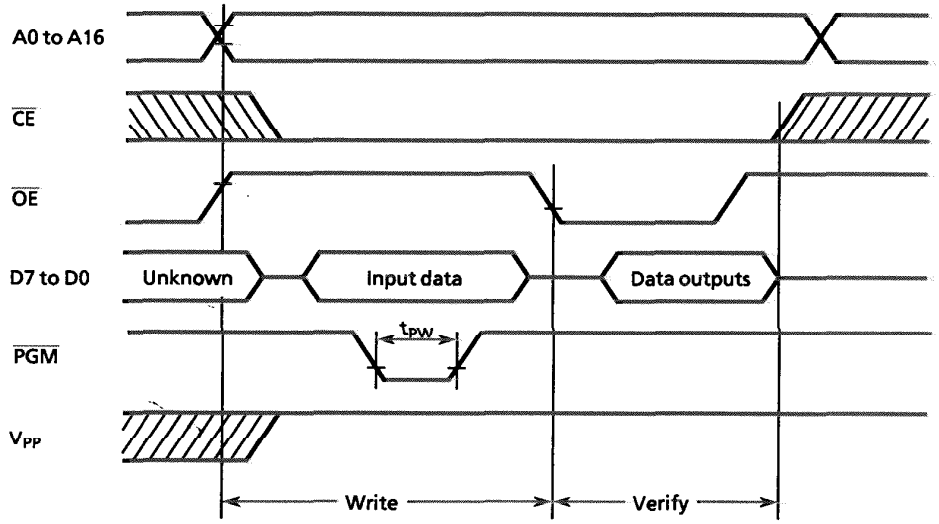
Note: tcyc = 400 ns at 10 MHz



(2) Program operation (High-speed) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH4}		2.2	–	V_{CC}	V
Low leve input voltage (TTL)	V_{IL4}		0	–	0.8	V
Power supply	V_{CC}		6.0	6.25	6.5	V
Power supply of program	V_{PP}		12.5	12.75	13.0	V
Pulse width of initializing program	t_{PW}	V_{CC} = 6.0 V	0.095	0.1	0.105	ms

High-speed program writing



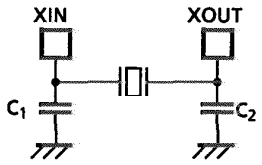
Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.

Note2 : The pulling up/down device on the condition of V_{PP} = 12.75 V ± 0.25 V causes a damage for the device. Do not pull up/down at programming.

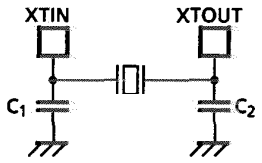
Note3 : Use the recommended adapter and mode.
Using other than the above condition may cause the trouble of the writting.

Recommended Oscillating Conditions (V_{SS} = 0 V, Topr = −30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	2.7 V to 5.5 V	MURATA CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	2.7 V to 5.5 V	SII VT-200	6 pF	6 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html