TOSHIBA

TC260 SD11 1.25/2.5Gb/s Dual Mode SerDes Macros

The TC260 SD11 macros enable building high speed interfaces — while consuming a limited number of pins — between integrated circuits (ICs) implemented in standard cell or as embedded array in Toshiba's TC260 technology. More specifically, SD11 is a dual mode serial 'SerDes' interface. It supports data rates in two bands: 1–1.25Gb/s and 2–2.5Gb/s. Designed for low power consumption, SD11 enables building interfaces with a high number of parallel channels. SD11 can be used in backplanes, on-board chip-to-chip connections, and in Fibre Channel and GigaEthernet applications.

FEATURES

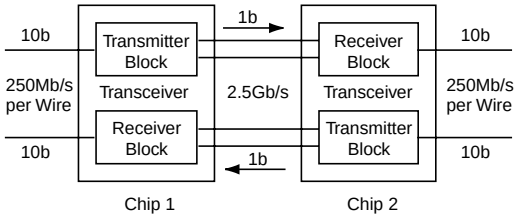
- Enables high bandwidth interfacing between System ICs, with few pins
- Supports data rates in two bands: 1–1.25Gb/s and 2–2.5Gb/s
- Width of parallel input and output programmable to 8b, 10b, 16b, 20b
- Supports:
  - Backplane applications
  - On-board chip-to-chip connections
  - 100MB/s & 200MB/s Fibre Channel applications
  - GigaEthernet applications
  - Other industry-standard interfaces
- Single channel or multi-channel, with modular macros for optimum configuration
- Built-in pre-emphasis and equalization for improved transmission
- With design-in support by Toshiba's high speed applications team
- Optimized for ASICs in Toshiba's advanced TC260 technology
  - 0.14µm drawn gate lengths
  - Logic CMOS or embedded DRAM process
  - IP library including MIPS processors
  - Standard cell or embedded array

DESCRIPTION

At each end of a SD11 interface is a SD11 transceiver. The transceiver contains a transmitter block and a receiver block. The transmitter accepts a 10-bit wide logic signal on its 10 parallel inputs and serializes this data to a 1-bit wide 2.5Gb/s NRZ signal. The transmitter driver outputs this signal as a differential signal over two wires. The bit rate on the 10 input wires is 250Mb/s per wire, in line with clock rates easily achievable in ASIC cores. At the receiver end the receiver buffer accepts the differential signal and recovers the timing information. The deserializer generates a 10-bit wide logic signal, together with an aligned clock. Standard comma detection is included. The SD11 transceiver requires one reference clock signal. The transmitter includes pre-emphasis and the receiver includes equalization to extend transmission over longer copper wires. The data rates and parallel input and output widths in this description are examples. Other data rates and widths are possible. The width of the parallel input and output can be set as 8b, 10b, 16b or 20b.

BLOCK DIAGRAM

Shown are block diagrams for a SD11 full-duplex interface and for a SD11 transceiver macro. The data rates in the figures are examples; other data rates are possible.



Each 2.5Gb/s signal is transmitted as a differential signal over two wires.

Figure: SD11 Full-duplex Connection

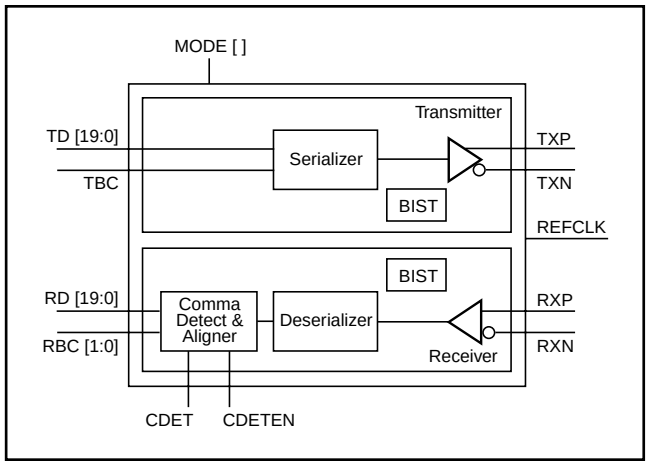


Figure: SD11 Transceiver Block Diagram

PIN DEFINITION

The pin description for the SD11 transceiver is shown below.

Pin name and signal	Description
TD[19:0]	Transmitter block input
TBC	Clock from chip core
REFCLK	Transmitter reference clock input
RD[19:0]	Receiver block output
RBC[1:0]	Recovered clock, to chip core
TXP, TXN	Differential transmitter output signal
RXP, RXN	Differential receiver input signal
CDETEN	Enables comma detection and byte alignment
CDET	Enabled when comma characters are detected
MODE[ ]	Settings determine serial bitrate band, parallel input and output width and data rate, and reference clock frequency

Table: SD11 Macro Pin Names and Descriptions

APPLICATIONS

Different applications require different data rates. SD11 handles a range of applications and data rates. The table lists various applications with the required or available data rate for the serial interface.

Application	SerDes interface data rate Gb/s
Backplanes	1–1.25 or 2–2.5
On-board chip-to-chip	1–1.25 or 2–2.5
100MB/s Fibre Channel	1.0625
GigaEthernet	1.25
200MB/s Fibre Channel	2.125
100MB/s & 200MB/s Fibre Channel	1.0625 & 2.125
Other industry-standard interfaces	1–1.25 or 2–2.5

Table: SD11 Applications and Data Rates

SD11 macros enable building single channel or multi-channel interfaces. In typical GigaEthernet or Fibre Channel applications the transmitter blocks and receiver blocks are kept together in transceivers. Backplane or on-board chip-to-chip applications may see separated transmitter blocks and receiver blocks as illustrated in the figure below. The maximum number of transceivers on a chip depends on the serial data rate and the power consumption budget. The macros are designed modular such that in multi-channel configurations, not all transceiver submacros need repeating.

In typical applications, the 10-bit frames are 8b10b coded. The SD11 macro does not include the required 8b10b encoder and decoder. These functions are provided by the user, or are available from third-party vendors or Toshiba.

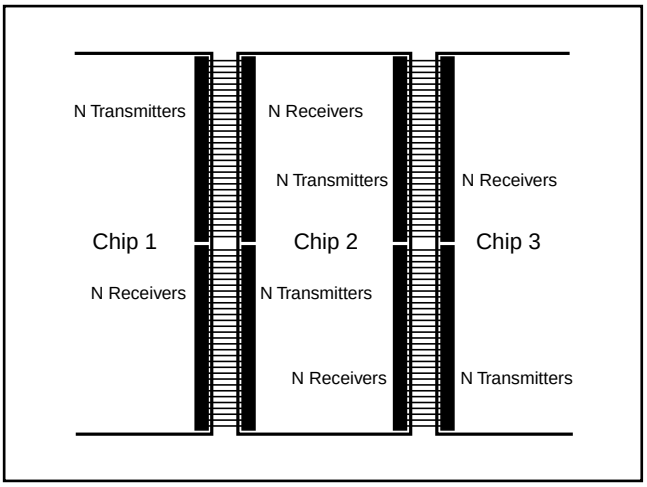


Figure: In this Example of Multi-channel Interfaces Between Multiple Chips, Chip 2 Contains Multiple Banks of Transmitters and Receivers.

SUPPORT AND TESTING

Toshiba provides a full design kit for design-in support. Applications support is available from Toshiba's experienced high-speed applications team. For testing purposes, the SD11 transceiver macro supports scan for its low speed digital circuits and BIST for its high speed circuits. The SD11 macro also contains internal loop backs for serial testing of the receiver transmitter path.

POSITIONING VERSUS SD10

Toshiba also offers the SD10 1.6/3.2Gb/s SerDes macro. This macro transmits and receives data in two bands: 1–1.6 and 2–3.2Gb/s and is designed for high performance. SD10 is more suitable for integrated physical layer circuit applications. Due to the higher power consumption, the number of channels in multi-channel interfaces is more limited. SD11 is designed for low power consumption.

REFERENCES

- IEEE Draft 802.3z
- ANSI T11.2 PC-PH
- NCITS T11.2, Fibre Channel Physical Interface (FC-PI)
- NCITS T11.2, Fibre Channel High-Speed Parallel Interface (HSPI)
- ITU-T G.825
- ITU-T G.958

CHARACTERISTICS

Selected characteristics and requirements are listed.

Parameter	Description	Minimum	Typical	Maximum	Unit
Zout	Transmitter single-ended output impedance	45	50	55	ohm
Zin	Receiver single-ended input impedance	45	50	55	ohm
Tosk**	Skew between transmitter outputs	–15	—	15	ps
Tisk	Tolerable skew between receiver inputs	–190	—	190	ps
Vod***	Differential transmitter output signal swing	1.1	—	2	V
Vi	Differential receiver input sensitivity	0.3	—	2	V
ToutR/ToutF	Transmitter output rise/fall time 20% — 80%	100	—	192	ps

** Output skew is package dependent

*** For 50ohm. More precise values: TBD

Table: Selected AC Characteristics and Requirements

Parameter	Description	Minimum	Typical	Maximum	Unit
Vcc2	Supply voltage	–5%	1.5	+5%	V
Vcc3	Supply voltage	–5%	2.5	+5%	V
Tstart	Start-up temperature	–40	25	125	C
Tj	Operating temperature	0	65	125	C

Table: Selected Characteristics and Requirements

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