TOSHIBA

TC260 SD10 1.6/3.2Gb/s Dual Mode SerDes Macros

The TC260 SD10 macros enable building high speed interfaces — while consuming a limited number of pins — between integrated circuits (ICs) implemented in standard cell or as embedded array in Toshiba's TC260 technology. More specifically, SD10 is a dual mode serial 'SerDes' interface. It supports data rates in two bands: 1–1.6Gb/s and 2–3.2Gb/s. Designed for high performance, SD10 can be used in backplanes, to build integrated physical layer circuits for Fibre Channel, GigaEthernet or 10GigaEthernet, and in on-board chip-to-chip connections.

FEATURES

- Enables high bandwidth interfacing between System ICs, with few pins
- Supports data rates in two bands: 1–1.6Gb/s and 2–3.2Gb/s
- Optional HSPI compatible 10b interface, and DDR coding
- Jitter compliance with GigaEthernet, Fibre Channel, and 10GigaEthernet
- Adjustable interface voltage swing
- Application support for:
  - High bandwidth backplanes
  - GigaEthernet transceivers
  - 10GigaEthernet XAUI interfaces
  - 100MB/s & 200MB/s Fibre Channel transceivers
  - Other industry-standard interfaces
  - On-board chip-to-chip connections
- Single channel or multi-channel, with modular macros for optimum configuration
- Built-in pre-emphasis and equalization for improved transmission over copper
- Internal impedance control
- Optional receiver and driver redundancy
- With design-in support by Toshiba's high speed applications team
- Optimized for ASICs in Toshiba's advanced TC260 technology
  - 0.14µm drawn gate lengths
  - Logic CMOS or embedded DRAM process
  - IP library including MIPS processors
  - Standard cell or embedded array

DESCRIPTION

At each end of a SD10 interface is a SD10 transceiver. The transceiver contains a transmitter block and a receiver block. The transmitter accepts a 10-bit wide 8b10b encoded data on its 10 parallel inputs and serializes this data to a 1-bit wide 3.2Gb/s NRZ signal. The transmitter driver outputs this signal as a differential signal over two wires. The data rate on the 10 input wires is 320Mb/s per wire, in line with clock rates easily achievable in the core area of ASICs. At the receiver end the receiver buffer accepts the differential signal and recovers the timing information. The deserializer generates a 10-bit wide logic signal, together with an aligned clock. Options are HSPI compatibility and DDR coding. Standard comma detection is included. The SD10 transceiver requires one reference clock signal. The transmitter includes pre-emphasis and the receiver includes equalization to extend transmission over longer copper wires. The data rates in this description are examples. Other data rates are possible.

BLOCK DIAGRAM

Shown are block diagrams for a SD10 full-duplex interface and for a SD10 transceiver macro.

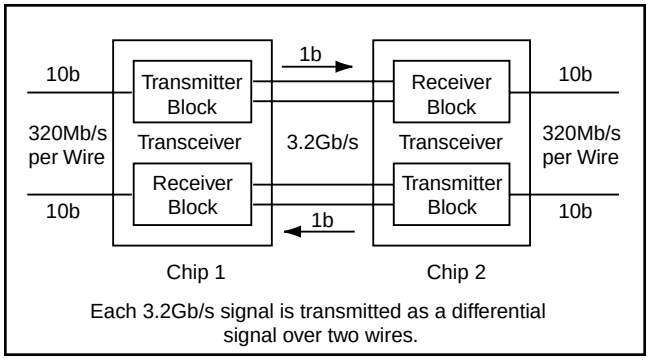

Figure: SD10 Full-duplex Connection

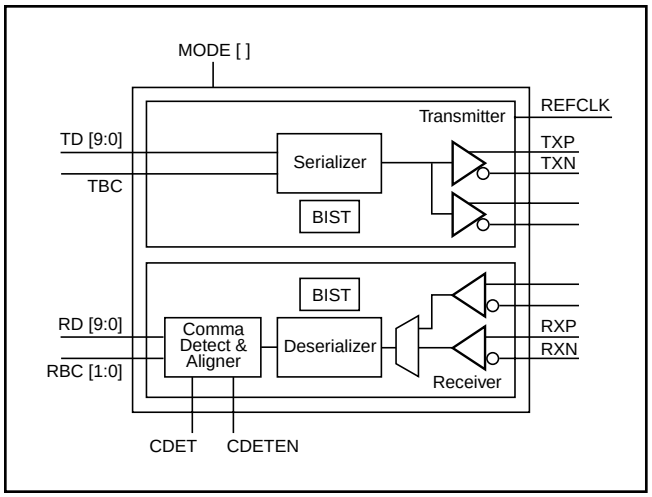

Figure: SD10 Transceiver Block Diagram

PIN DEFINITION

The pin description for the SD10 transceiver is shown below.

Pin name and signal	Description
TD[9:0]	Transmitter block input
TBC	Clock from chip core
REFCLK	Transmit reference clock input
RD[9:0]	Receiver block output
RBC[1:0]	Recovered clock, to chip core
TXP, TXN	Differential transmitter output signal
RXP, RXN	Differential receiver input signal
CDETEN	Enables comma detection and byte alignment
CDET	Enabled when comma characters are detected
MODE[ ]	Settings determine serial data rate band, parallel input and output data rate, and reference clock frequency

Table: SD10 Macro Pin Names and Descriptions

APPLICATIONS

Different applications require different data rates. Although designed for high performance, SD10 handles a range of applications and data rates.

Application	SerDes interface data rate Gb/s
Backplanes	1–1.6 or 2–3.2
On-board chip-to-chip	1–1.6 or 2–3.2
100MB/s Fibre Channel	1.0625
GigaEthernet	1.25
200MB/s Fibre Channel	2.125
100MB/s & 200MB/s Fibre Channel	1.0625 & 2.125
Other industry-standard interfaces *	1–1.6 or 2–3.2
10GigaEthernet *	3.125
1394b*	0.983

Table: SD 10 Applications and Data Rates

*Contact Toshiba for more information on the use of SD10 for building devices for these applications.

The figures below show how SD10 transceivers can be used in Fibre Channel, GigaEthernet or 10GigaEthernet applications.

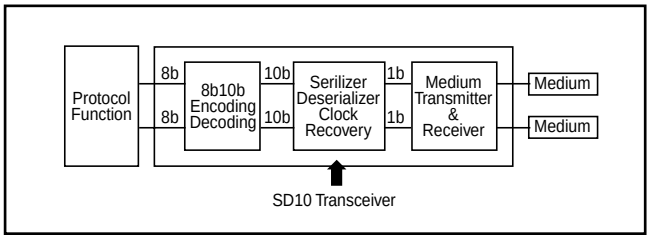

Figure: SD10 Transceiver Macro within a Fibre Channel Interface

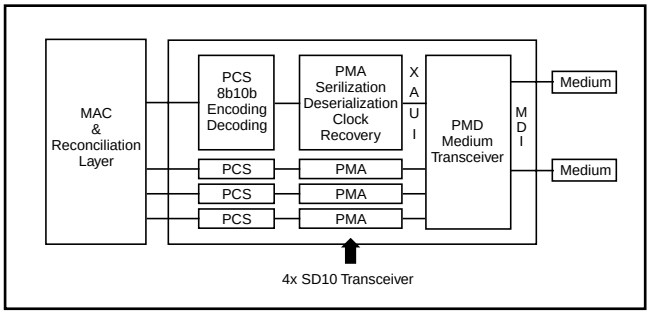

Figure: SD10 Transceivers within a 10GigaEthernet Interface

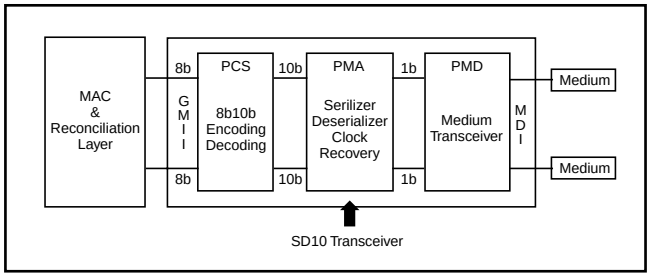

Figure: SD10 Transceiver within a GigaEthernet Interface

The abbreviations in the figure are consistent with the GigaEthernet standard and are explained.

PMD: Physical Medium Dependent sublayer

PMA: Physical Medium Attachment sublayer

PCS: Physical Coding Sublayer

MAC: Medium Access Control layer

GMII: Gb Medium Independent Interface

MDI: Medium Dependent Interface

Typically, the 10-bit frames are 8b10b coded. The SD10 macro does not include the 8b10b encoder and decoder. These functions are provided by the user, or are available from third-party vendors or Toshiba.

SD10 macros enable building single channel or multi-channel interfaces as shown in the figure to the right. In typical GigaEthernet or Fibre Channel applications the transmitter blocks and receiver blocks are kept together in transceivers. Backplane or on-board chip-to-chip applications may see separated transmitter blocks and receiver blocks. The number of SD10 transceivers per chip depends on the serial data rate and the power consumption budget.

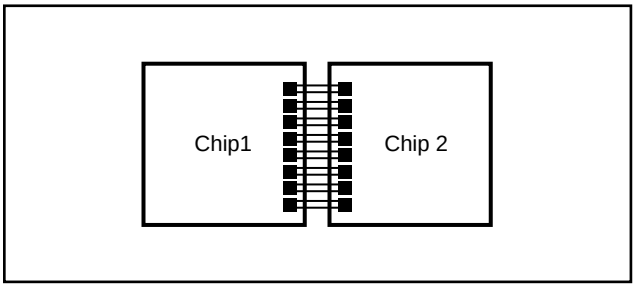

Figure: In this Example of a Multi-channel Interface each Chip Contains Eight SD10 Transceivers.

CHARACTERISTICS

Selected characteristics and requirements are listed.

Parameter	Description	Minimum	Typical	Maximum	Unit
Zout*	Transmitter single-ended output impedance	45	50	55	ohm
Zin*	Receiver single-ended input impedance	45	50	55	ohm
Tosk**	Skew between transmitter outputs	–15	—	15	ps
Tisk	Tolerable skew between receiver inputs	–190	—	190	ps
Vod***	Differential transmitter output signal swing	1.1	—	2	V
Vi	Differential receiver input sensitivity	0.3	—	2	V
ToutR/ToutF	Transmitter output rise/fall time 20% - 80%	100	—	192	ps

* 75ohm is also supported ** Output skew is package dependent *** For 50ohm. Voltage swing is adjustable

Table: Selected AC Characteristics and Requirements

Parameter	Description	Minimum	Typical	Maximum	Unit
Vcc2	Supply voltage	–5%	1.5	+5%	V
Vcc3	Supply voltage	–5%	2.5	+5%	V
Tstart	Start-up temperature	–40	25	125	C
Tj	Operating temperature	0	65	125	C

Table: Selected Characteristics and Requirements

SUPPORT AND TESTING

Toshiba provides a full design kit for design-in support. Applications support is available from Toshiba's experienced high-speed applications team. For testing purposes, the SD10 transceiver macro supports BIST. The SD10 macro also contains internal loop backs for serial testing of the receiver transmitter path.

POSITIONING VERSUS SD11

Toshiba also offers the SD11 1.25/2.5Gb/s dual mode SerDes macro. This macro transmits and receives data in two bands 1–1.25Gb/s and 2–2.5Gb/s. It consumes less power and enables building wider multi-channel interfaces. It also offers more flexibility in the width and data rate selection of the parallel input and output. SD10 is designed for high performance.

REFERENCES

- IEEE Draft 802.3z
- ANSI T11.2 PC-PH
- NCITS T11.2, Fibre Channel Physical Interface (FC-PI)
- NCITS T11.2, Fibre Channel High-Speed Parallel Interface (HSPI)
- ITU-T G.825
- ITU-T G.958

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