- **1.0 to 1.6 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Chip Scale Footprint With 80-Pin 5 mm × 5 mm Land Grid Array (LGA) Package (MicroStarJR™)**
- **Low Power Consumption < 250 mW at 1.25 Gbps**
- **PECL Compatible Differential I/O on High-Speed Interface**
- **Single Monolithic PLL Design**
- **Support For 10 Bit Interface (TBI) or Reduced Interface 5-Bit Double Data Rate (DDR) Clocking**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **IEEE 802.3 (Gigabit Ethernet) Compliant**
- **Advanced 0.25 μm CMOS Technology**
- **Interfaces To Backplane, Copper Cables or Optical Modules**
- **No External Filter Capacitors Required**
- **Comprehensive Suite of Built-In Testability**
- **IEEE 1149.1 JTAG Support**
- **2.5-V Supply for Lowest Power Operation**
- **3.3-V Tolerant on TTL Inputs**
- **Hot Plug Protection**
- **ESD Protection 2 kV HBM**

## description

The TLK2201JR is a member of the transceiver family of multigigabit transceivers, intended for use in ultrahigh-speed bidirectional point-to-point data transmission systems. The TLK2201JR gigabit ethernet transceiver is fully compliant with IEEE 802.3 requirements for serializer/deserializer functions at 1.25 Gbps. The TLK2201JR supports a wide range of serial data rates from 1.0 Gbps to 1.6 Gbps.

The primary application of this device is to provide building blocks for point-to-point baseband data transmission over controlled impedance media of 50 Ω or 75 Ω. The transmission media can be printed-circuit board traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

| | A | B | C | D | E | F | G | H | J | |
|---|---|---|---|---|---|---|---|---|---|---|
| 9 | RD1 | RD2 | RD3 | RD4 | RD5 | RD6 | RD7 | RD8 | RD9 | 9 |
| 8 | RD0 | VDD | VDD | JTMS | JTRST N | JTDI | VDD | VDD | SYNC | 8 |
| 7 | RXN | VDDA | GNDA | GNDA | GND | GND | GND | RBC MODE | RBC0 | 7 |
| 6 | RXP | VDDA | GNDA | GNDA | GND | GND | GND | TEST EN | RBC1 | 6 |
| 5 | LOS | VDDA | GNDA | GNDA | GNDA | GND | GND | JTCLK | JTDO | 5 |
| 4 | TXN | VDDA | GND | GND | GND | GND | GND | PRBS EN | SYNC EN | 4 |
| 3 | TXP | VDD PLL | Open | GND | GND | GND | GND | MODE SEL | REF CLK | 3 |
| 2 | TD0 | VDD | VDD | VDD | VDD | EN ABLE | VDD | VDD | LOOP EN | 2 |
| 1 | TD1 | TD2 | TD3 | TD4 | TD5 | TD6 | TD7 | TD8 | TD9 | 1 |
| | A | B | C | D | E | F | G | H | J | |

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## description (continued)

The TLK2201JR performs the data serialization, deserialization, and clock extraction functions for a physical layer interface device. The transceiver operates at 1.25 Gbps (typical), providing up to 1.0 Gbps of data bandwidth over a copper or optical media interface.

The TLK2201JR supports both the defined 10-bit interface (TBI) and a reduced 5-bit interface utilizing double data rate (DDR) clocking. In the TBI mode the serializer/deserializer (SERDES) accepts 10-bit wide 8-bit/10-bit (8b/10b) parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially at PECL compatible voltage levels. The SERDES extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte.

In the DDR mode the parallel interface accepts 5-bit wide 8-bit/10-bit encoded data aligned to both the rising and falling edge of the reference clock. The data is clocked most significant bit first, (i.e., bits 0 - 4 of the 8-bit/10-bit encoded data) on the rising edge of the clock and the least significant bits (i.e., bits 5 - 9 of the 8-bit/10-bit encoded data) are clocked on the falling edge of the clock.

The transceiver automatically locks onto incoming data without the need to prelock.

The TLK2201JR provides a comprehensive series of built-in tests for self-test purposes including loopback and PRBS generation and verification. An IEEE 1149.1 JTAG port is also supported.

The TLK2201JR is housed in a high performance, thermally enhanced, 80-pin land grid array (LGA) MicroStarJr™ package. Use of the MicroStarJr™ package does not require any special considerations. All ac performance specifications in this data sheet are measured with the MicroStarJr™ soldered to the test board.

The TLK2201JR is characterized for operation from 0°C to 70°C.

The TLK2201JR uses a 2.5 V supply. The I/O section is 3.3 V compatible. With the 2.5 V supply the chipset is very power efficient dissipating less than 250 mW typical power when operating at 1.25 Gbps.

The TLK2201JR is designed to be hot plug capable. A power-on reset holds RCB0 and RCB1 low and goes to high impedance to the parallel side output signal pins during power up as well as goes to TXP and TXN.

## differences between TLK2201JR and TNETE2201

The TLK2201JR is a functional equivalent of the TNETE2201B. There are several differences between the two devices as noted below.

- The $V_{CC}$ is 2.5 V for the TLK2201JR versus 3.3 V for TNETE2201.
- The PLL filter capacitors on pins 16, 17, 48, and 49 of the TNETE2201 are no longer required.
- No pulldown resistors are required on the TXP/TXN outputs.

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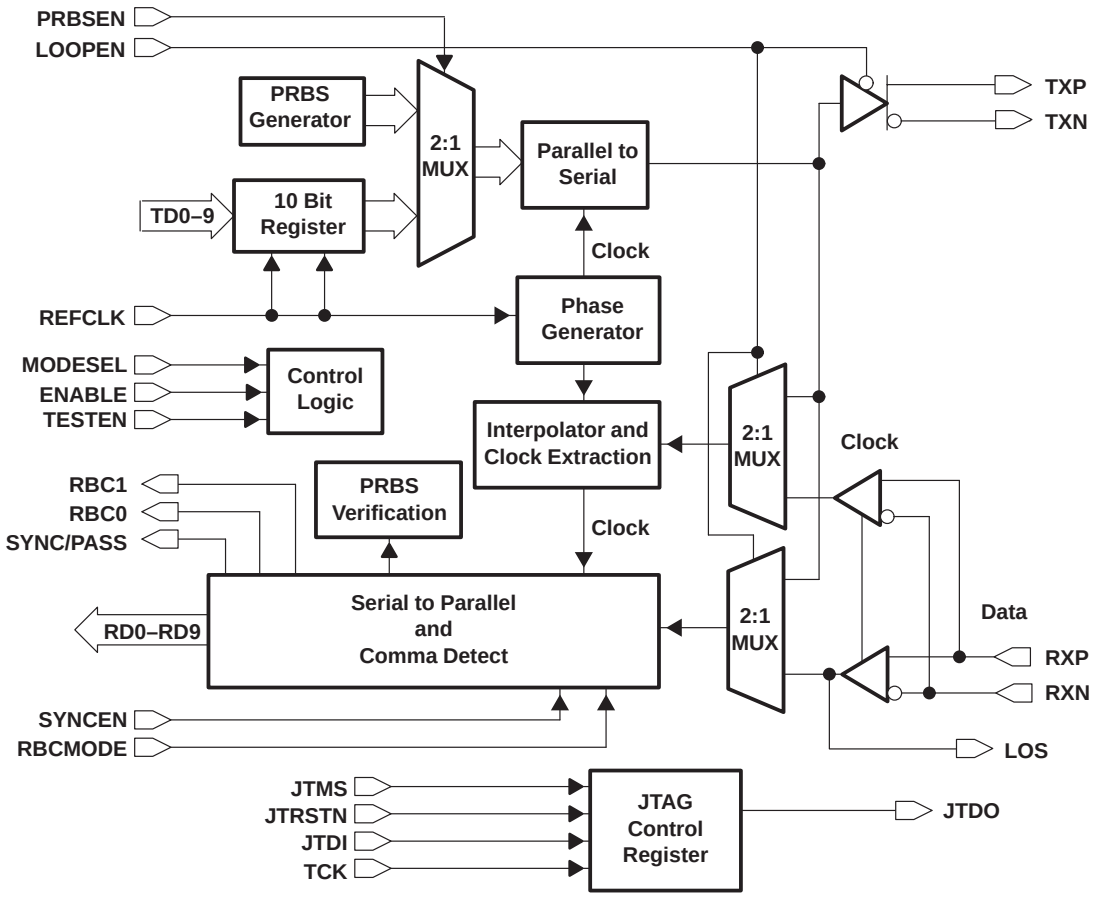
## transceiver family

The TLK2201JR is a member of the transceiver family of CMOS multi-gigabit transceivers, intended for use in high-speed bidirectional point-to-point data transmission systems. Other members of the the transceiver family include:

- **TLK1501** – A 0.6-Gbps to 1.5-Gbps transceiver with on chip 8-bit/10-bit ENDEC providing up to 1.28 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- **TLK2500/TLK2501** – A 1.6-Gbps to 2.5-Gbps transceiver with on chip 8-bit/10-bit ENDEC providing up to 2 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- **TLK2701** – A 2.5 Gbps to 2.7 Gbps transceiver with on-chip 8-bit/10-bit ENDEC, providing up to 2.16 Gbps of data bandwidth with k-character control, packaged in a 64-pin VQFP PowerPAD™ package.
- **TLK3101** – A 2.5-Gbps to 3.125-Gbps transceiver with on-chip 8-bit/10-bit ENDEC, providing up to 2.5 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- **TLK3104SC** – A 3-Gbps to 3.125-Gbps quad transceiver with on chip 8-bit/10-bit ENDEC, a 16-bit low voltage differential signaling (LVDS) parallel interface, packaged in 289 pin PBGA.
- **TLK3104SA** – A 3-Gbps to 3.125-Gbps quad transceiver with on chip 8-bit/10-bit ENDEC, an IEEE 802.3ae defined XGMII parallel interface with SSTL_2 I/O, packaged in 289 pin PBGA.

## functional block diagram

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