Application Report
SPRA469

Introduction to the TMS320LC549/TMS320VC549

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ABSTRACT

The TMS320LC549 and the TMS320VC549 are high performance, highly integrated members of TI's growing 'C54x product line. The 'LC549 delivers 66 or 80 MIPS performance with a 3.3V core power supply. The 'VC549 offers 80 or 100 MIPS performance with a 2.5V core power supply (I/O voltage remains at 3.3V). All the 'C549[1] devices provide 32K words of on-chip SRAM, 16K words of on-chip ROM, 3 serial ports, a host port interface, and a timer. The 'C549 was developed to service a variety of end-equipment in the wireless and wireline communications market that require high performance, very low power dissipation, and small physical size.

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[1] Use of 'C549 will designate reference to both the 'LC549 and the 'VC549 DSPs. 'LC549 and 'VC549 will be used only when specific reference to each is necessary.

TMS320C54x Architectural Overview

The TMS320C54x offers some of the most efficient MIPS in the industry with up to 40% higher quality MIPS in relation to other 16-bit DSPs and comparable MIPS efficiency to 24-bit instruction DSPs. There are several reasons behind this. The combination of an enhanced Harvard architecture, parallel bus structure, and optimized core empowers a sophisticated instruction set, with many single cycle and parallel instructions.

Parallelism of the CPU is readily evident by inspection of the 'C54x internal hardware. The CPU employs a non-pipelined MAC (multiply accumulate) unit with a 17x17 multiplier and a dedicated adder. In addition, a 40-bit ALU can perform various arithmetic or bit manipulation functions with the output connected to dual 40-bit accumulators. In general, multiple accumulators can contribute to improved coding efficiency by avoiding storage of intermediate results to memory. More importantly though, particular advantage of this feature is made by several of the signal processing instructions in which two accumulators function as destination registers for concurrent operations. For example, the square distance instruction (SQDST) uses the B accumulator as the destination for a vector difference calculation while the A accumulator keeps a running sum of prior differences.

Equally important as the CPU parallelism is having bus bandwidth to support multiple memory operands. The 'C54x has 4 sets of internal buses which can support 1 program fetch, 2 data memory reads, and 1 data memory write in a single cycle.

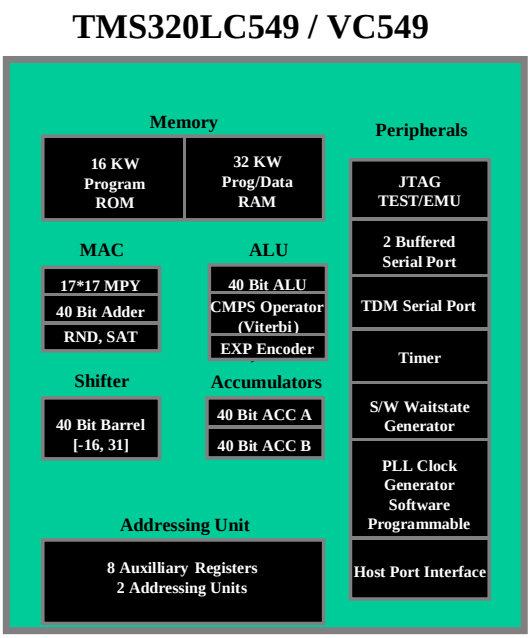
Other core highlights include:

- Split mode ALU which facilitates single cycle 32 bit sum or dual 16-bit sums (this feature is extremely useful in Viterbi decoder ACS butterfly calculations).
- H/W exponent detector which allows single cycle exponent encoding and single cycle mantissa normalization (this feature is useful in many vocoder applications).
- Non-pipelined MAC unit supporting single cycle 17-bit unsigned or 16-bit signed multiplication with or without rounding (rounding feature is advantageous for GSM applications).
- General purpose Compare, Select & Store Unit to facilitate Viterbi channel decode or MLSE equalization ACS buttefly calculations.
- Software stack implemented by Stack Pointer register (SP).
- Industry's most efficient fixed-point C Compiler may be used to speed development of less time critical functions.
- Extensive interrupt support in the form of 4 prioritized external interrupts, one non-maskable interrupt, and one reset interrupt. Interrupt processing is

directed by a software interrupt vector table and interrupts can be nested to any depth.

Figure 1 shows the block diagram for the TMS320LC549/VC549.

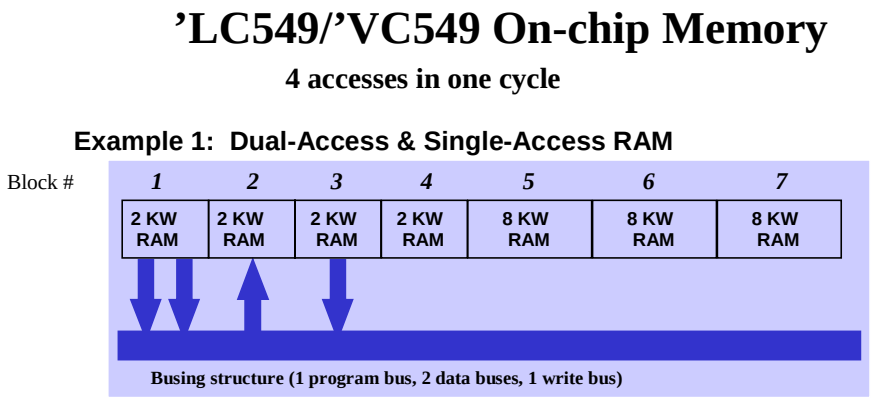
’C549: Power Efficient Performance



- **TMS320C54x CPU @ 66/80/100 MIPS**
- **66/80 MIPS performance @ 3.3V (’LC549)**
- **100 MIPS performance @ 2.5V (’VC549)**
- **32K words of on-chip SRAM consisting of:**
  - **8K x 16 bit Dual Access On-chip Program/Data RAM**
  - **24K x 16 bit Single Access On-chip Program/Data RAM**
- **16K x 16 bit Single Access On-chip ROM with boot code**
- **2 Auto-Buffered Serial Ports**
- **TDM Serial Port**
- **Host Port Interface**
- **Timer**
- **Extended Addressing**
- **Software programmable PLL**
- **Low Active Power Dissipation**
- **JTAG with Boundary Scan**
- **144 - pin TQFP (Thin Quad Flat Pack) and 144-BGA (Ball Grid Array) ;footprint compatible with the ’C542 and ’C548**

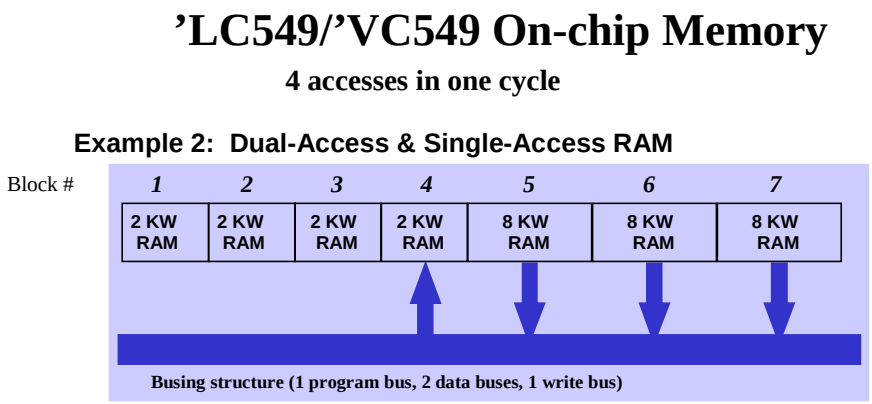
The ’LC549 at 3.3V and ’VC549 at 2.5V are very high performance 16-bit DSPs with a large integration of on-chip memory and peripherals. As you can see from figure 1, the ’LC549 has 32K words of on-chip RAM. 8K words of the on-chip RAM is dual-access RAM (broken into four 2K word blocks) and 24K words is single-access RAM (broken into three 8K word blocks). This memory integration, in conjunction with the advanced busing structure, allow 4 accesses in one cycle. The following two diagrams display just a couple of the numerous possibilities of the ’C549 architecture. Blocks 1,2,3, and 4 can each support 2 accesses in a single instruction cycle. Blocks 5,6, and 7 are 8K word blocks which allow 1 access per instruction cycle.

Figure 2



- 32K words total on-chip
- 1 program fetch from block 3
- 2 data reads from block 1
- 1 data write into block 2

Figure 3



- 32K words total on-chip
- 1 program fetch from block 7
- 1 data read from block 5
- 1 data read from block 6
- 1 data write into block 4

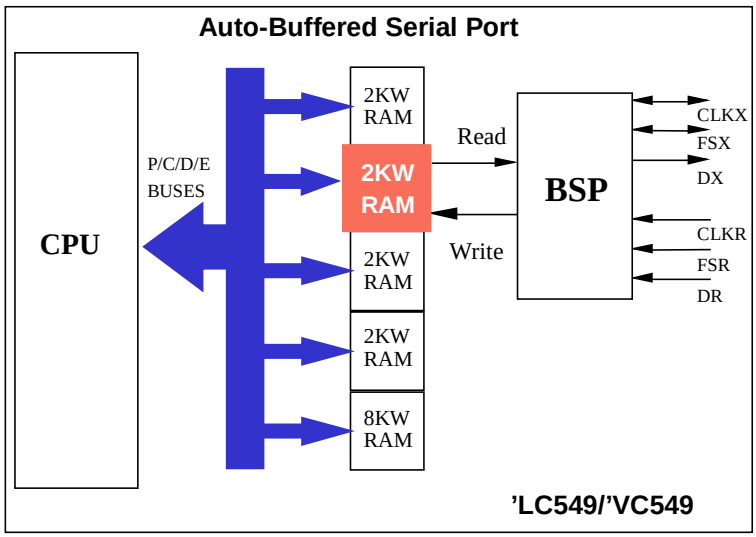
The previous examples are only a couple of the possibilities of utilizing the on-chip memory of the 'C549. It is important to note from the busing and memory examples above that the 'C549 does not suffer from the bandwidth problems that would affect many other architectures.

Up to this point, this document has shown how the core architecture of the 'C54x, the busing structure, and the large on-chip memory all collaborate to enable the 'C549 high quality of MIPS. A discussion on MIPS quality would not be complete

without the inclusion of the peripheral set. The ’C549 peripherals also greatly enhance MIPS quality.

Figure 4

Peripherals: BSP

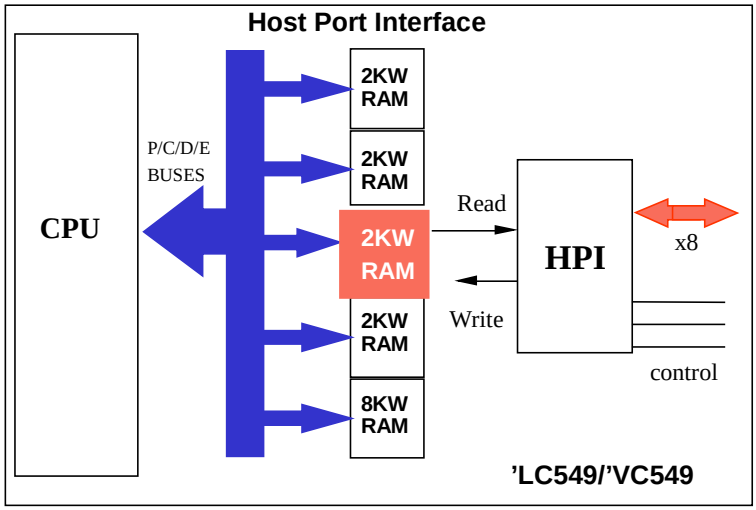


- ❖ **Superset of std serial port**
- ❖ **High speed data transfers**
- ❖ **Reduced interrupt latencies**
- ❖ **Read & Write to 2K words of RAM**
- ❖ **CPU not burdened**

The TMS320C549 has two buffered serial ports (BSPs). The diagram above demonstrates the operation of one of the two BSPs. Each BSP provides direct communication with serial A/D converters, codecs, and other serial devices with minimal hardware requirements. The BSP acts like a dedicated DMA channel. Both ’C549 BSPs have an extra feature which allows the detection of word mis-alignment in buffers. The BSP is a full-duplex, double-buffered serial port interface with an autobuffering unit (ABU). The autobuffering unit has its own set of circular addressing registers with corresponding address generation units. One of the 2K word blocks on the on-chip RAM can be dedicated to (or shared with) the BSP. As a result, data can be directly written to or ready from memory. This provides increased flexibility, improved data rates, and an unburdened CPU. The 2K word buffer can be accessed by the CPU at the same time due to the dual-access nature of the on-chip RAM. The throughput of the BSP is 50 Mbits/sec for a ’C549 running at 100 MIPS. Because the BSP operates independently of the CPU, the CPU can actually be placed into an IDLE mode while the BSP continues to operate and spool data into or out of on-chip memory.

Figure 5

Peripherals: HPI



- ❖ 8 bit parallel port
- ❖ Interfacing MCU
- ❖ Shared DARAM
  2K word memory
- ❖ SAM mode:
  - ➤ DSP and MCU
  - ➤ 64 MBps @ 40 MHz
- ❖ HOM mode:
  - ➤ DSP and MCU
  - ➤ 160 MBps @ 40 MHz
  - ➤ IDLE2

The Host Port Interface (HPI) is used to interface to a host processor (for example a microcontroller). It has an 8 line parallel bus adjoining a 2K word memory block and the external device. Similar to the BSP, the HPI has a dedicated bus into on-chip memory and can operate independent of the CPU. In this sense, it is another dedicated DMA channel. The HPI can operate in two modes: shared access mode (SAM) or host-only mode (HOM). In SAM mode, both the host and the 'C549 can access memory with asynchronous host accesses being resynchronized internally. If a conflict occurs, the CPU will wait. In this mode, the transfer rate is 64 Mbits/sec (or 8 Mbytes/sec). In the HOM mode, the host has unimpeded access to a 2K word memory block (a different block than is used by the BSP) and can input data while the CPU is in an IDLE state. The transfer rate for the HPI is 160 Mbits/sec (or 20 Mbytes/sec).

Other peripherals on the 'C549:

- TDM (Time Division Multiplexed) serial port can be configured as standard serial port where the transfer rate is ¼ of clockout or in multi-processing mode. Multi-processing is achieved by splitting the time frame into segments. This allows one 'C549 to interface to as many as 7 other 'C54x devices.
- Standard 16-bit timer
- Wait State Generator extends the external bus cycles up to 7. It is fully software programmable in order to interface to slower external memories

- Phase Locked Loop (PLL): The PLL allows the ’C549 to operate at a high on-chip frequency with a lower external frequency clock. The PLL is software programmable and has 31 different multiplier options ranging from x1/4 to x15.

Applications:

A useful way of segmenting the applications for the ’C549 is to look at three basic types:

’C54x Application Types

- Single channel / high performance: a single high performance algorithm or application (e.g. 40-50 MIPS algorithm on a 50 MIPS DSP)

- Channel stacking: ability to add more “channels” of a particular algorithm on 1 DSP (e.g. 32 channels of DTMF)

- Function stacking: ability to absorb functionality of multiple dedicated processors or ASICs into 1 DSP (e.g. 1 DSP does fax, data modem, telephony, audio algorithms simultaneously)

Often times, a processor’s MIPS numbers represent its “peak” performance. This is the performance of the processor given that all buses are used adequately, instructions and operands are in the correct memory locations, and slower off-chip accesses are minimized. Any instances of bus contention, memory bottlenecks, or ineffectual external accesses serve to decrease a processor’s quoted “peak” MIPS number. The resulting number of MIPS becomes a more realistic measure of a processor’s “sustained” performance. Because of the very high quality of MIPS on the ’C549, the “peak” performance MIPS numbers and the “sustained” performance MIPS numbers are nearly identical. This makes the ’C549 an excellent DSP for performance-enabling applications. These are applications where increased MIPS, larger amounts of on-chip memory, and intelligent peripherals are necessary to handle high performance applications in the wireless and wireline communications segments.

Channel stacking is a concept of adding more “channels” of a particular algorithm that was previously performed on multiple processors. Server line cards and

telecom switching equipment are examples where many channels of relatively simple algorithms (DTMF, echo cancellations, low level fax/modem code, etc.) can be handled by a single ’C549.

Function stacking is a system-cost reducing concept of combining the functionality and algorithms performed by multiple dedicated processors or ASICs into a single high performance, heavily integrated DSP, like the ’C549. Some applications use “fixed-function” processors that are cost-effective at handling a dedicated function. However, when several of these processors are used in conjunction with ASICs or FPGAs, it starts to make sense to integrate these into a single, high-performance ’C549 that has the MIPS and on-chip memory to accommodate the total application. The end-result is a decrease in board size, component cost, and system power.

The ’C549 has 23 address lines which allow for up to 8M address range for the program space. This enables many code modules and algorithms to be stored in low-cost, external, 8-bit EPROM. Different segments of code can be stored into the 32K words of on-chip SRAM and executed at the full-speed on the processor. This “reconfigurable” concept is useful for applications that require the use of multiple algorithms that must run zero wait-state. Algorithms can be loaded into on-chip memory when needed and discarded when it becomes necessary for the next algorithm to be loaded on-chip.

Power Dissipation:

One of the important design considerations for the ’C549 was low power dissipation.

As a result, there are multiple power reducing features on the ’C549. Several of these are listed below:

MECHANISMS TO LOWER POWER DISSIPATION ON THE ’C54x

- **Bus Keepers / Holders -- maintain state of ext. bus**
- **External Bus off control -- disables the external bus**
- **Static design - lower clock to DC**
- **IDLE 1, 2, 3 modes -- drop into various power down modes**
- **S/W PLL (31 options on C549)--use lower system clock**
- **MIPS efficiency -- fewer MIPS enables**

Active Core Power for the LC54x devices is, on average, .6 mA/MIPS while is is .45 mA/MIPS for VC54x devices.

The ’C54x incorporates 3 power down modes within its architecture: IDLE1, IDLE2, and IDLE3. These decrease power consumption when the CPU is not processing. The 3 power down modes have different degrees of power savings:

- IDLE1: core CPU shutdown, peripherals still active, 7.93 mA @ 3V/66MIPS
- IDLE2: core and peripherals shutdown, PLL still active, 2 mA @ 3V/66MIPS
- IDLE3: complete shutdown, <1 uA @ 3V/66MIPS

As the graphic shows, the ’C549 devices exhibit, on average, .6 mA/MIPS active core supply power. However, the true measure of power dissipation also takes into account the processor’s quality of MIPS.

THE TRUE MEASURE OF POWER DISSIPATION IS :

mA / MIPS

x

MIPS / algorithm

x

voltage

=

mW / algorithm

The typical power dissipation for ’C549 using on-chip resources (CPU and on-chip memory) is:

.45 mA/MIPS x 100 MIPS x 2.5V= 112.5 mW

Why is mW per function a more accurate measurement?

- mA/MIPS by itself disregards a processor’s quality of MIPS and the supply voltage
- a DSP’s power dissipation while performing the actual application or algorithm is the most accurate measurement
- if a DSP can complete a given task in fewer MIPS than another DSP, then it can get into IDLE mode sooner, thus lowering power dissipation even further.

The ’VC549 operates with a dual power supply to achieve superior power performance. The internal logic, including the CPU and all peripheral logic, is supplied with 2.5V, while the external logic is supplied with 3.3V. The dual-power supply allows the ’VC549 to maintain high performance at 100 MIPS, while achieving the lowest power dissipation possible.

Overall, the ’C549 has the high performance, large on-chip memory, and highly integrated peripheral set to meet the needs of a wide variety of wireless and wireline, data and voice, communications systems. In addition, the quality of the available MIPS and the ultra low power dissipation make the ’C549 a compelling choice for the ever demanding requirements of these systems.

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