Application Report
SPRA526

How to Begin Development Today With the TMS320VC33 DSP

Digital Signal Processing Solutions

Abstract

You can begin development now for the Texas instruments (TI™) TMS320VC33 digital signal processor (DSP) systems. Because of the compatibility between TMS320C3x generation devices, existing ‘C3x software tools and development platforms can be used to develop code for the ‘C33 and other future devices. This capability allows systems to be up and running when silicon becomes available.

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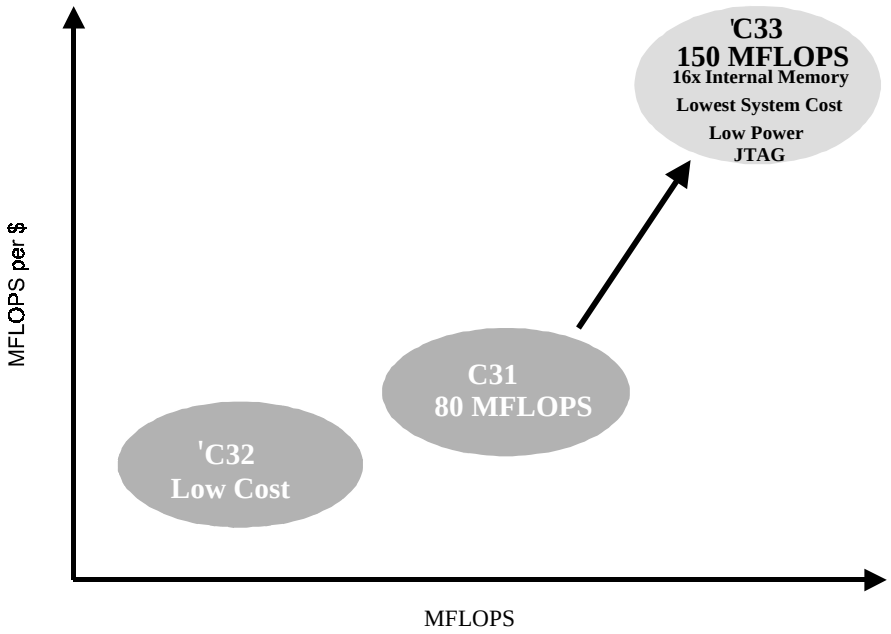
Introduction

The Texas Instruments TMS320C3x generation of low-cost floating-point digital signal processors (DSPs) now includes the TMS320C33. The ‘C33 is a low-cost version of the original ‘C31 floating-point device with 16x the internal memory and other added features targeted to reduce total system cost, power and ease of use. The ‘C33 provides up to 150 (MFLOPS) million floating-point operations per second at 150 MHz (75 MIPS). Samples are planned for fourth quarter 1999, with initial production starting in second quarter 2000.

The ‘C33 is the newest member of the popular ‘C3x family of low-cost and easy to use floating-point DSPs. Figure 1 shows the roadmap for ‘C3x family.

Figure 1. TMS320C3x Roadmap



TMS320C3x Compatibility

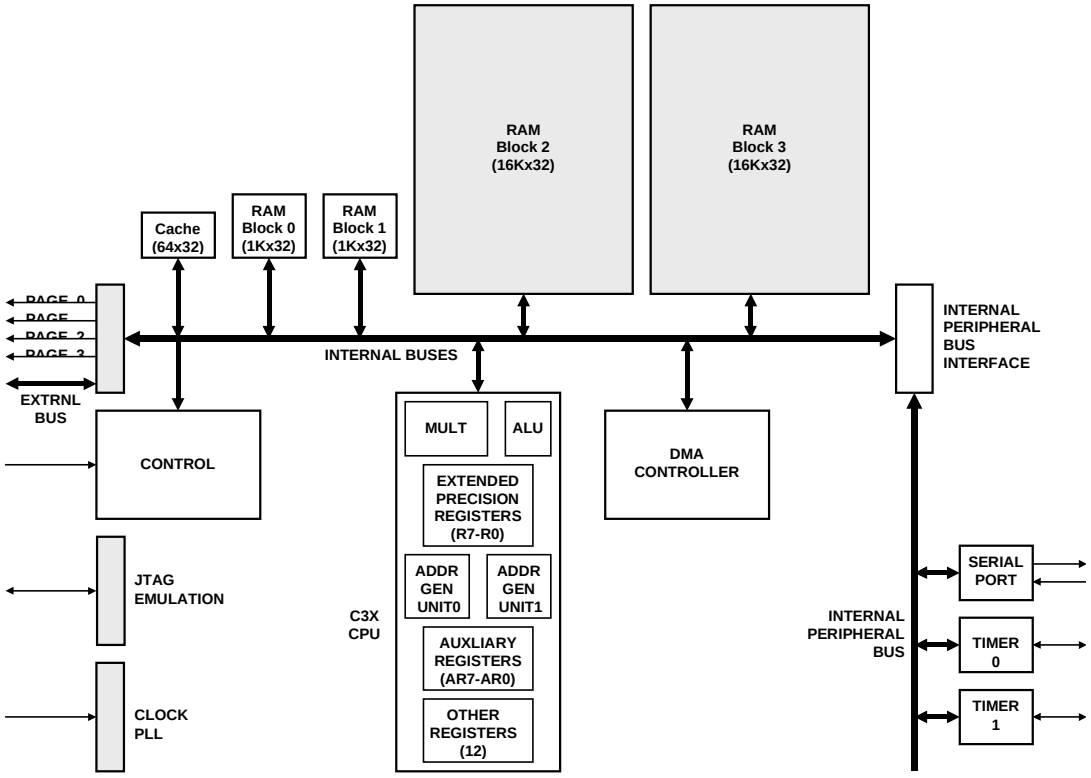
All ‘C3x generation devices are code-compatible with one another, except that some on-chip peripherals are available only on the ‘C32 member and a second external port and second serial port are available only on the ‘C30. All 'C3x devices are based on the same floating-point CPU that can also execute fixed-point instructions. The C3x CPU has register-based architecture with two address generation units and an efficient 32-bit wide instruction set.

In addition to standard ‘C3x features, the ‘C33 with a faster clock has increased the internal memory by 1 Mb (organized in two 16K x 32 blocks), with the original two 1K x 32 blocks remaining unchanged. The original MPSD emulation port on the ‘C31 has been replaced with the JTAG emulation port for faster emulation and multiprocessor debug capability. The power consumption has been reduced by an order of magnitude with a new process and 1.8-V internal and 3.3-V external voltage levels.

The common ‘C3x architecture allows designers to begin development with the existing ‘C3x software tools while the new derivatives are in development. This also allows migration from one ‘C3x processor to another, as design specifications require.

In addition to the CPU, all of the on-chip peripherals are common to the ‘C31 device. Figure 2 shows a block diagram of the ‘C33.

Figure 2. TMS320VC33 Digital Signal Processor



Note: The white blocks represent blocks shared between the ‘C31 and ‘C33. The gray blocks represent features new to the C33.

Similarities Between the TMS320C31 and TMS320VC31 DSPs

The ‘C33 is highly-compatible with one of the original ‘C31x derivatives—the ‘C31. The following device components are identical between the two devices:

- ‘C3x CPU
- Internal RAM0 and RAM1 blocks (1K x 32 bit each)
- 64 x 32-bit program cache
- One serial port
- Two 32-bit timers
- DMA controller
- Boot loader
- Four external interrupt inputs

Differences Between the TMS320C33 and TMS320C31 DSPs

The ‘C33 is available at a significantly lower cost than the original ‘C31, primarily through the 0.18-micron process and smaller package. The differences from the ‘C31 were driven by a requirement to further reduce system cost while improving system integration, performance improvement and ease of use. Differences include:

- **Faster clock rate**: The maximum clock frequency has been increased to 150 MHz. This translates to 75 MIPS and 150 MFLOPS.
- **16x increase in internal memory**: Two internal RAM blocks (16K x 32-bit each) were added to the two already existing (1K x 32-bit each) blocks, adding 1 Mb to the total internal memory space available to program or data. The architecture of new blocks permits simultaneous fetches of two 32-bit words in a single clock cycle.
- **New JTAG emulation port**: The new JTAG port will permit faster emulation of one or multiple ‘C33 devices in a single system. Other TI devices can be emulated with the same emulation hardware.
- **Internal clock PLL**: The new on-chip PLL (phase-locked loop) decreases system cost by allowing use of lower frequency input crystals or oscillators, despite the increase of internal machine cycle frequency.
- **Emulation:** The MPSD emulation port on the ‘C31 has been replaced with the JTAG port. The XDS 510 emulator still works. The MPSD cable must be replaced with the JTAG cable. TI will offer a special on the replacement cables when the samples are available.
- **External port:** The external port on the ‘C33 is a superset of the ‘C31 port. Four new PAGE output signals were added to identify the STRB signal as representing one of four predefined address pages. This feature removes the need for address decoding for cost-sensitive systems while increasing bus access time.
- **Dual power:** While the ‘C31 is a single voltage 5-V or 3.3-V device, the ‘C33 uses 1.8 V for the CPU/peripherals and 3.3 V for the I/Os. Thus, the overall power consumption has been drastically reduced.
- **Package:** Although the ‘C31 uses the 132-pin PQFP package, the initial ‘C33 will be offered in a 144-pin TQFP package. The additional pins represent the JTAG, four PAGE signals and dual power levels.
- **Clock PLL :** By using an on-chip PLL circuit, the ‘C33 can accept slower crystals and oscillators to clock the chip at up to twice the frequency of the ‘C31. The PLL divide ratio has not yet been finalized at this time.

Lowest System Cost

In addition to making the device even easier to use, the new features of the ‘C33 are primarily directed to further decrease cost of price-sensitive systems:

- The ‘C33 unit price has been reduced to $5.00 (in 100K quantities).
- The added 1-Mb internal memory decreases the system requirement on external memory and in many cases eliminates the external memory all together. Fewer external bus cycles also mean higher performance.

- Increased cycle speed may reduce the total number of DSPs necessary to support some applications that formerly required multiple ‘C31s.
- On-chip PLL circuit allows slower and less expensive crystals/oscillators to drive faster machine cycles.
- JTAG emulation port now requires only a single header to simultaneously emulate multiple DSPs.
- Page status signals reduce or eliminate decode glue logic components by signaling one of four address blocks with each external bus cycle strobe.
- Drastic reduction of power consumption per MIPS (60x reduction as compared to the 50-MHz ’C31) reduce total system power and cooling requirements.

Begin Writing Code for the TMS320C33 Today

The identical architectures of the ‘C33 and ‘C31 devices resolves many system-level issues prior to obtaining ‘C33 silicon. The high level of compatibility between the processors allows system development to begin now. By taking advantage of the existing ‘C3x software and hardware tools, ‘C33 systems have a running start at the time of silicon availability. The identical CPUs in the ‘C31 and ‘C33 devices allow code to be written for the ‘C33 using existing ‘C3x tools. ‘C31 code will require no modification to use on the ‘C33. All peripheral-specific code will also be able to run unchanged on the ‘C33. The ‘C3x compiler may be used for all members of the ‘C3x device platform. Code written for the ‘C31, ‘C32 or ‘C30 may be used by the ‘C33.

Code development for the ‘C33 may begin using the ‘C3x simulator. The simulator provides a cycle-accurate account of device. The simulator provides a good environment to learn the ‘C3x CPU and peripheral architecture. The peripherals on the ‘C33 are identical to those modeled by the current simulator.

For a development start in hardware, the ‘C3x evaluation module (EVM) may be used to understand the ‘C33 system level functionality. In this environment, floating-point code can be debugged while running in real time. All of the peripherals on the ‘C33 are identical to those of the ‘C31, so the EVM is a good tool to understand how to incorporate the peripherals into a real-time system.

In addition to the EVM, the low-cost C3x Design Starter Kit (DSK) can also be used for device familiarity and evaluation. Using these development platforms as well as the ‘C3x literature currently available will enable ‘C33 systems to be designed before ‘C33 silicon is made available.

TMS320C3x Tools Support

The ‘C3x tools are available now for use in all ‘C3x designs. The ‘C33 will be added to the development tools in early fourth quarter 1999. The following ‘C3x development tools are available today for the ‘C33:

- ‘C3x simulator software
- ‘C3x optimizing C compiler/assembler
- ‘C31 DSK

- TMS320C30 EVM
- XDS510 ‘C3x C source debugger software
- XDS510 emulator hardware with JTAG emulation cable
- Third-party hardware and software

Available TMS320C3x Literature

The following literature is available for the ‘C3x devices.

- *TMS320C3x User’s Guide*, literature number SPRU031
- *TMS320C3x General Purpose Applications Guide*, literature number SPRU194
- *TMS320C3x Programmer’s Guide*, literature number SPRU119
- *TMS320C3x Evaluation Module Reference Guide*, literature number SPRU069
- *TMS320C3x DSP Starter Kit Users Guide*, literature number SPRU163
- *TMS320C3x Digital Signal Processing Teaching Kit*, literature number *SPRP040*
- *TMS320C3x Assembly Language Tools User’s Guide*, literature number SPRA035
- *TMS320C3x Optimizing C Compiler User’s Guide*, literature number SPRU034
- *TMS320C3x C Source Debugger User’s Guide*, literature number SPRU053
- *JTAG/MPSD Emulation Technical Reference*, literature number SPDU079
- *TMS320C3x Simulator Getting Started*, literature number SPRU123
- *TMS320C31 Embedded Control*, literature number SPRU083
- *TMS320C3x Peripheral Control Library*, literature number SPRU086
- *TMS320C3x Digital Signal Processing Applications With the TMS320C30 Evaluation Module* Application Report, literature number SPRA021
- *Active Noise Control for Headphones Using the TMS320C3x DSP* Application Report, literature number SPRA160
- *EDRAM Memory Controller for the TMS320C31 DSP* Application Report, literature number SPRA172
- *How TMS320 Tools Interact With the TMS320C32's Enhanced Memory Interface* Application Report, literature number SPRA048
- *Booting a TMS320C32 Target System From a C Environment* Application Report, literature number SPRA067
- *Interfacing Memory to the TMS320C32 DSP* Application Report, literature number SPRA040
- *TMS320C3x DSP's Supercharge 3-D Graphics* Application Report, literature number SPRA024

- *Integrated Automotive Signal Processing and Audio System using the TMS320C3x* Application Report, literature number SPRA095

In addition to the existing ‘C3x application reports, three new ‘C33 specific application reports will be available prior to device sampling:

- *Memory Interface*
- *System Power Consumption*
- *Board Level Design Tips*

See http://www.ti.com/sc/docs/dsps/products/c3x/index.htm for more information.

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