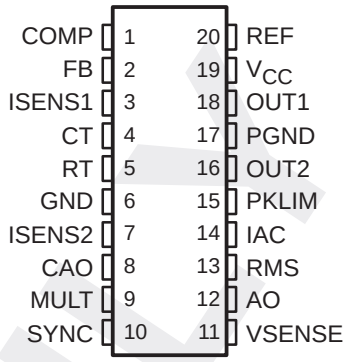
- **Single-Chip Solution for High-Power-Factor Switching Power Supply**
- **Current-Mode PWM Controller**
- **Fixed-Frequency Average-Current Power-Factor Corrector (PFC) Synchronized with PWM Controller**
- **Full Range ac Operation**
- **Low Start-Up Current**
- **Pulse-by-Pulse Current Limiting for PFC**
- **Undervoltage Lockout with Hysteresis**
- **Internally Trimmed Bandgap Reference**
- **External Synchronous Pin**
- **Overvoltage Protection for PFC**
- **Upper 8 Pins Configuration Same as UC3842**

N OR DW PACKAGE
(TOP VIEW)



description

The TLS1242 and TLS1244 are designed as optimal high-power-factor switching power supply systems with minimum external components. The current-mode PWM controller and the fixed-frequency average-current power-factor corrector (PFC) of each device are combined into a 20-pin DIP package. Internally implemented circuits include: undervoltage lockout (UVLO), featuring a low start-up current; a precision reference that can be trimmed for accuracy at the error amplifier input; a multiplier; two PWM comparators; overvoltage protection (OVP); and two totem-pole output stages designed to source or sink current. The output stage is suitable for driving n-channel MOSFETs, and is low when in the off state.

The fixed-frequency average-current-mode power-factor-correction controller circuit is synchronized with a current-mode PWM controller internally. Fixed-frequency power-factor correction helps prevent problems in frequency-sensitive applications such as video monitor, telecom, RF transmitters, and medical imaging. The synchronization of the PFC with the PWM controller helps reduce EMI problems as well.

The pin assignment of both the TLS1242 and the TLS1244 is intended to accommodate the UC3842/3844 as well, if PFC is not required in the application. The upper pins (1, 2, 3, 4, 17, 18, 19 and 20) have the same pin assignment as the UC3842, making the current-mode SPS application more flexible.

The PWM portion of the TLS1242 can operate to duty cycle approaching 100%. A duty cycle range of 0 to 50% is obtained using the TLS1244.

The TLS1242 and TLS1244 are characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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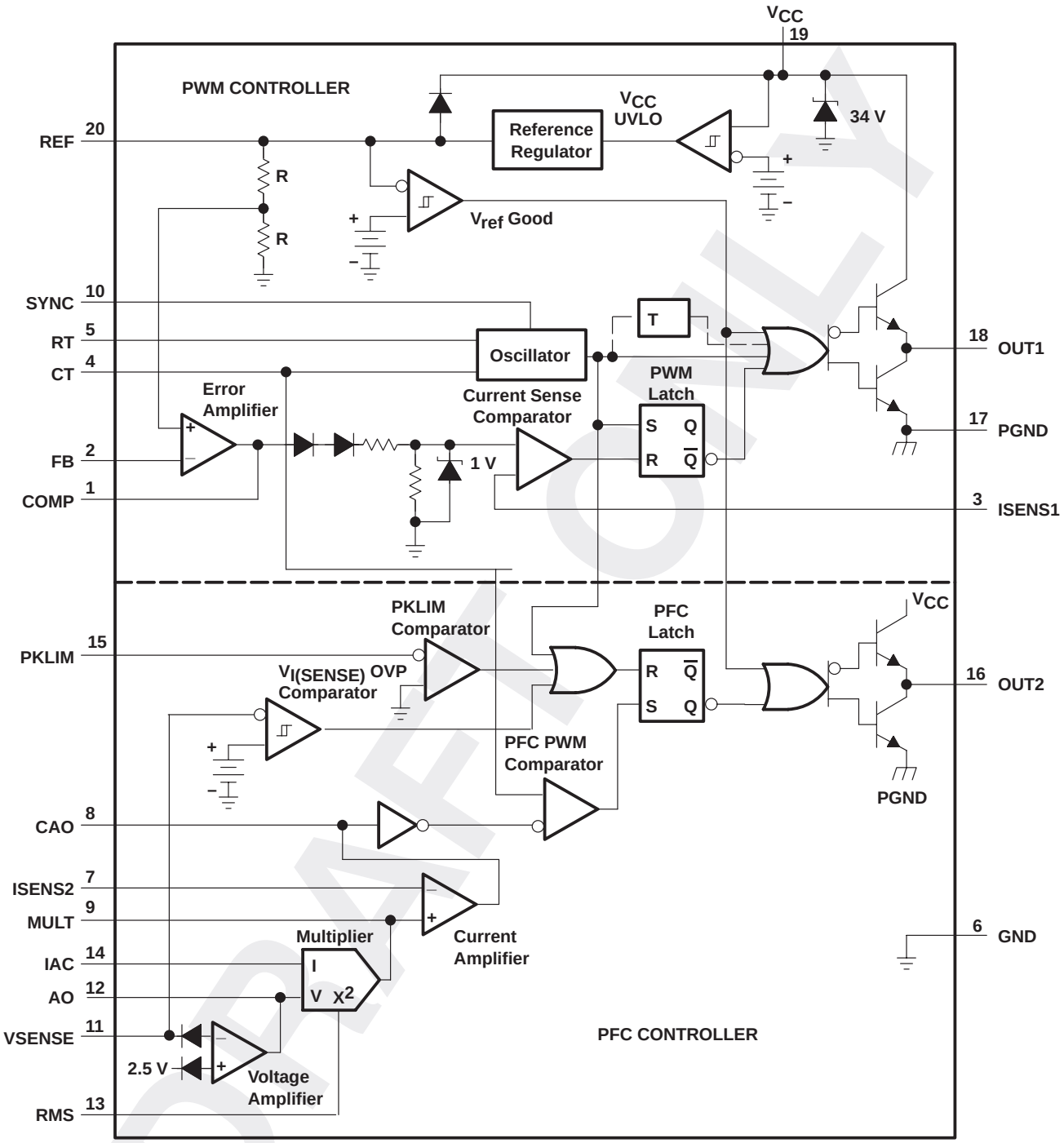
PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	12	Voltage amplifier output for frequency compensation
CAO	8	Current amplifier output for PFC
COMP	1	Error amplifier output for frequency compensation
CT	4	Oscillator timing control
FB	2	Error amplifier inverting input for PWM
GND	6	Control section ground
IAC	14	Current multiplier input
ISENS1	3	Input from current-sense device of PWM, connected to current-sense comparator
ISENS2	7	Input from current sense device of PFC, connected to current amplifier
MULT	9	Multiplier output
OUT1	18	Totem-pole output for PWM
OUT2	16	Totem-pole output for PFC
PGND	17	Output section ground
PKLIM	15	Peak current limit for PFC
REF	20	Output for the 5 V reference
RMS	13	Input for PFC rms line compensation
RT	5	Oscillator charge current control
SYNC	10	External synchronous signal input pin
V_{CC}	19	Positive supply
VSENSE	11	Voltage amplifier inverting input for PFC

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . Self-limiting
Analog input voltage range at FB, ISENS, VSENSE, RMS and PKLIM . . . . . 0.3 V to 6.3 V
Voltage at OUT1 and OUT2 . . . . . 30 V
Supply current, I_{CC} . . . . . TBD
Amplifier output sink current . . . . . 10 mA
Continuous total power dissipation . . . . . See dissipation rating table
Operation free-air temperature range, T_A . . . . . 0°C to 70°C

NOTE 1: All voltages are with respect to GND. Maximum package power dissipation limits must be observed.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1874 mW	15 mW/°C	1200 mW	975 mW
DW	1430 mW	11.4 mW/°C	915 mW	744 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			20	V
Input voltage at C_T input	0		5.5	V
Input voltage at FB, ISENS, VSENSE, RMS, SYNC and PKLIM	–0.3		5.5	V
Voltage on output	0		20	V
Supply current, externally limited, I_{CC}		2.5		mA
Average output current, I_O			200	mA
Reference output current			–20	mA
Timing capacitor, C_T	1	2.2		nF
Oscillator frequency		100	200	kHz
Operating free-air temperature, T_A	0		70	°C
Input current at IAC			750	μA

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (see Note 3), RT = 47 kΩ, CT = 2.2 nF, PKLIM = 1 V, RMS = 1.5 V, IAC = 100 μA, ISENS = 0 V, CAO = 4 V, AO = 3.5 V, VSENSE = 3 V, T_A = full range (unless otherwise specified)

reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	I_O = 1 mA, T_A = 25°C	4.95	5	5.05	V
Line regulation	V_{CC} = 12 V to 20 V		6	20	mV
Load regulation	I_O = 1 mA to 20 mA		6	25	mV
Temperature coefficient of output voltage			0.2	0.4	mV/°C
Output voltage, worst-case variation	V_{CC} = 12 V to 20 V, I_O = 1 mA to 20 mA	4.9		5.1	V
Output noise voltage	f = 10 Hz to 10 kHz, T_A = 25°C		50	100	μV
Output voltage, long-term drift	After 1000 at T_A = 125°C		5	25	mV
Short-circuit output current		–30	–100	–180	mA

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator frequency	T_A = 125°C	43	48	53	kHz
Frequency change with supply voltage	V_{CC} = 12 V to 20 V		1%	2%	
Frequency change with temperature	T_A = 0°C to 70°C		1%		
Peak-to-peak amplitude voltage at CT			4.6		V
Valley-point voltage	T_A = 25°C	1.15		1.65	V

current sense comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage amplification	See Note 2, See Note 3	2.85	3	3.15	V/V
Current-sense comparator threshold voltage	COMP at 5 V, See Note 2	0.9	1	1.1	V
Supply voltage rejection ratio	V_{CC} = 12 V to 20 V, See Note 2		70		dB
Input bias current			–2	–10	μA
Delay time to output			150	300	ns

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (see Note 2), RT = 47 kΩ, CT = 2.2 nF, PKLIM = 1 V, RMS = 1.5 V, IAC = 100 μA, ISENS = 0 V, CAO = 4 V, AO = 3.5 V, VSENSE = 3 V, T_A = full range (unless otherwise specified)

comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVP threshold voltage		2.6	2.7	2.8	V
OVP hysteresis voltage		80	115	150	mV
Threshold voltage, PKLIM		–0.2	0	0.2	V
Delay to OUT2, PKLIM	VSENSE < 2.5 V, See Note 4		150	300	ns

voltage amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	AO at 2.5 V	2.42		2.58	V
Bias current, VSENSE	VSENSE = 2.5 V	–500	–25	500	nA
Open-loop voltage amplification	V_O = 2 V to 6 V	70	100		dB
Gain-bandwidth product	f_I = 100 kHz, 10 mV $V_{O(PP)}$, See Note 4	0.7	1		MHz
Supply-voltage rejection ratio	V_{CC} = 12 V to 20 V	60	70		dB
Output short-circuit current	V_O = 0 V		–1.5	–3.5	mA
High-level output voltage	I_L = –500 μA	5	6		V
Low-level output voltage	I_L = 500 μA		0.7	1.1	V

current amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	$V_{I(CM)}$ = 0 V	–2		2	mV
Input bias current	$V_{I(CM)}$ = 0 V	–500		500	nA
Open-loop voltage amplification	$V_{I(CM)}$ = 0 V, V_O = 2 V to 6 V	80	110		dB
Gain-bandwidth product	f_I = 100 kHz, 10 mV $V_{O(PP)}$, See Note 4	1	3		MHz
Supply-voltage rejection ratio	V_{CC} = 12 V to 20 V	60	70		dB
Output short-circuit current	V_O = 0 V		–1.5	–3.5	mA
High-level output voltage	I_L = –500 μA	5	6		V
Low-level output voltage	I_L = 500 μA		0.7	1.1	V

multiplier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current , IAC limited	IAC = 100 μA, RMS = 1 V	–220	–200	–170	μA
Output current, zero	IAC = 0 μA	–2	–0.2	2	μA
Output current, power limited	RMS = 1.5 V, AO = 6 V	–220	–200	–170	μA
Output current	RMS = 1.5 V, AO = 5 V		–156		μA
	RMS = 1.5 V, AO = 2 V		–22		
	RMS = 5 V, AO = 5 V		–14		
	RMS = 5 V, AO = 2 V		–2		
Gain constant	RMS = 1.5 V, AO = 6 V, See Note 5	–1.1	–1	–0.9	A/A

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (see Note 3), RT = 47 kΩ, CT = 2.2 nF, PKLIM = 1 V, RMS = 1.5 V, IAC = 100 μA, ISENS = 0 V, CAO = 4 V, AO = 3.5 V, VSENSE = 3 V, T_A = full range (unless otherwise specified)

error amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Feedback input voltage	COMP = 2.5 V	2.42		2.58	V
Input bias current	FB = 2.5 V		–0.3	–2	μA
Open-loop voltage amplification	V_O = 2 V to 4 V	65	90		dB
Gain-bandwidth product	f_I = 100 kHz, 10 mV $V_{O(PP)}$, See Note 4	0.7	1		MHz
Supply-voltage rejection ratio	V_{CC} = 12 V to 20 V	60	70		dB
Output sink current	FB at 2.7 V, COMP AT 1.1 V	2	6		mA
Output source current	FB at 2.3 V, COMP AT 5 V	–0.5	–0.8		mA
High-level output voltage	FB at 2.3 V, R_L = 15 kΩ to GND	5	6		V
Low-level output voltage	FB at 2.7 V, R_L = 15 kΩ to REF		0.7	1.1	V

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up threshold voltage		14.5	16	17.5	V
Minimum operating voltage after start-up		8.5	10	11.5	V

output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	I_{OH} = –20 mA	13	13.5		V
	I_{OH} = –200 mA	12	13.5		
Low-level output voltage	I_{OL} = 20 mA		0.2	0.4	V
	I_{OL} = 200 mA		1	2.2	
Rise time	C_L = 1 nF, T_A = 25°C		50	150	ns
Fall time	C_L = 1 nF, T_A = 25°C		50	150	ns

pulse-width-modulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum duty cycle		93%	95%		
Minimum duty cycle				0	

supply voltage

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up current			0.7	1.1	mA
Operating supply current	FB and ISENS and IAC at 0 V			30	mA
Limiting voltage	I_{CC} = 25 mA		34		V

NOTES: 2. Adjust V_{CC} above the start threshold before setting it to 15 V.
3. These parameters are measured at the trip point of the latch with FB at 0 V.
4. Voltage amplification is measured between the input at ISENS1 and the output at COMP with the input changing from 0 V to 0.8 V.
5. Specified by design, not 100% tested in production
6. Gain constant (k) = $(I_{I(IAC)} \times [V_{I(AO)} – 1.5])/(V_{I(RMS)}^2 \times I_{I(MULT)})$

PARAMETER MEASUREMENT INFORMATION

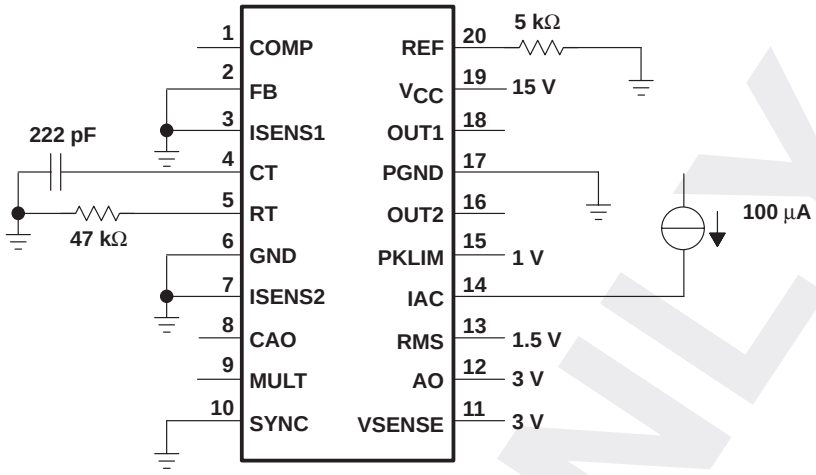
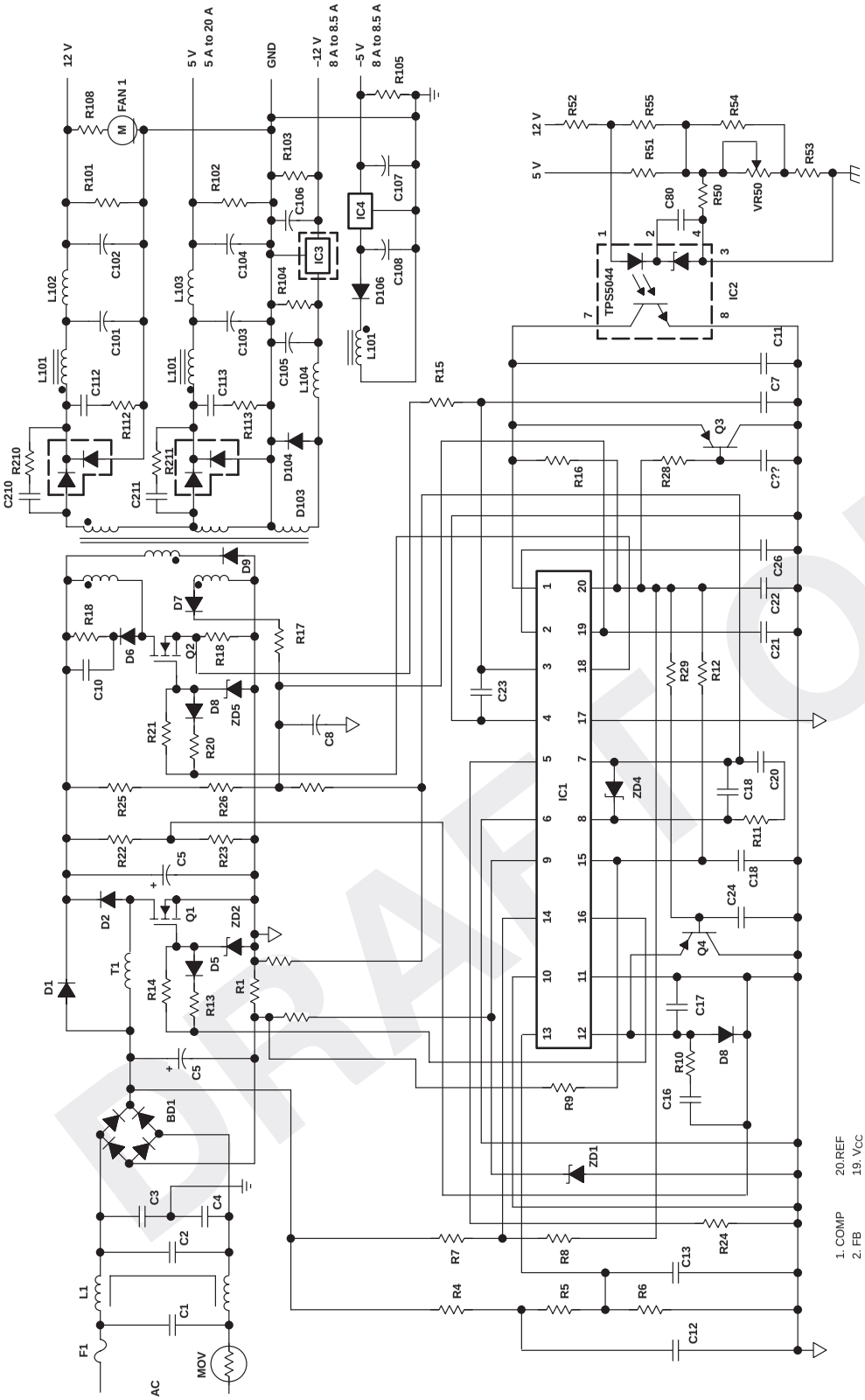


Figure 1. Test Circuit

APPLICATION CIRCUIT



NOTE: Recommended power MOSFET gate limit resistor, R13, R14, R20, R21 > 20Ω

Figure 2. Application Circuit, Forward

PRODUCT PREVIEW

APPLICATION CIRCUIT

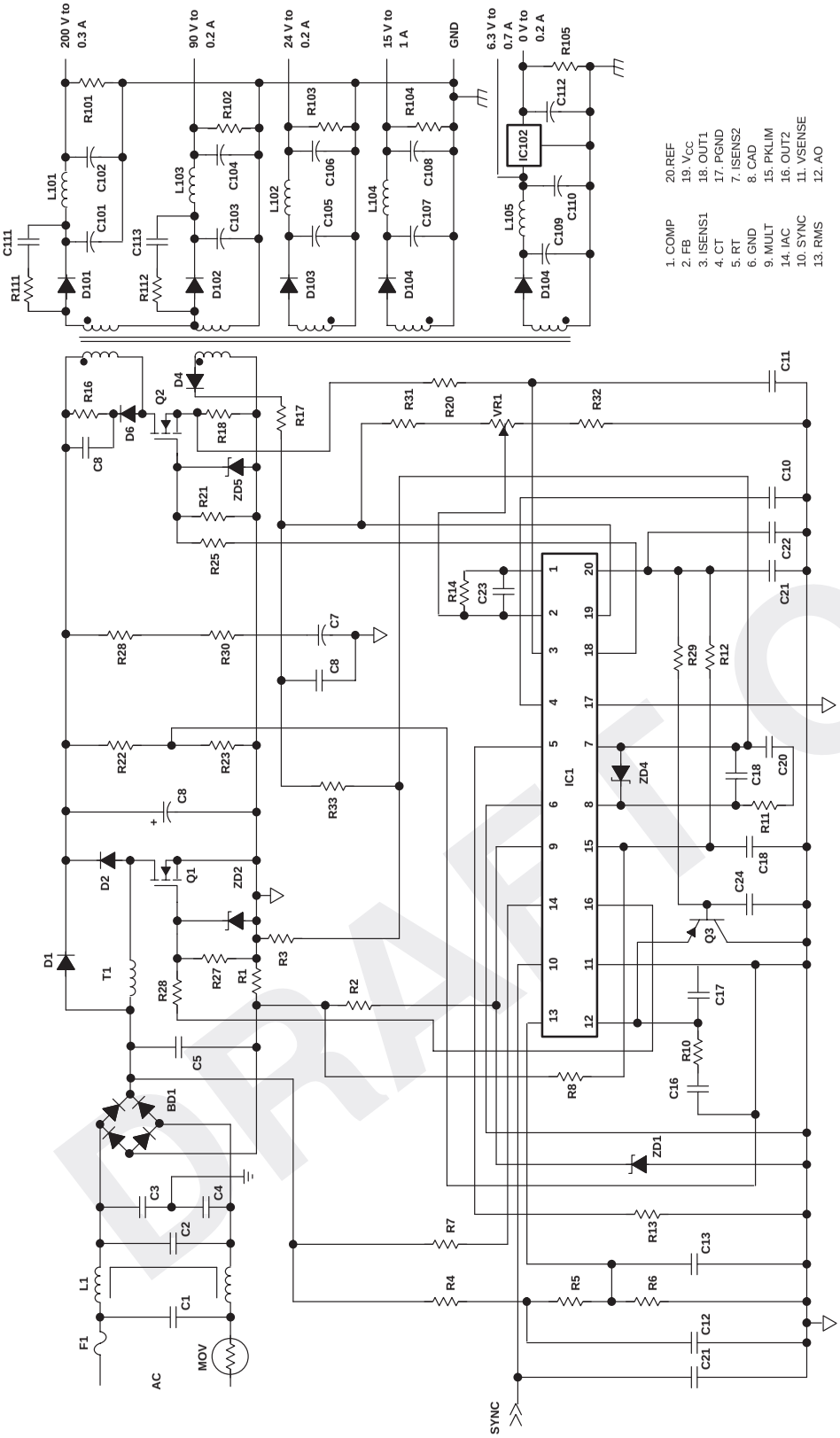


Figure 3. Application Circuit, Flyback

NOTE: Recommended power MOSFET gate limit resistor, R25, R26 > 20Ω

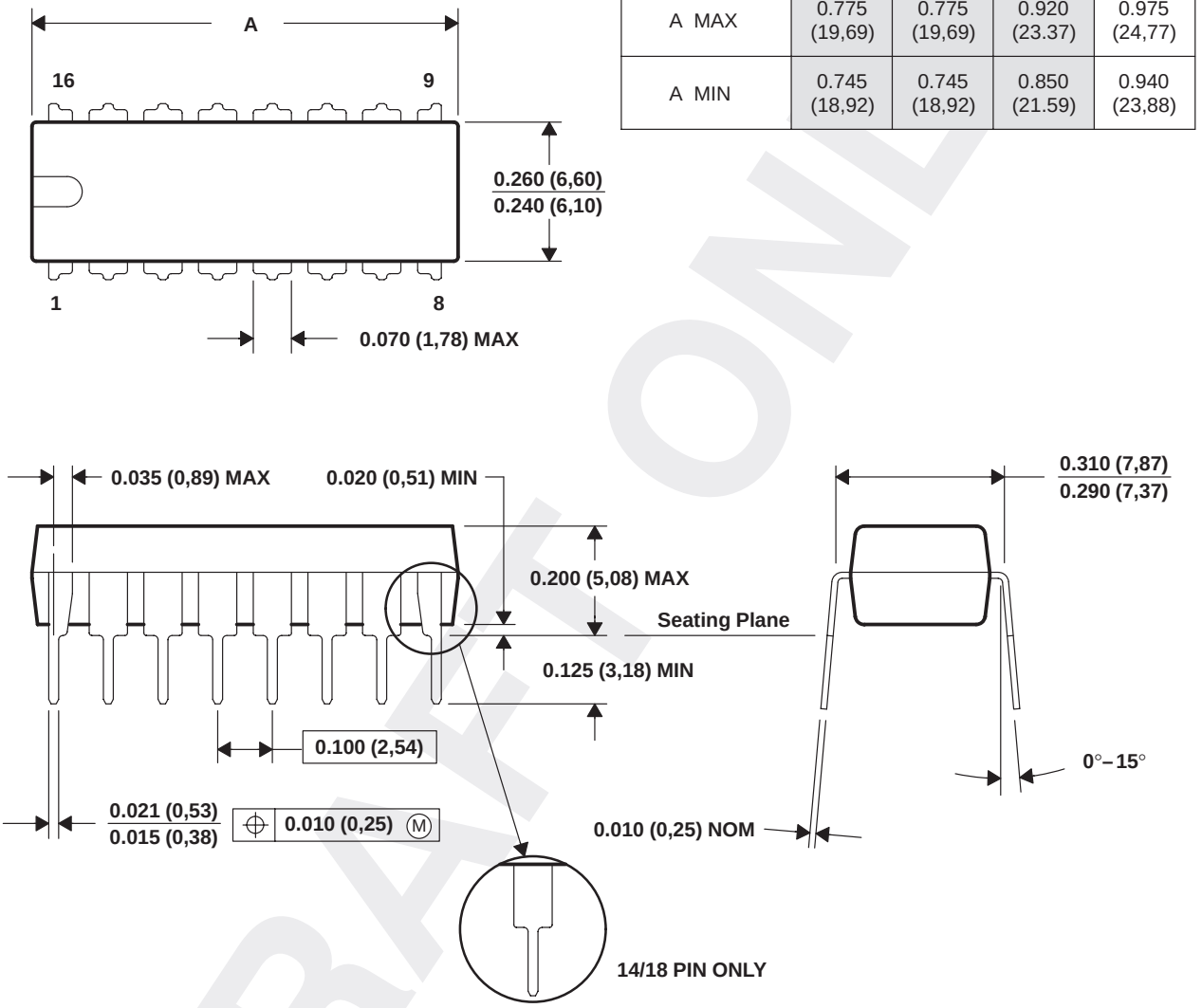
PRODUCT PREVIEW

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

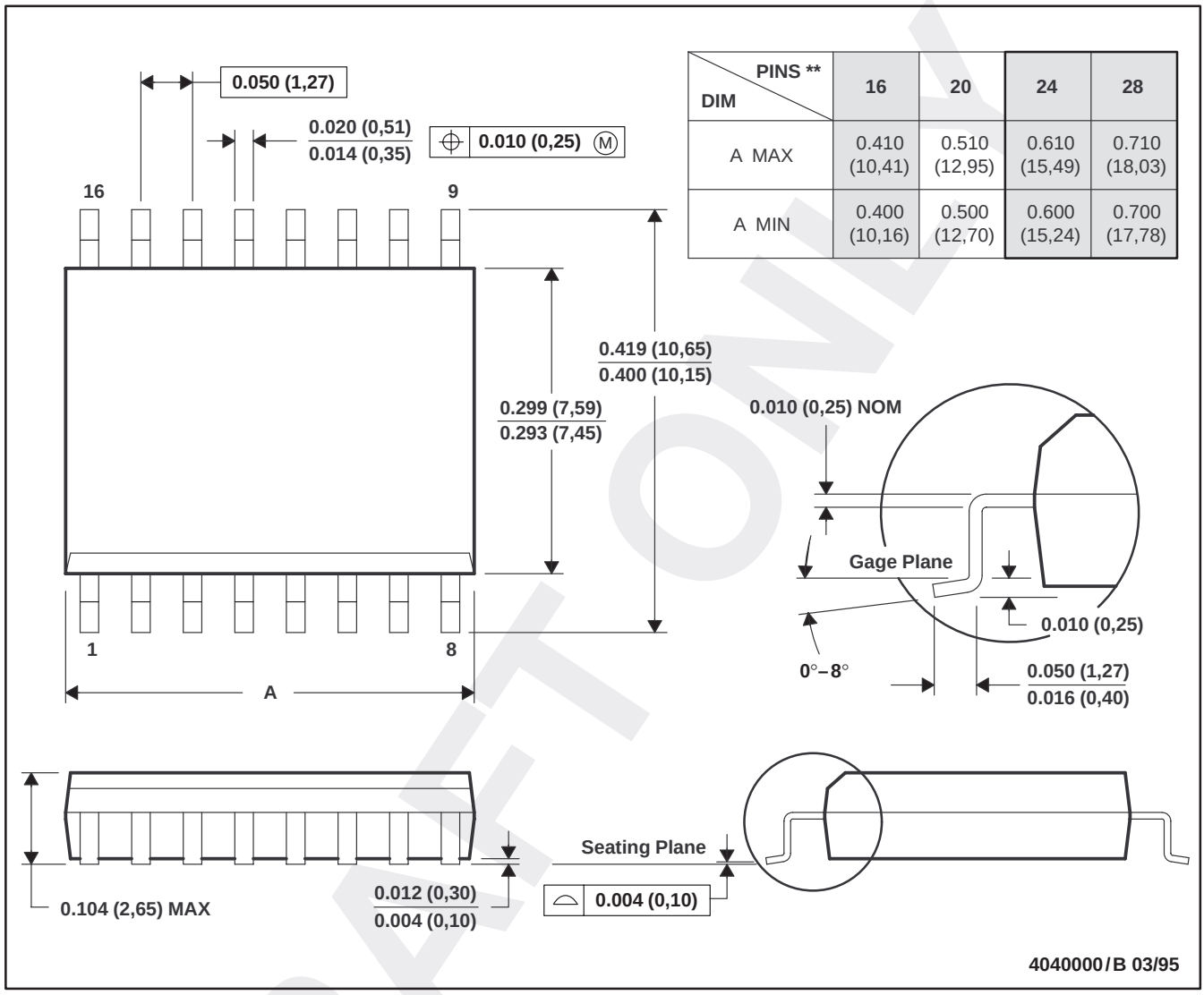


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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