- **Auto-Select V_{CC} and V_{PP} Voltages**
  - **2.7 V, 3.3 V, or 5 V Read Operation (V_{CC})**
  - **2.7 V, 3.3 V, 5 V, or 12 V Program Erase (V_{PP})**
- **Fast Read Access Time**
  - **5 V: 80/90 ns MAX**
  - **2.7 V, 3.3 V: 90/100 ns MAX**
- **Low Power Consumption (V_{CC} = 5.5V)**
  - **Active Write 220 mW (Byte Mode)†**
  - **Active Read 248 mW (Byte Mode)†**
  - **Active Write 220 mW (Word Mode)†**
  - **Active Read 248 mW (Word Mode)†**
  - **Block-Erase 220 mW†**
  - **Standby 0.55 mW**
  - **Deep Power-Down Mode 0.044 mW**
- **Automatic Power-Saving Mode**
- **Sector Architecture**
  - **One 16K-Byte Protected Boot Block**
  - **Two 8K-Byte Parameter Blocks**
  - **One 96K-Byte Main Block**
  - **Fifteen 128K-Byte Main Blocks**
  - **Top or Bottom Boot Locations**
- **User-Selectable x8 or x16 Operation**
- **Fully Automated On-Chip Erase and Byte/Word Program Operations**
- **All Inputs/Outputs TTL-Compatible**
- **Supports Concurrent Operations**
  - **Read During Program**
  - **Read During Erase**
  - **Program During Erase**
  - **Two-Byte/-Word Programming**
  - **Two Sector Combinations Erasure**
- **Enhanced Suspend Options**
  - **Sector-Erase-Suspend to Read**
  - **Sector-Erase-Suspend to Program**
  - **Program-Suspend to Read**
- **Command Set Compatible With Previous Generation of Flash**
- **Transition Between Single-Operation and Concurrent-Operations Mode by way of Software Command**
- **100000 Program/Erase Cycles Per Sector**
- **Hardware Write-Protection for Boot Block**
- **Two Temperature Ranges**
  - **Commercial 0°C to 70° C**
  - **Extended –40°C to 85° C**
- **Industry Standard Packaging (JEDEC)**
  - **48-Pin TSOP (DCD Suffix)**

PIN NOMENCLATURE	
$\overline{A0}$–A19	Address Inputs
$\overline{BYTE}$	Byte Enable
DQ0–DQ14	Data In/Data out
DQ15/A–1	Data In/Out (word-wide mode) Low Order Address (byte-wide mode)
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NC}$	No Internal Connection
$\overline{RP}$	Reset/Deep Power Down
V_{CC}	Power Supply
V_{PP}	Power Supply for Program/Erase
V_{SS}	Ground
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect

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description

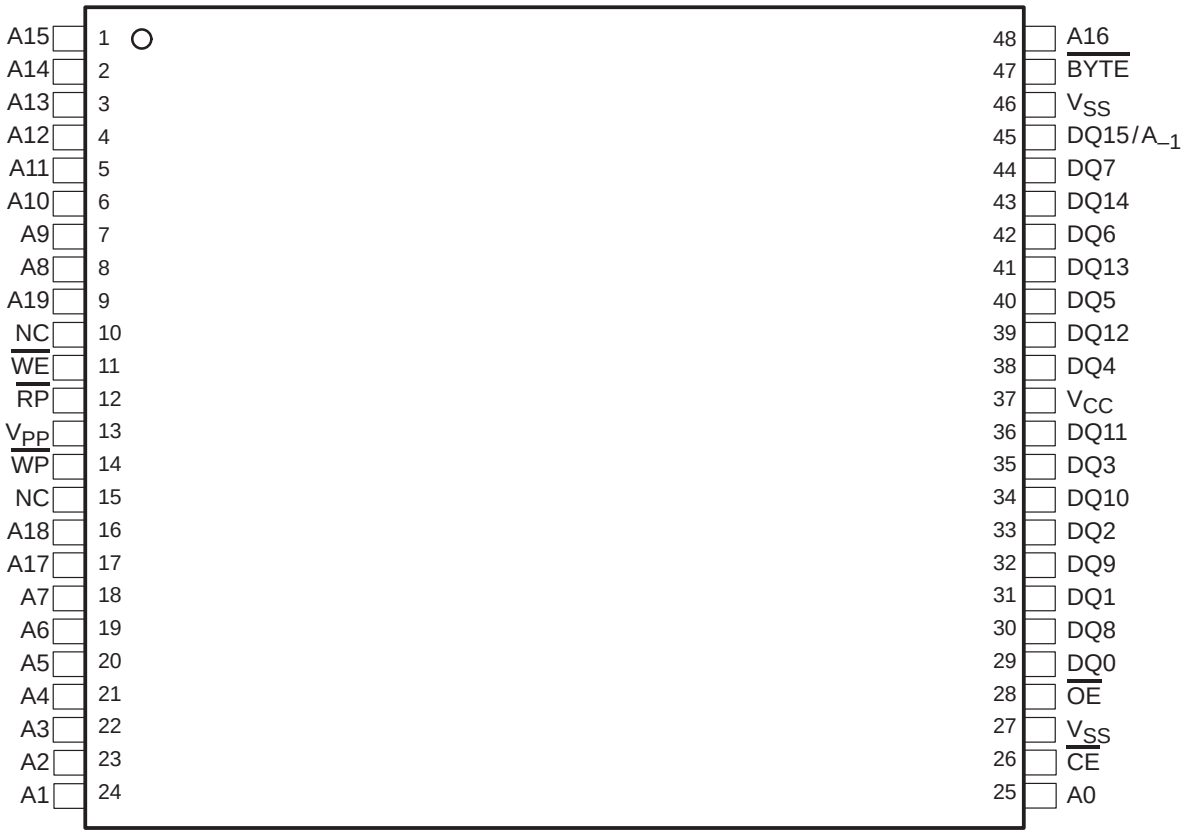
The TMS28F1600T/B is a 16777216-bit, boot-block flash memory that can be electrically block-erased and reprogrammed. The TMS28F1600T/B is organized in a sectored architecture consisting of one 16K-byte protected boot sector, two 8K-byte parameter sectors, one 96K-byte main sector, and fifteen 128K-byte main sectors. Operation as a 2M-byte (8-bit) or a 1M-word (16-bit) organization is user-selectable.

Embedded program and block-erase functions are fully automated by two on-chip write state machines (WSMs), simplifying these operations and relieving the system microcontroller of these secondary tasks. WSM statuses can be monitored by two on-chip status registers, one for each WSM, to determine progress of program/erase tasks.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† In single-operation mode

TMS28F1600T/B
48-PIN TSOP (DCD)
(TOP VIEW)



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description (continued)

The ’28F1600 has the auto-select feature that allows the user alternative read and program/erase voltages for maximum flexibility. Memory reads can be performed using V_{CC} = 2.7 or 3.3 V for optimum power consumption or at V_{CC} = 5 V for device performance. Erasing or programming the device can be accomplished with V_{PP} = 2.7 V, 3.3 V, or 5 V which eliminates having to use a 12-V source and/or in-system voltage converters. Alternatively, 12-V V_{PP} operation exists for systems that already have a 12-V power supply.

device symbol nomenclature

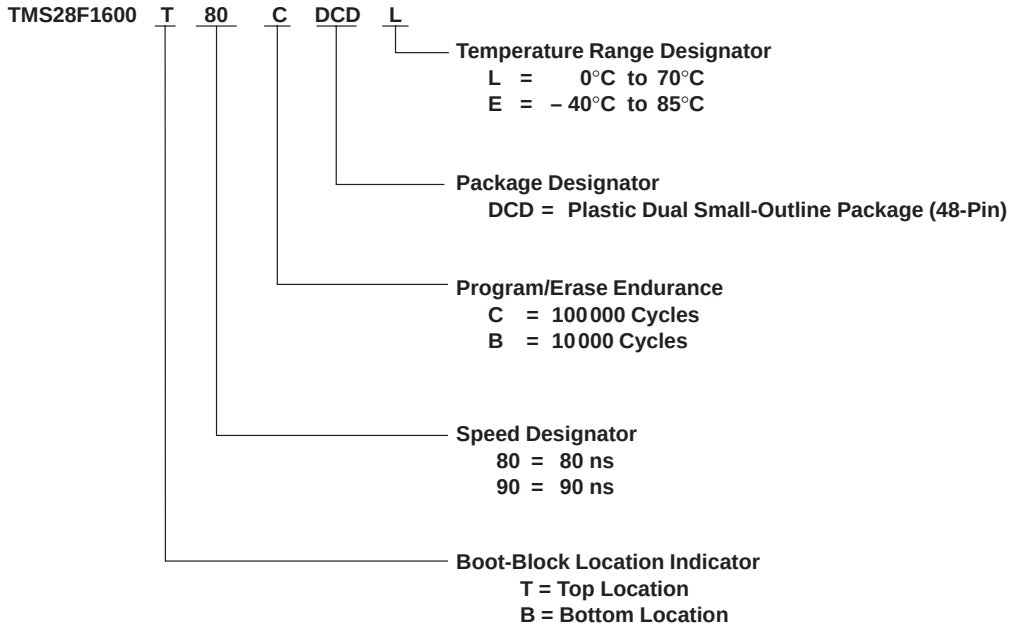

Table 1. V_{CC}/V_{PP} Voltage Configurations†

DEVICE CONFIGURATION	READ VOLTAGE (V_{CC})	PROGRAM/ERASE VOLTAGE (V_{PP})
TMS28F1600T	2.7 V to 3.6 V, 5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%
TMS28F1600B	2.7 V to 3.6 V, 5 V ± 10 %	3 V/5 V ± 10% or 12 V ± 5%

† 3-V range indicates 2.7 V to 3.6 V maximum.

architecture

The TMS28F1600T/B uses a sectored architecture to allow independent erasure of selected memory blocks. The sector to be erased is selected by using any valid address within that sector.

The TMS28F1600T/B has two (2) memory banks. Bank A consists of:

- One 16K-byte protected boot sector
- Two 8K-byte parameter sectors
- One 96K-byte main sector and
- Seven 128K-byte main sectors

and bank B consists of:

- Eight 128K-byte main sectors

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architecture (continued)

Embedded program and block-erase functions for each memory bank are fully automated by a separate and independent WSM. With two WSMs, each controlling one memory bank (8M bits of memory space), the overall system performance is greatly improved by allowing the device to be programmed/erased in one bank while simultaneously reading data from another sector of the other memory bank. The device also can be erased/programmed in one sector of one memory bank while simultaneously erased/programmed in another sector of the other memory bank.

Within each bank, the suspend command can be used to suspend the erase operation to read from or program data to another sector not being erased. The suspend command can be used also to suspend the program operation so that data from any address location other than the one being programmed can be read.

The TMS28F1600 is available with the sector architecture mapped with the boot block located at the top (TMS28F1600T) or at the bottom (TMS28F1600B) of the memory array, as required by different microprocessors. The bottom boot block is mapped with the 16K-byte boot block located at the low-order address range (00000h to 01FFFh, word mode). The top boot block is mapped with the 16K-byte boot block located at the high-order address range (FFFFFh to FE000h, word mode). Figure 1 and Figure 2 show the memory maps for the top and bottom boot block configuration, respectively.

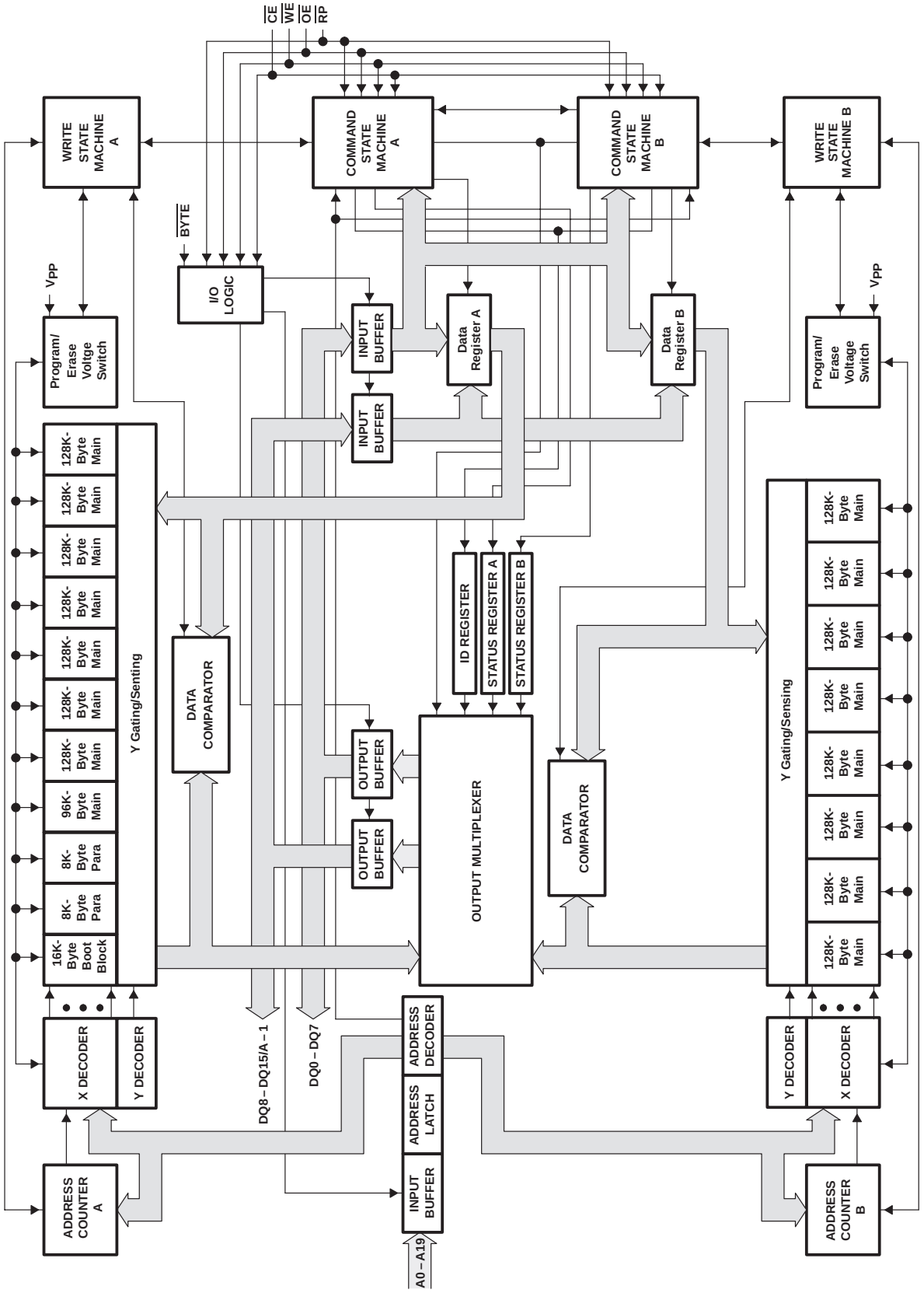
boot-sector data protection

The 16K-byte boot block can be used to store key system data that is seldom changed in normal operation. Data in this block can be protected by using different combinations of the reset/power-down pin ($\overline{RP}$), the write protect pin ($\overline{WP}$) and VPP supply levels. See Table 2 for a listing of these combinations.

Table 2. Data Protection Combinations

DATA PROTECTION PROVIDED	V_{PP}	$\overline{RP}$	$\overline{WP}$
All sectors locked	$\leq V_{PPLK}$	X	X
All sectors locked (reset)	X	V_{IL}	X
All sectors unlocked	$\geq V_{PPLK}$	V_{HH}	X
	$\geq V_{PPLK}$	V_{IH}	V_{IH}
Only boot block locked	$\geq V_{PPLK}$	V_{IH}	V_{IL}

functional block diagram



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parameter sector

Two parameter sectors of 8K bytes each can be used like a scratch pad to store frequently updated data. Alternatively, the parameter sectors can be used for additional boot or main-sector data. If a parameter sector is used to store additional boot-block data, caution should be exercised because the parameter sector does not have the boot-block data protection safety feature.

main sector

Primary memory on the TMS28F1600T/B is located in sixteen main sectors. Fifteen of the sectors have storage capacity for 128K-bytes and the remaining sector has storage capacity of 96K bytes.

main sector (continued)

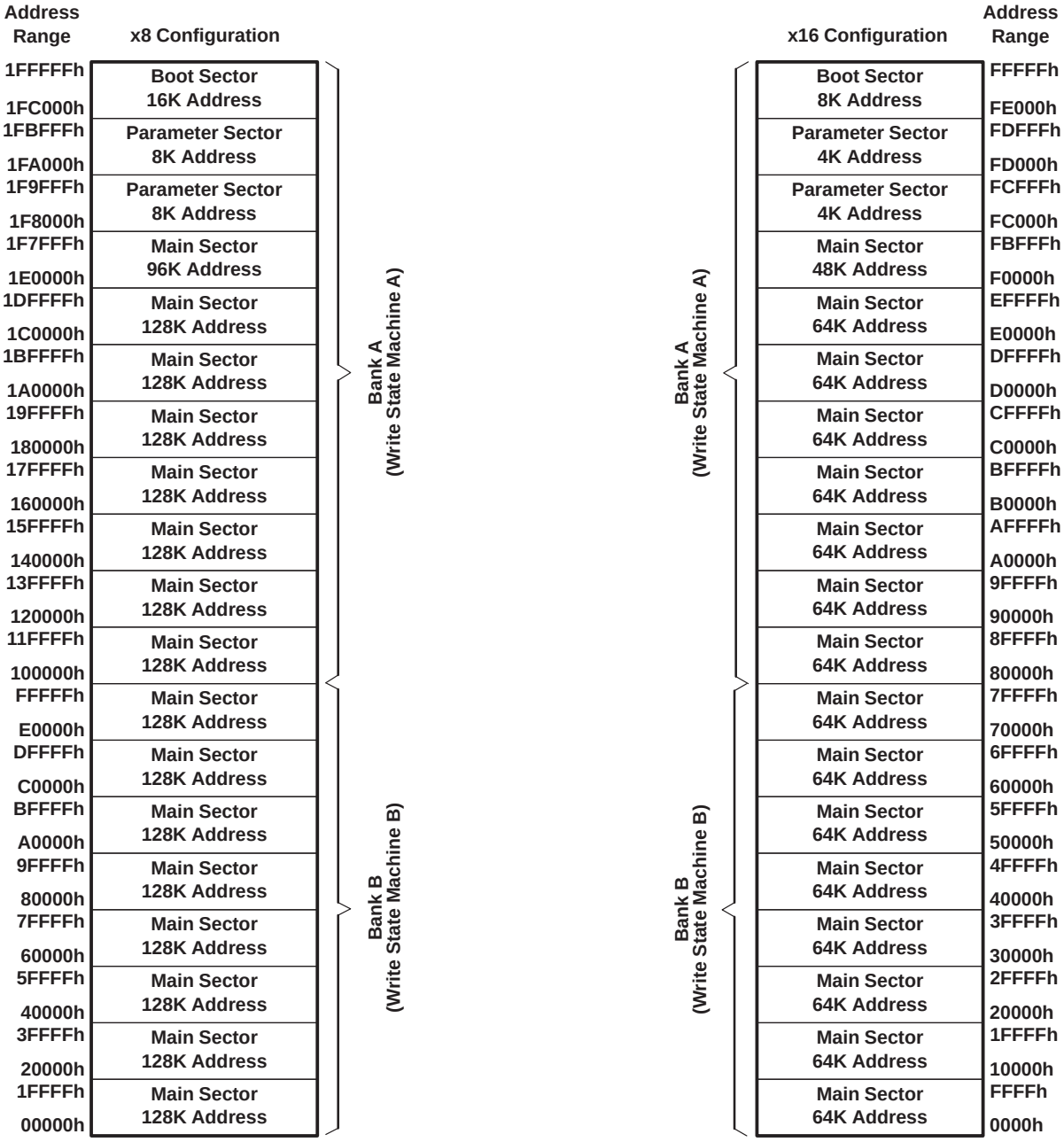

Figure 1. TMS28F1600T (Top Boot Sector) Memory Map

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main sector (continued)

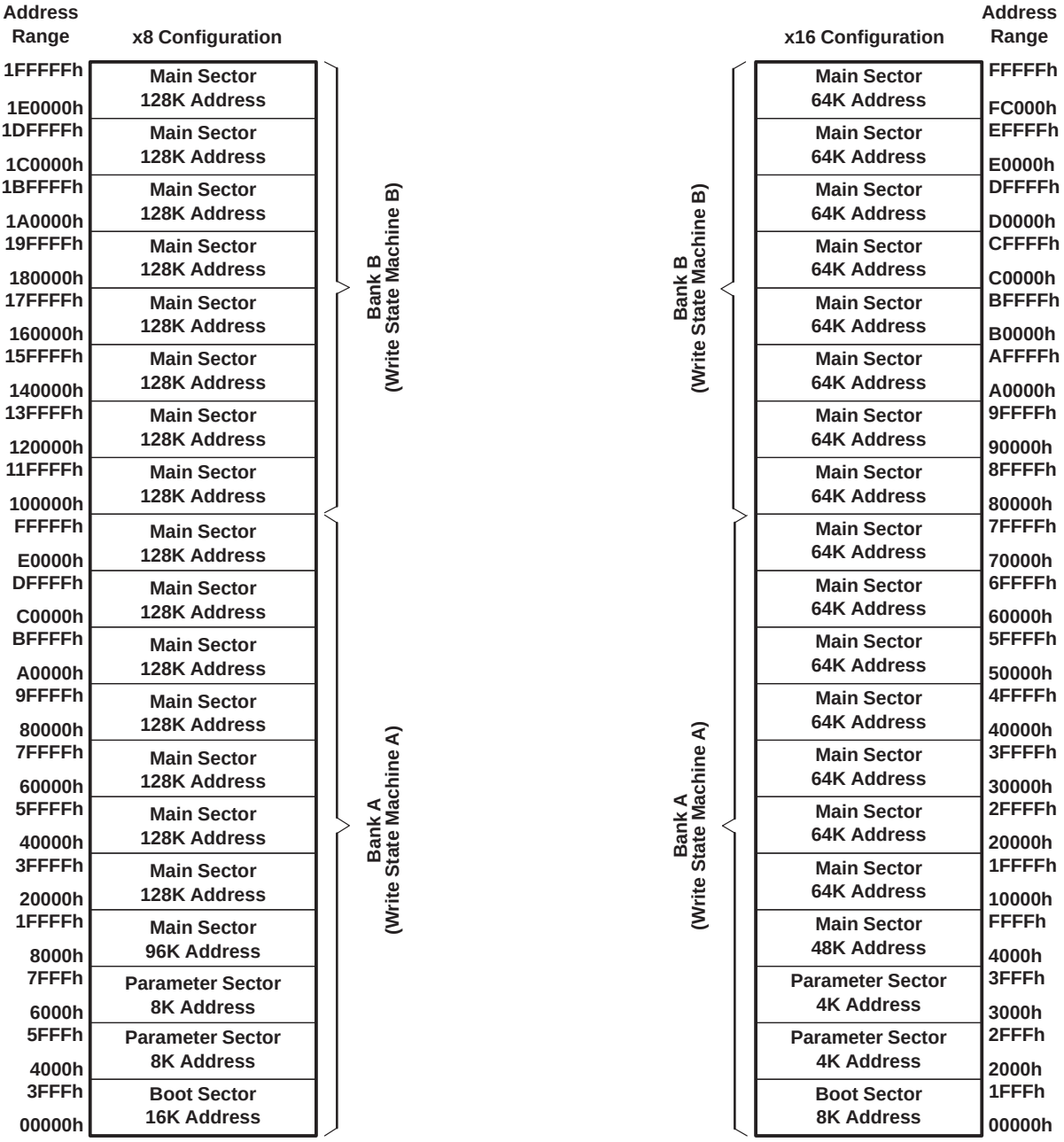

Figure 2. TMS28F1600B (Bottom Boot Sector) Memory Map

data protection

Data is secured or unsecured by using different combinations of the reset/power-down pin ($\overline{RP}$), the write protect pin ($\overline{WP}$) and V_{PP} supply levels. Table 2 lists these combinations.

There are two ways to secure the entire memory against inadvertent alteration of data. The V_{PP} supply pin can be held below the V_{PP} lock-out voltage level (V_{PPLK}) or the reset/deep power-down pin ($\overline{RP}$) can be pulled to a logic-low level. Note that if $\overline{RP}$ is held low, the device resets, which means it powers down and, therefore, cannot be read. Typically, this pin is tied to the system reset for additional protection during system power up.

The boot sector has an additional security feature through the $\overline{WP}$ pin. When the $\overline{RP}$ pin is at logic-high level, the $\overline{WP}$ pin controls whether the boot sector is protected. When $\overline{WP}$ is held at logic-low level, the boot sector is protected. When $\overline{WP}$ is held at logic-high level, the boot sector is unprotected along with the rest of the other sectors. Alternatively, the entire memory can be unprotected by pulling the $\overline{RP}$ pin to V_{HH} (12 V).

command state machine (CSM)

There are two CSMs and each is corresponded to one WSM. The CSMs act as an interface between the external microprocessor and the two internal WSMs. Commands are issued to the CSMs using standard microprocessor write timings. Since both CSMs share the same data path, commands issued to the device are processed by both CSMs simultaneously. If CSM A determines that the command is not applicable to the memory bank/WSM that it is interfacing with (memory bank A), then that command is ignored and CSM B sends the command to bank B/WSM B for execution. The CSM main task is to determine if the inputted command is valid and to send the valid command to the corresponding WSM. In single-operation mode, the contents of both status registers and the state of both CSMs are synchronized. Therefore, from the user's point of view, the device behaves as if there is only one CSM, one status register and one WSM that control both memory banks. In concurrent-operations mode, the contents of both status registers and the state of both CSMs are independent.

When a program or erase command is issued to the CSM for one memory bank, the WSM for that memory bank controls the internal program/erase sequences and the CSM responds to status-read and suspend/resume only. After the WSM completes its task, the WSM status bit (SB7) is set to a logic-high level (1), allowing the CSM to respond to the full command set again (see Table 5 for the status register bit definition). The complete command sets are listed in Table 3 and the description of these commands are shown in Table 4.

Table 3. Command State Machine Codes for Device-Mode Selection

COMMAND CODE ON DQ0 – DQ7†	DEVICE MODE
Standard Command Set	
00h	Invalid / Reserved
10h	Alternate Program Setup
20h	Block-Erase Setup
40h	Program Setup
50h	Clear Status Register
70h	Read Status Register
90h	Algorithm Selection
B0h	Erase-Program Suspend
D0h	Erase-Program Resume / Block-Erase Confirm
FFh	Read Array
Extended Command Set	
CBh	Enable Concurrent Mode
CEh	Disable Concurrent Mode

† DQ0 is the least significant bit. DQ8–DQ15 can be any valid 2-state level.

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command state machine (CSM) (continued)

Table 4. Command Definitions for Single and Concurrent Operations

COMMAND	BUS CYCLE REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	DATA INPUT	OPERATION	ADDRESS	DATA IN/OUT
Read Operations							
Read Array	1	Write	See Notes 1 and 2	FFh	Read	RA	Data Out
Read Algorithm-Selection Code	3	Write	X	90h	Read	A0	M/D
Read Status Register	2	Write	X	70h	Read	See Note 1	SRB
Clear Status Register	1	Write	See Notes 1 and 2	50h			
Program Operations							
Program-Setup / Program (byte/word)	2	Write	PA	40h or 10h	Write	PA	PD
Program-Suspend/ Program-Resume	2	Write	See Notes 1 and 2	B0h	Write	See Note 1	D0h
Erase Operations							
Block-Erase Setup/ Block-Erase Confirm	2	Write	BEA	20h	Write	BEA	D0h
Erase-Suspend/ Erase-Resume	2	Write	See Notes 1 and 2	B0h	Write	See Notes 1 and 2	D0h
Concurrent Operations							
Enable Concurrent Mode (see Note 2)	1	Write	X	CBh			
Disable Concurrent Mode (see Note 2)	1	Write	X	CEh			

Legend:
BEA Block-erase address. Any address selected within a block selects that block for erase.
M/D Manufacturer-equivalent / device-equivalent code
PA Address to be programmed
PD Data to be programmed at PA
RA Address to be read from
SRB Status-register data byte that can be found on DQ0–DQ7
X Don't care

NOTES: 1. For single operation: address = don't care
For concurrent operation:
address = 0xxxxxh for low-order address memory bank/WSM
address = 1xxxxxh for high-order address memory bank/WSM
2. To operate the device concurrently, the user must first issue the enable concurrent mode command. This command is valid only when the device is not busy performing any operation (that is, WSM is not active). To exit the concurrent-operation mode, the user must issue the disable concurrent mode command. This command is valid only when the device is in concurrent-operations mode and none of the memory banks/WSMs are active.

operation

The TMS28F1600T/B is capable of performing either single or concurrent operations. Single operation means that the device is performing one operation on one memory bank at a time, or in other words, only one WSM is active. A WSM is considered active even when it is in a suspended state. Therefore, from the user's point of view, the device behaves as if there is only one WSM that controls both memory banks. Concurrent operations mean that the device is performing two operations on two memory banks simultaneously, or in other words, both WSMs are active.

Device operations are selected by entering 8-bit command codes with conventional microprocessor timing into two on-chip CSMs through I/O pins DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the CSMs to single-operation, read-array mode. In single-operation mode, the device is functionally compatible with the existing 8-Mbit boot-block devices (TMS28F800T/B). Changing the mode of operation requires a command code to be entered into the CSM. Table 3 lists the CSM codes for all modes of operation.

To enable the concurrent-operations mode, the user must issue the enable concurrent mode command to the CSM. This command is valid only when the device is not busy performing any operation (that is, WSM is not active). Once the concurrent-operations mode is enabled, both status registers are cleared, both CSMs are reset to the read-array mode, and any commands issued to the CSMs from that point forward must be in accordance with the concurrent-operations command definitions. Command definitions for both single and concurrent-operations modes are listed in Table 4. Note that both command definitions are the same except for four commands: read array, read status register, clear status register, and suspend/resume. In single-operation mode, the addresses are don't care for those commands. However, in concurrent-operations mode, the user must indicate to the CSMs to which write-state machine/memory bank the command is applicable by supplying the memory bank address. This is the only difference between single and concurrent operations as far as command definitions are concerned.

To initiate concurrent operations once the concurrent mode is enabled, the user sequentially issues two commands to the CSMs, one for each memory bank; the issued commands must be in accordance with the concurrent-operations command definitions. Note that while the concurrent mode is enabled, the user does not have to operate the device concurrently; the user can operate the device as in single-operation mode but with the command definitions slightly modified. In addition, the user can access and clear each status register individually in concurrent mode.

To exit the concurrent-operations mode and return to the standard flash single-operation mode, the user must issue a disable concurrent mode command to the CSMs. This command is valid only when the device is in concurrent-operations mode and none of the memory banks/WSMs are active. Once concurrent-operations mode is disabled, both status registers are cleared and both CSMs reset to the read-array mode. Alternatively, the user can use the reset/power-down mode to reset the device to single-operation, read-array mode.

Since both registers are cleared when concurrent-operations mode is enabled/disabled, it is recommended that the status register be read, if required, before the concurrent mode is enabled/disabled.

concurrent operations

Since the TMS28F1600T/B has two independent WSMs, two operations can be performed on two memory banks concurrently. However, there are some rules and restrictions that must be adhered to when operating the device concurrently.

First, read is an operation that cannot be performed concurrently with another read. Second, if read is to be a part of a concurrent operation, then read must be the last command issued to the CSM. Third, once a read command is issued, the CSM does not accept *any other command* until the read operation is complete. Read array, read algorithm-selection, read status register and clear status register commands are considered to be the same (that is, a read operation) as far as concurrent operations are concerned.

concurrent operations (continued)

For example, a concurrent read-erase operation is *not* possible because as soon as the CSM receives the read command, no other command is processed until the read operation is complete. Whereas, a concurrent erase-read operation is possible because the erase command is given first (for example, to erase a sector in memory bank A) and the read command is given last (for example, to access bank B). Only when the read operation is complete, is the CSM ready to accept any other valid command. At this point, the user has two options from which to choose. If operation on memory bank B is desired, then the user can send a read, program, or erase command. If operation on memory bank A is desired, then the user can either do an erase-suspend to read or an erase-suspend to program; both of which must be done in a sector that is not being erased.

Two rules/restrictions govern the suspend operation:

- Read array, read status register, and program-resume are the only valid commands for the applicable WSM/memory bank after a program operation is suspended; all other commands are invalid and are ignored by the CSM. If concurrent-operations mode is enabled, then the other CSM will accept any other valid command for the other WSM/memory bank.
- Read array, read status register, program, and erase-resume are the only valid commands for the applicable WSM/memory bank after a sector-erase operation is suspended; all other commands are invalid and are ignored by the CSM. If concurrent-operations mode is enabled, then the other CSM will accept any other valid command for the other WSM/memory bank.

In general, any operation or combination of operations is possible as long as it does not violate the rules/restrictions mentioned above. Note that multiple suspension within the same memory bank is allowed. For example, if an erase operation is suspended for a program operation, then that program operation can also be suspended to read data. Table 5 shows all the legal operations that can be performed concurrently.

concurrent operations (continued)

Table 5. Concurrent Operations State Matrix†

		MEMORY BANK A												
		Read Array‡	Algorithm Selection‡§	Read Status Register‡	Clear Status Register‡	Program	Program-Suspend	Program-Suspend-Read‡¶	Sector-Erase	Erase-Suspend	Erase-Suspend-Read‡¶	Erase-Suspend-Program	Erase-Suspend Program-Suspend	Erase-Suspend Program-Suspend-Read‡¶
MEMORY BANK B	Read Array‡	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed
	Algorithm Selection‡§	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed
	Read Status Register‡	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed
	Clear Status Register‡	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed
	Program	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Program-Suspend	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Program-Suspend-Read‡¶	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed
	Sector-Erase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Erase-Suspend	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Erase-Suspend-Read‡¶	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed
	Erase-Suspend-Program	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Erase-Suspend Program-Suspend	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Erase-Suspend Program-Suspend-Read‡¶	Not Allowed	Not Allowed	Not Allowed	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed	Yes	Yes	Not Allowed

† Reset/deep power-down places both write-state machines/memory banks in the reset/deep power-down mode.
‡ Read array, algorithm-selection, read status register, and clear status register are considered “read” operations. Therefore, if a read operation is to be a part of concurrent operations, it must be the last command issued. If the read operation is issued first, then the CSM will not process any other command until the read operation is complete.
§ Either WSM can access the manufacturer and device ID information
¶ The clear-status-register and read-algorithm-selection commands are not functional during erase-suspend and program-suspend modes.

command definition

Command definitions for both single and concurrent operations are listed in Table 4. Note that both command definitions are the same except for four commands: read array, read status register, clear status register, and suspend/resume. In single-operation mode, the address is a don't care for these commands. However, in concurrent-operations mode, the user must indicate to the CSM which write-state machine/memory bank the command is applicable to by supplying the memory bank address.

In single-operation mode, the user can use either single or concurrent operations command definitions to send the desired command to the CSM. However, once the concurrent-operations mode is enabled, all subsequent commands issued must be in accordance with the concurrent-operations mode command definitions.

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data. See Table 4 for the CSM command definitions and data for each of the bus cycles.

Following the read-algorithm-selection-code command, two read cycles are required to access the manufacturer-equivalent code and the device-equivalent code. Table 7 and Table 8 show the code for word-wide mode and byte-wide mode, respectively.

status register

There are two 8-bit on-chip status registers. Status register A corresponds to WSM A and status register B corresponds to WSM B. The status register can be monitored to see whether the state of a program/erase operation is pending or complete by writing a read-status command to the CSM and reading the resulting status code on I/O pins DQ0–DQ7. This is valid for operation in either the byte or word-wide mode. When writing to the CSM in word-wide mode, the high-order I/O pins (DQ8–DQ15) can be set to any valid 2-state level. When reading the status bit during a word-wide read operation, the high-order I/Os (DQ8–DQ15) are set to 00h internally, so the user needs to interpret only the low-order I/O pins (DQ0–DQ7).

After a read-status command has been given, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

Register data is updated on the falling edge of $\overline{OE}$ or $\overline{CE}$. The latest falling edge of either of these two signals updates the latches within a given read cycle. Latching the data prevents errors from occurring should the register input change during a status register read. To assure that the status register output contains updated status data, $\overline{CE}$ or $\overline{OE}$ must be toggled for each subsequent status read.

The status registers provide the internal state of the WSMs to the external microprocessor. During periods when the WSMs are active, the status registers can be polled to determine the status of the WSMs. Table 6 defines the status register bits and their functions.

In single-operation mode, the contents of both status registers and the state of both CSMs are synchronized. Therefore, from the user's point of view, the device behaves as if only one CSM, one status register, and one WSM are controlling both memory banks. In concurrent-operations mode, the contents of both status registers and the state of both CSMs are independent. Therefore, in concurrent-operations mode, the user can access and clear each status register individually.

status register (continued)

Table 6. Status-Register Bit Definitions and Functions (see Note 3)

STATUS BIT	FUNCTION	DATA	COMMENTS
SB7	Write state machine status	1 = Ready 0 = Busy	If SB7 = 0 (busy), the WSM has not completed an erase or programming operation. If SB7 = 1 (ready), other polling operations can be performed. Until this occurs, the other status bits are not valid. If the WSM status bit shows busy (0), the user must periodically toggle $\overline{CE}$ or $\overline{OE}$ to determine when the WSM has completed an operation (SB7 = 1) since SB7 is not updated automatically at the completion of a WSM task.
SB6	Erase-suspend status (ESS)	1 = Erase suspended 0 = Erase in progress or completed	When an erase-suspend command is issued, the WSM halts execution and sets the ESS bit high (SB6 = 1), indicating that the erase operation has been suspended. The WSM status bit also is set high (SB 7 =1) indicating that the erase-suspend operation has been completed successfully. The ESS bit remains at a logic-high level until an erase-resume command is input to the CSM (code D0h).
SB5	Erase status (ES)	1 = Sector-erase error 0 = Sector-erase good	SB5 = 0 indicates that a successful sector erasure has occurred. SB5 = 1 indicates that an erasure error has occurred. In this case, the WSM has completed the maximum allowed erase pulses determined by the internal algorithm, but this was insufficient to erase the device completely.
SB4	Program status (PS)	1 = Byte/word program error 0 = Byte/word program good	SB4 = 0 indicates successful programming has occurred at the addressed sector location. SB4 = 1 indicates that the WSM was unable to program the addressed sector location correctly.
SB3	Vpp status (Vpps)	1 = Program abort : Vpp range error 0 = Vpp good	SB3 provides information on the status of Vpp during programming. If Vpp is lower than V_{PPL} after a program or erase command has been issued, SB3 is set to a 1, indicating that the programming operation is aborted. If Vpp is between V_{PPH} and V_{PPL}, SB3 is not set.
SB2	Program-suspend status (PSS)	1 = Program suspended 0 = Program in progress or completed	When a program-suspend command is issued, the WSM halts execution and sets the PSS bit high (SB2 = 1), indicating that the program operation has been suspended. The WSM status bit also is set high (SB 7 =1) indicating that the program-suspend operation has been completed successfully. The PSS bit remains at a logic-high level until a program-resume command is input to the CSM (code D0h).
SB0 – SB1	Reserved		These bits must be masked out when reading the status register.

NOTE 3: V_{PPL} and V_{PPH} correspond to the minimum and maximum operating voltage range of V_{PP}, respectively.

byte- or word-wide mode selection

Device operation is either byte-wide or word-wide mode user-selectable and is determined by the logic state of $\overline{BYTE}$. When $\overline{BYTE}$ is at logic-high level, the device is in the word-wide mode and data is written to, or read from, I/O pins DQ0–DQ15. When $\overline{BYTE}$ is at logic-low level, the device is in the byte-wide mode and data is written to, or read from, I/O pins DQ0–DQ7. In the byte-wide mode, I/O pins DQ8–DQ14 are placed in the high-impedance state and DQ15/A-1 becomes the low-order address pin. Table 7 and Table 8 summarize operations for word-wide mode and byte-wide mode, respectively.

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byte- or word-wide mode selection (continued)

Table 7. Operation Modes for Word-Wide Mode ($\overline{BYTE}$ = V_{IH}) (see Note 4)

MODE	$\overline{WP}$	$\overline{CE}$	$\overline{OE}$	$\overline{RP}$	$\overline{WE}$	A9	A0	V_{PP}	DQ15–DQ0
Read	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A9	A0	X	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	Manufacturer-equivalent code 0089h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	Device-equivalent code 00xxh (top boot block)
									Device-equivalent code 00xxh (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	Hi-Z
Write (see Notes 3 and 5)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	A9	A0	V_{PPL} or V_{PPH}	Data in

Table 8. Operation Modes for Byte-Wide Mode ($\overline{BYTE}$ = V_{IL}) (see Note 4)

MODE	$\overline{WP}$	$\overline{CE}$	$\overline{OE}$	$\overline{RP}$	$\overline{WE}$	A9	A0	VPP	DQ15/ A–1	DQ14–DQ8	DQ7–DQ0
Read lower byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A9	A0	X	V_{IL}	Hi-Z	Data out
Read upper byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A9	A0	X	V_{IH}	Hi-Z	Data out
Algorithm-selection mode	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IL}	X	X	Hi-Z	Manufacturer-equivalent code 89h
	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	V_{IH}	X	X	Hi-Z	Device-equivalent code ??h (top boot block)
											Device-equivalent code ??h (bottom boot block)
Output disable	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	Hi-Z
Standby	X	V_{IH}	X	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z
Reset/deep power down	X	X	X	V_{IL}	X	X	X	X	X	Hi-Z	Hi-Z
Write (see Notes 3 and 5)	V_{IL} or V_{IH}	V_{IL}	V_{IH}	V_{IH} or V_{HH}	V_{IL}	A9	A0	V_{PPL} or V_{PPH}	X	Hi-Z	Data in

NOTES: 3. V_{PPL} and V_{PPH} correspond to the minimum and maximum operating voltage range of V_{PP}, respectively.
4. X = don't care
5. When writing commands to the '28F1600T/B, V_{PP} must be in the appropriate V_{PP} voltage range for sector-erase or program commands to be executed. Also, depending on the combination of $\overline{RP}$ and $\overline{WP}$, the boot block can be secured and, therefore, is not programmable (see Table 2 for the combinations).

command state machine (CSM) operations

The CSM decodes instructions for read, read algorithm-selection code, read status register, clear status register, program, erase, erase/program suspend, and erase/program resume. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 3 for CSM codes). The CSMs act as an interface between the external microprocessor and the two internal WSMs. During a program/erase cycle, the CSM informs the applicable WSM (based on the input address) that a program or erase has been requested. The selected WSM controls the program/erase sequences during a program/erase cycle and the CSM responds only to status read and program/erase suspend commands. If concurrent-operations mode is enabled, then the other CSM will respond to the full command set (if idle) or any valid command (if busy) for the other bank.

command state machine (CSM) operations (continued)

When the WSM has completed its task, the WSM status bit (SB7) of the status register is set to a logic-high level and the CSM responds to the full command set again. In single-operation mode, the states of both CSMs are synchronized and remain in the last issued command state until the microprocessor issues another command. In concurrent-operations mode, the state of each CSM is independent and they also remain in the last issued command state until the microprocessor issues another command.

The WSM successfully initiates an erase or program operation only when V_{PP} is within its correct voltage range. To prevent inadvertent program/erase to the device, it is recommended that $\overline{RP}$ be tied to the system reset signal.

clear status register

The internal circuitry can set only the V_{PP} status (SB3), the program status (SB4), and the erase-status bit (SB5) of the status register. The clear-status register command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. When the status bits are cleared, the CSM returns to the read-array mode. This is true for both single and concurrent operations mode. In single-operation mode, the clear-status-register command clears both status registers. In concurrent operations mode, the memory bank address determines which register to clear (see Table 4 for concurrent operations command definitions). Note that clear status register command is not functional during program-suspend and erase-suspend modes.

read operations

There are three read operations available: read array, read algorithm-selection code, and read status register.

- Read array. The array is read by entering the command code FFh on DQ0–DQ7. Control pins $\overline{CE}$ and $\overline{OE}$ must be at a logic-low level (V_{IL}) and $\overline{WE}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}) to read data from the memory bank. Data is available on DQ0–DQ15 (word-wide mode) or DQ0–DQ7 (byte-wide mode). Any valid address within any of the sectors selects that sector and allows data to be read from the sector.
- Read algorithm-selection code. Algorithm-selection codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation: the first to enter the command code and the next two to read the manufacturer equivalent and the device-equivalent codes. Control pins $\overline{CE}$ and $\overline{OE}$ must be at the logic-low level (V_{IL}) and $\overline{WE}$ and $\overline{RP}$ must be at the logic-high level (V_{IH}). Two identifier bytes are accessed by toggling A0. The manufacturer-equivalent code is obtained on DQ0–DQ7 with A0 at the logic-low level (V_{IL}). The device-equivalent code is obtained when A0 is set to a logic-high level (V_{IH}). Alternately, the manufacturer- and device-equivalent codes can be read by applying V_{ID} (nominally 12 V) to A9 and selecting the desired code by toggling A0 high or low. All other addresses are “don’t care” (see Table 4, Table 7 and Table 8). Note that algorithm-selection operation can be done concurrently with the program/erase operation since the information can be accessed by either WSM (see Table 5).
- Read status register. The status register is read by entering the command code 70h on DQ0–DQ7. Control pins $\overline{CE}$ and $\overline{OE}$ must be at a logic-low level (V_{IL}) and $\overline{WE}$ and $\overline{RP}$ must be at a logic-high level (V_{IH}). Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a given read cycle, status-register contents are updated on the falling edge of $\overline{CE}$ or $\overline{OE}$, whichever occurs last within the cycle. For concurrent operations, the user must specify which register to read status from by supplying the memory bank address. For single operations, the address is a don’t care (see Table 4).

programming operations

There are three CSM commands for programming: program setup, alternate program setup, and program suspend/resume (see Table 4).

Program setup and alternate program setup are the same as far as the programming operation is concerned except that they have different command codes.

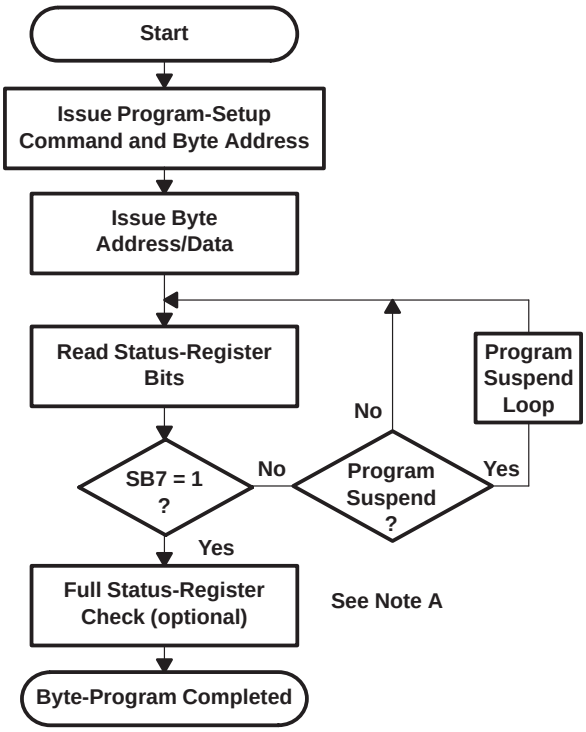
- Program setup. After the program setup command code is entered, the selected WSM takes over and correctly sequences the device to complete the program operation. During this time, the CSM responds only to status-read and -suspend commands (see Figure 3 and Figure 4). If the concurrent-operations mode is enabled, then the other CSM will respond to the full command set or any valid command for the other bank.

  Taking $\overline{RP}$ to V_{IL} during programming aborts the program operation. During programming, V_{PP} must remain in the appropriate V_{PP} voltage range as shown in the recommended operating conditions table. Different combinations of $\overline{RP}$, $\overline{WP}$, and V_{PP} pin voltage levels ensure that data in certain sectors are protected, and, therefore, cannot be programmed (see Table 2 for a list of combinations). Only 0s are written and compared during a program operation. If 1s are programmed, the memory-cell contents do not change and no error occurs.

  A program-setup command can be aborted by writting FFh (in byte-wide mode) or FFFFh (in word-wide mode) during the second cycle. After writing all 1s during the second cycle, the CSM responds only to status reads. When the WSM status bit (SB7) is set to a logic-high level, signifying that the nonprogram operation is terminated, all commands for the applicable bank to the CSM become valid again.

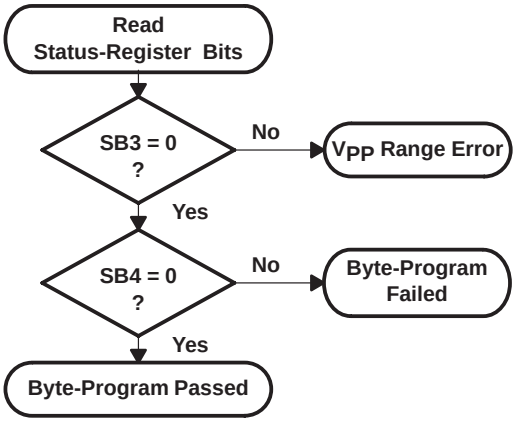
- Program suspend/program resume. During the execution of a programming operation, the program-suspend command (B0h) can be entered to direct the WSM to suspend the programming operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status register, and program-resume commands. While the selected WSM is in the program-suspend state, data from any address location except for the location that was being programmed can be read. To resume the programming operation, a program-resume command (D0h) must be issued to make the CSM clear the suspend state that was set previously.

  If concurrent-operations mode is enabled, then the user must specify which memory bank/WSM to suspend/resume by supplying the memory bank address. Programming on the low-order address memory bank is suspended/resumed if the address input is within its valid address range (that is, A19 = 0). Programming on the high-order address memory bank is suspended/resumed if the address input is within its valid address range (that is, A19 = 1). While the selected memory bank/WSM is in the program-suspend state, data from any address location *within the same memory bank* (except for the location that was being programmed) can be read. Figure 5 shows the program suspend/resume flowchart.



BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of byte to be programmed
Write	Write data	Data = Byte to be programmed Addr = Address of byte to be programmed
Read		Status-register data. Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent bytes. Write FFh after the last byte-programming operation to reset the device to read-array mode		

FULL STATUS-REGISTER-CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Byte-program error (see Note C)

NOTES: A. Full status-register check can be done after each byte or after a sequence of bytes.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 3. Automated Byte-Programming Flowchart

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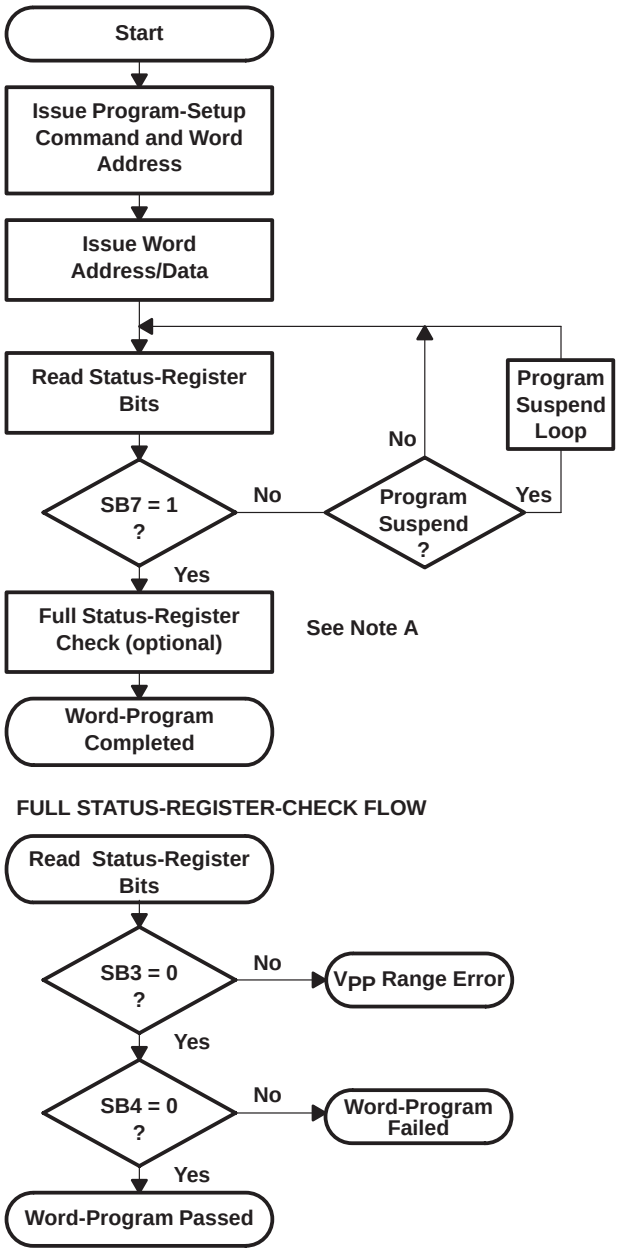


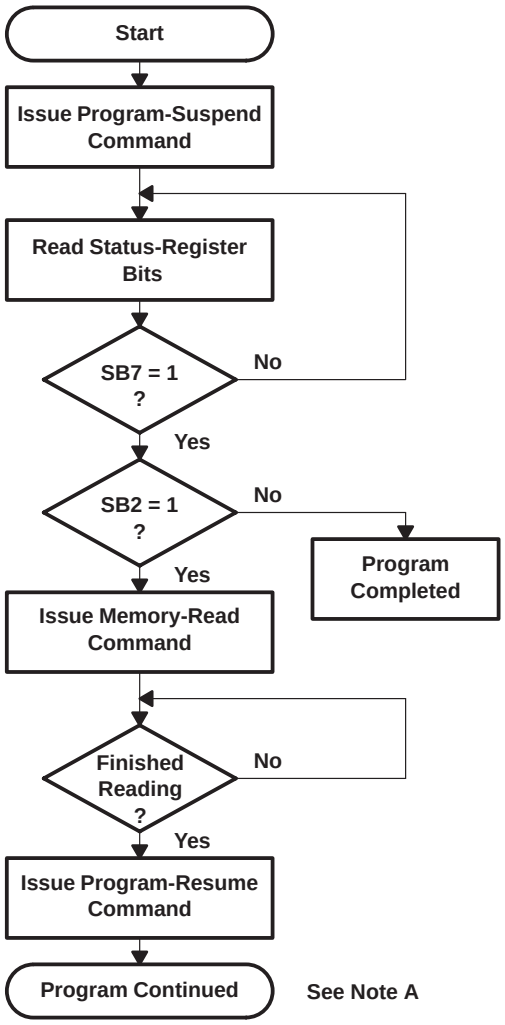
FULL STATUS-REGISTER-CHECK FLOW

BUS OPERATION	COMMAND	COMMENTS
Write	Write program setup	Data = 40h or 10h Addr = Address of word to be programmed
Write	Write data	Data = Word to be programmed Addr = Address of word to be programmed
Read		Status-register data. Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank Toggle $\overline{OE}$ or $\overline{CE}$ to update status register.
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word-programming operation to reset the device to read-array mode.		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 1 = Word-program error (see Note C)

NOTES: A. Full status-register check can be done after each word or after a sequence of words.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB4 is cleared only by the clear-status-register command, but it does not prevent additional program operation attempts.

Figure 4. Automated Word-Programming Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Program suspend	Data = B0h Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank
Read		Status-register data. Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready
Standby		Check SB2 1 = Program suspended
Write	Read memory	Data = FFh Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank
Read		Read data from locations other than that being programmed.
Write	Program resume	Data = D0h Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank

NOTE A: Refer to programming flowchart for complete programming procedure

Figure 5. Program-Suspend/Resume Flowchart

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erase operations

There are two erase operations that can be performed by the TMS28F1600T/B: sector erase and erase suspend/erase-resume. An erase operation must be used to initialize all bits in a sector to 1s. After sector-erase confirm is issued, the CSM responds only status reads or erase-suspend commands for the applicable bank until the applicable WSM completes its task. If concurrent mode is enabled, then the other CSM responds to the full command set or any valid command for the other bank.

- Sector erasure. Sector erasure inside the memory array sets all bits within the addressed sector to logic 1s. Erasure is accomplished only by sectors; data at single address locations within the sector cannot be individually erased. The sector to be erased is selected by using any valid address within that sector. Note that different combinations of $\overline{RP}$, $\overline{WP}$ and V_{PP} pin voltage levels ensure that data in certain sectors are protected and, therefore, cannot be erased (see Table 2 for a list of combinations). Sector erasure is initiated by a command sequence to the CSM: sector-erase setup (20h) followed by sector-erase confirm (D0h) (see Figure 6). A two-command erase sequence protects against accidental erasure of memory contents.

  Erase setup and confirm commands are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Sector addresses are latched during the sector-erase-confirm command on the rising edge of $\overline{WE}$ or $\overline{CE}$ (See Figure 13 and Figure 14). When the sector-erase-confirm command is complete, the selected WSM automatically executes a sequence of events to complete the sector erasure (see Figure 6). During this sequence, the sector is programmed with logic 0s, data is verified, all bits in the sector are erased to logic 1s, and finally, verification is performed to assure that all bits are erased correctly. Monitoring of the erase operation is possible through the use of the status register. If the concurrent-operations mode is enabled, then status registers A and B can be used to monitor the erase operation of the corresponding memory bank.

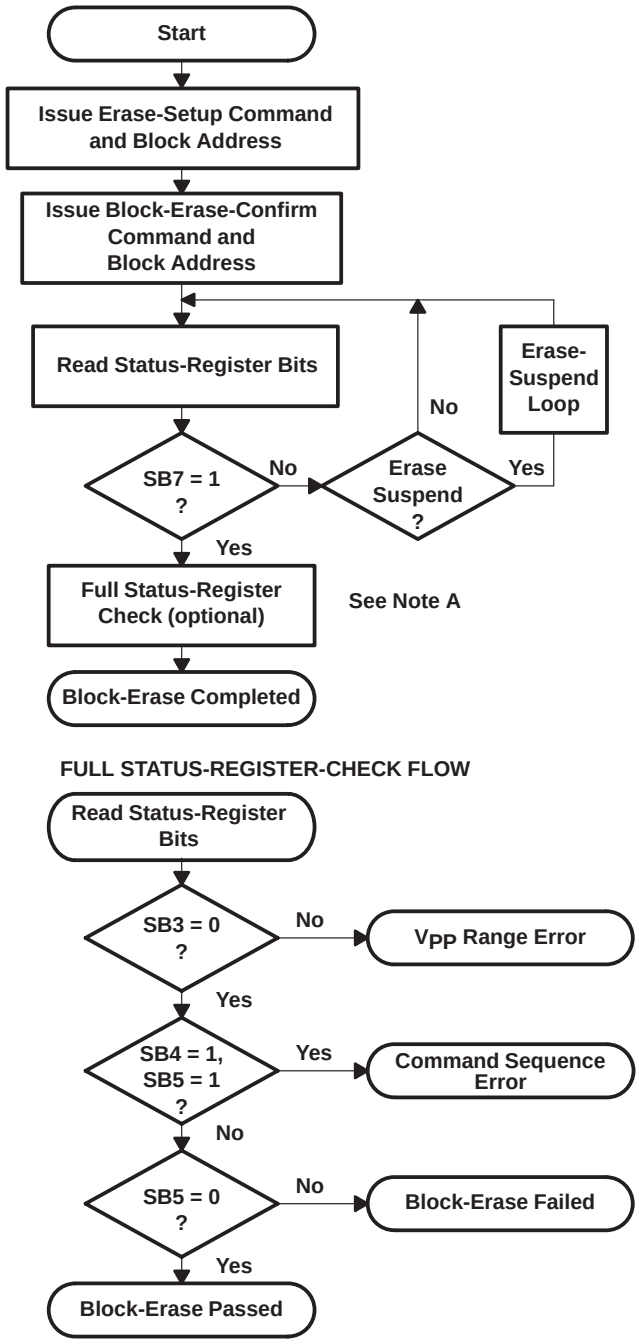
- Erase suspend/erase resume. During the execution of an erase operation, the erase-suspend command (B0h) can be entered to direct the WSM to suspend the erase operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the read-array, read-status register, program, and erase-resume commands. While the selected WSM is in the erase-suspend state, data can be read from any sector except for the sector that is being erase-suspended. Similarly, data can be programmed to any address location except for the sector that is being erase-suspended. To resume the erase operation, an erase-resume command (D0h) must be issued to cause the CSM to clear the suspend state previously set. It is important to note that erase cannot be resumed until the program operation initiated during erase-suspend has been completed. The following steps must be completed in sequence to continue the erase operation.

  1. Sector-erase operation is suspended to program
  2. Program operation is suspended to read
  3. Program operation is resumed by the user
  4. Program operation is completed
  5. Another resume command is issued

  If the concurrent-operations mode is enabled, then the user must specify which memory bank/WSM to suspend/resume by supplying the memory bank address. An erase operation on a low-order address memory bank is suspended/resumed if the address input is within its valid address range (that is, A19 = 0). An erase operation on a high-order address memory bank is suspended/resumed if the address input is within its valid address range (that is, A19 = 1). While the selected memory bank/WSM is in the erase-suspend state, data from any sector *within the same memory bank* (except for the sector that was being erased) can be read. Similarly, data can be programmed to any address location of the memory bank except for the sector that is being erase-suspended. Figure 7 shows the erase-suspend/erase-resume flowchart.

automatic power-saving mode

Substantial power savings are realized during periods when the array is not being read. During this time, the device switches to the automatic power-saving (APS) mode. When the device switches to this mode, I_{CC} is typically reduced from 40 mA to 1 mA (I_{out} = 0 mA). The low level of power is maintained until another read operation is initiated. In this mode, the I/O pins retain the data from the last memory address read until a new address is read. There is no wake-up time associated with the APS mode; the device can be read with standard access time from the APS mode. This mode is entered automatically if no control pins toggle within a 200-ns time-out period. At least one transition on $\overline{CE}$ must occur after power up to activate this mode.

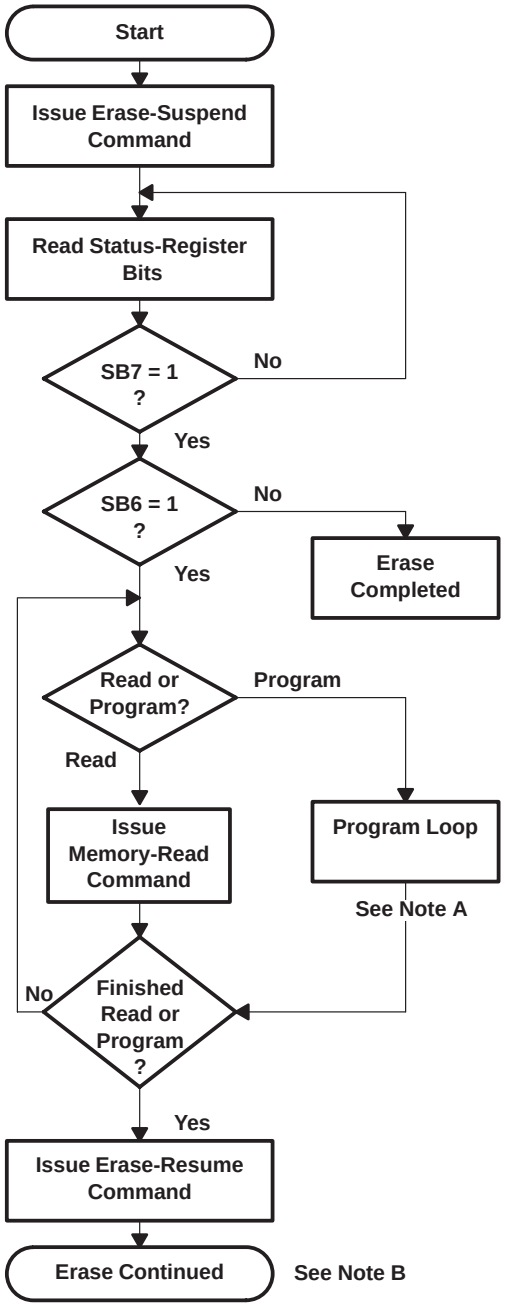


BUS OPERATION	COMMAND	COMMENTS
Write	Write erase setup	Data = 20h Sector Addr = Address within sector to be erased
Write	Erase	Data = D0h Sector Addr = Address within sector to be erased
Read		Status-register data. Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last block-erase operation to reset the device to read-array mode		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SB3 1 = Detect V_{PP} low (see Note B)
Standby		Check SB4 and SB5 1 = Sector-erase error
Standby		Check SB5 1 = Sector-erase error (see Note C)

NOTES: A. Full status-register check can be done after each block or after a sequence of blocks.
B. SB3 must be cleared before attempting additional program/erase operations.
C. SB5 is cleared only by the clear-status-register command in cases where multiple blocks are erased before full status is checked.

Figure 6. Automated Block-Erase Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase suspend	Data = B0h Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank
Read		Status-register data. Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank Toggle $\overline{OE}$ or $\overline{CE}$ to update status register
Standby		Check SB7 1 = Ready
Standby		Check SB6 1 = Suspended
Write	Erase resume	Data = D0h Single-operation mode: Addr = don't care Concurrent-operations mode: Addr = 0xxxxxh for low-order address memory bank = 1xxxxxh for high-order address memory bank

NOTES: A. Refer to the programming flowchart for complete programming procedures.
B. Refer to block-erase flowchart for complete erasure procedure

Figure 7. Erase-Suspend/Resume Flowchart

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reset/deep power-down mode

Very low levels of power consumption can be attained by using a special pin, $\overline{RP}$, to disable the internal device circuitry. When $\overline{RP}$ is at a CMOS logic-low level of 0.0 V ± 0.2 V, a much lower I_{CC} value or power is achievable. This is important in portable applications where extended battery life is of major concern.

A recovery time is required when exiting from deep power-down mode. For a read-array operation, a minimum of $t_{d(RP)}$ is required before data is valid, and a minimum of $t_{rec(RPHZ)}$ and $t_{rec(RPHW)}$ in deep power-down mode is required before data input to the CSM can be recognized. With $\overline{RP}$ at ground, both WSMs are reset and both status registers are cleared, effectively eliminating accidental programming to memory banks during system reset. After restoration of power, the device does not recognize any operation command until $\overline{RP}$ is returned to a V_{IH} or V_{HH} level.

Should $\overline{RP}$ go low during a program or erase operation, the device powers down and, therefore, becomes nonfunctional. Data being written or erased at that time becomes invalid or indeterminate, requiring that the operation be performed again after power restoration.

power supply detection

$\overline{RP}$ must be connected to the system reset/power good signal to ensure that proper synchronization is maintained between the CPU and the flash memory operating modes. The default state after power up and exit from deep power-down mode is the single-operation, read-array mode. $\overline{RP}$ also is used to indicate that the power supply is stable so that the operating supply voltage can be established (2.7 V, 3.3 V, or 5 V). Figure 9 shows the proper power-up sequence. To reset the operating supply voltage, the device must be completely powered off (V_{CC} = 0 V) before the new supply voltage is detected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 6) . . . . . – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 6) . . . . . – 0.6 V to 14 V
Input voltage range: All inputs except A9, $\overline{RP}$ . . . . . – 0.6 V to V_{CC} + 1 V
$\overline{RP}$, A9 (see Note 7) . . . . . – 0.6 V to 13.5 V
Output voltage range (see Note 8) . . . . . – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range, T_A, during read/erase/program: L suffix . . . . . 0°C to 70°C
E suffix . . . . . – 40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 6. All voltage values are with respect to V_{SS}.
7. The voltage on any input can undershoot to – 2 V for periods less than 20 ns.
8. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

The TMS28F1600 allows memory reads to be performed using V_{CC} = 2.7 V to 3.6 V for optimum power consumption or V_{CC} = 5 ± 10% for device performance. Erasing or programming the device can be accomplished with V_{PP} = 2.7 V–12 V for maximum flexibility.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program/read/erase suspend	3-V V_{CC} range	2.7	3	3.6	V
			5-V V_{CC} range	4.5	5	5.5	
V_{PP}	Supply voltage	During read only (V_{PPL})		0		6.5	V
		During program/erase suspend, V_{PP} can have V_{CC} as MIN or NOM		2.7		12.6	
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	V_{SS} – 0.2		V_{SS} + 0.2	
V_{LKO}	V_{CC} lock-out voltage from program/erase			2			V
V_{HH}	$\overline{RP}$ unlock voltage			11.4	12	13	V
V_{PPLK}	V_{PP} lock-out voltage from program/erase					1.5	V
T_A	Operating free-air temperature during read/erase/program		L Suffix	0		70	°C
			E Suffix	–40		85	°C

word/byte typical write and sector-erase duration for TMS28F1600T/B (see Notes 9 and 10)

PARAMETER	3-V V_{CC} RANGE	5-V V_{CC} RANGE	UNIT
128K sector-erase time	2	1	s
16K sector-erase time	0.5	0.3	s
128K sector byte-program time	1.3	1	s
128K sector word-program time	0.8	0.6	s

NOTES: 9. Excludes system-level overhead
10. Typical values shown are at T_A = 25°C

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electrical characteristics for TMS28F1600T/B over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	$V_{CC} = V_{CC}MIN$, $I_{OH} = -2.5$ mA		2.4		V
		CMOS	$V_{CC} = V_{CC}MIN$, $I_{OH} = -100$ µA		$V_{CC} - 0.4$		
V_{OL}	Low-level output voltage		$V_{CC} = V_{CC}MIN$, $I_{OL} = 5.8$ mA			0.45	V
V_{ID}	A9 selection code voltage		During read algorithm-selection mode		11.4	12.6	V
I_I	Input current (leakage), except for A9 when A9 = V_{ID} (see Note 11)		$V_{CC} = V_{CC}MAX, V_I = 0$ V to $V_{CC}MAX$, $\overline{RP} = V_{HH}$			±1	µA
I_{ID}	A9 selection code current		A9 = V_{ID}			500	µA
I_{RP}	$\overline{RP}$ boot-block unlock current					500	µA
I_O	Output current (leakage)		$V_{CC} = V_{CC}MAX, V_O = 0$ V to $V_{CC}MAX$			±10	µA
I_{PPS}	V_{PP} standby current (standby)		$V_{PP} \le V_{CC}$	3-V V_{CC} range		10	µA
				5-V V_{CC} range		10	
I_{PPL}	V_{PP} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V, $V_{PP} \le V_{CC}$	3-V V_{CC} range		5	µA
				5-V V_{CC} range		5	
I_{PP1}	V_{PP} supply current (active read)		$V_{PP} \ge V_{CC}$	3-V V_{CC} range		50	µA
				5-V V_{CC} range		50	
I_{PP2}	V_{PP} supply current (active byte-write) (see Notes 12 and 13)		Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		17	mA
				5-V V_{PP} range, 5-V V_{CC} range		15	
				12-V V_{PP} range, 3-V V_{CC} range		12	
				12-V V_{PP} range, 5-V V_{CC} range		10	
I_{PP3}	V_{PP} supply current (active word-write) (see Notes 12 and 13)		Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		17	mA
				5-V V_{PP} range, 5-V V_{CC} range		15	
				12-V V_{PP} range, 3-V V_{CC} range		12	
				12-V V_{PP} range, 5-V V_{CC} range		10	

NOTES: 11. $DQ15/A_{-1}$ is tested for output leakage only.
12. Not 100% tested; characterization data available
13. All ac current values are RMS unless otherwise noted.

electrical characteristics for TMS28F1600T/B over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
I_{PP4}	V_{PP} supply current (sector-erase) (see Notes 12 and 13)		Sector-erase in progress	5-V V_{PP} range, 3-V V_{CC} range		15	mA
				5-V V_{PP} range, 5-V V_{CC} range		15	
				12-V V_{PP} range, 3-V V_{CC} range		10	
				12-V V_{PP} range, 5-V V_{CC} range		10	
I_{PP5}	V_{PP} supply current (erase/program-suspend) (see Notes 12 and 13)		Erase/program suspended	5-V V_{PP} range, 3-V V_{CC} range		50	µA
				5-V V_{PP} range, 5-V V_{CC} range		50	
				12-V V_{PP} range, 3-V V_{CC} range		50	
				12-V V_{PP} range, 5-V V_{CC} range		50	
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$\overline{CE} = \overline{RP} = V_{IH}$, $V_{CC} = V_{CC}MAX$	3-V V_{CC} range		1	mA
				5-V V_{CC} range		1	
		CMOS-input level		3-V V_{CC} range		80	µA
				5-V V_{CC} range		100	
I_{CCL}	V_{CC} supply current (reset/deep power-down mode)		$\overline{RP} = V_{SS} \pm 0.2$ V; $V_{CC} = V_{CC}MAX$			8	µA
I_{CC1}	V_{CC} supply current (active read)	TTL-input level	$\overline{CE} = V_{IL}$, $I_{OUT} = 0$ mA, f = 5 MHz	3-V V_{CC} range		25	mA
			$\overline{CE} = V_{IL}$, $I_{OUT} = 0$ mA, f = 10 MHz	5-V V_{CC} range		35	
		CMOS-input level	$\overline{CE} = V_{IL}$, $I_{OUT} = 0$ mA, f = 5 MHz	3-V V_{CC} range		25	mA
			$\overline{CE} = V_{IL}$, $I_{OUT} = 0$ mA, f = 10 MHz	5-V V_{CC} range		35	
I_{CC2}	V_{CC} supply current (active byte-write) (see Notes 12, 13, and 14)		$V_{CC} = V_{CC}MAX$, Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
				5-V V_{PP} range, 5-V V_{CC} range		35	
				12-V V_{PP} range, 3-V V_{CC} range		30	
				12-V V_{PP} range, 5-V V_{CC} range		35	

NOTES: 12. Not 100% tested; characterization data available
13. All ac current values are RMS unless otherwise noted.
14. These values are the current for one memory bank. If both memory banks are active, then the current for each bank should be added together in order to calculate the total current for the chip. For example, if bank A is in the erase mode and bank B is in the read mode, then I_{CC} total = $I_{CC4} + I_{CC1}$.

PRODUCT PREVIEW

electrical characteristics for TMS28F1600T/B over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC3}	V_{CC} supply current (active word-write) (see Notes 12, 13, and 14)	$V_{CC} = V_{CC}MAX$, Programming in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
			5-V V_{PP} range, 5-V V_{CC} range		35	
			12-V V_{PP} range, 3-V V_{CC} range		30	
			12-V V_{PP} range, 5-V V_{CC} range		35	
I_{CC4}	V_{CC} supply current (sector-erase) (see Notes 12, 13, and 14)	$V_{CC} = V_{CC}MAX$, Sector-erase in progress	5-V V_{PP} range, 3-V V_{CC} range		30	mA
			5-V V_{PP} range, 5-V V_{CC} range		35	
			12-V V_{PP} range, 3-V V_{CC} range		30	
			12-V V_{PP} range, 5-V V_{CC} range		35	
I_{CC5}	V_{CC} supply current (erase/program-suspend) (see Notes 12, 13, and 14)	$V_{CC} = V_{CC}MAX$, $\overline{CE} = V_{IH}$, Sector-erase/program suspended	3-V V_{CC} range		4	mA
			5-V V_{CC} range		4	

NOTES: 12. Not 100% tested; characterization data available
13. All ac current values are RMS unless otherwise noted.
14. These values are the current for one memory bank. If both memory banks are active, then the current for each bank should be added together in order to calculate the total current for the chip. For example, if bank A is in the erase mode and bank B is in the read mode, then I_{CC} total = $I_{CC4} + I_{CC1}$.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz, V_I = 0 V

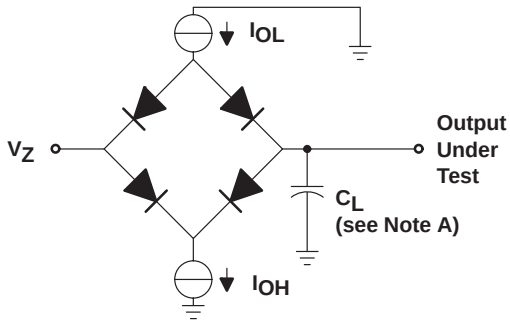
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_i	Input capacitance			8	pF
C_o	Output capacitance	V_O = 0 V		12	pF

power-up and reset switching characteristics for TMS28F1600T/B over recommended ranges of supply voltage (commercial and extended temperature ranges)(see Notes 12 and 15)

PARAMETER		ALT. SYMBOL	'28F1600y-80				'28F1600y-90				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(VCC)}$	Setup time, $\overline{RP}$ low to V_{CC} at 4.5 V MIN. (to V_{CC} at 2.7 V MIN or 3.6 V MAX) (see Note 16)	t_{PL5V} t_{PL3V}	0		0		0		0		ns
$t_{a(DV)}$	Access time, address valid to data valid	t_{AVQV}		90		80		100		90	ns
$t_{su(DV)}$	Setup time, $\overline{RP}$ high to data valid	t_{PHQV}		800		450		800		450	ns
$t_{h(RP5)}$	Hold time, V_{CC} at 4.5 V (MIN) to $\overline{RP}$ high	t_{5VPH}	2		2		2		2		µs
$t_{h(RP3)}$	Hold time, V_{CC} at 2.7 V (MIN) to $\overline{RP}$ high	t_{3VPH}	2		2		2		2		µs

NOTES: 12. Not 100% tested; characterization data available
15. $\overline{CE}$ and $\overline{OE}$ are switched low after power up.
16. The power supply can switch low concurrently with $\overline{RP}$ going low.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and fixture capacitance.
B. AC test conditions are driven at V_{IH} and V_{IL}. Timing measurements are made at V_{OH} and V_{OL} levels on both inputs and outputs. Refer to Table 9 for values based on V_{CC} operating range.
C. Each device should have a 0.1-µF ceramic capacitor connected to V_{CC} and V_{SS} as close as possible to the device pins.

Figure 8. Load Circuit and Voltage Waveforms

Table 9. AC Test Conditions

V_{CC} RANGE	I_{OL}	I_{OH}	V_Z†	V_{OL}	V_{OH}	V_{IL}	V_{IH}	C_L	tf	tr
5 V ± 10%	2.1	–0.4	1.5	0.8	2.0	0.45	2.4	100	< 10	< 10
3.3 ± 0.3 V	0.5	–0.5	1.5	1.5	1.5	0.0	3.0	50	< 10	< 10
2.7 to 3.6 V	0.1	–0.1	1.35	1.35	1.35	0.0	2.7	50	< 10	< 10

† V_Z is the measured value used to detect high impedance.

PRODUCT PREVIEW

switching characteristics for TMS28F1600T/B over recommended ranges of supply voltage (commercial and extended temperature ranges)

read operations

PARAMETER		ALT. SYMBOL	'28F1600y-80				'28F1600y-90				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from A0–A19 (see Note 17)	t_{AVQV}		90		80		100		90	ns
$t_{a(E)}$	Access time from $\overline{CE}$	t_{ELQV}		90		80		100		90	ns
$t_{a(G)}$	Access time from $\overline{OE}$	t_{GLQV}		60		40		65		45	ns
$t_{c(R)}$	Cycle time, read	t_{AVAV}	90		80		100		90		ns
$t_{d(E)}$	Delay time, $\overline{CE}$ low to low-impedance output	t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{OE}$ low to low-impedance output	t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Disable time, $\overline{CE}$ to the high-impedance output	t_{EHQZ}		55		30		55		35	ns
$t_{dis(G)}$	Disable time, $\overline{OE}$ to the high-impedance output	t_{GHQZ}		45		30		45		35	ns
$t_{h(D)}$	Hold time, DQ valid from A0–A19, $\overline{CE}$, or $\overline{OE}$, whichever occurs first (see Note 17)	t_{AXQX}	0		0		0		0		ns
$t_{su(EB)}$	Setup time, $\overline{BYTE}$ from $\overline{CE}$ low	t_{ELFL} t_{ELFH}		7		5		7		5	ns
$t_{d(RP)}$	Delay time, output time from $\overline{RP}$ high	t_{PHQV}		800		450		800		450	ns
$t_{dis(BL)}$	Disable time, $\overline{BYTE}$ low to DQ8–DQ15 in the high-impedance state	t_{FLQZ}		90		80		100		90	ns
$t_{a(BH)}$	Access time from $\overline{BYTE}$ going high	t_{FHQV}		90		80		100		90	ns

NOTE 17: A_{-1}–A19 for byte-wide

timing requirements for TMS28F1600T/B over recommended ranges of supply voltage (commercial and extended temperature ranges)

write/erase operations — $\overline{WE}$-controlled writes

		ALT. SYMBOL	’28F1600y-80				’28F1600y-90				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	90		80		100		90		ns
$t_{c(W)OP}$	Cycle time, duration of programming operation	t_{WHQV1}	6		6		6		6		µs
$t_{c(W)ERB}$	Cycle time, erase operation (boot block)	t_{WHQV2}	0.3		0.3		0.3		0.3		s
$t_{c(W)ERP}$	Cycle time, erase operation (parameter block)	t_{WHQV3}	0.3		0.3		0.3		0.3		s
$t_{c(W)ERM}$	Cycle time, erase operation (main block)	t_{WHQV4}	0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A19 (see Note 17)	t_{WHAX}	0		0		0		10		ns
$t_{h(D)}$	Hold time, DQ valid	t_{WHDX}	0		0		0		0		ns
$t_{h(E)}$	Hold time, $\overline{CE}$	t_{WHEH}	0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status register bit	t_{QVPH}	0		0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0		0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		50		90		50		ns
$t_{su(A)}$	Setup time, A0–A19 (see Note 17)	t_{AVWH}	90		50		90		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVWH}	90		50		90		50		ns
$t_{su(E)}$	Setup time, $\overline{CE}$ before write operation	t_{ELWL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{WE}$ going high	t_{PHHWH}	200		100		200		100		ns
$t_{su(VPP)1}$	Setup time, V_{PP} to $\overline{WE}$ going high	t_{VPWH}	200		100		200		100		ns
$t_{w(W)}$	Pulse duration, $\overline{WE}$ low	t_{WLWH}	90		50		90		50		ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	t_{WLWL}	20		30		20		30		ns
$t_{rec(RPHW)}$	Recovery time, $\overline{RP}$ high to $\overline{WE}$ going low	t_{PHWL}	800		450		800		450		ns

NOTE 17: A_{-1}–A19 for byte-wide

PRODUCT PREVIEW

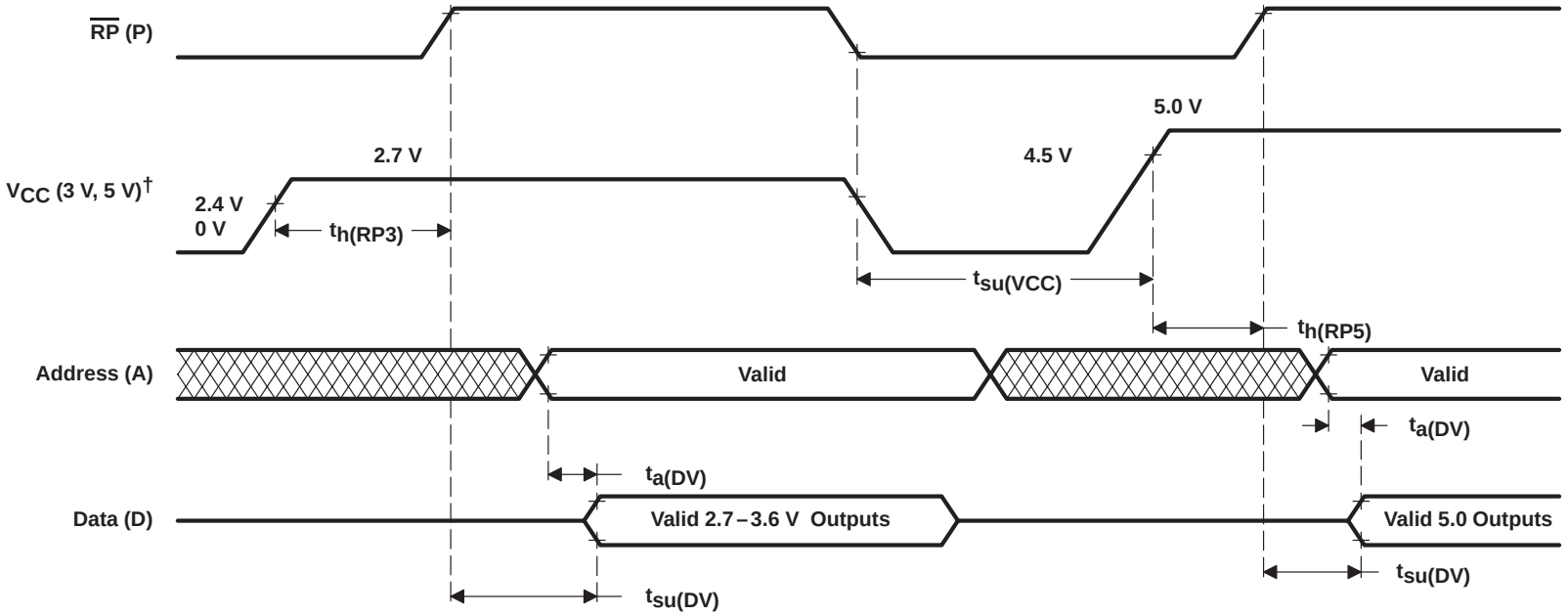
timing requirements for TMS28F1600T/B over recommended ranges of supply voltage (commercial and extended temperature ranges) (continued)

write/erase operations — $\overline{CE}$-controlled writes

		ALT. SYMBOL	’28F1600y-80				’28F1600y-90				UNIT
			3-V V_{CC} RANGE		5-V V_{CC} RANGE		3-V V_{CC} RANGE		5-V V_{CC} RANGE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(E)}$	Cycle time, write	t_{AVAV}	90		80		100		90		ns
$t_{c(E)OP}$	Cycle time, duration of programming operation	t_{EHQV1}	6		6		6		6		µs
$t_{c(E)ERB}$	Cycle time, erase operation (boot block)	t_{EHQV2}	0.3		0.3		0.3		0.3		s
$t_{c(E)ERP}$	Cycle time, erase operation (parameter block)	t_{EHQV3}	0.3		0.3		0.3		0.3		s
$t_{c(E)ERM}$	Cycle time, erase operation (main block)	t_{EHQV4}	0.6		0.6		0.6		0.6		s
$t_{d(RPR)}$	Delay time, boot-block relock	t_{PHBR}		200		100		200		100	ns
$t_{h(A)}$	Hold time, A0–A19 (see Note 17)	t_{EHAX}	0		0		0		0		ns
$t_{h(D)}$	Hold time, DQ valid	t_{EHDX}	0		0		0		0		ns
$t_{h(W)}$	Hold time, $\overline{WE}$	t_{EHWH}	0		0		0		0		ns
$t_{h(VPP)}$	Hold time, V_{PP} from valid status-register bit	t_{QVVL}	0		0		0		0		ns
$t_{h(RP)}$	Hold time, $\overline{RP}$ at V_{HH} from valid status-register bit	t_{QVPH}	0		0		0		0		ns
$t_{h(WP)}$	Hold time, $\overline{WP}$ from valid status register bit	t_{WHPL}	0		0		0		0		ns
$t_{su(WP)}$	Setup time, $\overline{WP}$ before write operation	t_{ELPH}	90		50		90		50		ns
$t_{su(A)}$	Setup time, A0–A19 (see Note 17)	t_{AVEH}	90		50		90		50		ns
$t_{su(D)}$	Setup time, DQ	t_{DVEH}	90		50		90		50		ns
$t_{su(W)}$	Setup time, $\overline{WE}$ before write operation	t_{WLEL}	0		0		0		0		ns
$t_{su(RP)}$	Setup time, $\overline{RP}$ at V_{HH} to $\overline{CE}$ going high	t_{PHHEH}	200		100		200		100		ns
$t_{su(VPP)2}$	Setup time, V_{PP} to $\overline{CE}$ going high	t_{VPEH}	200		100		200		100		ns
$t_{w(E)}$	Pulse duration, $\overline{CE}$ low	t_{ELEH}	90		50		90		50		ns
$t_{w(EH)}$	Pulse duration, $\overline{CE}$ high	t_{EHEL}	20		30		20		30		ns
$t_{rec(RPHE)}$	Recovery time, $\overline{RP}$ high to $\overline{CE}$ going low	t_{PHEL}	800		450		800		450		ns

NOTE 17: A_{-1}–A19 for byte-wide

PARAMETER MEASUREMENT INFORMATION



† 3-V range indicates 2.7 V to 3.6 V maximum

Figure 9. Power-Up Timing and Reset Switching

PARAMETER MEASUREMENT INFORMATION

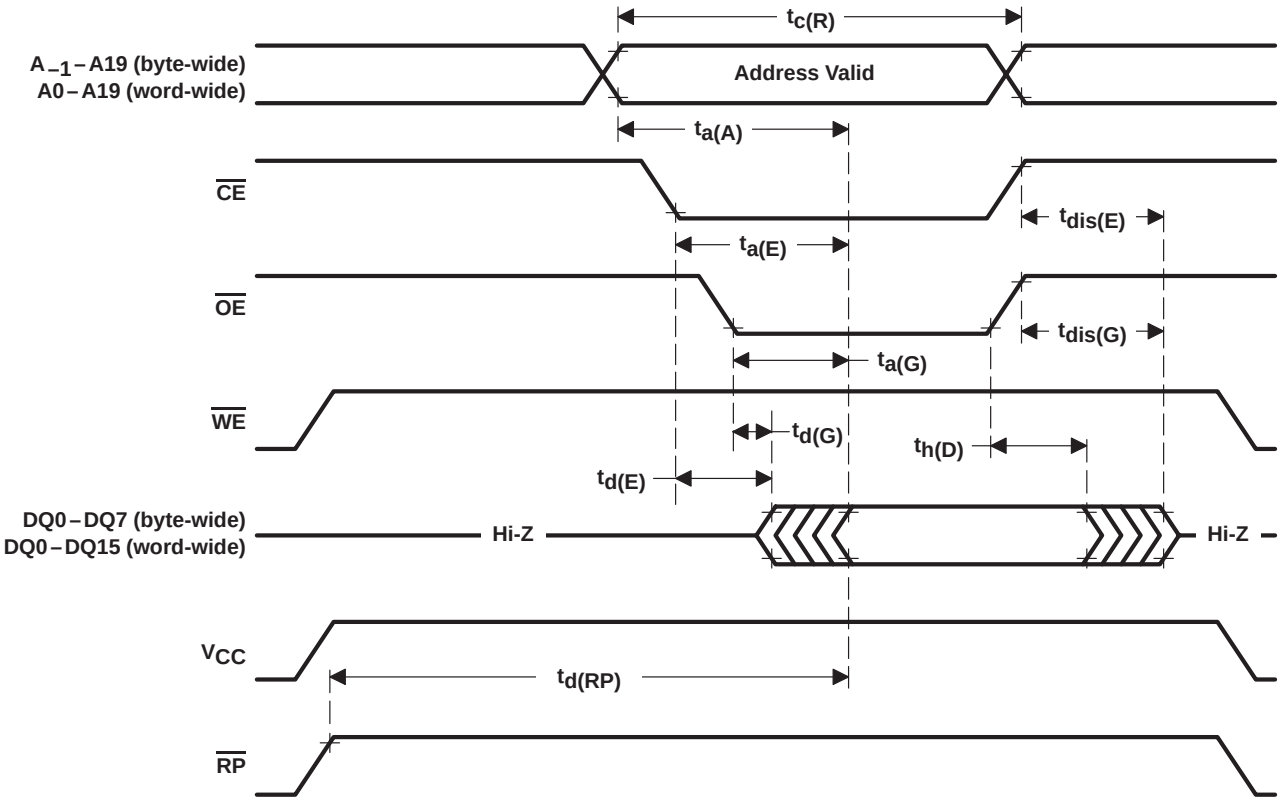
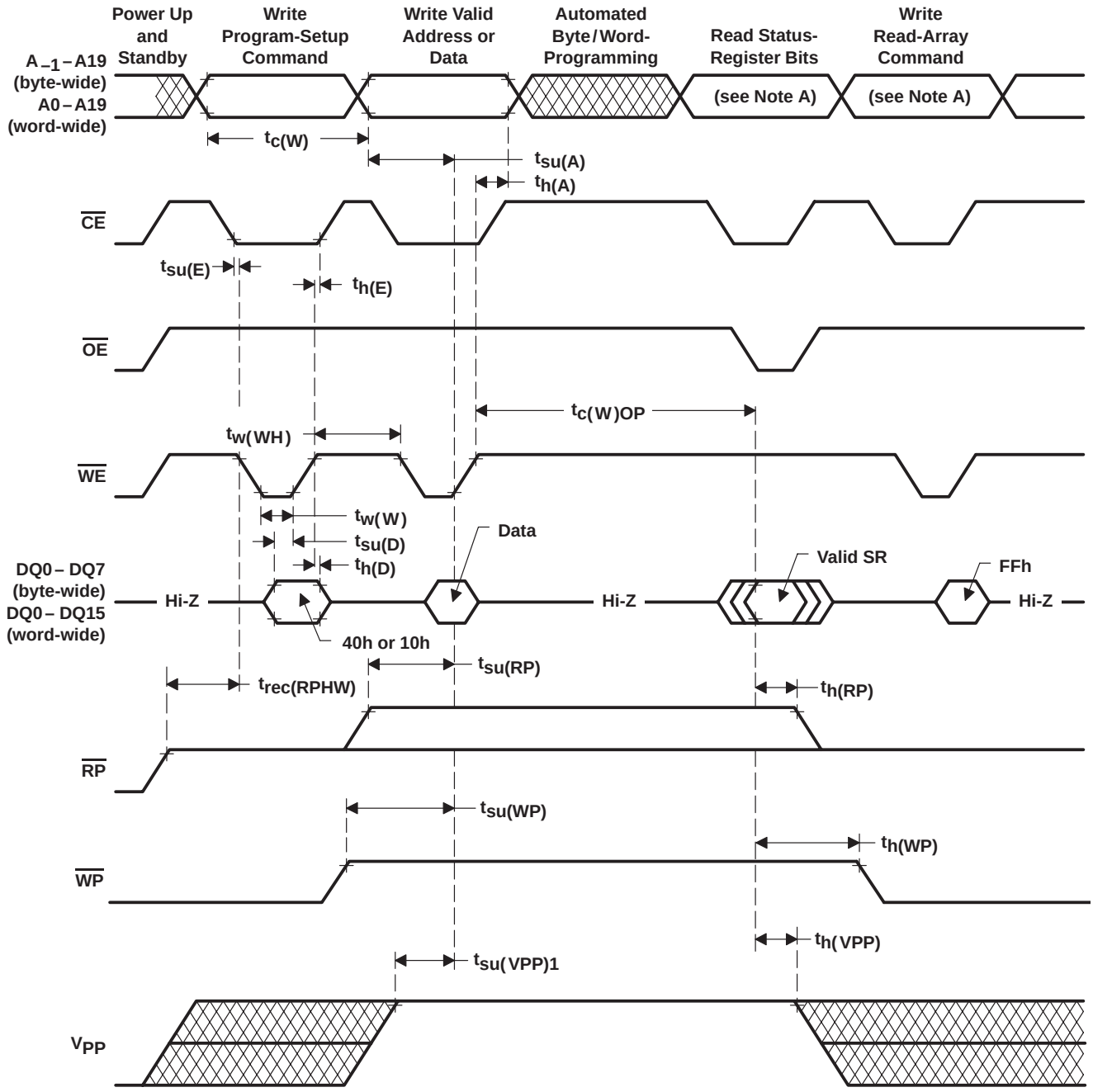


Figure 10. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

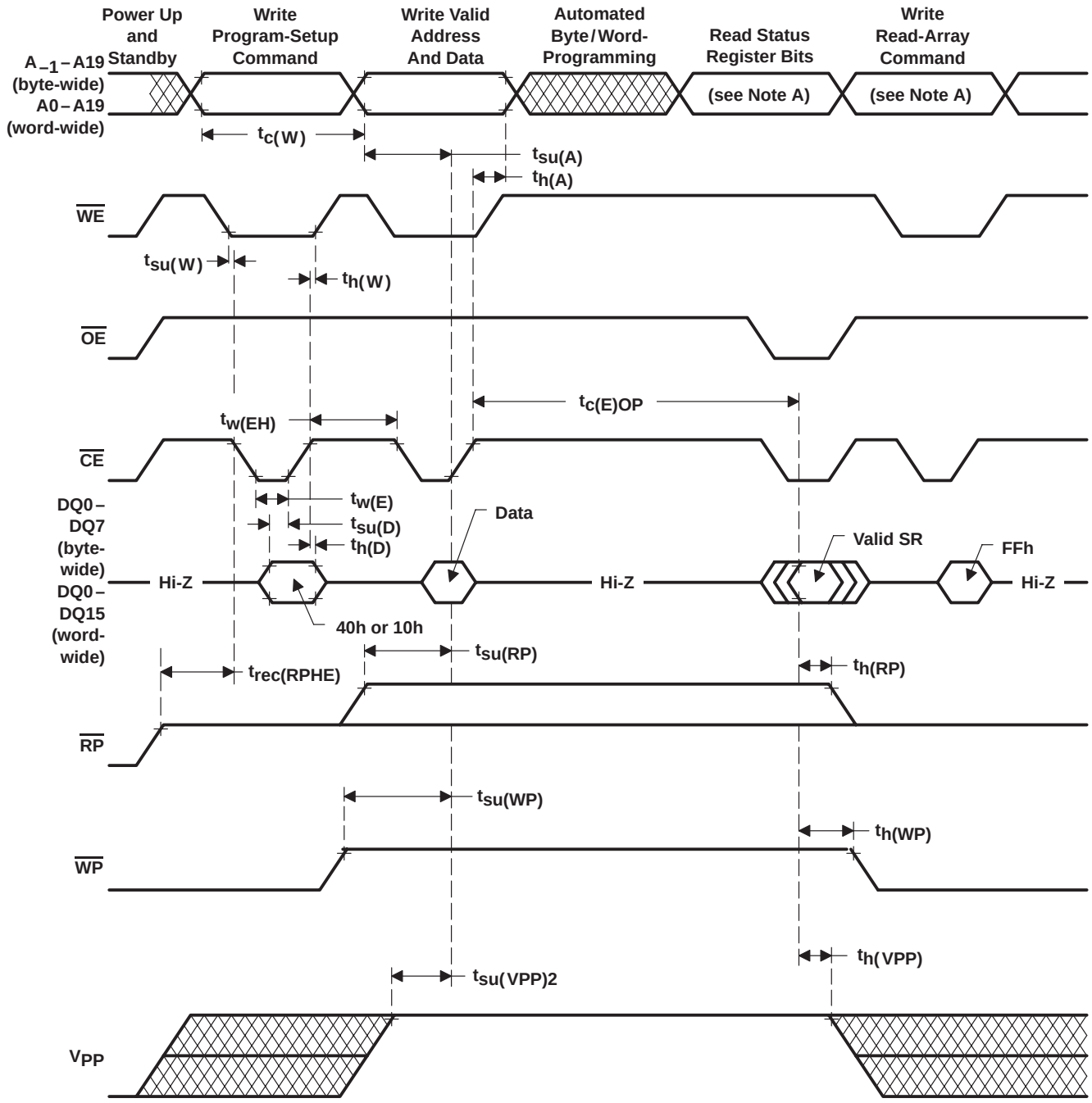


NOTE A: Single-operation mode: Address = Don't Care
Concurrent-operations mode: Address = 0xxxxxh for low-order address memory bank
= 1xxxxxh for high-order address memory bank

Figure 11. Write-Cycle Timing ($\overline{WE}$-Controlled Write)

PRODUCT PREVIEW

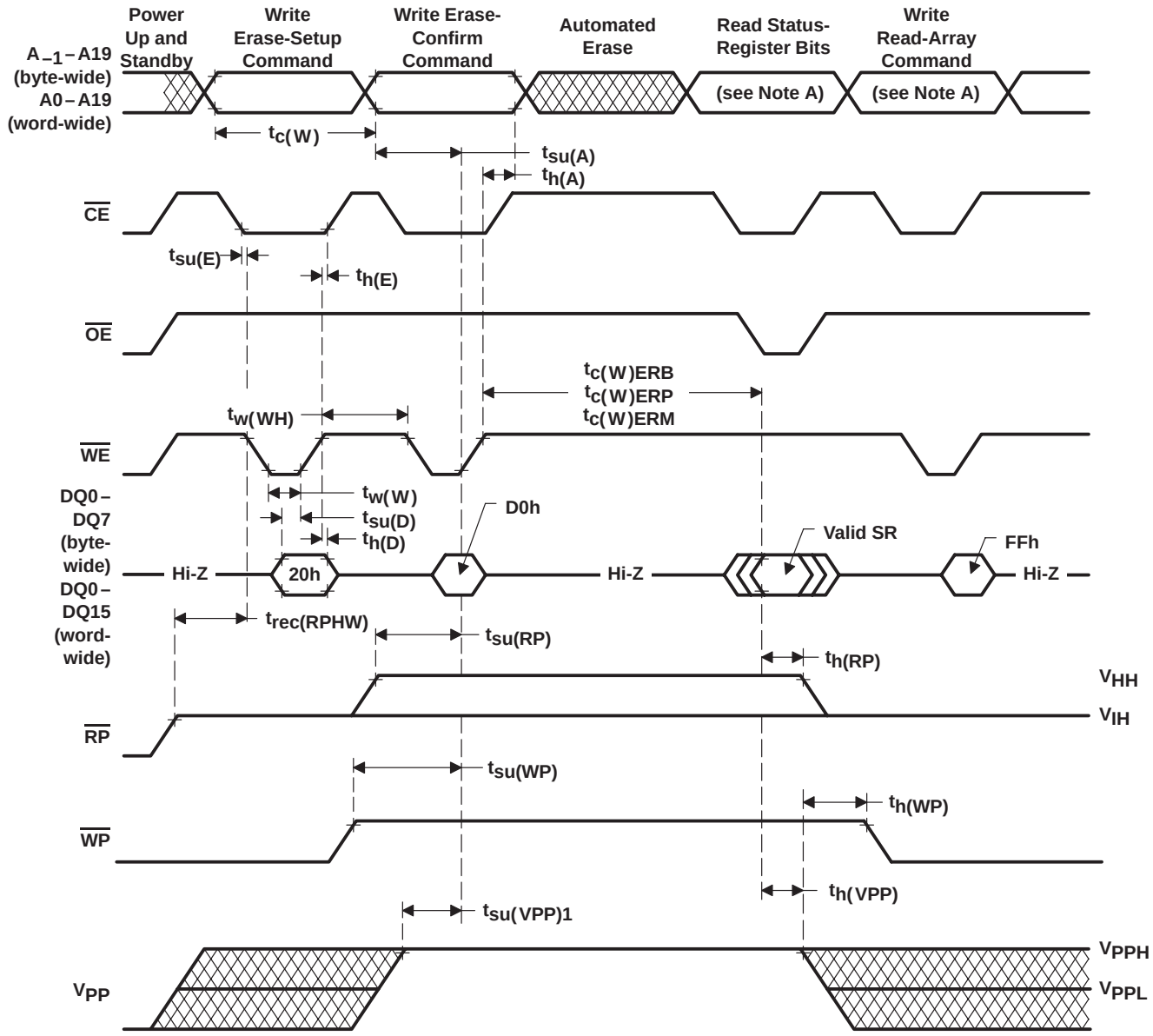
PARAMETER MEASUREMENT INFORMATION



NOTE A: Single-operation mode: Address = Don't Care
Concurrent-operations mode: Address = 0xxxxxh for low-order address memory bank
= 1xxxxxh for high-order address memory bank

Figure 12. Write-Cycle Timing ($\overline{CE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

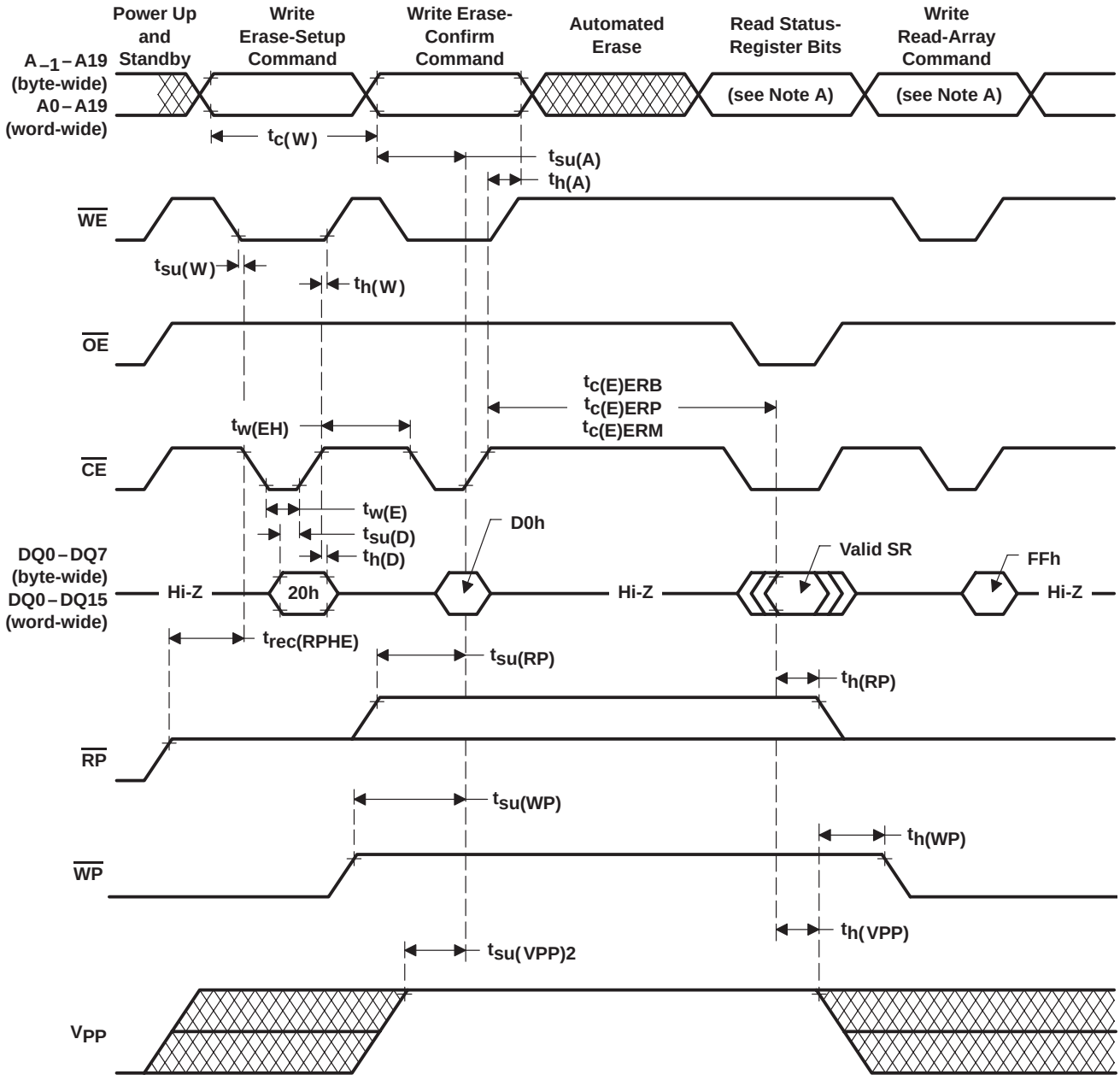


NOTE A: Single-operation mode: Address = Don't Care
Concurrent-operations mode: Address = 0xxxxxh for low-order address memory bank
= 1xxxxxh for high-order address memory bank

Figure 13. Erase-Cycle Timing ($\overline{WE}$-Controlled Write)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Single-operation mode: Address = Don't Care
Concurrent-operations mode: Address = 0xxxxxh for low-order address memory bank
= 1xxxxxh for high-order address memory bank

Figure 14. Erase-Cycle Timing ($\overline{CE}$-Controlled Write)

PARAMETER MEASUREMENT INFORMATION

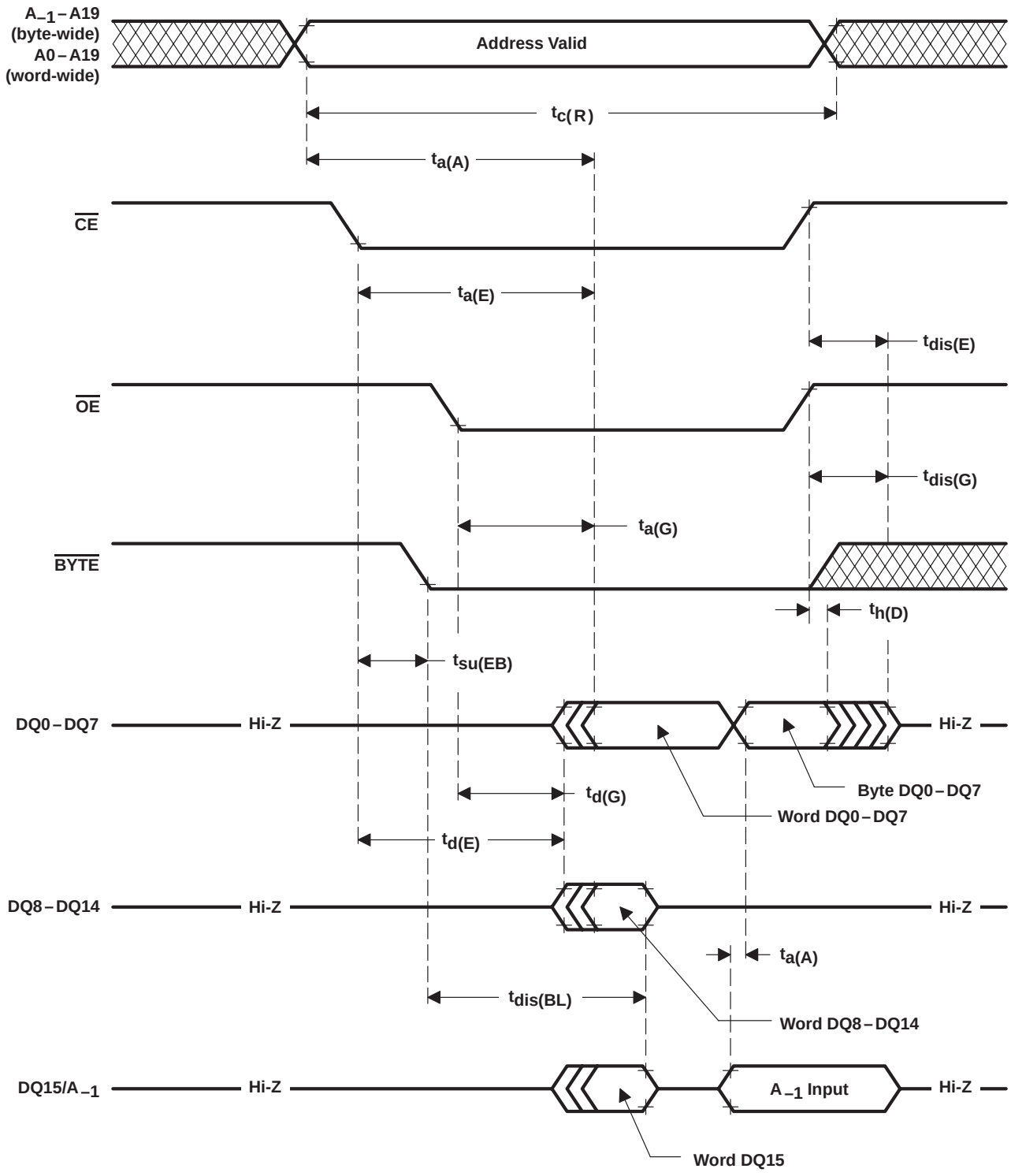


Figure 15. $\overline{\text{BYTE}}$ Timing, Changing From Word-Wide to Byte-Wide Mode

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

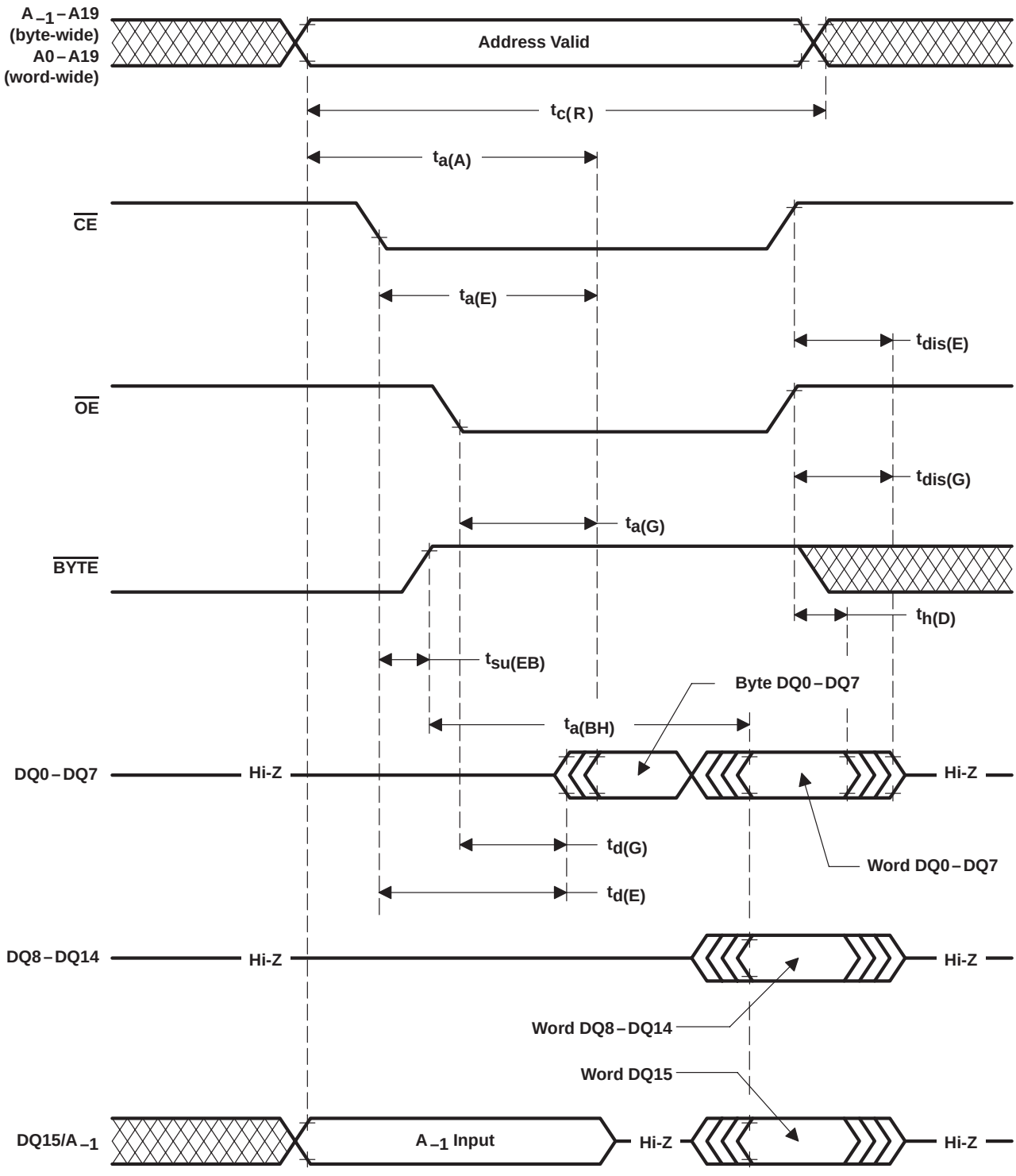
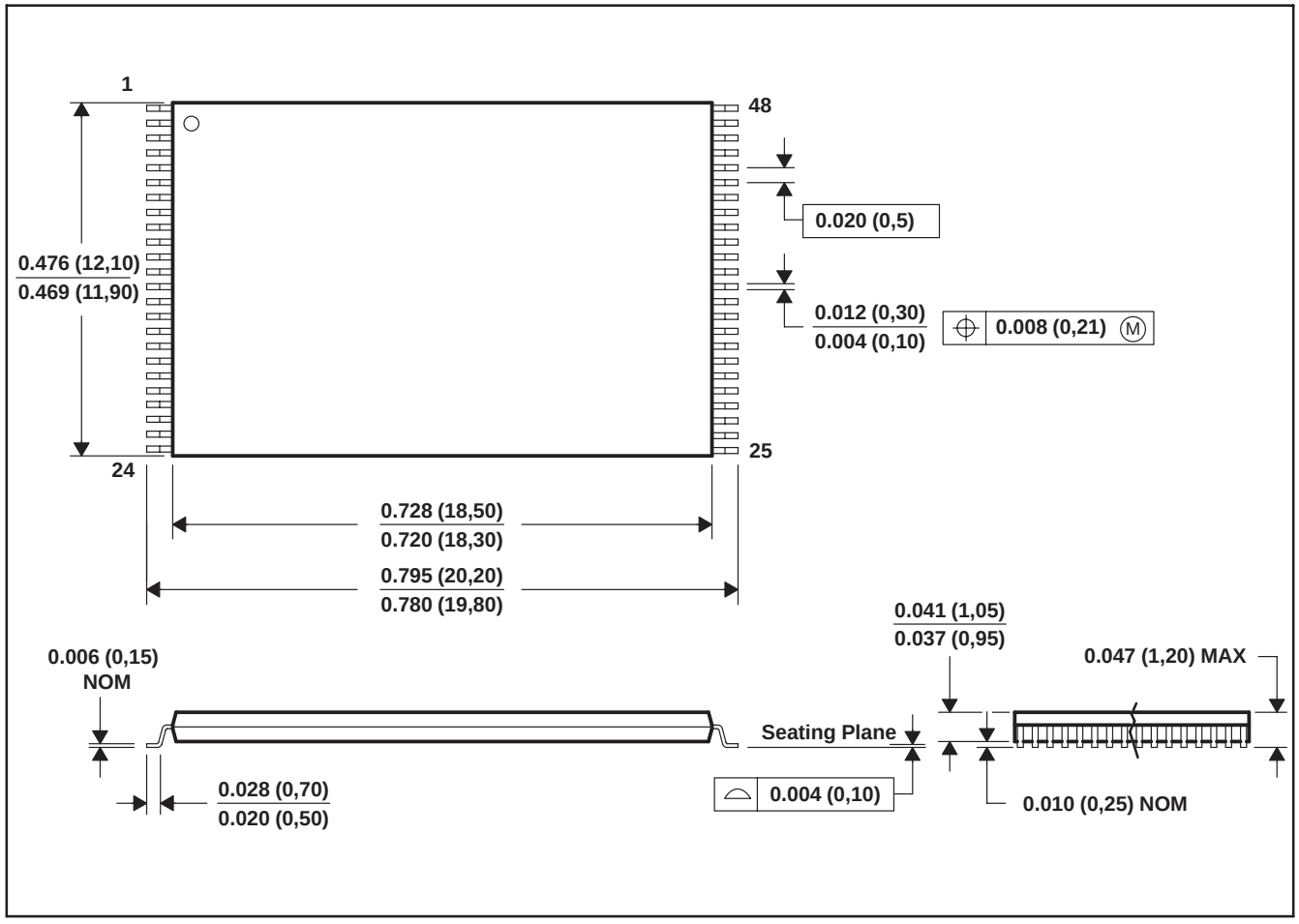


Figure 16. $\overline{\text{BYTE}}$ Timing, Changing From Byte-Wide to Word-Wide Mode

MECHANICAL DATA

DCD (R-PDSO-G48) **PLASTIC DUAL SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

PRODUCT PREVIEW

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