

TPIC5424L H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

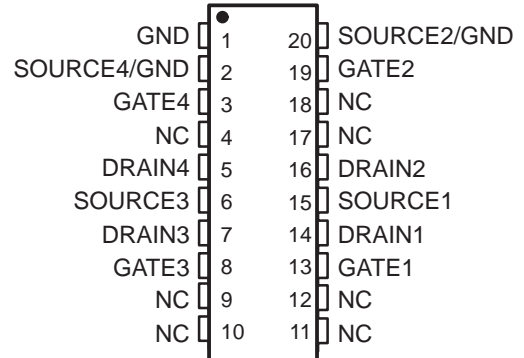
- Low $r_{DS(on)}$. . . 0.4 Ω Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

description

The TPIC5424L is a monolithic logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with a common source.

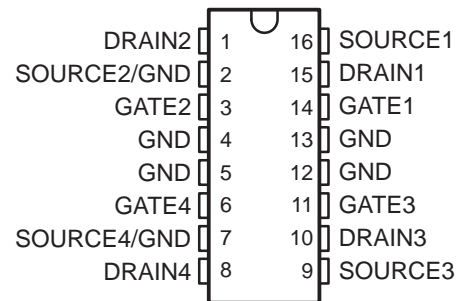
The TPIC5424L is offered in a 16-pin thermally enhanced dual-in-line (NE) package and a 20-pin wide-body surface-mount (DW) package. The TPIC5424L is characterized for operation over the case temperature range of -40°C to 125°C .

DW PACKAGE (TOP VIEW)

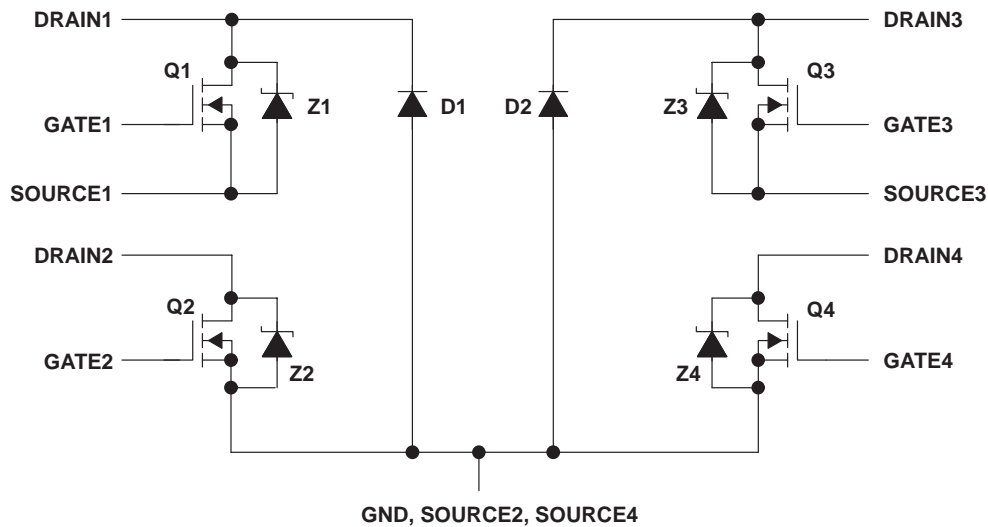


NC – No internal connection

NE PACKAGE (TOP VIEW)



schematic



TPIC5424L

H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage, V_{GS}	± 20 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	1 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	1 A
Pulsed drain current, each output, I_{max} , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figure 4)	180 mJ
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1389 mW	11.1 mW/ $^\circ\text{C}$	279 mW
NE	2075 mW	16.6 mW/ $^\circ\text{C}$	415 mW

TPIC5424L

H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	60			V
$V_{GS(th)}$ Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5 $V_{DS} = V_{GS}$	1.5	1.85	2.2	V
$V_{(BR)}$ Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = $250\ \mu\text{A}$	100			V
$V_{DS(on)}$ Drain-to-source on-state voltage	$I_D = 1\ \text{A}$, $V_{GS} = 5\ \text{V}$, See Notes 2 and 3		0.4	0.48	V
$V_{F(SD)}$ Forward on-state voltage, source-to-drain	$I_S = 1\ \text{A}$, $V_{GS} = 0$ (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12		1	1.2	V
V_F Forward on-state voltage, GND-to-drain	$I_D = 1\ \text{A}$ (D1, D2), See Notes 2 and 3		4.6		V
I_{DSS} Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	μA
		$T_C = 125^\circ\text{C}$	0.5	10	
I_{GSSF} Forward gate current, drain short circuited to source	$V_{GS} = 5\ \text{V}$, $V_{DS} = 0$		10	100	nA
I_{GSSR} Reverse gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$, $V_{DS} = 0$		10	100	nA
I_{lkg} Leakage current, drain-to-GND	$V_{DGND} = 48\ \text{V}$ (D1, D2)	$T_C = 25^\circ\text{C}$	0.05	1	μA
		$T_C = 125^\circ\text{C}$	0.5	10	
$r_{DS(on)}$ Static drain-to-source on-state resistance	$V_{GS} = 5\ \text{V}$, $I_D = 1\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.4	0.48	Ω
		$T_C = 125^\circ\text{C}$	0.65	0.68	
g_{fs} Forward transconductance	$V_{DS} = 15\ \text{V}$, $I_D = 0.5\ \text{A}$, See Notes 2 and 3 and Figure 9	1.25	1.39		S
C_{iss} Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$, See Figure 11		220	275	pF
C_{oss} Short-circuit output capacitance, common source			120	150	
C_{rss} Short-circuit reverse-transfer capacitance, common source			100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{rr}	Reverse-recovery time	I _S =0.5 A, V _{GS} = 0, See Figures 1 and 14	V _{DS} = 48 V, di/dt = 100 A/μs,	Z1 and Z3	55		ns
				Z2 and Z4	150		
				D1 and D2	200		
Q _{RR}	Total diode charge			Z1 and Z3	0.06		μC
				Z2 and Z4	0.3		
				D1 and D2	0.7		

TPIC5424L

H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

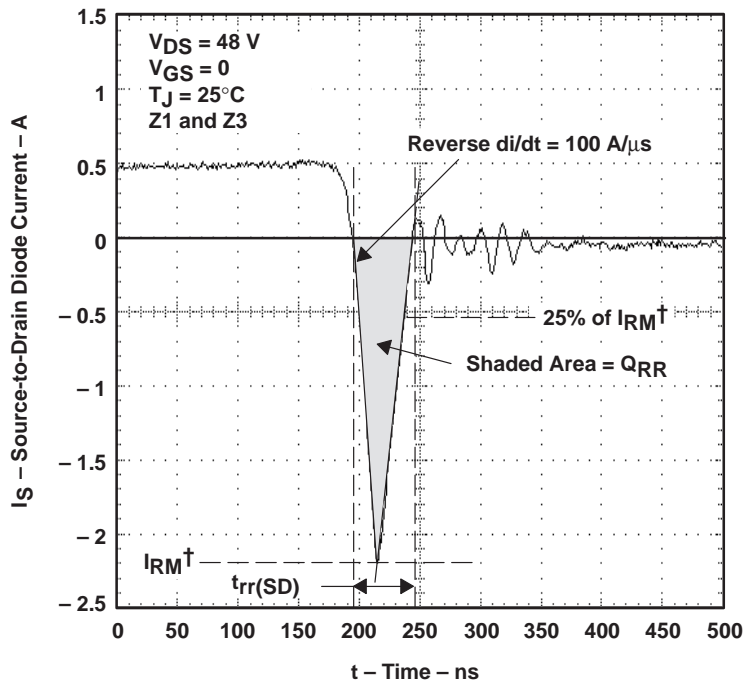
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $R_L = 25\ \Omega$, $t_{en} = 10\text{ ns}$, $t_{dis} = 10\text{ ns}$, See Figure 2		34	68	ns
$t_{d(off)}$ Turn-off delay time			40	82	
t_r Rise time			21	42	
t_f Fall time			25	50	
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, See Figure 3		3.9	5	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.55	0.8	
Q_{gd} Gate-to-drain charge			2.5	3.6	
L_D Internal drain inductance			5		nH
L_S Internal source inductance			5		
R_g Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance (see Note 4)	DW package		90		$^\circ\text{C/W}$
	NE package		60		
$R_{\theta JP}$ Junction-to-pin thermal resistance	DW package		30		$^\circ\text{C/W}$
	NE package		25		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$ = maximum recovery current

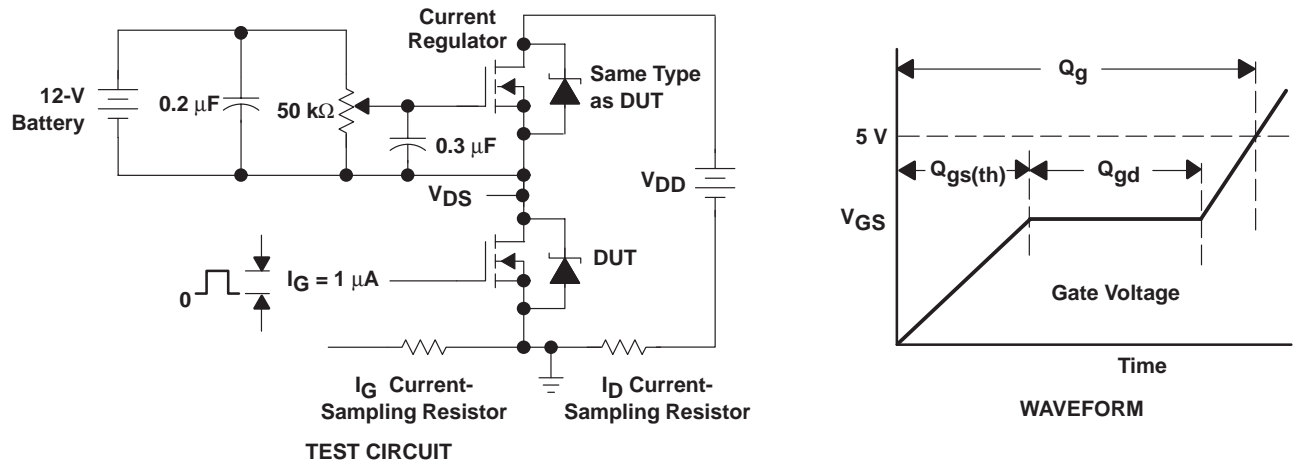
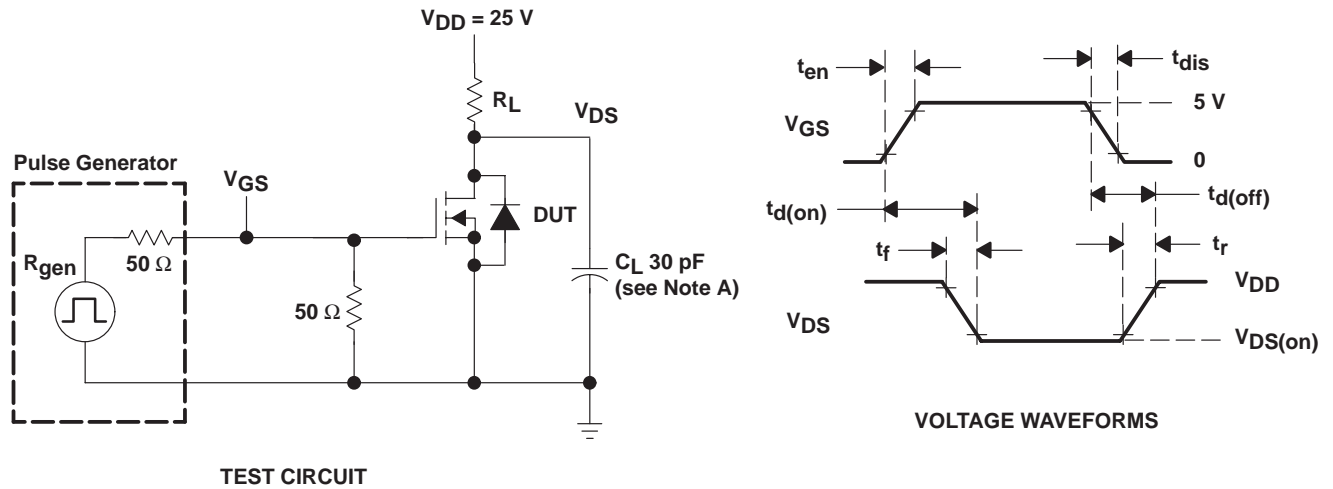
NOTE A. The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

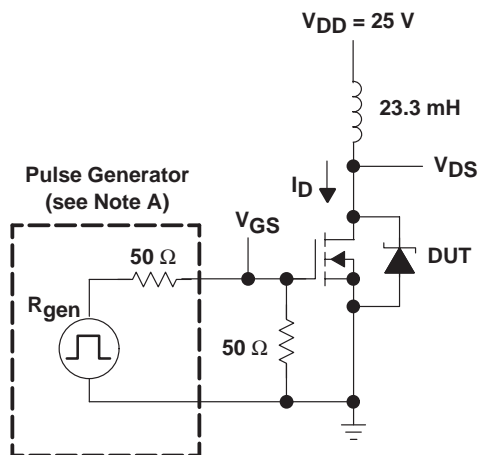


TPIC5424L

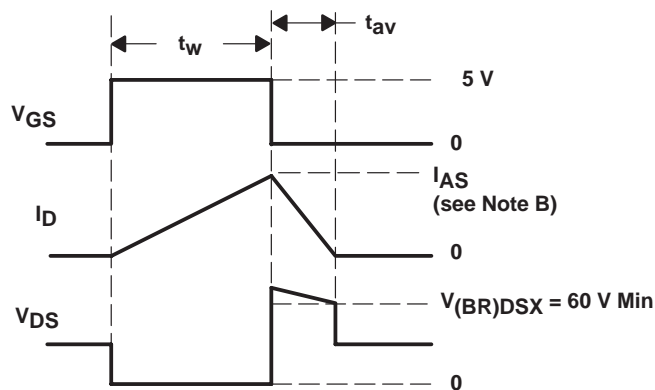
H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180 \text{ mJ.}$$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

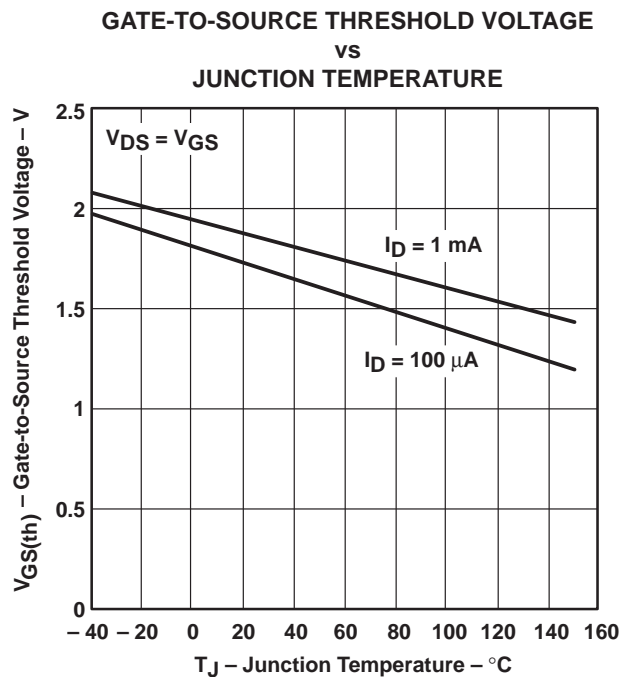


Figure 5

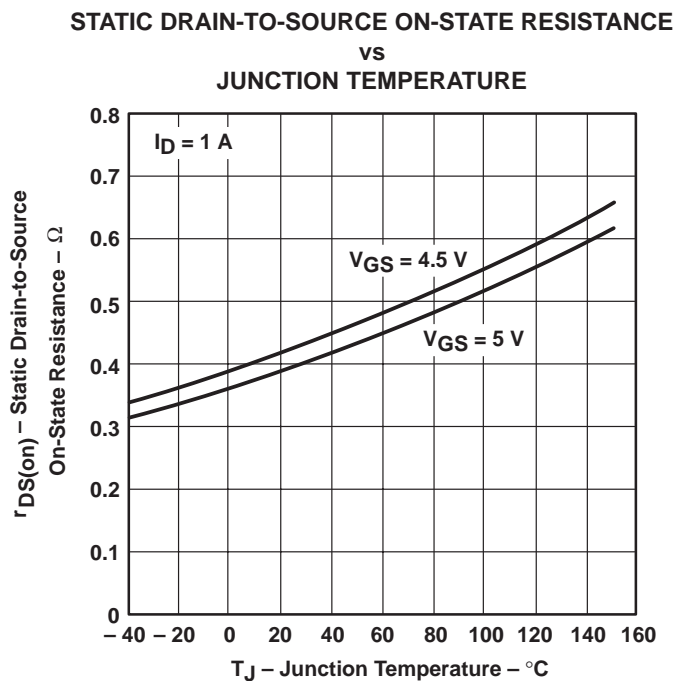


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

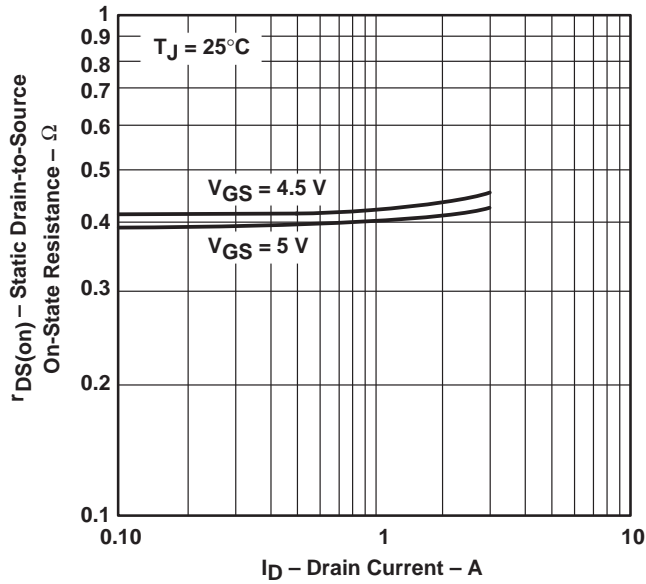


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

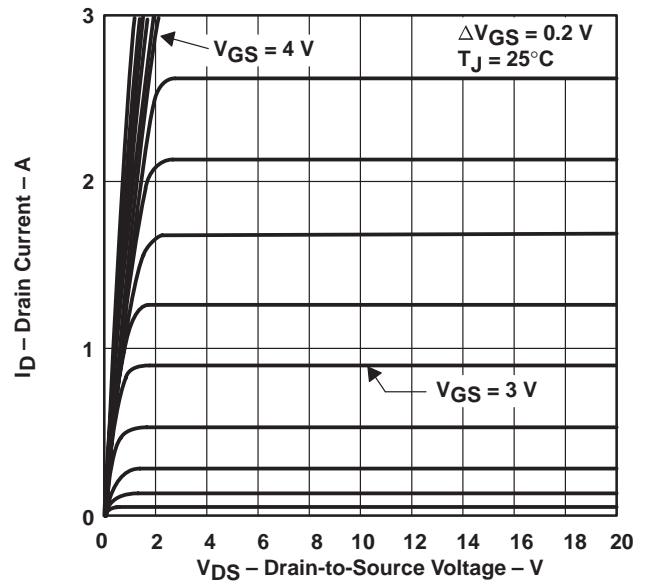


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

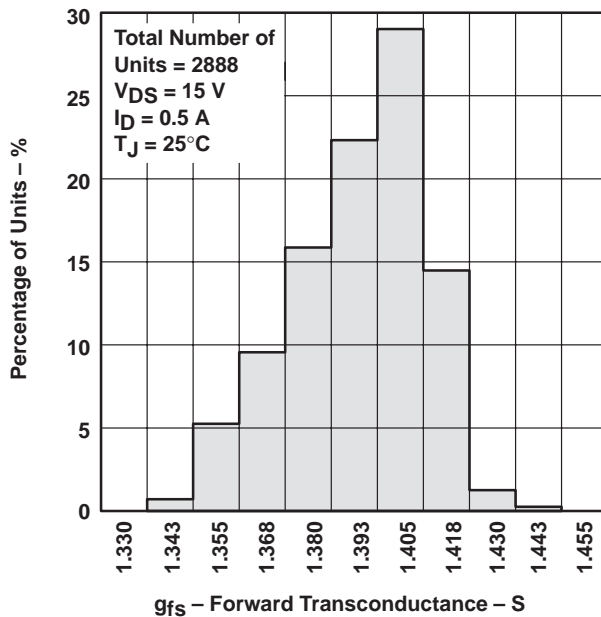


Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

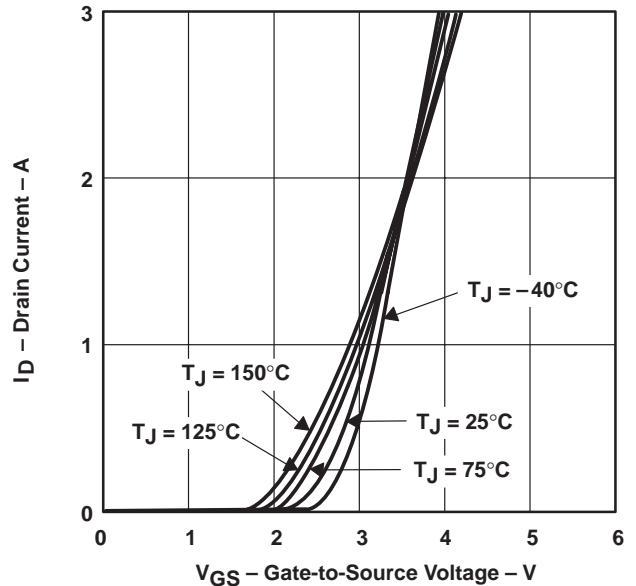


Figure 10

TPIC5424L

H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

TYPICAL CHARACTERISTICS

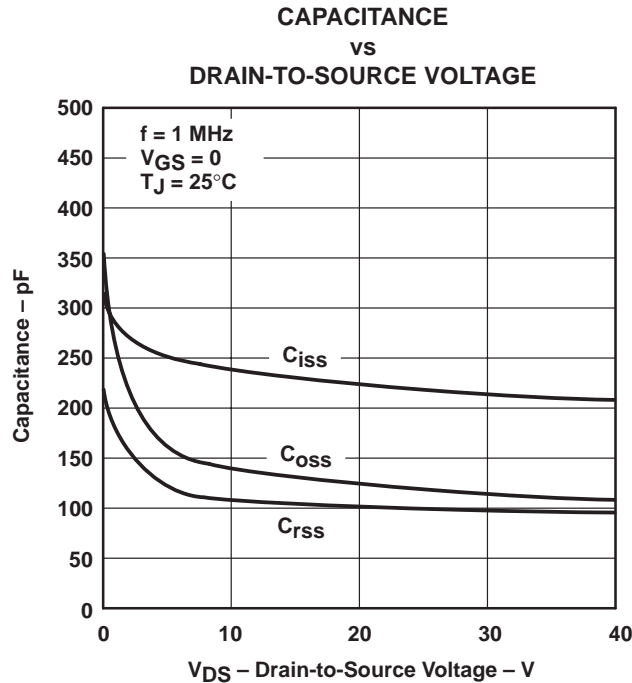


Figure 11

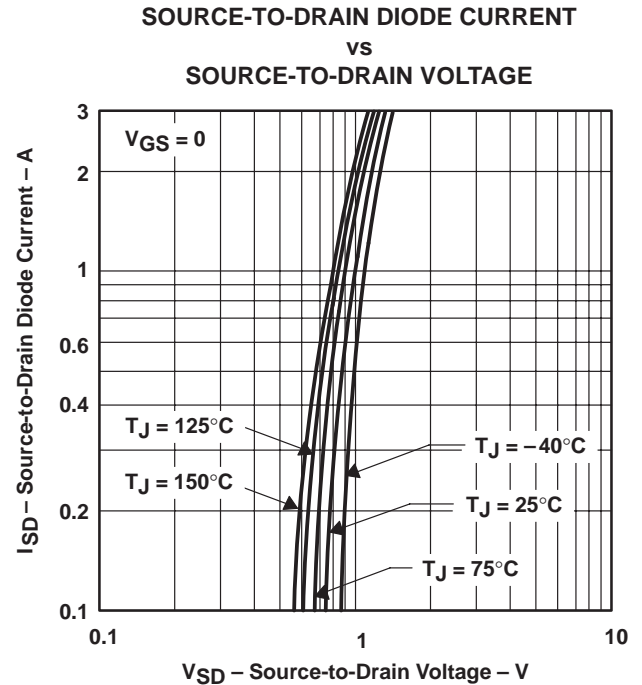


Figure 12

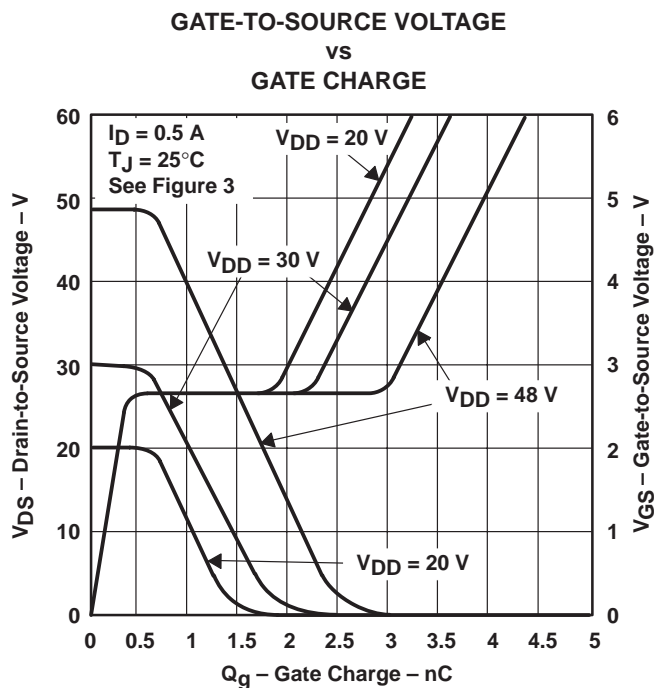


Figure 13

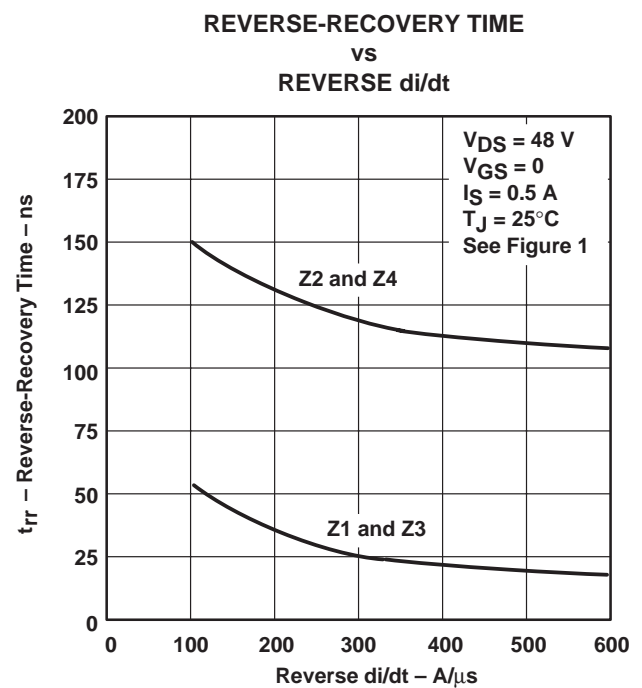
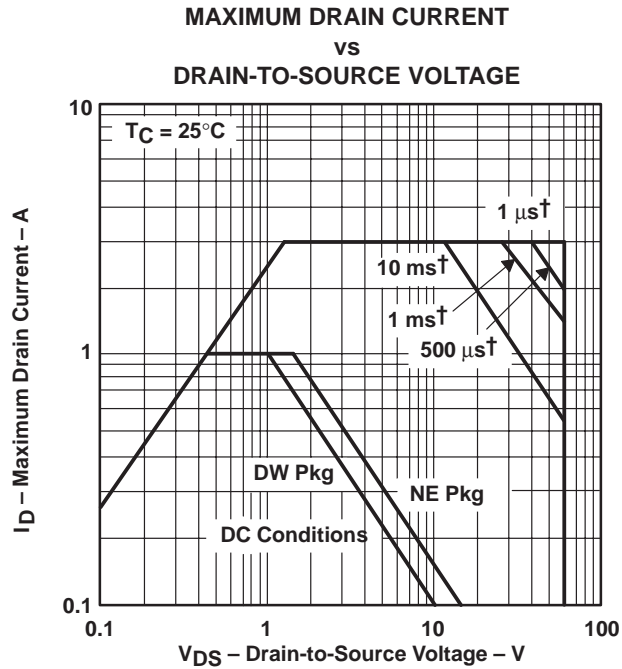


Figure 14

THERMAL INFORMATION



† Less than 2% duty cycle

Figure 15

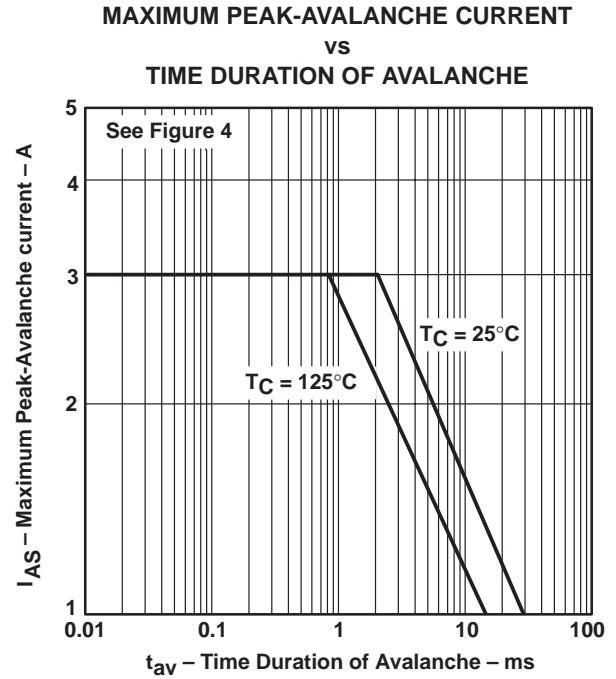


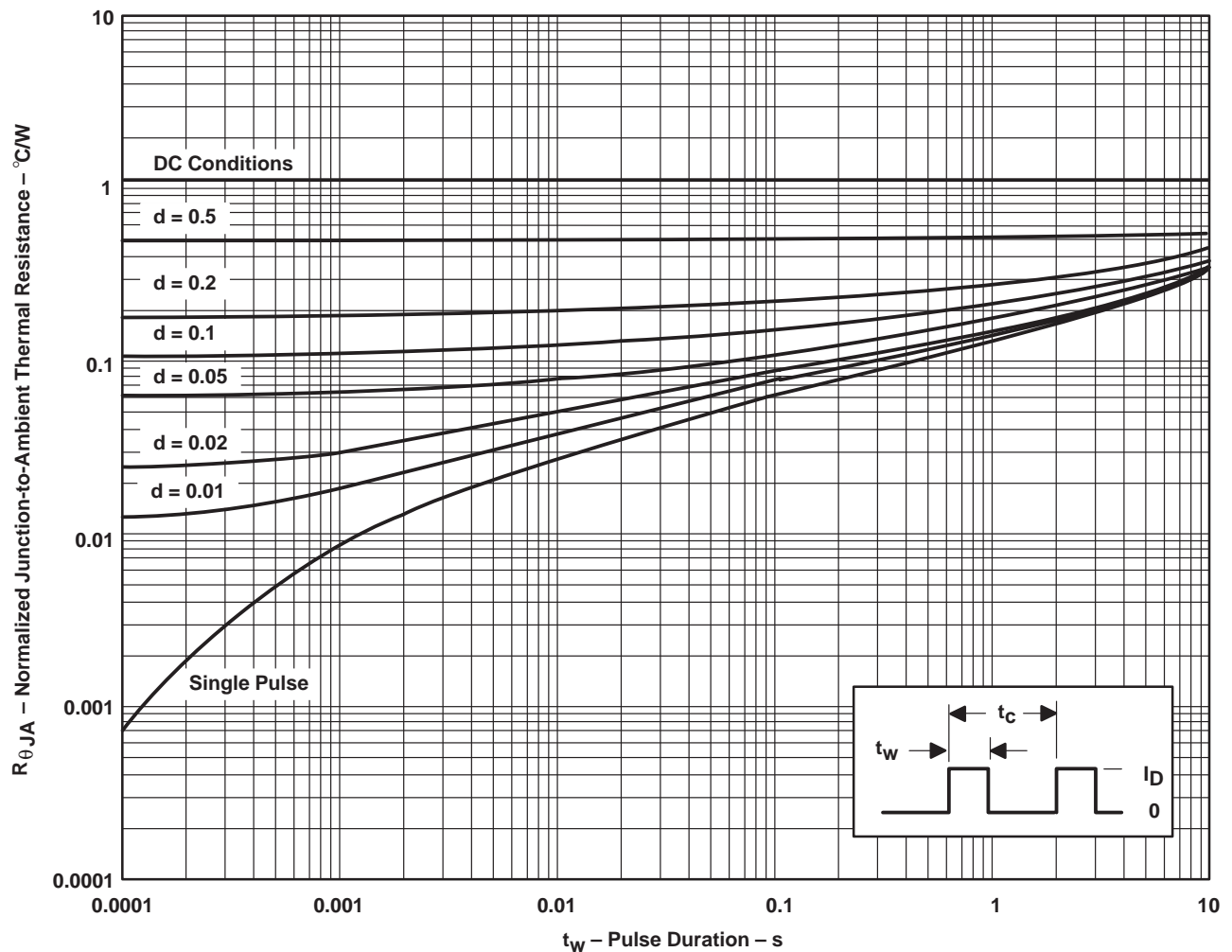
Figure 16

TPIC5424L H-BRIDGE LOGIC-LEVEL POWER DMOS ARRAY

SLIS026A – JUNE 1994 – REVISED NOVEMBER 1994

THERMAL INFORMATION

NE PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t) R_{\theta JA}$

t_W = pulse duration

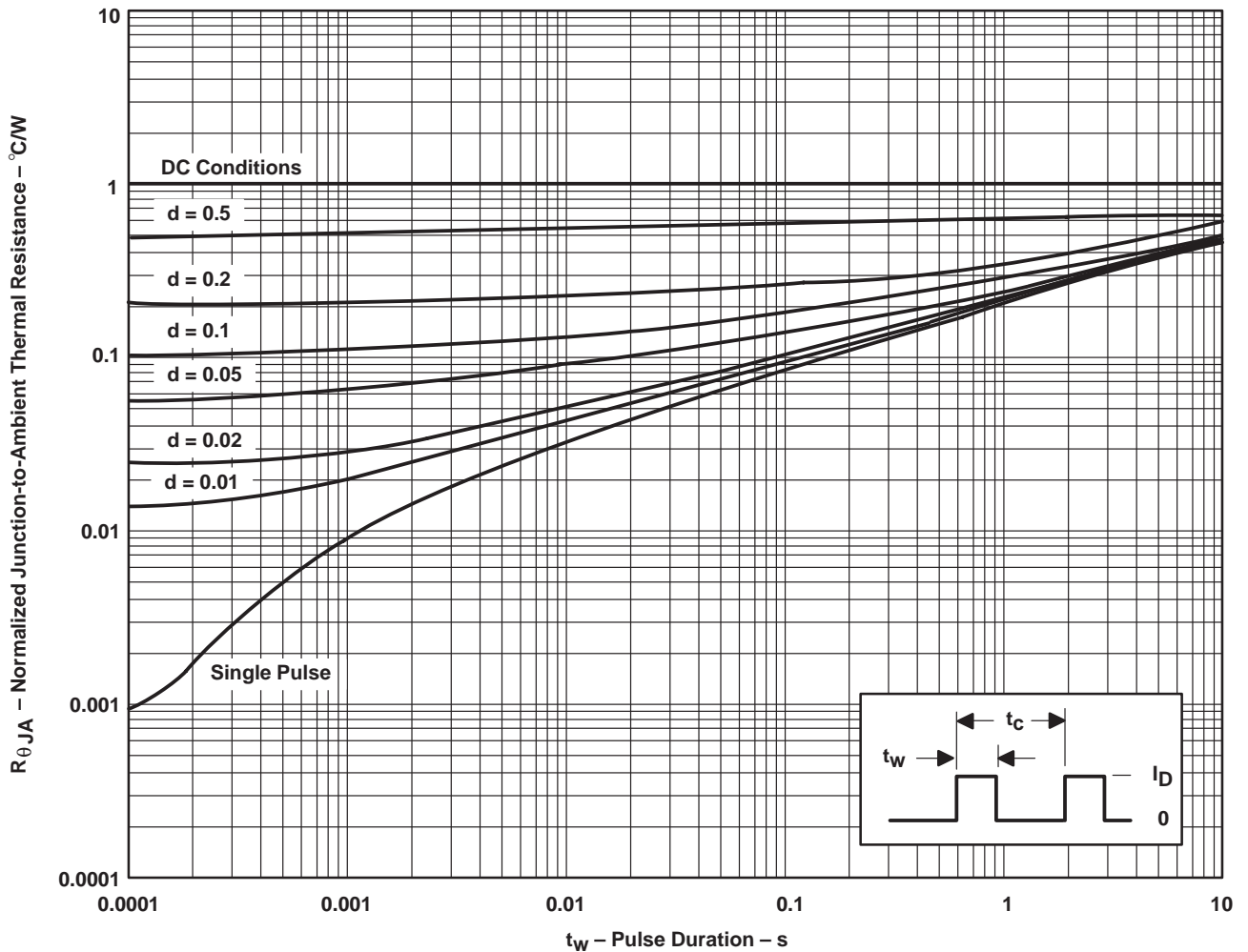
t_C = cycle time

d = duty cycle = t_W/t_C

Figure 17

THERMAL INFORMATION

DW PACKAGE† NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE VS PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t) R_{\theta JA}$
 t_W = pulse duration
 t_C = cycle time
 d = duty cycle = t_W/t_C

Figure 18

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.