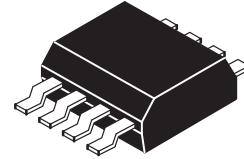
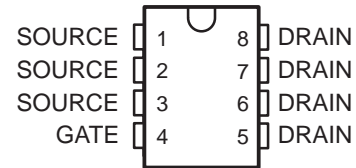


# TPS1110, TPS1110Y SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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- Low  $r_{DS(on)}$  . . . 65 m $\Omega$  Typ at  $V_{GS} = -4.5$  V
- High Current Capability  
6 A at  $V_{GS} = -4.5$  V
- Logic-Level Gate Drive (3 V Compatible)  
 $V_{GS(th)} = -0.9$  V Max
- Low Drain-Source Leakage Current  
<100 nA From 25°C to 75°C  
at  $V_{DS} = -6$  V
- Fast Switching . . . 5.8 ns Typ  $t_{d(on)}$
- Small-Outline Surface-Mount Power Package

D PACKAGE  
(TOP VIEW)



## description

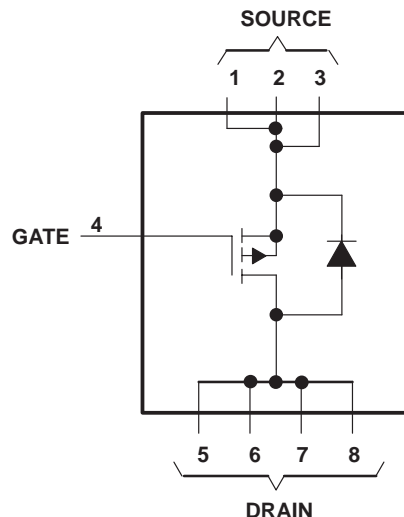
The TPS1110 is a single, low- $r_{DS(on)}$ , P-channel enhancement-mode power MOS transistor. The device features extremely low- $r_{DS(on)}$  values coupled with logic-level gate-drive capability and very low drain-source leakage current. With a maximum  $V_{GS(th)}$  of  $-0.9$  V and an  $I_{DSS}$  of only  $-100$  nA, the TPS1110 is the ideal high-side switch for low-voltage, portable battery-management power-distribution systems where maximizing battery life is an important concern. The thermal performance of the 8-pin small-outline (D) package has been greatly enhanced over the standard 8-pin SOIC, further making the TPS1110 ideally suited for many power applications. For compatibility with existing designs, the TPS1110 has a pinout common with other P-channel MOSFETs in small-outline integrated circuit (SOIC) packages. The TPS1110 is characterized for an operating junction temperature range,  $T_J$ , from  $-40^\circ\text{C}$  to  $150^\circ\text{C}$ . The D package is available packaged in standard sleeves or in taped and reeled formats. When ordering the tape-and-reel format, add an R suffix to the device type number (e.g., TPS1110DR).

AVAILABLE OPTIONS

$T_J$	PACKAGED DEVICE†	CHIP FORM (Y)
	SMALL OUTLINE (D)	
$-40^\circ\text{C}$ to $150^\circ\text{C}$	TPS1110D	TPS1110Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1110DR). The chip form is tested at  $25^\circ\text{C}$ .

## schematic



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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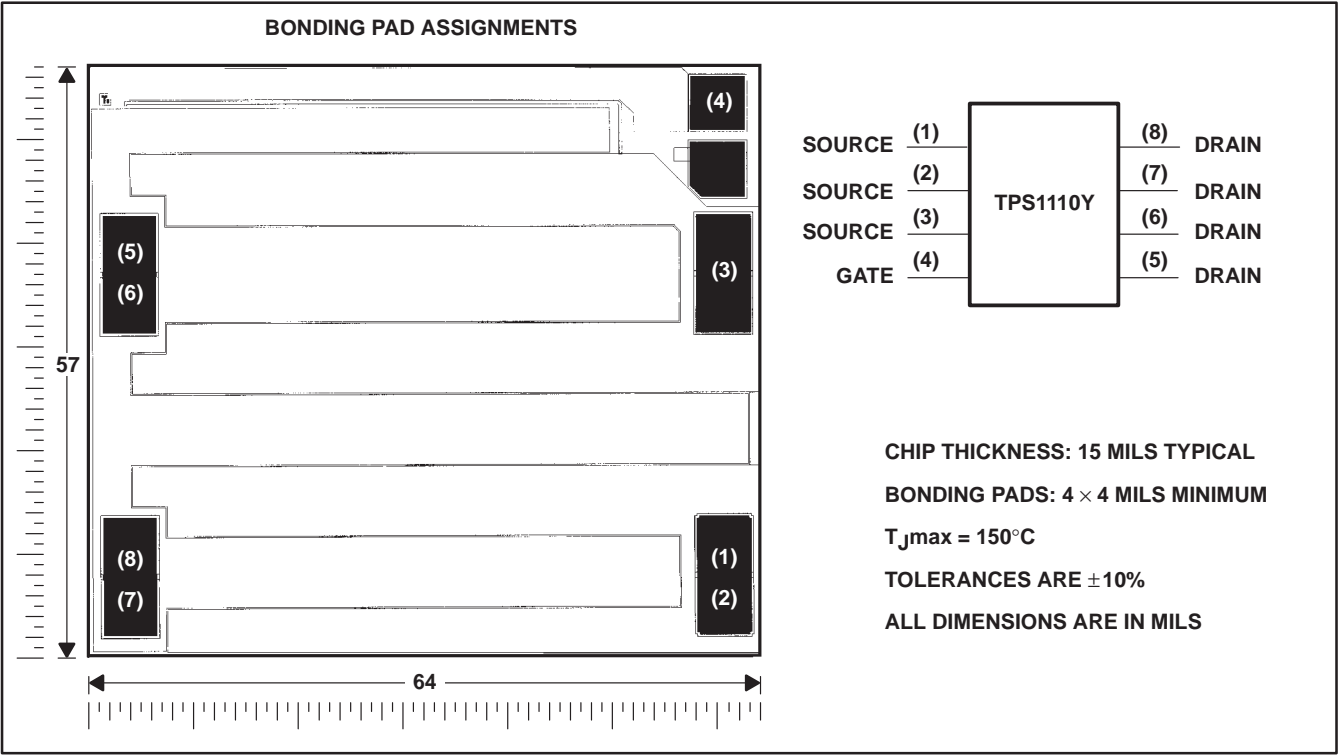
# TPS1110, TPS1110Y

## SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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### TPS1110Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1110C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.



# TPS1110, TPS1110Y SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

				UNIT
Drain-to-source voltage, $V_{DS}$			-7	V
Gate-to-source voltage, $V_{GS}$			$\pm 7$	V
Continuous drain current, $I_D$	$V_{GS} = -2.7\text{ V}$	$T_P = 25^\circ\text{C}^\ddagger$	-5	A
		$T_P = 125^\circ\text{C}^\ddagger$	-2.3	
	$V_{GS} = -4.5\text{ V}$	$T_P = 25^\circ\text{C}^\ddagger$	-6	
		$T_P = 125^\circ\text{C}^\ddagger$	-2.7	
Pulse drain current, $I_D$		$T_A = 25^\circ\text{C}$	-24	A
Continuous source current (diode conduction), $I_S$		$T_A = 25^\circ\text{C}$	-6	A
Continuous total power dissipation		$T_P = 25^\circ\text{C}^\ddagger$	4	W
Junction-to-pin thermal resistance ( $\theta_{JP}$ )			31	$^\circ\text{C}/\text{W}$
Continuous total power dissipation		$T_A = 25^\circ\text{C}$	1.25	W
Junction-to-ambient thermal resistance ( $\theta_{JA}$ )			100	$^\circ\text{C}/\text{W}$
Storage temperature range, $T_{stg}$			-65 to 150	$^\circ\text{C}$
Operating junction temperature range, $T_J$			-40 to 150	$^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	$^\circ\text{C}$

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup>  $T_P$  – Temperature of drain pins measured close to the package

## electrical characteristics at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

### static

PARAMETER		TEST CONDITIONS		TPS1110			TPS1110Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , See Figure 9 I <sub>D</sub> = −250 μA,		−0.5	−0.75	−0.9	−0.75			V
V <sub>SD</sub>	Source-to-drain voltage (diode forward voltage)§	I <sub>SD</sub> = −3 A, See Figure 8 V <sub>GS</sub> = 0 V,		−0.8			−0.8			V
I <sub>GSS</sub>	Reverse gate current, drain short circuited to source	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = −6 V		±100						nA
I <sub>DSS</sub>	Zero-gate-voltage drain current	V <sub>DS</sub> = −7 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C	−100						nA
		V <sub>DS</sub> = −6 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 75°C	−100						nA
			T <sub>J</sub> = 125°C	−10						μA
r <sub>DS(on)</sub>	Static drain-to-source on-state resistance§	V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −6 A, See Figure 5		65	75	65			mΩ	
		V <sub>GS</sub> = −2.7 V, I <sub>D</sub> = −2 A, See Figure 5		100	110	100				
g <sub>fs</sub>	Forward transconductance§	V <sub>DS</sub> = −5 V,	I <sub>D</sub> = −6 A	5			5			S
C <sub>iss</sub>	Short-circuit input capacitance, common source	V <sub>DS</sub> = −6 V, V <sub>GS</sub> = 0 V, f = 1 MHz See Figure 6		275			275			pF
C <sub>oss</sub>	Short-circuit output capacitance, common source			415			415			
C <sub>rss</sub>	Short-circuit reverse transfer capacitance, common source			73			73			

<sup>§</sup> Pulse test: pulse duration  $\leq 300$   $\mu\text{s}$ , duty cycle  $\leq 2\%$



# TPS1110, TPS1110Y SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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## dynamic

PARAMETER	TEST CONDITIONS	TPS1110			TPS1110Y			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$Q_g$ Total gate charge	$V_{DS} = -6\text{ V}$ , $V_{GS} = -6\text{ V}$ , $I_D = -3\text{ A}$ See Figures 1 and 10	4.3	5.4		4.3			nC
$Q_{gs}$ Gate-to-source charge		0.66	0.83		0.66			
$Q_{gd}$ Gate-to-drain charge		0.52	0.68		0.52			
$t_{d(on)}$ Turn-on delay time	$V_{DD} = -6\text{ V}$ , $R_L = 6\ \Omega$ , $I_D = -1\text{ A}$ , $R_G = 6\ \Omega$ , See Figure 2	5.8	8		5.8			ns
$t_{d(off)}$ Turn-off delay time		22	29		22			ns
$t_r$ Rise time		22	29		22			ns
$t_f$ Fall time		4.5	7		4.5			
$t_{rr(SD)}$ Source-to-drain reverse-recovery time	$V_{DS} = -6\text{ V}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $I_D = -3\text{ A}$	65	98		65			nC
$Q_{rr}$ Total diode charge		71			71			

## PARAMETER MEASUREMENT INFORMATION

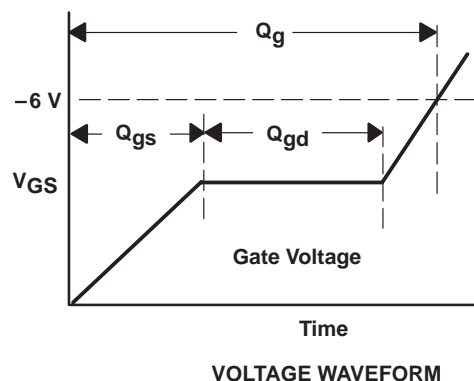
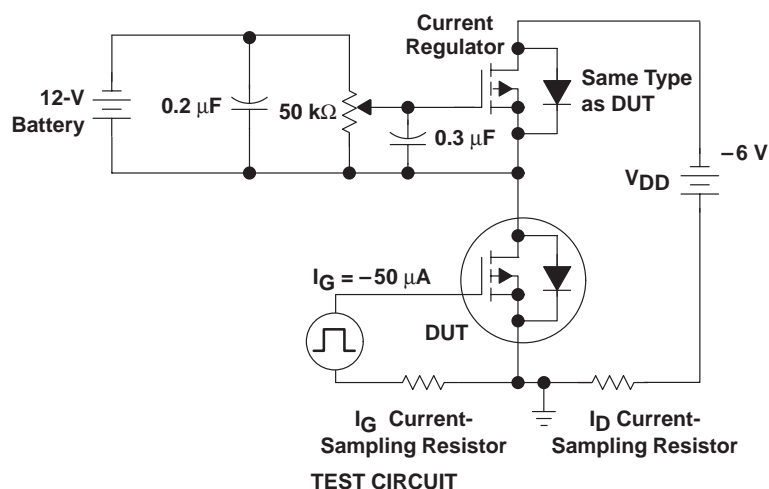


Figure 1. Gate-Charge Test Circuit and Waveform

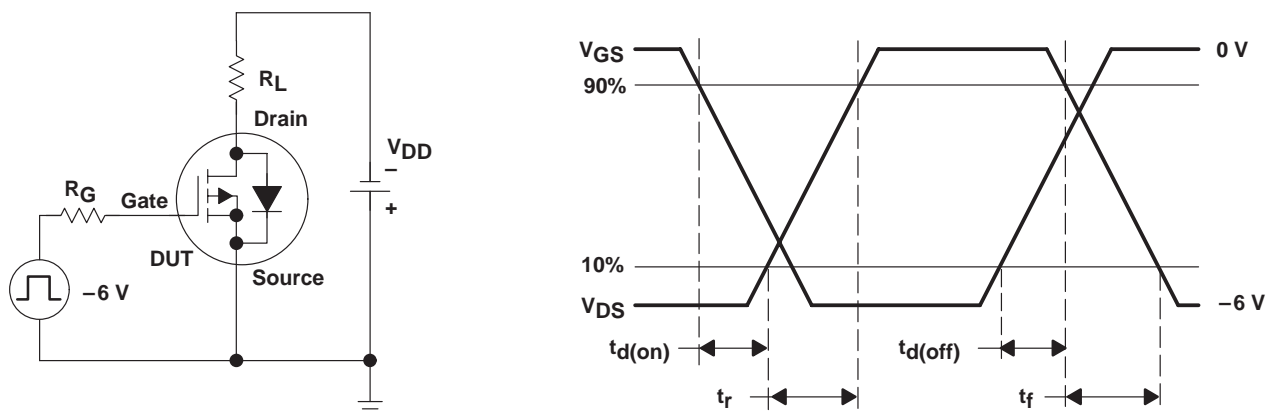


Figure 2. Resistive Switching

TPS1110, TPS1110Y

SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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TYPICAL CHARACTERISTICS

Table of Graphs

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Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Gate-to-source threshold voltage	vs Junction temperature	9
Gate-to-source voltage	vs Gate charge	10

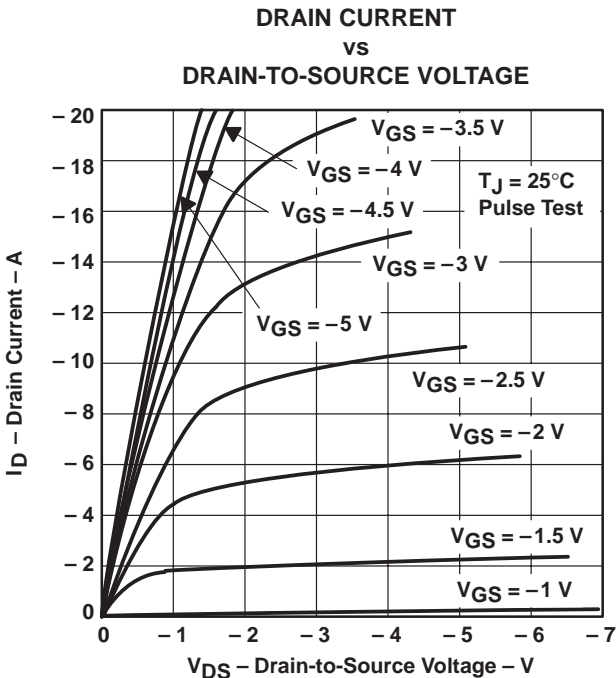


Figure 3

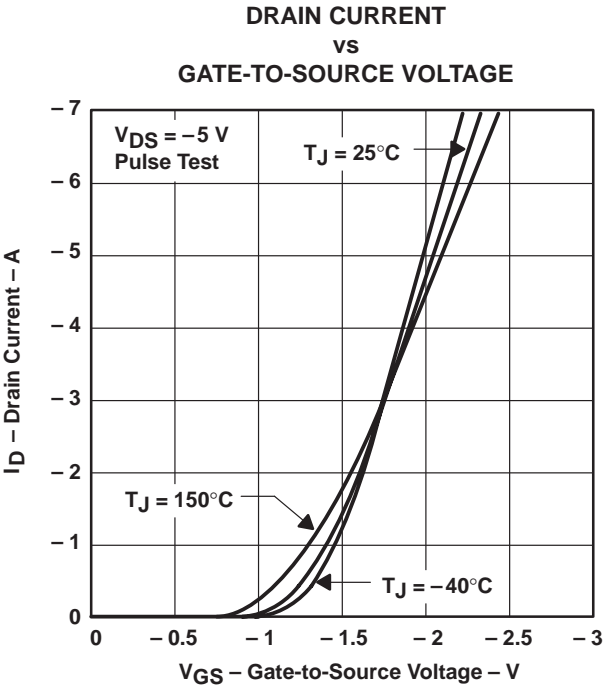


Figure 4

# TYPICAL CHARACTERISTICS

## STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

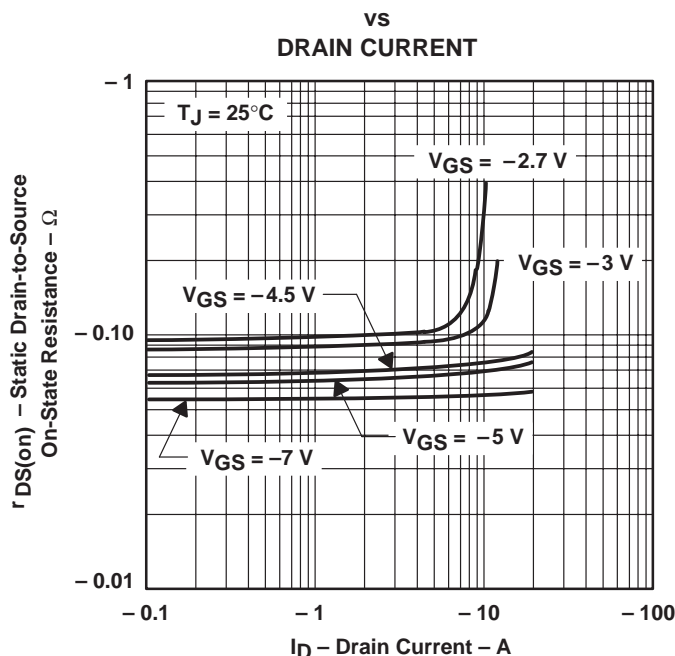
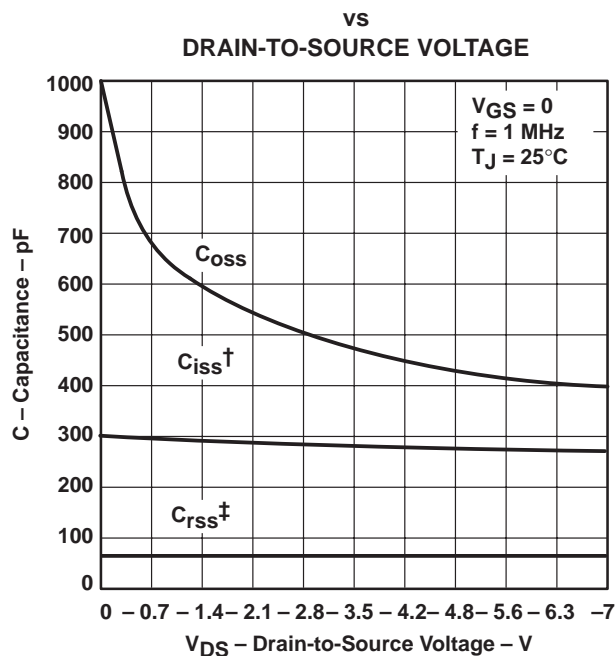


Figure 5

## CAPACITANCE†



$$^\dagger C_{iss} = C_{gs} + C_{gd}, \quad C_{ds(\text{shorted})}$$

$$^\ddagger C_{rss} = C_{gd}, \quad C_{oss} = C_{ds} + C_{gd}$$

Figure 6

## STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED)

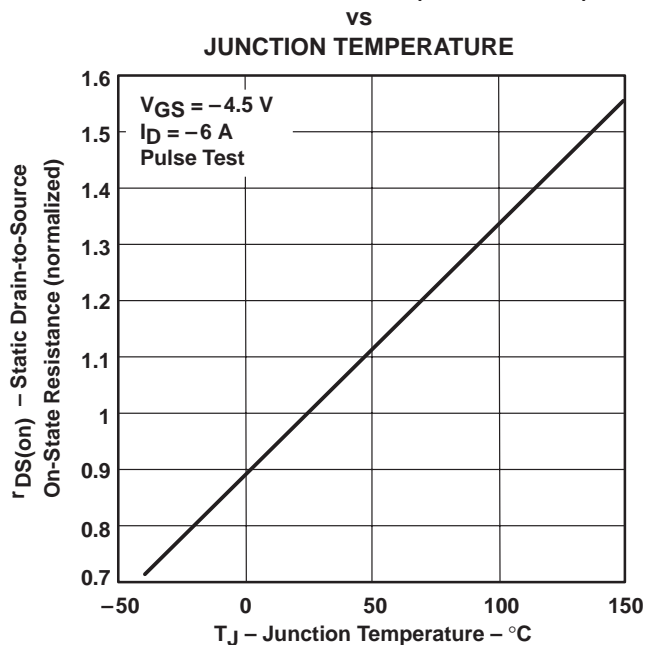


Figure 7

## SOURCE-TO-DRAIN DIODE CURRENT

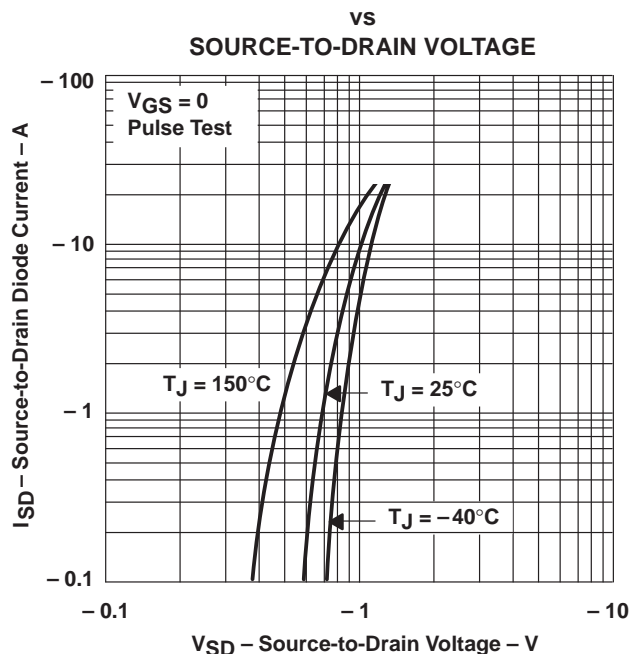


Figure 8

TPS1110, TPS1110Y  
SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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TYPICAL CHARACTERISTICS

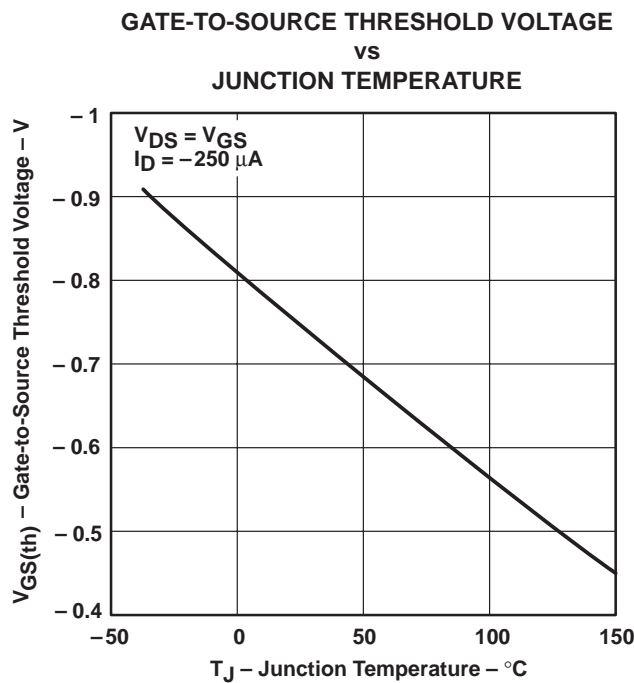


Figure 9

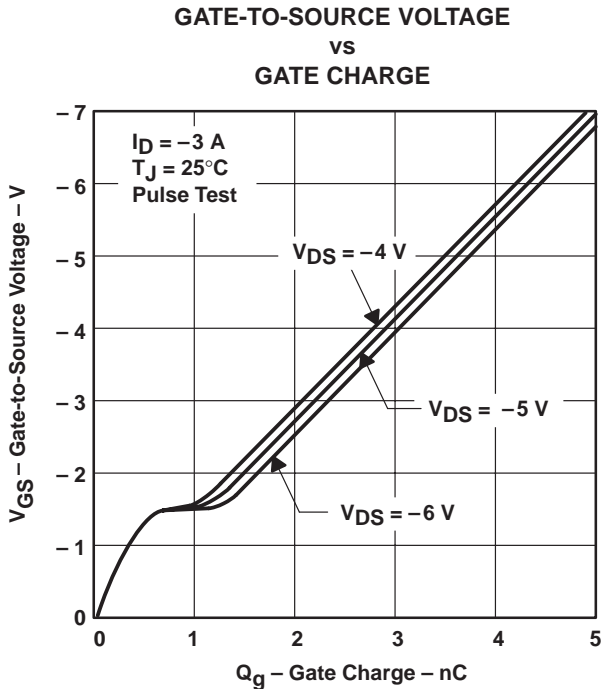


Figure 10

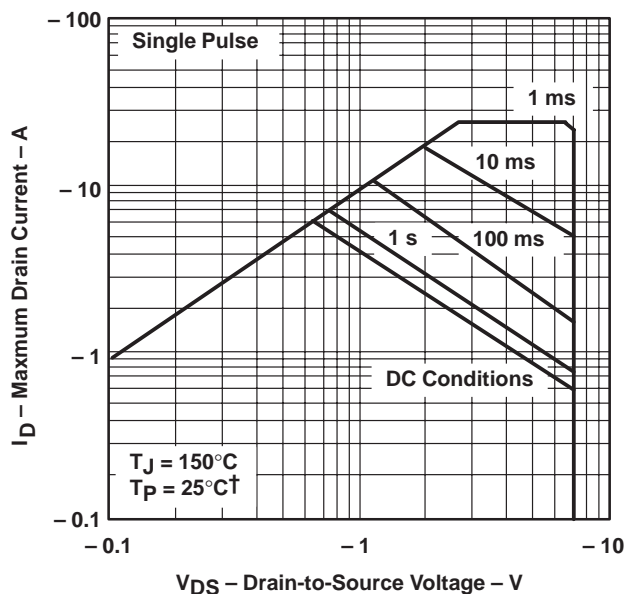


## THERMAL INFORMATION

Table of Graphs

		FIGURE
Maximum drain current	vs Drain-to-source voltage	11
Junction-to-pin thermal resistance (normalized)	vs Pulse duration	12
Junction-to-ambient thermal resistance (normalized)	vs Pulse duration	13

MAXIMUM DRAIN CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE



$^\dagger T_P$  – Temperature of drain pins measured close to the package

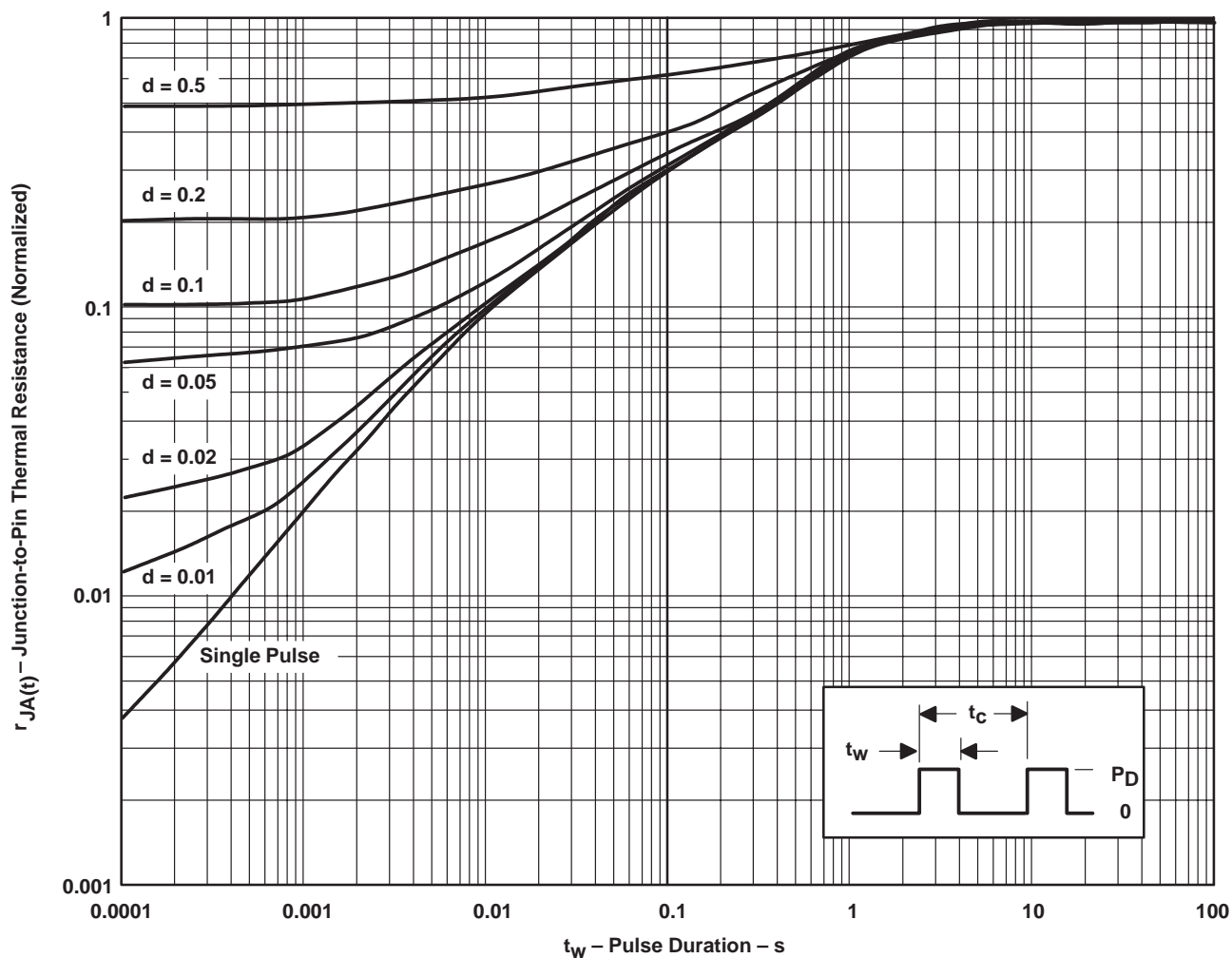
Figure 11

# TPS1110, TPS1110Y SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

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## THERMAL INFORMATION

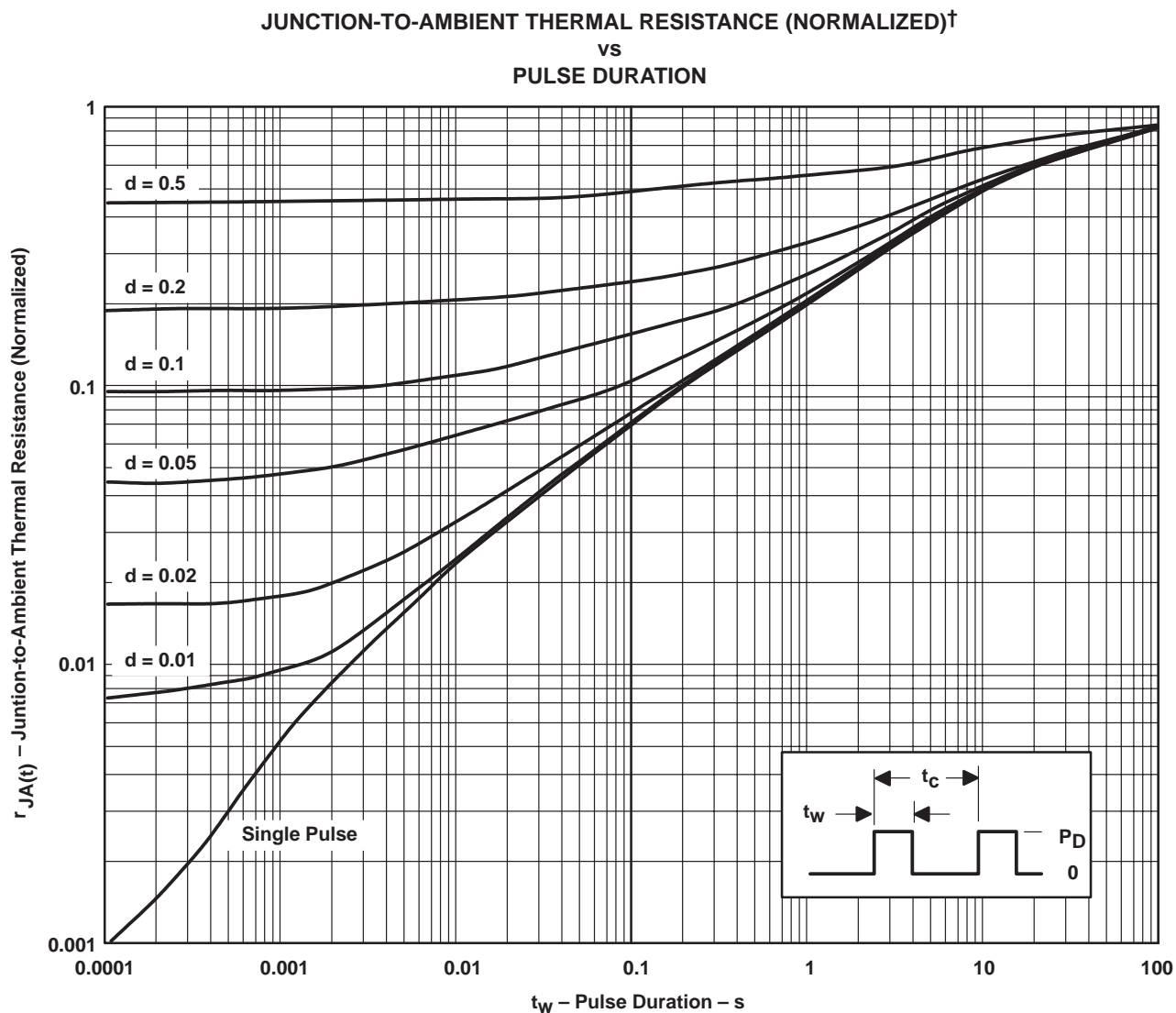
### JUNCTION-TO-PIN THERMAL RESISTANCE (NORMALIZED) vs PULSE DURATION



NOTE A:  $Z_{\theta JP(t)} = r_{JP(t)} \cdot \theta_{JP}$   
 $t_W$  = pulse duration  
 $t_C$  = cycle time  
 $d$  = duty cycle =  $t_W / t_C$   
 peak  $T_J = P_D \cdot Z_{\theta JP(t)} + T_P$

Figure 12

## THERMAL INFORMATION



<sup>†</sup> Device mounted on FR4 printed-circuit board with no special thermal considerations.

NOTE A:  $Z_{\theta JA}(t) = r_{JA}(t) \cdot \theta_{JA}$   
 $t_W$  = pulse duration  
 $t_C$  = cycle time  
 $d$  = duty cycle =  $t_W/t_C$   
 peak  $T_J = P_D \cdot Z_{\theta JA}(t) + T_A$

Figure 13

# TPS1110, TPS1110Y SINGLE P-CHANNEL LOGIC-LEVEL MOSFETS

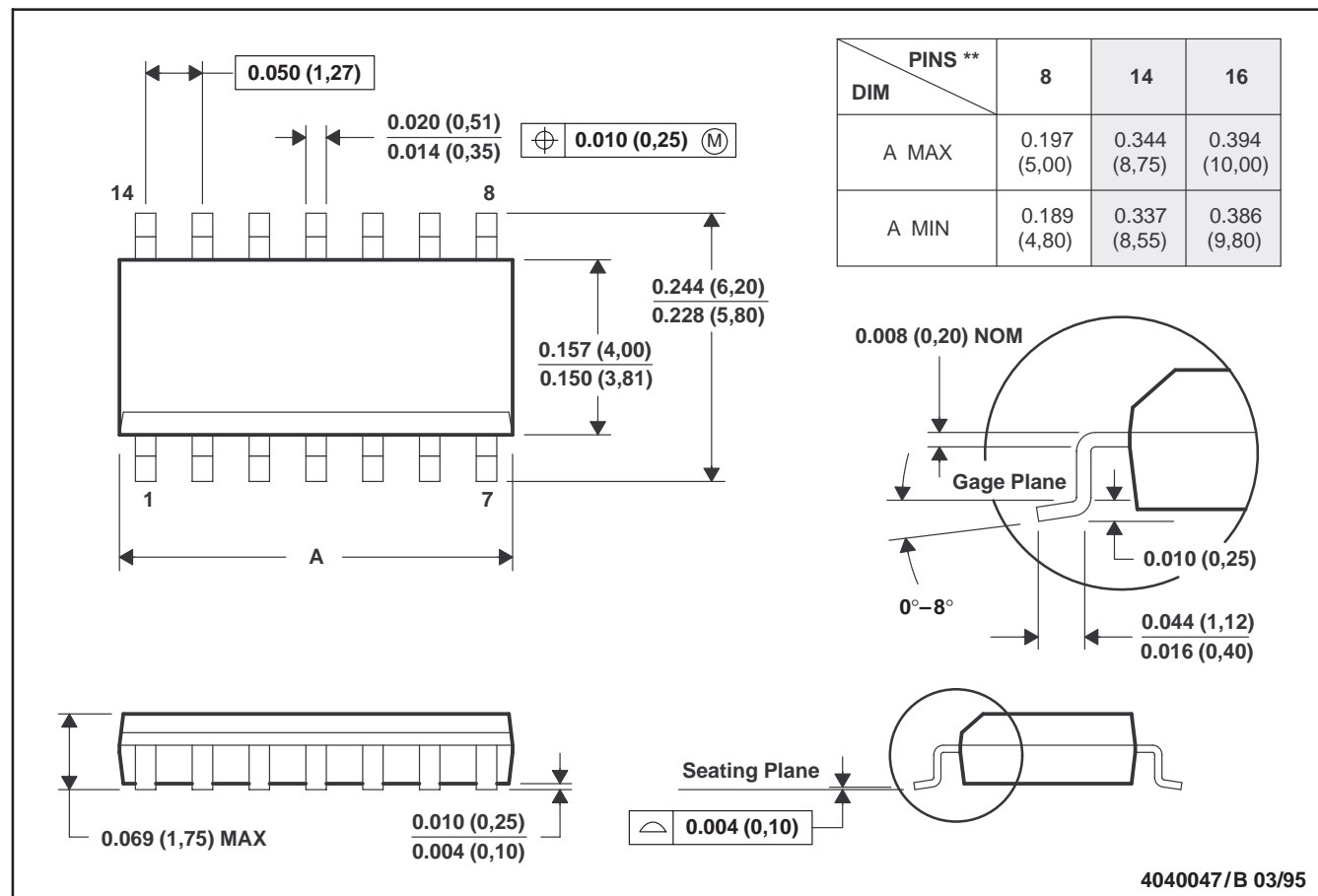
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## MECHANICAL INFORMATION

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - Four center pins are connected to die mount pad.
  - Falls within JEDEC MS-012

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