TMXF84622 Ultramapper
622/155 Mbits/s SONET/SDH x DS3/E3/DS2/DS1/E1/DS0

The documentation package for the TMXF84622 Ultramapper 622/155 Mbits/s SONET/SDH x DS3/E3/DS2/DS1/E1/DS0 system chip consists of the following documents:

- The *Ultramapper Register Description.* This documents is available on a password protected website.
- The *Ultramapper Product Description* (this document), the *Ultramapper System Design Guide,* and the *Ultramapper Hardware Design Guide*. These documents are available on the public website shown below.

To contact Agere please see the last page of this document. To access related documents, please contact your Agere representative, or click on the following address: http://www.agere.com/enterprise_metro_access/mappers_muxes.html

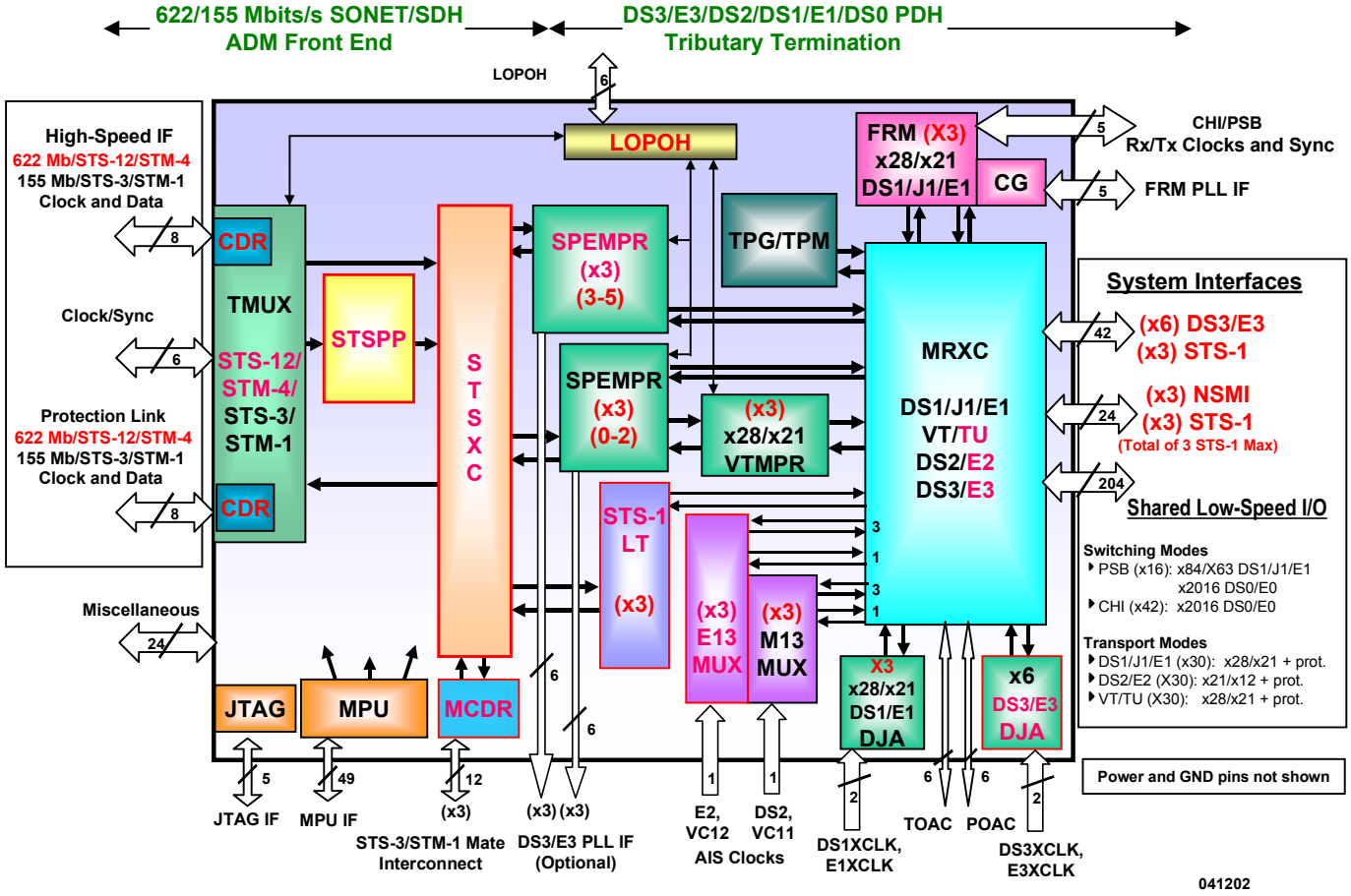

Figure 1. Ultramapper Functional Block Diagram

1 Features

- Versatile IC supports SONET/SDH 622.08/ 155.52 Mbits/s interface solutions for DS3/E3, DS2/E2, DS1/E1/J1 and DS0/E0/J0 applications.
- Terminates up to 84 DS1/J1 or 63 E1 framed or unframed signals. All popular framing formats are supported.
- Terminates up to six DS3/E3, 21 DS2, or 12 E2 channelized or unchannelized signals with grooming for channelized DS3/E3/DS2/E2.
- Mates with up to three other Ultramappers to provide full 336/252 DS1/J1/E1 terminations.
- Terminated DS3/E3, DS2/E2, DS1/E1/J1 signals may be flexibly mapped into the SONET/SDH interface using all allowed MUXing structures.
- Supports 1:1, 1 + 1, and 1:N (DS2/DS1/E1) protection schemes with dedicated interfaces.
- 3.3 V I/O, 1.5 V CORE, low power (<3 W) and –40 °C to +85 °C temperature range allows for uncontrolled or convection cooled environments.
- Built-in clock and data recovery circuits with optional input for forward clocking of STS-3 input.
- Full SONET/SDH compliant alarm reporting.
- Supports full processing for all line/section/path overhead with inhibitable automatic generation of AIS, RDI, and REI and N times filtering on critical overhead.
- Allows extraction/insertion of DCC-L, DCC-S, or up to 20 Mbits/s using specified overhead bytes for the data communications channel. The data signal may be optionally framed and routed to/from one of the DS1/E1 I/Os.
- Provides full high-speed pointer processing and synchronization of the 8 kHz frame/2 kHz superframe to the system timing.
- Loopbacks, manual error insertion, internal pattern generator/monitor, and internal cross connects simplify debugging and diagnostics.
- Standard 700-pin ball grid array (PBGA).
- Complies with all appropriate *Telcordia* ™, ITU, *ANSI* ®, ETSI, and Japanese TTC standards as noted.

TMUX and CDR Features (x1)

- Multiplexes/demultiplexes twelve STS-1 signals or four STS-3c signals to/from a SONET STS-12 signal.
- Multiplexes three STS-1 signals into a SONET STS-3 signal.
- Multiplexes/demultiplexes four STM-1 (AU-4 or 3xAU-3) signals to/from an SDH STM-4 signal.
- Multiplexes/demultiplexes three VC-3 signals to/from an SDH STM-1 (3xAU-3) signal.
- Multiplexes/demultiplexes three VC-3 signals to/from an SDH STM-1 (AU-4) signal via a TUG-3 construction.
- Provides STS-1-only mode for receive and transmit directions.
- Provides separate protection input for support of 1:1 and 1 + 1.
- Provides SONET/SDH loss-of-signal (LOS), out-of-frame (OOF), loss-of-frame (LOF), and loss-of-clock (LOC) detection.
- Provides STS-12/STM-4/STS-3/STM-1/STS-1 selectable scrambler/descrambler functions.
- Provides STS-12/STM-4/STS-3/STM-1/STS-1, and B1/B2/B3 generation/detection.
- Provides STS-12/STM-1/STS-3/STM-1/STS-1 pointer interpretation.
- Complies with GR-253-CORE, T1.105, G.707, G.783, G.806, G.821, and ETSI 417-1-1.

CDR

- Receives data at STS-12/STM-4 (622.08 Mbits/s) data rate.
- 155.52 MHz/622.08 MHz ± 20 ppm input reference clock for on-chip PLL.
- On-chip PLL for clock synthesis, requiring only one external resistor, generating 16 phases, providing resolution of ~200 ps.
- PLL bypass mode for functional test.
- Meets type B jitter tolerance specification of ITU-T recommendation G.958.
- No output clock drift in absence of data transitions once lock is acquired.

STS-12 Pointer Processor (STSPP) Features (x1)

- SONET and SDH compliant.
- Configurable STS-3/STM-1 or STS-12/STM-4 mode.
- Supports an arbitrary mix of STS-1 and STS-3c tributaries, and SDH equivalents for passthrough from receiver to transmitter.
- Supports STS-n add/drop capability.
- Complies with GR-253-CORE, T1.105, G.707, G.783, G.806, G.821, and ETSI 417-1-1.

1 Features (continued)

STS Cross Connect (STSXC) Features (x1)

- Internal clocks and controls are user transparent.
- 30 x 30 STS-1 strictly nonblocking cross connect.
- The following STSXC outputs may be sourced from the subsequent list of inputs without restriction per STS-1/STM-0.

Number of STS-1s	Output Block
12	TMUX
6	SPEMPR
3	STS-1LT or STS-1LT PP
9	Mate CDR (from TMUX only)

Number of STS-1s	Input Block
12	TMUX or STS-12PP
6	SPEMPR
3	STS-1LT
9	Mate CDR (to TMUX only)

Mate Clock and Data Recovery (MCDR) Features (x1)

- Provides glueless capability to connect Ultramappers in a master/slave configuration.
- Loss-of-clock detection from the three external 155.52 MHz clock inputs.
- Loss-of-frame (LOF), out-of-frame (OOF), and B2 error detection on the three 155.52 Mbits/s interfaces. Also RDI and REI monitoring and generation is available.
- Manual B2 error insertion for debugging.
- Provisionable delay between output data frame and 8 kHz sync to accommodate variable length paths to slave Ultramappers.

STS-1 Line Terminating (STS1LT) Features (x3)

- Supports standard SPE mappings for sub-STS-1 payloads (VT mapped: 28 DS1, 28 J1, or 21 E1 signals).
- Supports standard SPE mappings for STS-1 payloads (DS3).
- Detects STS-1 loss-of-signal (LOS), out-of-frame (OOF), loss-of-frame (LOF), AIS-P, and LOP conditions.
- Provides STS-1 selectable scrambler/descrambler functions and B1/B2/B3 generation/detection.
- Provides STS-1 pointer interpretation/processing.
- Complies with GR-253-CORE, T1.105, G.707, G.783, G.826, G.821, and ETSI 417-1-1.

Synchronous Payload Envelope Mapper (SPEMPR) Features (x6)

- The SPE mapper accepts/delivers TUG-2 data from/to the VT mapper. The TUG-2 data is mapped/demapped either to/from an AU-3/STS-1 signal for the North American digital systems or to/from a TUG-3 signal for the ITU-based systems. Only available for SPEMPR 0—2.
- The SPE mapper accepts/delivers channelized DS3 data from/to the M13 MUX/deMUX. The DS3 data is mapped/demapped either to/from an AU-3/STS-1 signal for the North American digital systems or to/from a TUG-3 signal for the ITU-based systems.
- The SPE mapper accepts/delivers channelized or unchannelized DS3 signals at a 44.736 Mbits/s rate from external I/O. The DS3 signals are mapped/demapped the same way as the M13 signal described above.
- The SPE mapper accepts/delivers channelized E3 data from/to the E13 MUX/deMUX. The E3 data is mapped/demapped either to/from an AU-3/STS-1 signal for the North American digital systems or to/from a TUG-3 signal for the ITU-based systems.
- The SPE mapper accepts/delivers channelized or unchannelized E3 signals at a 34.368 Mbits/s rate from external I/Os. These E3 signals are mapped/demapped the same way as the E13 signal described above.
- The SPE mapper has a DS3/E3 loopback circuit placed to demap and remap a DS3/E3 signal. It is particularly useful in cases where a DS3/E3 signal mapped as an AU-3/STS-1 signal requires remapping as a TUG-3 signal or vice versa.
- The SPE mapper supports a path overhead access channel (POAC). Seven path overhead bytes (J1, C2, F2, H4, F3, K3, and N1) can be inserted/dropped through this channel. This channel works as the master, meaning it provides a clock in both the transmit and receive directions and POH data can be inserted on the transmit side or dropped on the receive side.
- Path overhead byte B3 (BIP error) generation/detection and programmable BIP-8 bit error rate insertion.
- Signal fail and signal degrade indicators available to report bit error rates above standard provisionable thresholds.

1 Features (continued)

- Capable of detecting/inserting AIS, RDI, and REI.
- Monitoring is provided on all the TUG-3 path overhead bytes.
- N1 tandem connection support is provided.
- TUG-3 pointer processor supports add/drop multiplexing.
- Provides control signals for an optional external DS3/E3 PLL clock smoothing circuit.
- Complies with GR-253-CORE, T1.105, ITU-T G.707, ITU-T G.831, G.783, ETS 300 417-1-1.

Test Pattern Generator/Monitor (TPG/TPM) Features (x1)

- Configurable test pattern generator: DS1, E1, E2, E3, DS2, DS3, and STS-1 formats.
- Provisionable test pattern data from the following options: quasirandom signal source (QRSS), pseudorandom bit stream length of $2^{15}-1$ (PRBS15), PRBS20, PRBS23, alternating 1 and 0 (ALT_01), ALL_ONES, user pattern (16 bits, repeating).
- The test pattern can be transmitted either unframed or as the payload of a framed signal as defined in ITU-T.
- Under register control, single bit or framing errors can be injected into any test pattern.
- Any sink or receiving channel can be replaced by a test pattern monitor, which can detect and count bit errors or misconfigurations, and/or detect idle conditions or AIS.
- Datalink (DS1-ESF DL) and SSM (E1 multiframe Sa) fields read/writable.
- Supports all Ultramapper modes of operation.
- Complies with T1.107, T1.231, T1.403, G.703, G.704, O.150.

Virtual Tributary Mapper (VTMPR) Features (x3)

- Maps DS1/J1/E1 into VT/TU structures:
  - DS1 into VT1.5/TU-11/TU-12.
  - J1 into VT1.5/TU-11/TU-12.
  - E1 into VT2/TU-12.
- Maps VC-11/VC-12 into VTG/TUG-2 structures:
  - VC-11 into VT1.5/TU-11/TU-12/VTG/TUG-2.
  - VC-12 into VT2/TU-12/VTG/TUG-2.
- Synchronizes VT/TU SPE to system-shelf-timing reference by setting the transmit VT/TU pointers to fixed values for asynchronous mapping or by dynamically changing the transmit VT/TU pointers for byte synchronous mapping.
- Supports asynchronous, byte synchronous, and bit synchronous mappings.
- Supports automatic generation or microprocessor overwrite of one bit RDI-V or enhanced RDI-V, and one bit RFI-V.
- Supports ADM applications with tributary loopback and tributary pointer processing.
- Provides a low-order path overhead access channel.
- Supports TIM-V generation and termination for all 28/21 VT/TU signals.
- Supports BIP-V BER insertion and detection.
- Supports fast AIS generation for downstream devices.
- Supports a one second error counter for BIP-V and REI-V.
- Allows grooming of VTs/TUs in granularity of TUG-2s within the STS-3/STM-1 signal.
- Configurable VT/TU slot selection for DS1, E1, and J1 insertion and drop.
- Automatic receive monitor functions include VT/TU RDI-V, REI-V, BIP-2 errors, AIS-V, and LOP-V.
- Datalink (DS1-ESF DL) and SSM (E1 multiframe Sa) fields read/writable.
- Supports all Ultramapper modes of operation.
- Complies with O.150, T1.105, T1.107, T1.231, T1.403, G.703, G.704, G.707, G.783, GR-253-CORE, GR-499, JT-G707, ETS 300 417-1-1.

M13/E13 MUX Features (x3)

M13 Features

- Configurable multiplexer/demultiplexer for 28 DS1 signals, 21 E1 signals, or seven DS2 signals to/from a DS3 signal.
- Operates in either M23 or C-bit parity mode.
- Provisionable time-slot selection for DS1, E1, and DS2 insertion or drop.
- Full alarm monitoring and generation (LOS, BPV, EXZ, OOF, SEF, AIS, RAI, FEAC, P-bit and C-bit parity errors, FEBE).

1 Features (continued)

- HDLC transmitter with 128-byte data buffer and HDLC receiver with 128-byte data FIFO for the C-bit parity path maintenance data link.
- DS3, DS2, DS1, and E1 loopback and loopback request generation.
- Complies with T1.102, T1.107, T1.231, T1.403, T1.404, GR 499, G.747, and G.775.

E13 Features

- Configurable multiplexer/demultiplexer for up to 16 E1 signals, or four E2 signals, to/from an E3 signal.
- Independently configurable four E12 multiplexer/demultiplexers for up to 16 E1 signals to/from four E2 signals.
- Provisionable time-slot selection for E1 and E2 insertion or drop via the multirate cross connect functional block.
- E12 and E23 multiplexers capable of generating alarm indication signal (AIS) and remote alarm indicator (RAI) signals.
- Configurable HDB3 encoder/decoder for E3 output/input.
- E1 and E2 transmit path monitors that detect loss-of-clock (LOC) and AIS.
- E2 receive path monitor that detects LOC, AIS, and RAI.
- E3 receive monitor that detects loss-of-signal (LOS), LOC, bipolar violation (BPV), AIS, and RAI.
- E3 and E2 loopback modes.
- Complies with ITU G.703, G.742, G.751, and G.775.

T1/E1/J1 Framing Features (FRM) (3x28/21)

- 28/21 DS1/E1/J1 channels.
- Line coding: B8ZS, HDB3, ZCS, AMI, and CMI (JJ20-11).
- DS1 framing modes: ESF, D4, *SLC* ®-96, T1 DM DDS, and SF (F_t only).
- E1 framing: G.704 basic and CRC-4 multiframe consistent with G.706.
- J1 framing modes: JESF (Japan).
- Supports DS1 and E1 unframed and transparent transmission format.
- DS1 signaling modes: transparent; register and system access for ESF 2-state, 4-state, and 16-state; D4 2-state, 4-state, and 16-state; *SLC*-96 2-state, 4-state, and 16-state; J-ESF handling groups maintenance and signaling; VT 1.5 SPE 2-, 4-, 16-state.
- E1 signaling modes: transparent; register and system access for entire TS16 multiframe structure as per ITU G.732.
- Signaling debounce and change of state interrupt.
- V5.2 Sa7 processing.
- Alarm reporting and performance monitoring per *AT&T* ®, *ANSI*, ITU-T, and ETSI standards.
- Facility data link features:
  - HDLC or transparent access for either ESF or DDS + FDL frame formats.
  - Register/stack access for *SLC*-96 transmit and receive data.
  - Extended superframe (ESF): automatic transmission of the ESF performance report messages (PRM). Automatic transmission of the *ANSI* T1.403 ESF performance report messages. Automatic detection and transmission of the *ANSI* T1.403 ESF FDL bit-oriented codes.
  - Register/stack access for all CEPT Sa bits transmit and receive data.
- HDLC features:
  - HDLC or transparent mode.
  - Programmable logical channel assignment: any time-slot, any bit for ISDN D channel, also inserts/extracts C-channels for V5.1, V5.2 interfaces.
  - 64 logical channels in both transmit and receive direction (any framing format).
  - Maximum channel data rate is 64 kbits/s.
  - Minimum channel data rate is 4 kbits/s (DS1/FDL or E1 Sa bit).
  - 128-byte FIFO per channel in both transmit and receive direction.
  - Tx to Rx loopback supported.
- System interfaces:
  - Concentration highway interface:
    - Single clock and frame synchronizing signals; programmable clock and data rates at 2.048 MHz, 4.096 MHz, 8.192 MHz, and 16.384 MHz; programmable clock edges and bit/byte offsets.
  - Parallel system bus interface at 19.44 MHz for data and signaling: single clock and frame synchronizing signals.
  - Time-division multiplex data rate serial interface at 1.544 MHz or 2.048 MHz. Twenty-eight receive data, clock, and frame synchronizing signals. Twenty-eight transmit data signals with a global clock and frame synchronization.
  - Network serial multiplexed interface (NSMI) minimal pin count serial interface at 51.84 MHz optimized for data and IMA applications.

1 Features (continued)

STS-1/DS3/E3/DS2/E2/DS1/E1/VT/TU Multirate Cross Connect (MRXC) Features (x1)

- Configurable cross point interconnect for up to 84/63 DS1/E1 signals to/from the FRM, VTMPR, M13/E13, TPG/TPM, DS1/E1 DJA, and 30 external I/O pins. Also supports 21/12 DS2/E2 to/from external I/O pins to the M13/E13 functional block.
- Connects six DS3, E3 signals from the external pins to the M13/E13 MUX, DS3/E3 DJA, SPEMPR, and three STS-1 signals from external pins to the STS-1-LT.
- Also connects three external NSMI interfaces to the SPEMPR, M13/E13, or FRM functional blocks.
- Three NSMI ports are shared with three STS-1 line terminations.
- Provides grooming capability for up to 168 (84 receive plus 84 transmit) DS1, E1 connections between the FRM, VTMPR, M13/E13, DS1/E1 DJA, and 30 bidirectional sets of pins. This allows for cross connect grooming of any block signal port "n" to any other signal port "m" on a different block or output pin, or on the same block in the case of a groomed loopback.
- Multicast operation (one to many) is supported for 168 sources and destinations.
- Any mix of DS2, E2, DS3, or E3 signals can interconnect.
- Multirate cross connect allows 16 x 3 E1 signals to/from E13 modules to the framer, VT mapper, TPG/TPM, and external pins.
- There are 4 x 3 E2 signals to/from E13 to external pins, TPG/TPM.
- There are three E3 signals to/from the E13 functional block to external pins, TPG/TPM, and the SPE mapper.
- Jitter attenuation can also be inserted in-line on any DS3/E3 or DS1/E1 channel. (Note that cascading of jitter attenuators is not allowed.)
- Standard network loopback or straight-away facility testing is supported for DS1/E1 and DS3/E3. A test-pattern generator capable of injecting idle standards-based pseudorandom bit sequence test patterns, or AIS (blue) alarm, can replace any source or transmitter. A test-pattern monitor that can detect/count bit errors in a pseudorandom test sequence, or loss of frame or synchronization, can replace any sink or receiver.
- One to any number of loopbacks are supported for up to 84/63 channels in DS1/E1 channels from the VT mapper, M13, E13, and framer functional blocks. One-to-one loopback is supported in all DS1/E1 channels. One-to-one loopback is supported for DS3/E3/STS-1 channels from the M13, E13, and SPE mapper functional blocks.
- Loopbacks can be configured to sectionalize a circuit for identifying faults or misconfiguration during out of service maintenance.
- Fast alarm channels are supported for VT mapper (E13, or M13) to framer interconnects for alarm indication signal (AIS or blue alarm) and VT mapper only for remote alarm indicator (RAI or yellow alarm). This feature reduces the propagation delay of the alarms by eliminating multiple integration of alarm conditions.
- Supports framer-only, transport (framer LIU, M13, E13, and VT mapper) and switching (CHI and PSB) modes of operation.
- TOAC outputs are available in DS1/E1 framed format at any destination. Any DS1/E1 channel can be used as TOAC inputs. The TOAC and POAC I/O is also available on dedicated pins for the device. The TOAC and POAC I/O is also available on dedicated pins for the device.

DS1/E1 Digital Jitter Attenuation (DJA) Features (x3x28/21)

- The PLL bandwidth, damping factor, and sampling rates are programmable.
- Configurable to meet jitter and MTIE requirements.
- Supports one DJA per each DS1/E1. (Note that the DJA may not be cascaded.) 28/21 DJAs per block.

DS3/E3 Digital Jitter Attenuation (DJA) Features (x1)

- The PLL bandwidth, damping factor, and sampling rates are programmable.
- The DJA functional block accepts/delivers DS3/E3 clock and data from/to the multirate cross connect functional block.
- Supports one DJA per each DS3/E3. (Note that the DJA may not be cascaded.) 6 DJAs per block.

1 Features (continued)

Microprocessor Unit (MPU) Features (x1)

- 21-bit address/16-bit data bus microprocessor interface (little endian).
- Synchronous (16 MHz to 60 MHz)/asynchronous microprocessor interface modes.
- Microprocessor data bus parity monitoring.
- Summary of two level priority interrupts from major functional blocks/maskable.
- Separate device interrupt outputs for automatic protection switch and the Ultramapper global interrupt.
- Global configuration of network performance-monitoring counters operation.
- Global software resets.
- Global enabling and powerdown of major functional blocks.
- Registers provisionable for clear on read/clear on write.
- Compatible with most industry-standard processors.

JTAG

- *IEEE* ® 1149.1 JTAG boundary scan.

2 Overview

The SONET/SDH Ultramapper device integrates the SONET/SDH section, line, path, and tributary termination functions with M13/E13 multiplex functions and the primary rate framing function. It interfaces to an OC-3/STM-1 optical signal directly or to an OC-12/STM-4 to allow for modular growth in terminal or add/drop applications.

The SONET/SDH Ultramapper device provides a versatile interface for all STS-12/STM-4, STS-3/STM-1, and STS-1 termination applications for point-to-point scenarios and ring applications. Used in tributary shelf applications, this chip enables up to 4 x 84 T1 or J1 (for a total of 336), or 4 x 63 E1 (for a total of 252) line interfaces, to provide all possible mappings into SONET/SDH.

Mapping flexibility allows for software upgrades from M13/E13 mapped connections to VT/TU mapped connections. This device can also be used for DS3/E3/DS2 applications.

A single Ultramapper can map one STS-3/STM-1 to 84/63 DS1/E1s, and a single Ultramapper can terminate six DS3s from one STS-12/STM-4, or two STS-3/STM-1s. A single Ultramapper can also function as an STS-12/STS-3/STM-4/STM-1 add/drop multiplexer by terminating up to three STS-1 channels or one AU-4 channel and, using the internal pointer processors, it can forward any nonterminated channels. By connecting to three other mate devices through serial STS-3/STM-1 mate interconnects, termination of the full STS-12/STM-4 payload is possible.

3 Application Diagrams

This section shows several typical Ultramapper applications. Figure 2 through Figure 9 depict system-level diagrams for the following sample Ultramapper scenarios:

- 8064 DS0/E0 channels to STS-12/STM-4 configuration.
- System-level DS3/E3 interfaces to a DS0 switch fabric.
- System-level OC-3 interface to STS-1, DS1/E1 and DS3/E3 signals.
- System-level OC-12/STM-4 transport of DS1/E1/J1/DS3/E3/EC1.
- System-level OC-12/STM-4 transport with unprotected ring.
- System-level transMUX of 12 M13/E13 DS3/E3s to OC-12/STM-4.
- System-level view of six STS-1s with VT/TU tributaries transferred to/from six STS1s with bulk SPEs of M13/E13 data.
- System-level view of 12 DS3 terminations using two Ultramappers.

3.1 DS0 Switching Application

Figure 2 shows an 8064 DS0 channel to STS-12/STM-4 configuration. The following points describe this scenario:

- The application assumes STS-12/STM-4 is mapped with the VT/TU signal structure.
- Ultramapper 1 is configured for master mode (interface STS-12/STM-4).
- Ultramappers 2—4 are configured for slave mode (interface STS-3/STM-1).
- There are a total of 8064 DS0s/E0s (2016 DS0s/E0s per Ultramapper).
- The mate interconnect utilizes an STS-3 connection between the master and each slave device.
- The system interface can be CHI (concentrated highway interface) or PSB (parallel system bus).
- CHI can be programmed to operate at 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz clock and data rates.
- The PSB interface consists of a 16-bit wide parallel bus operating at 19.44 Mbits/s.

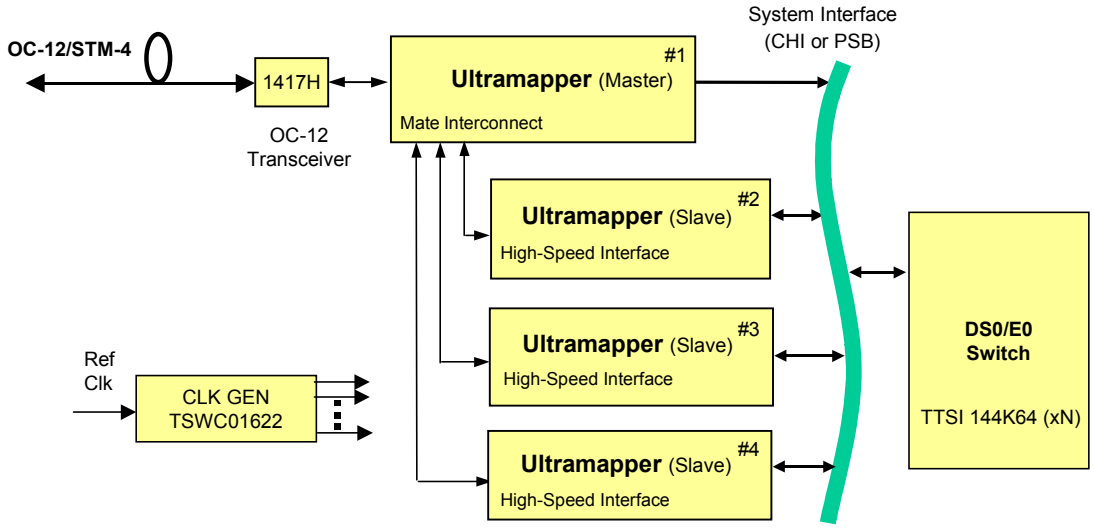

Figure 2. 8064 DS0/E0 Channels to STS-12/STM-4 Configuration

3 Application Diagrams (continued)

3.2 Ultraframer Switching Application

Figure 3 shows 2016 DS0/E0s input via CHI or PSB.The DS1/E1s are framed, multiplexed to three DS3/E3s, and then framed and output to DS3/E3 LIUs. The following points describe this scenario:

- 2016 DS0/E0s are input from a switch, DS1/E1are framed, and then MUXed to DS3/E3. These are then framed and output to three DS3/E3 LIUs.
- Similarly, three DS3/E3s are input from the LIUs, deMUXed to DS1/E1, framed, and output to 2016 DS0/E0s.
- The M13/E13 are connected to three sets of DS3/E3s I/O of the system interface.
- The framer is connected to the shared low-speed I/O of the system interface, which can be configured for the following:
  — Concentration highway interface (at 2 MHz, 4 MHz, 8 MHz, or 16 MHz clock and data).
  — Parallel system bus (at 19 MHz, 16-bit parallel data, plus syncs and clocks).
- All three instances of the 28/21 channel M13/E13 MUXs are configured identically for M13 mode.
- All three instances of the 28/21 channel framers are configured identically for switching.

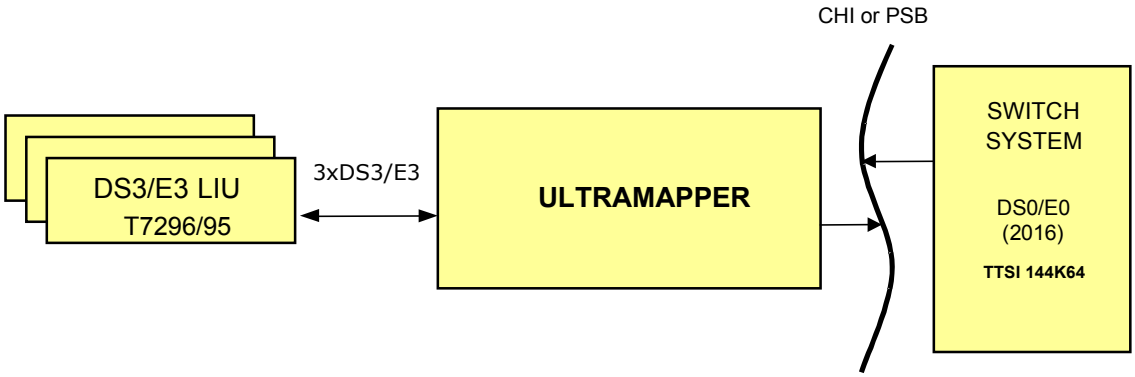

Figure 3. System-Level DS3/E3 Interfaces to a DS0 Switch Fabric

3 Application Diagrams (continued)

3.3 Data NSMI Application

Figure 4 shows three network serial multiplex interfaces (NSMI) configured for slipless clear channel data transport. The following points describe this scenario:

- Three NSMIs are available on the Ultramapper for slipless clear channel data transport application.
- NSMI supports four modes of data transport:
  - STS-1 SPE (SPEMPR blocks).
  - DS3 payload (M13/E13 blocks).
  - DS1 unchannelized payload (FRM blocks).
  - DS1 channelized payload (FRM blocks).
- All data transport modes are supported in OC-12 mode, with the Ultramapper provisioned as an add/drop multiplexer.

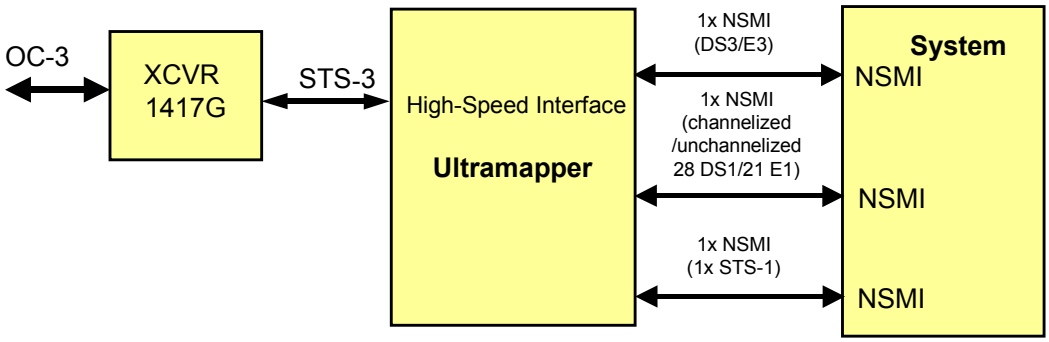

Figure 4. System-Level OC-3 Interface to STS-1, DS1/E1, and DS3/E3 Signals

3 Application Diagrams (continued)

3.4 OC-12/STM-4 Transport Application

Figure 5 shows 56/42 DS1/J1/E1s plus ten DS3/E3s mapped and multiplexed to STS-12/STM-4. The following points describe this scenario:

- There is a high-speed STS-12/STM-4 interface to the optical OC-12 transceiver.
- Two Ultramappers are interconnected to provide full STS-12 payload transport terminations.
- The Ultramapper interfacing with the OC-12 is configured as the master and is configured for STS-12 mode.
- The slave Ultramapper is configured for the STS-3 mode.
- This application shows simultaneous physical terminations of mixed low-speed DS1/J1/E1 traffic and DS3/E3 traffic.
- This application maps up to 56 DS1/J1 or 42 E1s on transport PDH rate interfaces.
- The remainder of the STS-12 payload is terminated as DS3/E3.

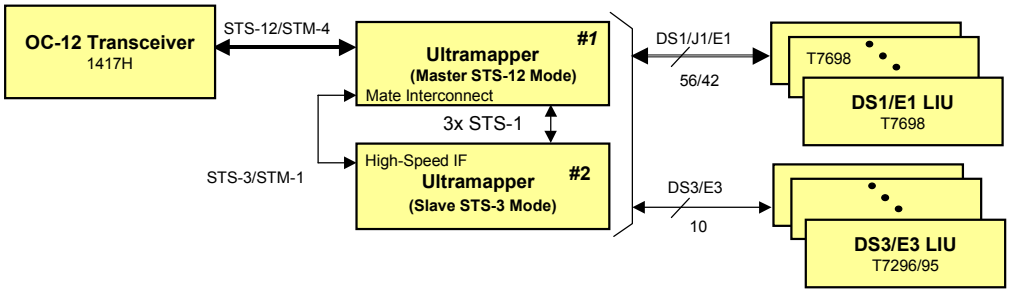

Figure 5. System-Level OC-12/STM-4 Transport of DS1/E1/J1/DS3/E3/EC1

3 Application Diagrams (continued)

3.5 OC-12/STM-4 Transport Add/Drop Ring Application

Figure 6 shows up to three EC1s, plus three DS3/E3s, plus 28/21 DS1/E1s add/drop from an OC-12 ring. The following points describe this scenario:

- Single device ring add/drop configuration.
- High-speed STS-12/STM-4 interface to OC-12 receiver and OC-12 transmitter on the ring.
- Up to 28 DS1/J1s or 21 E1s can be terminated on PDH rate interfaces (out of 84).
- Additionally up to eight STS-1 payloads can be terminated as five DS3/E3s plus three EC1s interfaces.
- Unterminated traffic is mapped through from west to east.
- Low-order (VT) path overhead (LOPH), STS path overhead (POAC), and transport path overhead access for ring maintenance functions.
- STS and VT grooming as well as drop and continue capabilities are available.
- OC-3 add/drop ring configuration is also possible.
- Alternatively, DS1/J1/E1 can be terminated using the NSMI interfaces or as DS0s via CHI, PSB, or NSMI.

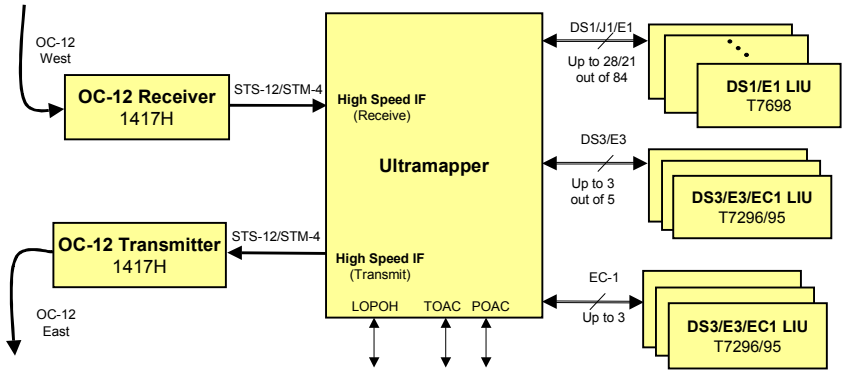

Figure 6. System-Level OC-12/STM-4 Transport with Unprotected Ring

3 Application Diagrams (continued)

3.6 TransMUX Application

Figure 7 shows twelve M13 DS3s transmultiplexed to/from twelve STS-1s with VT via four Ultramappers. The following points describe this scenario:

- Transmultiplexing between twelve M13 DS3s and one STS-12 with full VT mapped DS1s
- Each of the four Ultramappers converts three M13 DS3s into three STS-1s with VT mapped DS1s
- Each of the four Ultramappers converts three STS-1s with VT mapped DS1s into three M13 DS3s
- OC-12 optics interfaces to the high-speed interface of the master Ultramapper
- Mate interconnect of the master Ultramapper interfaces with the high-speed interfaces of the slave Ultramappers

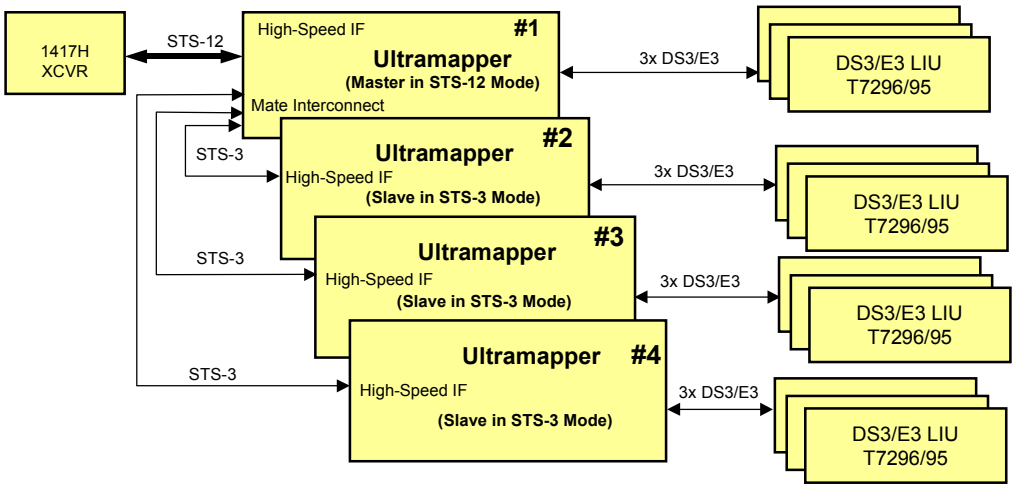

Figure 7. System-Level TransMUX of 12 M13/E13 DS3/E3s to OC-12/STM-4

3 Application Diagrams (continued)

3.7 Portless TransMUX Application

Figure 8 shows how to translate x6 M13/E13-mapped STS-1s to x6 VT-1.5/TU-11/TU-12-mapped STS-1s and conversely translate x6 VT-1.5/TU-11/TU-12-mapped STS-1s to x6 M13/E13-mapped STS-1s. The following points describe this scenario:

- OC-12/STS-12 consists of x6 VT/TU-mapped STS-1, and x6 M13/E- mapped STS-1.
- Two Ultramappers are required to map x6 STS-1 (DS3/E3-mapped) to/from x6 STS-1 (VT/TU-mapped).
- Master Ultramapper is configured in STS-12 mode.
- Slave Ultramapper is configured in STS-3 mode.
- Each device translates three VT/TU-mapped signals to three M13/E13-mapped signals and three M13/E13 signals to three VT/TU-mapped signals.
- Slave device receives and sends a total of x6 STS-1s; three via the STS-3 high-speed interface, and three via the x3 STS-1 system interface.

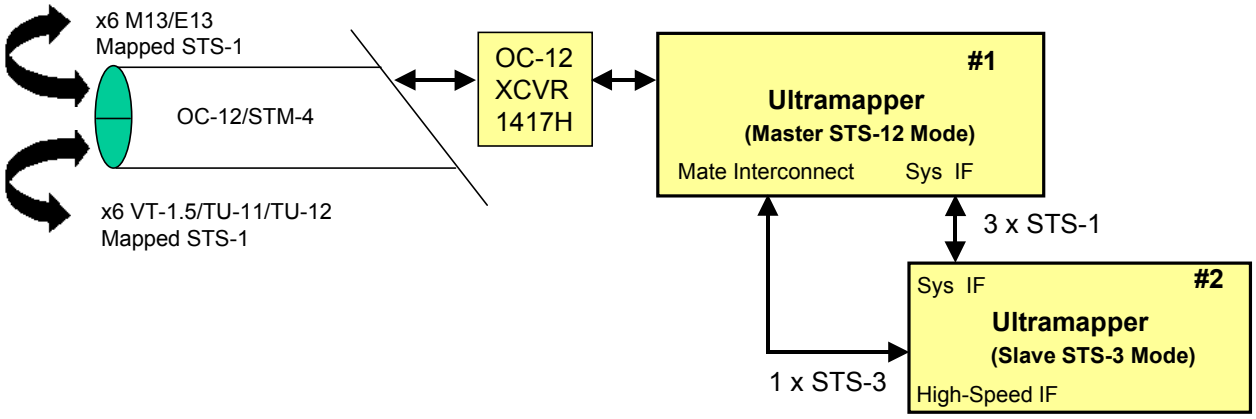

Figure 8. System-Level View of Six STS-1s with VT/TU Tributaries Transferred to/from Six STS-1s with Bulk SPEs of M13/E13 Data

3 Application Diagrams (continued)

3.8 12 DS3 Termination Application

Figure 9 shows two Ultramappers terminate an STS-12; the mate interconnect and NSMI are used to pass six DS3/E3s from the master to a slave. The following points describe this scenario:

- Terminate twelve DS3/E3s from the STS-12 with two Ultramappers.
- OC-12 optics interfaces with high-speed interface of the master Ultramapper, which terminates six DS3/E3s.
- The other six DS3/E3s are terminated by the slave Ultramapper.
- Three DS3/E3s are routed to the slave Ultramapper via the mate interconnect.
- Three DS3/E3s are routed to the slave Ultramapper via the NSMI/STS-1 shared I/O.

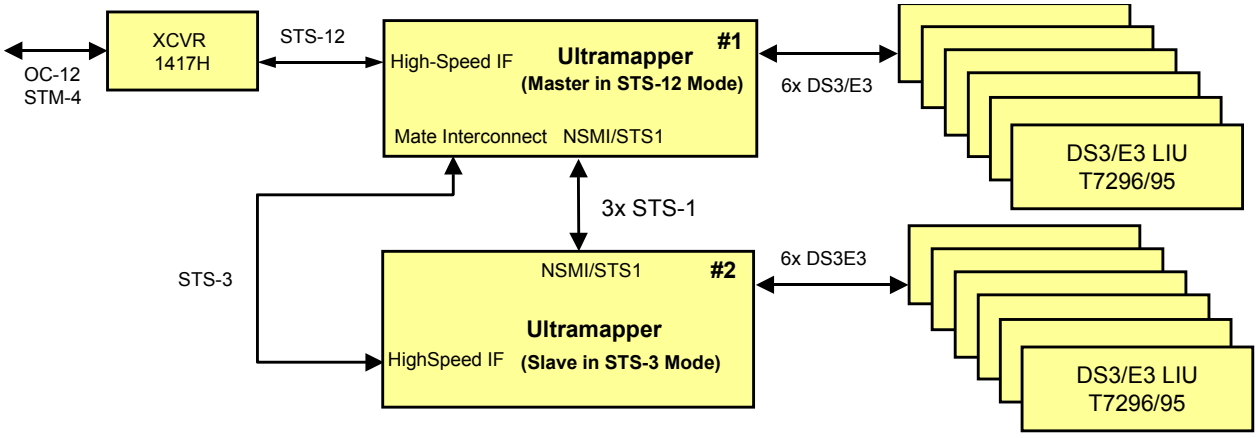

Figure 9. System-Level View of 12 DS3 Terminations Using Two Ultramappers

4 Block Description

4.1 TMUX/Clock and Data Recovery (CDR) Blocks

The TMUX and CDR blocks (one per device) provide the high-speed interface to the SONET/SDH line and terminate the section and line signals. Several features are incorporated in these blocks to allow for a variety of system applications. First, a redundant interface is provided with the appropriate selectors and bridges to allow easy implementation of 1:1, 1 + 1, or ring protection schemes. Second, a separate interface is provided for access to selected overhead bytes. In SONET applications, the section DCC-S may be added/dropped at 192 kbits/s, while SDH applications may use the same I/O for adding/dropping the DCC-L at 576 kbits/s. Alternately, any bytes in the entire overhead may be added/dropped. A third feature of these blocks is that they can operate at both 622.08 Mbits/s or 155.52 Mbits/s, where the 155.52 Mbits/s mode may use a clock forwarded from the external PHY device. In this mode, both the receive and transmit directions of the device may operate asynchronously. In the 622 Mbits/s mode, a CDR is provided for ease of retiming the data signal. The fourth and final function of these blocks is to terminate/generate the section, line, and path overhead (only for the SONET/SDH STS-12/3 or STM-4/1 signals). Automatic generation of AIS/RDI/REI is possible since the protection path is available on the device. Additionally, N times filtering is provided for critical bytes such as K1/K2. All variations in overhead processing between SONET and SDH are also accommodated. A summary of the overhead processing follows and includes the pointer interpretation function necessary for AIS detection.

4.1.1 Transmit Path Section/Line Overhead

Transmit path section/line overhead is as follows:

- Synchronizing status byte (S1) insertion
- M0/M1 REI-L insertion; automatic insertion may be inhibited
- K1 and K2 insertion, AIS-L insertion
- B2 calculation and insertion
- F1 byte insertion
- B1 generation and error insertion
- Scrambler, J0 insert control
- A2 error insertion

The entire APS value or K2[2:0] can be inserted via microprocessor control. Automatic RDI insertion is supported with individual inhibit for each contributor. A protection switch selects the RDI-L value for insertion from the protection board rather than from the working side.

B1 and B2 BIP-8 values are calculated and inserted. Both values can be inverted.

4.1.2 Receive Path Section/Line Overhead

Receive path section/line overhead is as follows:

- Frame alignment (STS-12/STM-4 or STS-3)
- B1 BIP-8 check
- J0 monitoring
- Descrambling
- F1 monitoring
- B2 BIP-8 check
- APS and K2 monitoring
- AIS-L and RDI-L detection
- M1 REI-L detection
- S1 synchronization status monitoring

Framer states and all other state changes are reported. These cause an interrupt if not masked.

The B1 and B2 parity check supports bit and block mode. The counters count up to one second’s worth of BIP errors. These stay at their maximum value in case of overflow or rollover and should be read (and cleared) at least once per second.

The J0 monitor supports nonframed, SONET-framed, and SDH-framed 16-byte sequences, as well as single J0 byte monitoring modes.

APS monitoring is performed on K1[7:0] and K2[7:3]. The value is stored, and changes are reported. Bits [2:0] of the K2 byte are monitored independently.

The alarm indication signal (AIS-L/MS-AIS) and remote defect indication (RDI-L/MS-RDI) are monitored separately, and changes are reported. This information is also sent to the protection device for ADM applications.

The M1 monitor operates either in bit or block mode and allows access of the remote error indication (REI-L/MS-REI) errored bit count.

The S1 byte can be monitored either as an entire 8-bit word or as one 4-bit nibble (bits 7:4).

4 Block Description (continued)

4.1.3 Pointer Interpreter

The TNMUX pointer interpreter conforms to ETS 300 417-1-1: January 1996—Annex B.

The pointer interpreter evaluates the current pointer state for the normal state, path AIS state, or LOP (loss of pointer) conditions, as well as pointer increments and decrements. The current pointer state and any changes in pointer condition are reported to the control system. The number of consecutive frames for invalid pointer and invalid concatenation indication is fixed at nine.

4.1.4 Path Termination Function

In STS-3/STM-4 mode, path termination is performed on either all three STS-1s or on the VC-4. In the STS-12/STM-4 mode, path termination is performed either on all twelve STS-1s/four STS-3Cs, or on the four VC-4 POH. On the receive side, it includes the following:

- J1 monitoring
- B3 BIP-8 checking
- C2 signal label monitoring
- REI-P and RDI-P detection
- H4 multiframe monitoring
- F2, F3, and K3 automatic protection switch monitoring
- N1 tandem connection monitoring
- Signal degrade BER and signal fail BER detection
- Path overhead access channel (RPOAC) drop
- AIS-P/HO-AIS insertion
- Automatic AIS generation (with individual inhibit)

The J1 monitor provides the following five modes of operation on a programmable length (1 byte—64 bytes) of the trace identifier:

- Cyclic checking against the last received sequence
- Comparing against a programmed sequence
- SONET framing mode
- SDH framing mode
- Consecutively consistent occurrences of a new pattern

B3 is monitored either in bit or block mode. Provisionable N-times detection counters are implemented for C2, F2, F3, N1, and K3 bytes. The K3 APS byte and N1 TCM byte can be monitored as an entire 8-bit word or as two 4-bit nibbles.

4.2 STS-12/STM-4 Pointer Processor (STSPP) Block

A pointer processor (one per device) is used to move a SONET/SDH payload from the line clock domain to the system clock domain. The Ultramapper's STS-12 pointer processor is SONET and SDH compliant and offers a configurable STS-3/STM-1 or STS-12/STM-4 mode. It supports an arbitrary mix of STS-1/STS-3c tributaries and SDH equivalents, and complies with GR-253-CORE, T1.105, G.707, G.783, G.826, G.821, and ETSI 417-1-1.

4.3 STS-1 Line Terminating (STS-1LT) Block

The STS-1 line terminating block (three per device) allows termination of an STS-1 line signal routed from the multirate cross connect. It provides access to the section/line and path overhead similarly to the TMUX. It can also source an SPE to the STS cross connect for transport on the high-speed line interface.

4.4 STS Cross Connect (STSXC) Block

The high-order cross connect connects the SONET/SDH interfaces to the PDH portion of the device. It will permit connections that support a variety of applications. The data paths, clocks, and syncs are internally configured as appropriate for the different signal rates and interconnects. A significant portion of the STSXC block is mate interconnect described in Section 4.5.

4.5 Mate Interconnect and Clock Data Recovery (MCDR) Block

The Ultramapper can be configured to terminate an STS-12/STM-4 signal by connecting four devices together via the mate interconnect. Each interconnect operates at 155 Mbits/s and is connected between a single Ultramapper configured as master and up to three Ultramappers with high-speed TMUX input configured as slaves. The mate interconnect uses SONET/SDH framing and overhead so there is performance monitoring of the link between devices. In addition, the frame position of the slave's data signal is adjustable to allow for variations in application board delays.

4 Block Description (continued)

4.6 SPE/AU-3 Mapper (SPEMPR) Block

The SPE mapper functional block (six per device) operates either as an AU-3/STS-1 mapper or as a TUG-3 mapper. In either mode, it maps/demaps data from/to either the VT mapper, the M13 MUX/deMUX, the DS3 clear channel, or the DS3 loopback channel. The SPE mapper supports numerous automatic monitoring functions and provides interrupts to the control system, or it can be operated in a polled mode.

In DS3 mapping mode, the SPE mapper functional block accepts/delivers structured DS3 data from/to the M13 functional block or a clear DS3 signal at 44.736 Mbits/s rate and maps/demaps it asynchronously to/from the STS-1 SPE or a TU-3. The DS3 mapper generates a fixed pointer value of 522.

On the receive side, pointer interpretation is performed, detecting LOP, AIS, NDF, NORM, INC, and DEC. A DS3 loopback mode allows demapping and remapping of a DS3 signal. It is particularly useful in cases where a DS3 signal mapped as AU-3/STS-1 needs to be remapped as a TU-3 signal or vice versa. B3ZS encoding/decoding is included.

This functional block also connects to the path overhead access channel (POAC) to insert/drop path overhead bytes J1, C2, F2, H4, F3, K3, and N1 into the STS-1 SPE or VC-3.

The SPE mapper block supports unidirectional path switch ring (UPSR) applications, as well as N1 tandem connection functions.

The SPE mapper functional block complies with GR-253-CORE, T1.105, ITU-T G.707, ITU-T G.831, G.783, and ETS 300 417-1-1.

4.7 VT/TU Mapper (VTMPR) Block

The VT/TU mapper (three per device) maps any valid combination of DS1 and E1 signals into a stream at a rate of 51.84 Mbits/s (STS-1 or AU-3). The mapping methods (VT1.5, VT2, and VT group in *ANSI* nomenclature; TU-11, TU-12, and TUG-2 in ITU nomenclature) are analogous. The VT/VC mapper supports the following mappings:

- 84 asynchronous, byte-, or bit-synchronous DS1 signals are mapped into seven VT groups or TUG-2s.
- 84 asynchronous, byte-, or bit-synchronous J1 signals are mapped into seven VT groups or TUG-2s.
- 63 asynchronous, byte-, or bit-synchronous E1 signals are mapped into seven VT groups or TUG-2s.
- Maps T1 into VT1.5/TU-11/TU-12, J1 into VT1.5/TU-11/TU-12, and E1 into VT2/TU-12.

ADM and unidirectional path switch ring (UPSR) applications are supported via tributary loopback, tributary pointer processing, and low-order path overhead access channel.

The VT/TU mapper supports automatic generation or microprocessor overwrite 1-bit RDI-V, enhanced RDI-V, 1-bit RFI-V, automatic downstream AIS generation, and five J2 trace identifier modes.

The VT/TU mapper complies with GR-253-CORE, G.707, T1.105, G.704, G.783, JT-G707, GR-499, and ETS 300 417-1-1.

4.7.1 Receive Direction

In the receive direction, the VT mapper terminates the data stream it receives from the SPE mapper. It demultiplexes the AU-3/TUG-3 into the VTs/TUs and checks the H4 multiframe alignment. A pointer interpreter for up to 28 VTs/TUs detects LOP, AIS, NDF, NORM, INC, and DEC on each channel.

The low-order path termination includes V5 byte termination, J2 path trace, Z6/N2 tandem connection, Z7/K4 enhanced RDI-V and low-order APS monitor, and the payload termination for asynchronous, byte- or bit-synchronous signals. The V5 byte termination performs BIP-2 check (bit- or block-mode), REI-V count, RFI-V, and RDI-V detection, signal label monitor, and automatic AIS-V insertion (which can be inhibited).

The J2 monitor supports the following four different modes:

- Cyclic check
- SONET framing mode
- SDH framing mode
- Single byte check

In byte-synchronous modes, the receive demapper generates a frame synchronization signal to indicate the DS1 frame bit or the MSB of the E1 time-slot 0. Additionally, it provides the framer access to the received signaling bits. Output of the VT mapper is a DS1/J1/E1 signal with a gapped clock. It can be overwritten with AIS automatically or upon microprocessor request.

4.7.2 Transmit Direction

In the transmit direction, the VT mapper gets a clock, data, and frame synchronization signal from the multirate cross connect. The input is retimed and is checked for a digital loss of clock (LOC), an AIS condition, and low zeros density. In byte-synchronous mode, the input signal is additionally checked for loss-of-frame (LOF).

4 Block Description (continued)

A transmit elastic store synchronizes the incoming DS1/J1/E1 signals to the local STS-1 clock. In asynchronous and bit-synchronous mode, it works as a bit-oriented (64-bit) FIFO, and in byte-synchronous mode, as a byte-wide (8-byte) buffer using a V5 byte marker bit (8-bit). Overflow or underflow conditions are monitored and reported.

In asynchronous and bit-synchronous mode, a fixed VT pointer of 78 (VT1.5/TU-11) and 105 (VT2/TU-12) is generated and the payload is mapped into the container using a positive/null/negative bit stuffing mechanism (C- and S-bits). In bit-synchronous mode, the bit stuffing mechanism is disabled. In byte-synchronous mode, a dynamic VT pointer value is generated using the V5 marker, implementing NORM, NDF, INC, and DEC pointers.

The VT POH generation comprises V5 byte with BIP2-generation, AIS-, signal label-, UNEQ-V insertion, automatic REI-V, RFI-V, RDI-V, and enhanced RDI-generation (*Bellcore* ®, ITU-T), J2 path trace insertion via microprocessor, Z6/N2 byte insertion, and Z7/K4 byte insertion via the microprocessor or low-order path overhead (LOPOH) access channel.

The data stream is synchronized to the received, internal 2 kHz synchronization pulse, and is multiplexed to form the STS-1/AU-3 signal, which is then output to the SPE mapper.

When operating in byte-synchronous mode, the phase and signaling bits from the framer are stored and inserted into the mapped frame.

4.8 M13/E1 Multiplexer (M13/E13 MUX) Blocks

The M13/E13 block (three blocks per device) is a highly configurable multiplexer/demultiplexer for which each block can be configured for M13 or E13 operation. The features are as described below.

4.8.1 M13 MUX

The M13may operate in the C-bit parity or M23 mode, a mixed M13/M23 mode, or in an M23 mode. In the C-bit parity mode, the M13 provides a far-end alarm and control (FEAC) code generator and receiver, an HDLC transmitter and receiver, and an automatic far-end block error (FEBE) generator.

Each internal M12 MUX/deMUX and the M23 MUX/deMUX can be configured to operate as independent MUXs/deMUXs. 28 DS1 inputs (in groups of four), or 21 E1 input signals (in groups of three) can feed into individual M12 MUXs, while the M23 MUX can take DS2 signals from outputs of M12 MUXs, or direct DS2 inputs, or loopback deMUXed DS2s.

The M13 supports numerous automatic monitoring functions. It can provide an interrupt to the control system, or it can operate in a polled mode.

The M13 complies with T1.102, T1.107, T1.231, T1.403, T1.404, GR-499, G.747, and G.775.

4.8.1.1. Receive Direction

The receive DS3 is monitored for loss of clock and loss of signal (LOS) according to T1.231. The B3ZS decoder accepts either the unipolar clock and data or unipolar clock, and positive and negative data. It also checks for bipolar coding violations. The transmit DS3 can be looped back into the receive side after B3ZS decoding. The M23 demultiplexer checks for valid DS3 framing by finding the frame alignment pattern (F-bits) and then locating the multiframe alignment signal (M-bits). During each M frame, the data stream is checked for the presence of the AIS (1010) or idle (1100) pattern.

C-bits 13, 14, and 15 can be used as a 28.2 kbits/s data link and are available directly at device output via an internal HDLC receiver. The receiver is composed of a 128-byte FIFO, a CRC-16 frame check sequence (FCS) error detector, and control circuits.

Within the M23 demultiplexer, there are four performance monitoring counters for F- or M-bit, P-bit, E-bit parity, and FEBE errors. Each M12 demultiplexer contains two performance monitoring counters.

4.8.1.2. Transmit Direction

The incoming DS1/E1 clocks are first checked for activity or loss-of-clock (LOC). The data signals are retimed and checked for AIS and activity. DS1/E1 loopback selectors allow the individual DS1/E1 signals within the received DS2 or DS3 to be looped back toward the DS2/DS3 input. This loopback can be performed automatically, or the user can force a DS1 or E1 loopback.

The four DS1 or three E1 signals for each M12 MUX are fed into single-bit, 16-word-deep FIFOs to synchronize the signals to the DS2 frame generation clock. The fill level of each FIFO determines the need for bit stuffing its DS1/E1 input. The M13 can handle DS1/E1 signals with nominal frequency offsets of ±130 ppm and up to five unit intervals peak jitter. The DS2/DS3 transmit clock is used to derive the clock source for DS2 frame generation.

The M23 multiplexer generates a transmit DS3 frame, and fills the information bits in the frame with data from the seven DS2 select blocks.

4 Block Description (continued)

The M23 MUX can be provisioned to operate in either the M23 mode or the C-bit parity mode. It contains seven DS2 FIFOs, each with a depth of 8. The fill level of each FIFO determines the need for bit stuffing its DS2 input.

The transmit DS3 output can either be in the form of a unipolar clock and data or unipolar clock, and positive and negative data. The DS3 data is B3ZS-encoded and can be looped back from the receive DS3 input.

4.8.2 E13 MUX

The E13 is a functional block that performs MUX/deMUX from/to 16 E1s, four E2s, and one E3 signals compliant with ITU G.742 and ITU G.751. The E13 functional block is a highly configurable multiplexer/demultiplexer. It can operate in E12, E13, or E23 modes. Each internal E12 MUX/deMUX and E23 MUX/deMUX is independently configurable. The E3 inputs to the receive path can be HDB3-encoded dual rail (bipolar) signals or already decoded single rail signal with or without a BPV indication input. The E1 and E2 inputs are expected to be decoded prior to the E13 functional block. E3 transmit direction output can be configured as HDB3-encoded dual rail (bipolar) or as single rail. The E13 provides status and two-level priority maskable interrupt outputs to the microprocessor.

The E13 functional block is a configurable multiplexer/demultiplexer for up to 16 E1 signals, or four E2 signals to/from an E3 signal. It is an independently configurable four E12 multiplexer/demultiplexer for up to 16 E1 signals to/from four E2 signals, and has provisionable time-slot selection for E1, E2 insertion or drop via the multirate cross connect functional block. E12/E23 multiplexers are capable of generating alarm indicator signal (AIS) and remote alarm indicator (RAI) signals. The HDB3 encoder/decoder is configurable for E3 output/input.

E1 and E2 transmit path monitors detect loss of clock (LOC) and AIS. The E2 receive path monitor detects loss of clock (LOC), AIS, and RAI. The E3 receive monitor detects loss of signal (LOS), loss of clock (LOC), bipolar violation (BPV), AIS, and RAI. E3 and E2 loopback modes are also available.

4.9 Multirate Cross Connect (MRXC) Block

The multirate cross connect (MRXC) functional block (one per device) is a crosspoint switch for DS1/E1/J1/DS2/E2, VT/TU, DS3, and path overhead I/O. The multirate cross connect routes signals to/from the major functional blocks and external I/O pins as necessary for each application. The MRXC can multicast, route test patterns, idles, or alarm conditions to any channel, and can provide system loopbacks.

For DS1/E1 applications, the multirate cross connect can interconnect up to 84 individual DS1/E1 channels between the framer, M13 multiplexer, VT mapper, jitter attenuator, or external I/O. The external I/O pins support an application-dependent mix of up to 30 T1/E1 interfaces (two/nine dedicated protection channels), seven DS2 interfaces, or one of four available system interfaces.

Independent signal paths for remote alarm indication (RAI), alarm indication signal (AIS), and byte-synchronous frame synchronizing signals on channels between the VT mapper or M13 and the framer are supported. Receive pointer adjustment information is routed to the jitter attenuator functional block for each channel originating in the VT mapper.

The multirate cross connect has independent DS2 interfaces for the M12 and M23 blocks of the M13 MUX. Full split access to the external I/O device pins provides the capability to add, drop, or rearrange the DS2 signals within the M13.

For DS3 signals, the multirate cross connect supports configuration of interconnects between the following:

- The M13 and the SPEMPR
- External I/O interconnection to the M13 or SPEMPR
- Insertion/monitoring of DS3 test patterns from the test-pattern generator functional block

The test-pattern generator functional block (TPG) provides test signals and monitors inputs (test pattern monitor) for signals to/from the multirate cross connect. The TPG can generate a set of test signals or idles at DS1, E1, DS2, or DS3 rates. There is only one test pattern generator and monitor per signal rate.

For overhead, the MRXC provides an access channel connection (TOAC and POAC) to the SPEMPR or to the TMUX functional blocks.

The MRXC also provides the interface to the external pins. The external pins may be configured to work in four modes: a transport mode, a concentration highway interface (CHI) mode, a parallel system bus (PSB) mode, and a network serial multiplexed interface (NSMI) mode. The first mode is used to provide dedicated access to the device for DS3/E3/DS2/E2/DS1/E1 signals, and the last three modes are described below.

- Concentration highway interface (serial time-division multiplex interface) CHI:
  - — Global frame synchronization.
  - — Global clock: 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz.
  - — 84 transmit and receive data ports; data rates: 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or 16.384 Mbits/s.

4 Block Description (continued)

- Parallel system bus (parallel time-division multiplex interface/transmit and receive) PSB:
  - Global frame synchronization.
  - Global clock: 19 MHz.
  - Data rate: 19 MHz.
  - 8 bits of data + associated parity bit.
  - 4 bits of signaling + 2 bits of signaling control + 1 bit of parity.
- Network serial multiplexed bus (NSMI):
  - 6- or 8-pin serial interface.
  - Transmit and receive clock and data at 51.84 MHz.
  - Accommodates one STS-1 SPE.
  - Provides a minimal pin count interface for data and inverse multiplexing for ATM (IMA) applications without slip buffers.
  - Three modes of operation:
    - —Framer—NSMI payload assembled/disassembled into DS1/E1s.
    - —M13—proprietary transport format with DS3 framing.
    - —SPE—proprietary transport format mapped into an STS-1/AU-3.

4.10 DS1 Digital Jitter Attenuator (DS1/E1 DJA) Block

The DS1/E1 digital jitter attenuator (DS1DJA) block (three per device), contains 28 copies of the digital jitter attenuator for a total of 84/63 DS1/E1 DJAs. These digital jitter attenuator functional blocks can operate in two different modes, as a DS1 or as an E1 jitter attenuator.

In both modes, the digital jitter attenuator can be provisioned to always operate as a second-order PLL, or it can switch to act as a first-order PLL during VT pointer adjustments to help meet MTIE requirements. The period of time in the first-order mode is provisionable. The PLL bandwidth is provisionable between 0.1 Hz and 0.5 Hz, and the damping factor for these bandwidths varies between 2 and 0.5 to accommodate a number of different system constraints.

The DS1/E1 allows automatic pass-through an AIS from both the VTMPR or M13/E13 blocks.

4.11 DS3 Digital Jitter Attenuator (DS3/E3 DJA) Block

The Ultramapper device contains a single DS3/E3 digital jitter attenuator block containing six DS3/E3 digital jitter attenuators. These digital jitter attenuators can operate in two different modes: as a DS3 or as an E3 jitter attenuator. The PLL bandwidth and the sampling ratio can be set over a wide range to accommodate a number of different system constraints.

The DJA functional block accepts/delivers DS3/E3 clock and data from/to the multirate cross connect functional block. The PLL bandwidth, damping factor, and sampling rates are programmable. Output is programmable as data only, as B3ZS-coded, or as HDB3-coded.

4.12 Test Pattern Generator/Monitor (TPG/TPM) Block

The test pattern generator and test pattern monitor functional blocks (TPG and TPM) are a set of configurable test pattern generators and monitors for local self-test, maintenance, and troubleshooting operations.

The TPG feeds one or more T1/E1/DS2 test signals (via data, clock, and FS or AIS signal paths) to the multirate cross connect, which can redistribute or broadcast these signals to any valid channel in the framer, external I/O, M13 mapper, or VT mapper functional blocks. The TPG can also generate DS3 test signals.

Any channel arriving at the multirate cross connect can be routed to the test monitor. The test monitor can automatically detect/count bit errors in a pseudorandom test sequence, loss of frame, or loss of synchronization situation. The TPM can provide an interrupt to the control system, or it can be operated in a polled mode.

Simultaneous testing of DS1, E1, DS2, and DS3 signals is supported with one channel for each.

Supported test patterns are a quasirandom signal (QRSS), a pseudorandom bit sequence (PRBS23, PRBS20, PRBS15), alternating zeros/ones, an all-ones pattern, and a 16-bit user-provisionable pattern.

The test pattern can be transmitted as either unframed or as the payload of a framed signal, as defined in ITU-T Recommendation O.150.

Under register control, single bit-errors can be injected into any test pattern.

4.13 Low-Order Path Over Head

This block is shown in Figure 1 but it cannot be addressed by the MPU. It is shown as a virtual block to highlight that the LOPOH bytes from the TMUX, SPEMPR and VTMPR can be provisioned to appear at the LOPOH device pins. Provisioning is accomplished by setting registers in the device via the MPU.

4 Block Description (continued)

4.14 Clock Generator (CG) Block

The clock generator block may optionally be used to override the device configuration specified by the MODE[2:0]_PLL device pins. If the block is not provisioned, the default mode will generate all the necessary FRM block PDH clocks, based upon the logic states on the MODE[2:0]_PLL pins (see the *Ultramapper Hardware Design Guide*).

4.15 Framer Block

The DS1J1//E1 framer block's (three per device) internal components are shown in Figure 10, along with other relevant Ultramapper blocks. A particular application will determine which of the components within the framer are used.

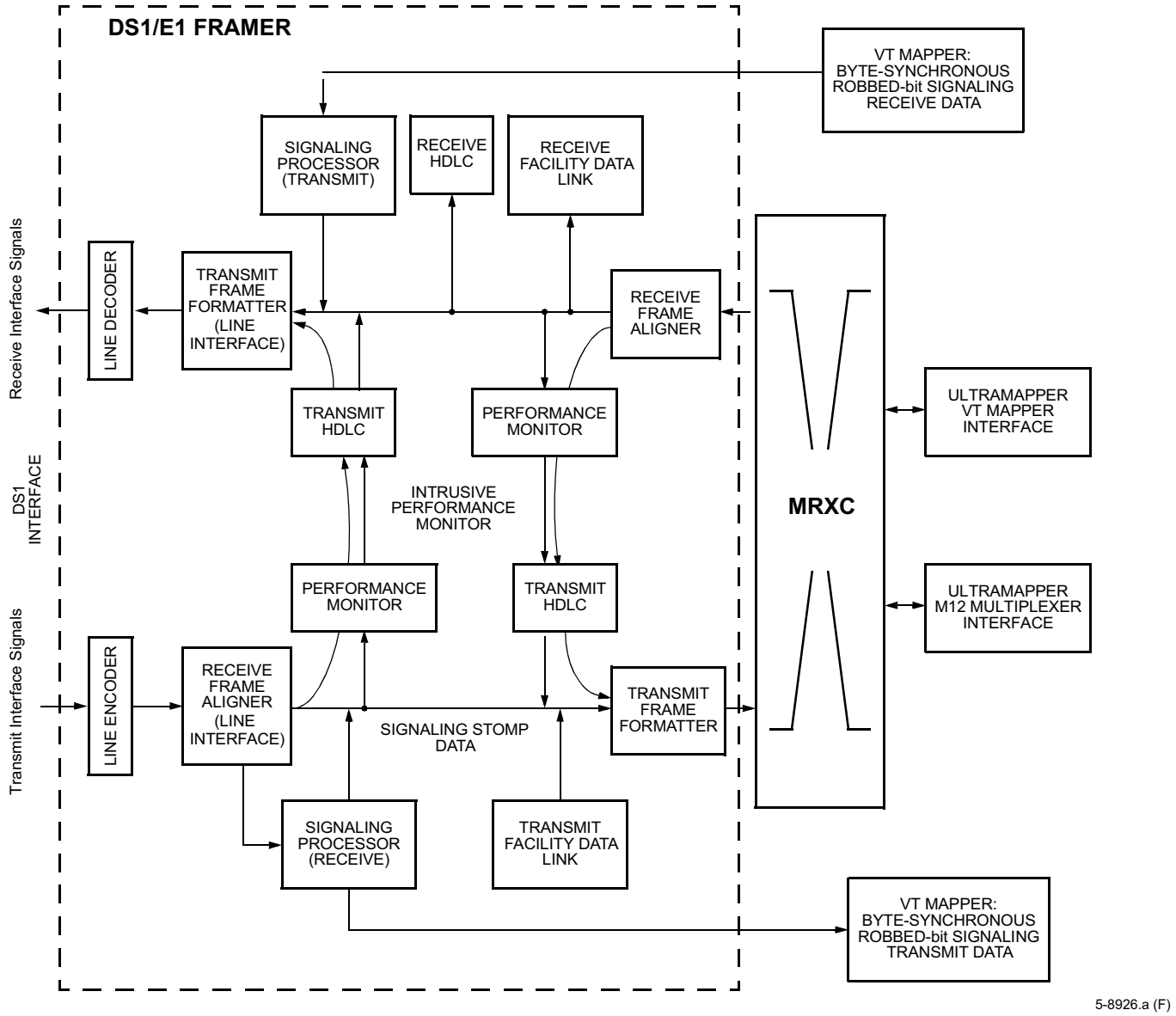

Figure 10. Internal Components of DS1/E1 Framer Block

4 Block Description (continued)

Functionalities present in each component are shown below.

4.15.1 Line Decoder/Encoder

The line decoder/encoder supports either single-rail or dual-rail transmission. In dual-rail mode, the line codes supported are as follows:

- Alternate mark inversion (AMI)
- DS1 binary 8 zero code suppression (B8ZS)
- ITU-CEPT high-density bipolar of order three (HDB3)

In the single-rail mode, a line interface unit (LIU) decodes/encodes the data. In the dual-rail mode, loss-of-signal is monitored.

In the case of coded mark inversion (CMI) coding (Japanese TTC standard JJ-20.11), the LIU decodes the data, listing both the CMI coding rule violations (CRVs) and line coding violations as bipolar violations. (In the CMI mode, the framer is in the single-rail mode.)

4.15.2 Receive Frame Aligner/Transmit Frame Formatter

The receive frame aligner and transmit frame formatter support the following frame formats:

- D4 ultraframe
- SF D4 ultraframe: FT framing only
- J-D4 ultraframe with Japanese remote alarm
- DDS
- *SLC*-96
- ESF
- J-ESF (J1 standard with different CRC-6 algorithm)
- Nonalign DS1 (193 bits—clear channel)
- CEPT basic frame (ITU G.706)
- CEPT CRC-4 multiframe with 100 ms timer (ITU G.706)
- CEPT CRC-4 multiframe with 400 ms timer (automatic CRC-4/non-CRC-4 equipment interworking) (ITU G.706 Annex B)
- Nonalign E1 (256 bits—clear channel)
- 2.048 coded mark inversion (CMI) coded interface (TTC standards JJ-20.11)

4.15.3 Receive Performance Monitor

The receive performance monitor detects the following alarms:

- Loss of receive clock
- Loss-of-signal
- Loss-of-frame
- Alarm indication signal (AIS)
- Remote frame alarms
- Remote multiframe alarms

These alarms are detected as defined by the appropriate *ANSI*, *AT&T*, ITU, and ETSI standards.

Performance monitoring, as specified by *AT&T*, *ANSI*, and ITU, is provided through counters monitoring the following:

- Bipolar violation
- Frame bit errors
- CRC errors
- Errored events
- Errored seconds
- Bursty errored seconds
- Severely errored seconds

In-band loopback activation and deactivation codes can be transmitted to the line via the payload or the facility data link. In-band loopback activation and deactivation codes in the payload or the facility data link are detected.

4.15.4 Signaling Processor

The signaling processor supports the following modes:

- Ultraframe (D4, *SLC*-96): 2-state, 4-state, and 16-state
- VT 1.5 SPE: 2-state, 4-state, and 16-state
- Extended Ultraframe: 2-state, 4-state, and 16-state
- CEPT: common channel signaling (CCS) (TS-16)
- Transparent (pass through) signaling
- J-ESF handling groups

Signaling features supported per channel are as follows:

- Signaling debounce
- Signaling freeze
- Signaling interrupt upon change of state
- Associated signaling mode (ASM)
- Signaling inhibit
- Signaling stomp

4 Block Description (continued)

Voice and data channels are programmable in the DS1 robbed-bit signaling modes. The entire payload can be forced into a data-only (no signaling channels) mode (i.e., transparent mode, achieved by programming one control bit).

Signaling access occurs through the on-chip signaling registers or the system interface. Data and its associated signaling information can be accessed through the system in either DS1 or CEPT-E1 modes.

4.15.5 Facility Data Link (FDL) Processor

The receive facility data link processor monitors the bit-oriented ESF data-link messages defined in *ANSI* T1.403. The transmit facility data link unit overrides the FDL-FIFO for the transmission of the bit-oriented ESF data-link messages defined in *ANSI* T1.403-1995.

The FDL processor extracts and stores data link bits from three different frame types as follows:

- D-bits and delineator bits from the *SLC*-96 multiultraframe.
- Data link bits from DDS frames (bit 6 of time-slot 24).
- Two multiframes of Sa[4:8] bits from timeslot 0 in CEPT basic and CRC-4 multiframes.

The respective bits are always extracted from frame-aligned frames and are stored in a stack. The processor control notification of stack updates through the interrupt mask registers.

The transmit FDL functional block performs the transmission of D-bits into *SLC*-96 Ultraframes, Sa-bits in CEPT frames, and D-bits in DDS frames.

- In *SLC*-96 frames, the D and delineator bits are always sourced from this functional block when the block is enabled for insertion.
- In DDS frames, the data link bits are always sourced from this functional block when this block is enabled for insertion. This functional block also provides the capability to transmit BOMs (bit oriented messages) in the data link channel of ESF links.
- In CEPT frames, the Sa bits are sourced from either the Sa stack within this functional block or from the system interface. The data link functional block only responds with valid data when selected by the Sa source control bits.

4.15.6 HDLC Unit

The HDLC processor formats the HDLC packets for insertion into the programmable channels. A channel can be any number of bits (1 to 8) from a time-slot.

The maximum number of channels is 64. The maximum channel bit rate is 64 kbits/s. The minimum channel bit rate is 4 kbits/s. Each channel is allocated 128 bytes of storage.

HDLC processing of data on the facility data link (PRMs, Sa-bits, or otherwise) is implemented by assigning the FDL bit position to a logical HDLC channel.

The application assumes the following:

STS-12/STM-4 is mapped with VT/TU signal structure.

Ultramapper 1 is configured for master mode (interface STS-12/STM-4).

Ultramappers 2—4 is configured for slave mode (interface STS-3/STM-1).

There are a total of 8064 DS0s/E0s (2016 DS0s/E0s per Ultramapper).

Mate interconnect utilizes STS-3 connection between master and each slave device.

System interface can be concentrated highway interface (CHI) or parallel system bus (PSB).

CHI can be programmed to operate at 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz clock and data rates.

The PSB interface consists of a 16-bit wide parallel bus operating at 19.44 Mbits/s.

5 Glossary

AIS	Alarm indication signal
AMI	Alternate mark inversion
APS	Automatic protection switch
ASM	Associated signaling mode
BER	Bit error rate
BLSR	Bidirectional line switching ring
BOM	Bit oriented message
BPV	Bipolar violation
B8ZS	Bipolar 8 zero substitution
CCI	Common channel signaling
CDR	Clock and data recovery
CHI	Concentrated highway interface
CMI	Coded mark inversion
CRC	Cyclic Redundancy Check
CRV	Coding rule violation
DACS	Digital access cross connects
DJA	Digital jitter attenuation
ESF	Extended superframe
EXZ	Excessive zeros
FCS	Frame check sequence
FDL	Facility data link
FEAC	Far-end alarm and control
FEBE	far-end block error
HDB3	High-density bipolar of order three
HDLC	High-Level Data Link Control
LIU	Line interface unit
LOC	Loss-of-clock
LOF	Loss-of-frame
LOS	Loss of signal
LOPOH	Lo-order path overhead
OOF	Out of frame
MCDR	Mate clock and data recovery
MRXC	Multirate cross connect
NSMI	Network serial multiplexed interface
PBGA	Plastic ball grid array
POAC	Path overhead access channel
PRBS	Pseudorandom bit sequence
PRM	Performance report message
QRSS	Quasirandom signal source
RAI	Remote alarm indicator
RDI	Remote defect indication
REI	Remote error indication
SDH	synchronous digital hierarchy
SEF	Severely errored frame
TCM	Tandem connection monitoring
TOAC	Transport overhead access channels
UPSR	Unidirectional path switch ring

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