SERTECH LABS
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TSC373/374
Up-Down Counters
• Decade
• Hexadecimal

Features

Choice of Output – Decade (373)
Or Hexadecimal (374)

High Noise Immunity – 3.5 Volts Min

Carry And Borrow Outputs For N-Bit Cascading

Clear Input Is Independent Of Count And Load

Individual Preset To Each Flip-Flop

Synchronous Operation

General Description

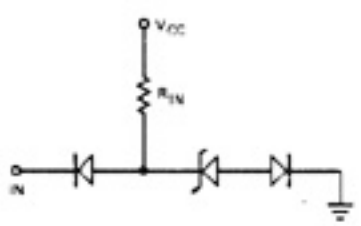
The 373/374 is a synchronous reversible (up/down) counter featuring master-slave flip-flops with active outputs. The outputs of the flip-flops are triggered by a low-to-high level transition of either of two clock inputs while the other is high. Pulsing one clock input causes the device to count up, while pulsing the other causes it to count down.

Provision has been made for setting information into the flip-flops. Whenever the load enable input is low, the flip-flop outputs will change to agree with the data inputs (independently of the count pulses). A master reset input resets all flip-flops to zero whenever it is high (regardless of the count and load inputs). Borrow and carry outputs are provided to allow cascading.

The 373 is a decade and the 374 a hexadecimal counter.

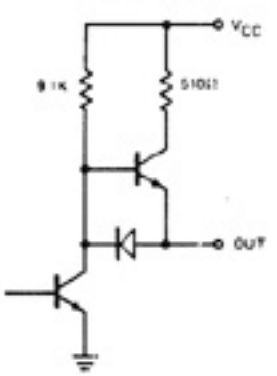
Equivalent Circuits

Typical Input



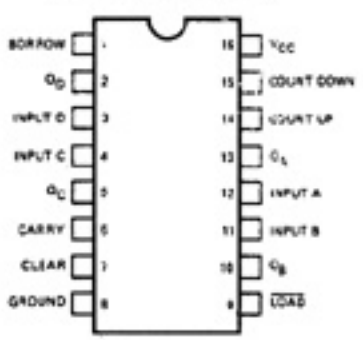
Input	R_{IN} (Typ)
CLEAR, LOAD	10K
DATA A, B, C, D	18K
CLOCK	10K

Typical Output



Connection Diagram

L Package
16 Lead Ceramic DIP



Order Part Numbers:
373AL, 374AL
(V_{CC} = 15V ±1V,
$-30°C \leq T_A \leq +70°C$)
373CL, 374CL
(V_{CC} = 12V ±1V, –30°
$-30°C \leq T_A \leq +85°C$)

Absolute Maximum Ratings

	Ceramic Package
Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100 ms)	18V
Input Voltage (any input)	−0.5 to +18V
Surge Sink Current (less than 100 ms at 25°C T_A)	20mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case 10ns max)	300°C

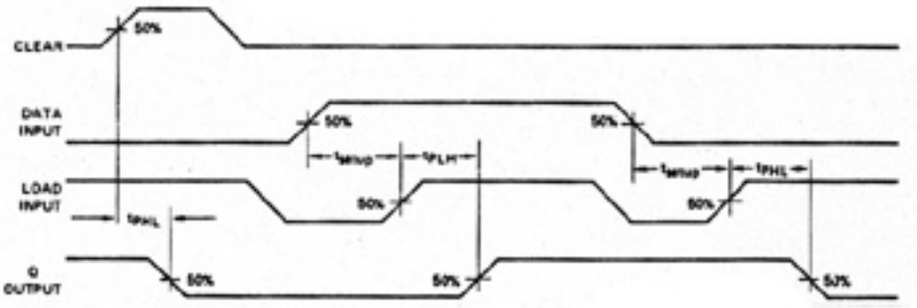
Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Electrical Characteristics

Parameter	Definition	Type C V_{CC} = +12V ± 1.0V	Type A V_{CC} = +15V ± 1.0V	Test Condition
V_{INL}	Input Threshold Voltage, Low	5.0V Min	5.0V Min	Guaranteed Input Low Threshold
V_{INH}	Input Threshold Voltage, High	6.5V Max	6.5V Max	Guaranteed Input High Threshold
I_{INL}	Input Current, Low	−2.1mA Max	−2.6mA Max	At V_{CC} Max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current	10μA Max	10μA Max	At V_{CC} Max with V_{IN} = V_{CC} Max
V_{OL}	Output Low Voltage	1.5V Max	1.8V Max	I_{OL} = 5 U.L. (1 U.L. = I_{INL})
V_{OH}	Output High Voltage	10V Min	13V Min	I_{OH} = 5 U.L. (1 U.L. = I_{INH})
V_{OHL}	Output High Voltage, Loaded	7.0V Min	9.5V Min	At V_{CC} Nominal, I_{OHL} = 5.0mA
I_{CC}	Power Supply Current	50mA Max	55mA Max	At V_{CC} Max Worst Case Condition (Q Outputs Low)
f_{MAX}	Max Input Count Freq.	1 MHz	1 MHz	Output Loaded with 5 U.L.
t_{setup}	Data to Load	250ns Min	250ns Min	
t_{PLH}	Count Up to Carry	425ns Max	425ns Max	t_{PLH} and t_{PHL} Based on Low to High (or High to Low) Transition of Output.
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Count Down to Borrow	525ns Max	525ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Either Count to Q	725ns Max	725ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Load to Q	725ns Max	725ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PHL}	Clear to Q	525ns Max	525ns Max	

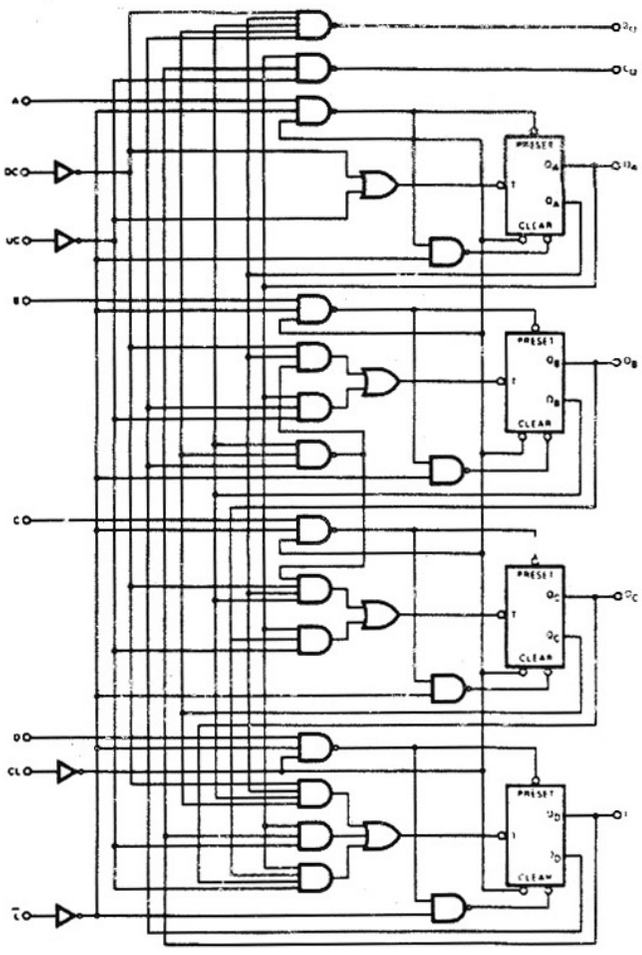
Note: I_{CC} is tested at V_{CC} (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range.

Switching Waveforms

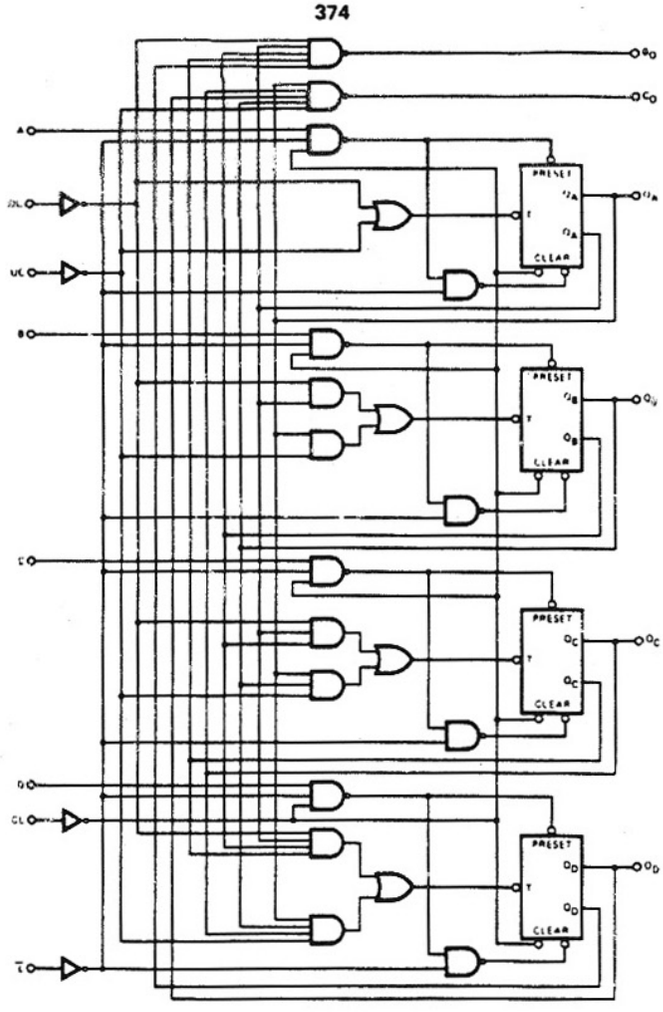


Logic Diagrams

373



374

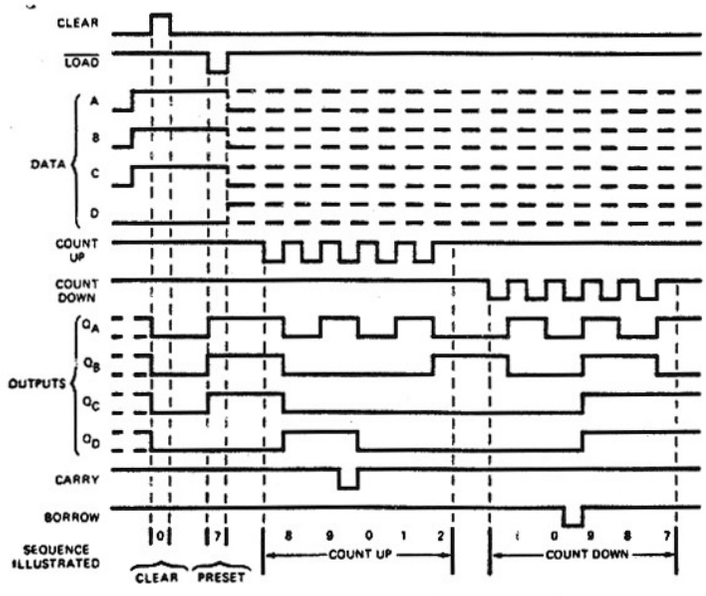


Timing Diagrams

373

The following sequence is illustrated below:

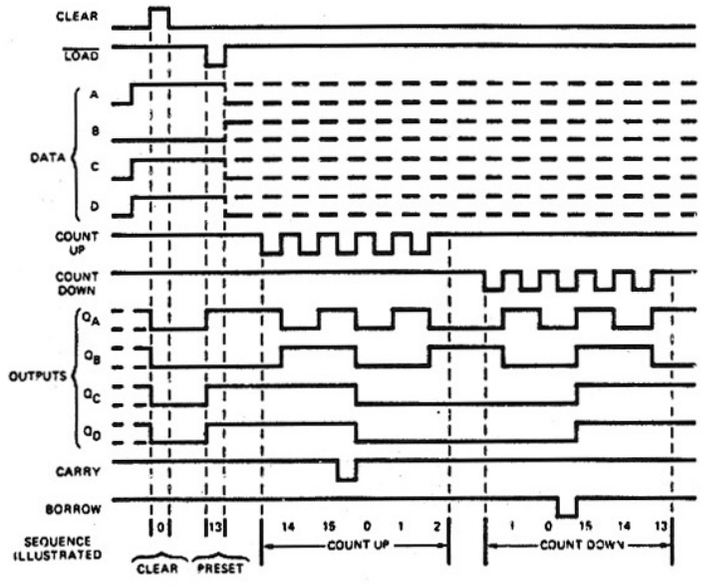
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, (carry), zero, one, and two.
4. Count down to one, zero, (borrow), nine, eight, and seven.



374

The following sequence is illustrated below:

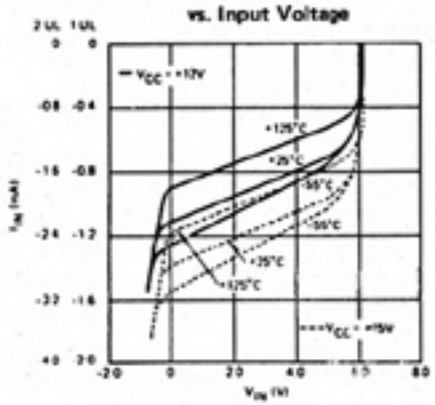
1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, (carry), zero, one, and two.
4. Count down to one, zero, (borrow), fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides loads, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

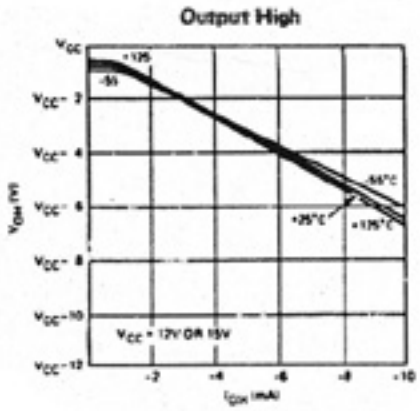
Typical Characteristics

Input Current vs. Input Voltage

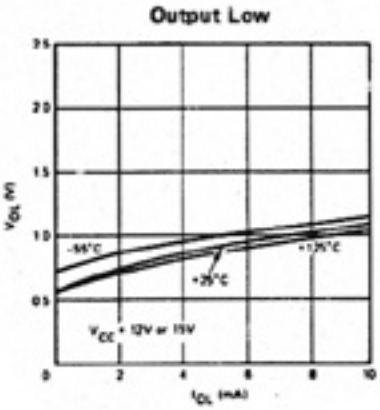


Output Current vs. Output Voltage

Output High



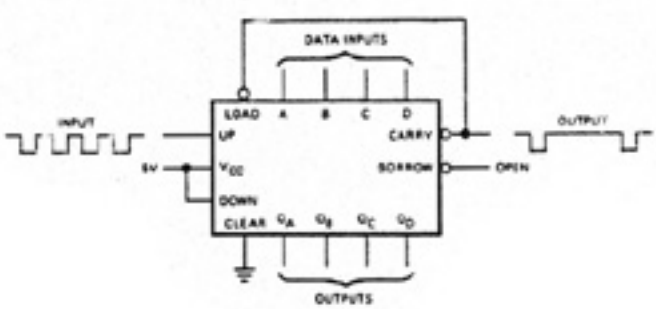
Output Low



Applications Information

Modulo-N Divider

The 374 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. Connect the carry output to the load input and the counter will count to the maximum state (15). The data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated. The 373 may be used in the same manner to perform division by any number from 1 to 10.



Cascading

Circuitry is provided internally for cascading these counters. No external components are required. The mode shown below is ripple borrow/carry.