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TSC371/372
Counters
- Decade
- Hexadecimal

Features

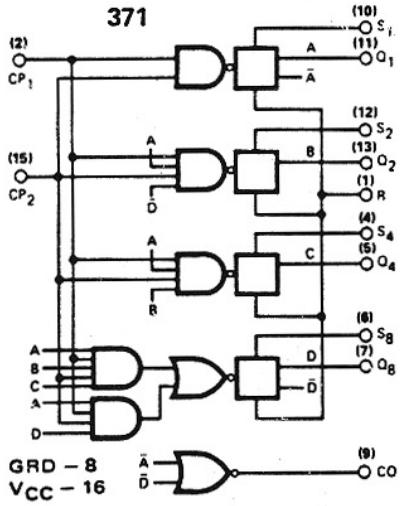
- DIRECT PRESET OR RESET TO ZERO
- TWO CLOCK LINES FACILITATE INPUT ENABLE
- NINTH COUNT (371) AND 15TH COUNT (372) OUTPUTS FOR CASCADING
- 1 MHz TYPICAL TOGGLE RATE

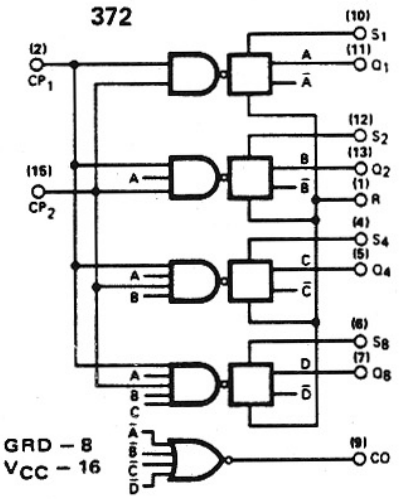
General Descriptions

The 371 is a master-slave decade counter that generates BCD outputs. It also provides two clock inputs to facilitate input enable control, direct set and reset inputs, and a ninth count output (carry output) so 371 cascades can generate counts of 100, 1,000, and so forth. Its outputs are ideal as inputs to the 380, 381, or 382 BCD to decimal decoders.

The 372 master-slave counter generates 4-bit binary outputs from 0 to 15 in the standard 1-2-4-8 binary code. It also provides two clock inputs to facilitate input enable control, direct set and reset inputs, and a 15th count output (carry output) to allow cascading to N binary stages.

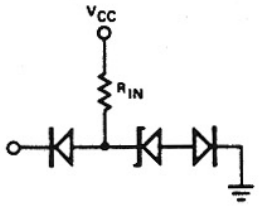
Logic Diagrams





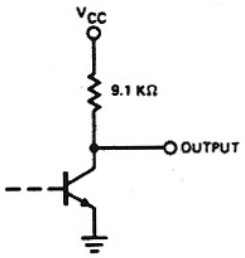
Equivalent Circuits

TYPICAL INPUT



INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	20 KΩ TYP.
ALL SETS	20 KΩ TYP.

TYPICAL OUTPUT



Truth Tables

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CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	CO
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	1
0	0	1	0	1	1
1	0	1	0	1	1

372

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	CO
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	0
0	0	0	1	1	0
1	0	0	1	1	0
0	1	0	1	1	0
1	1	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	1	1	1	1
1	1	1	1	1	1

Specifications

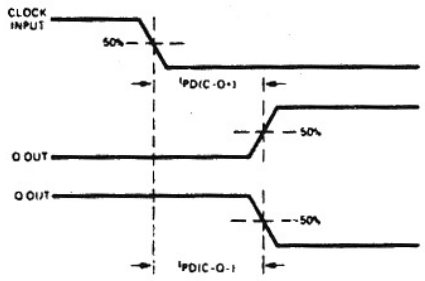
I_{CC} (WORST-CASE)	41 mA @ 13V, 53 mA @ 16V			
t_{PD} I/O FUNCTION FOR t_{PD}	600 ns S+Q+	200 ns R+Q−	800 ns C−Q+	300 ns C−Q−

TYPICAL TOGGLE RATE IS 1 MHz

Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at $V_{CC} \pm 1$V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



Loading Table

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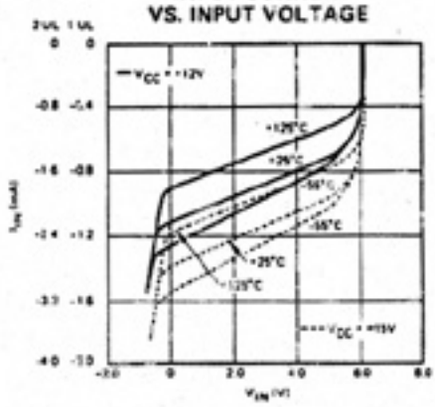
PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1 UL
CO	Carry output	2 UL
Q	Outputs	5 UL

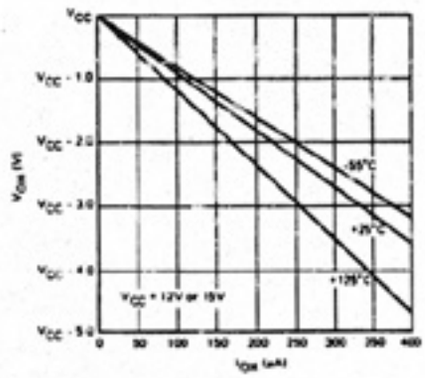
Typical Performance Characteristics

INPUT CURRENT
VS. INPUT VOLTAGE

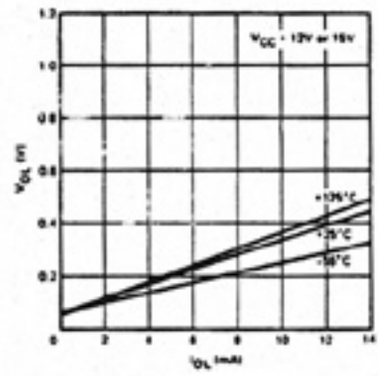


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH



OUTPUT LOW



Typical Applications

The 371 counts as the clock goes from high to low. Setting or resetting must be done only with the clock line low (either clock). To set, or to reset the device to zero, the desired set or reset line is switched high. The count operation is inhibited by grounding either clock input, allowing one clock input to be an enable control. All unused direct set and reset pins should be grounded.

Except for the different internal gating, to provide hexadecimal counting, the operation of the 372 is the same as the operation of the 371.

COUNTER MODES

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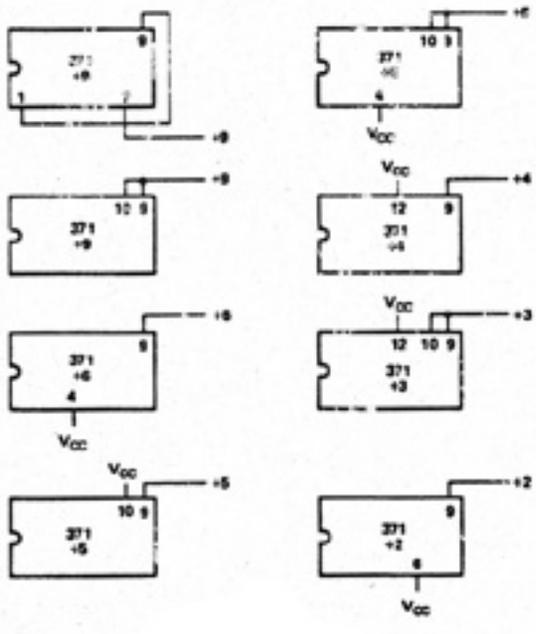

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