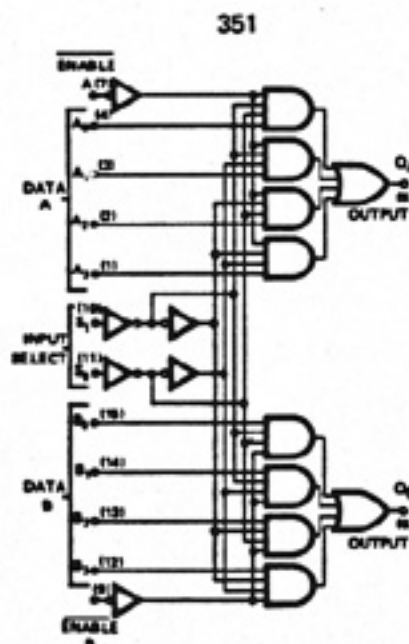
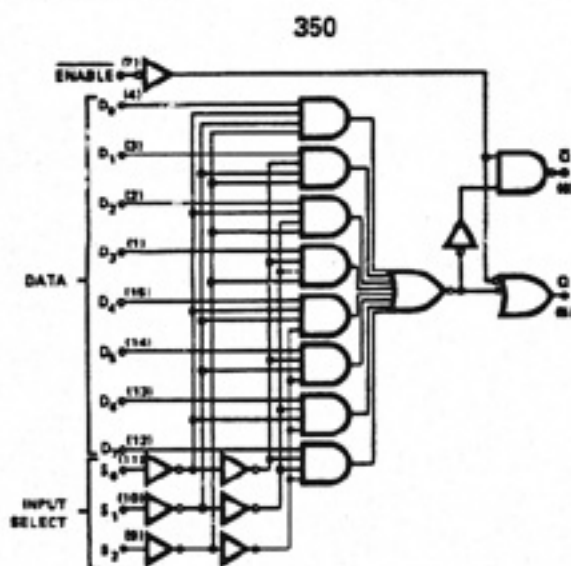


Features

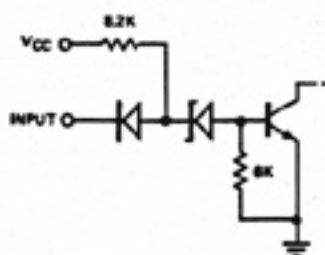
- VERSATILE DESIGN CONFIGURATION
- 3.5V (MIN) NOISE IMMUNITY
- ACTIVE PULLUP OUTPUTS – 12mA I_{OH} ENABLES LONG LINES TO BE DRIVEN
- SEPARATE ENABLE INPUTS (ON 351) – ALLOWS INDEPENDENT OPERATION
- COMPLEMENTARY OUTPUTS (ON 350) – FOR GREATER LOGIC FLEXIBILITY
- FULLY BUFFERED INPUTS – ONLY 1 UNIT LOAD (UL)
- INPUT ENABLE

Logic Diagrams

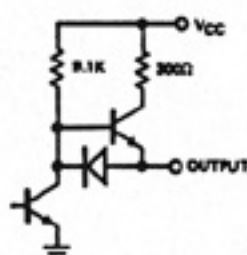


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Truth Tables

350

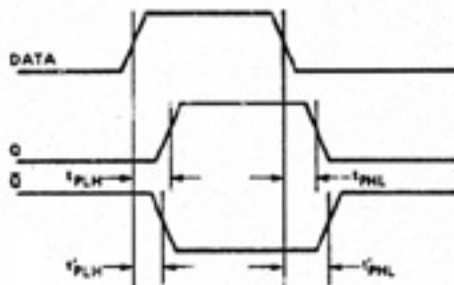
Enable	S ₀	S ₁	S ₂	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	Q	$\bar{Q}$
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	1	0	0	0	X	0	X	X	X	X	X	0	1
0	1	0	0	1	X	1	X	X	X	X	X	1	0
0	0	1	0	0	X	X	0	X	X	X	X	0	1
0	0	1	0	1	X	X	1	X	X	X	X	1	0
0	1	1	0	0	X	X	X	0	X	X	X	0	1
0	1	1	0	1	X	X	X	1	X	X	X	1	0
0	0	0	1	0	X	X	X	0	X	X	X	0	1
0	0	0	1	1	X	X	X	1	X	X	X	1	0
0	1	0	1	0	X	X	X	X	0	X	X	0	1
0	1	0	1	1	X	X	X	X	1	X	X	1	0
0	0	1	1	0	X	X	X	X	0	X	X	0	1
0	0	1	1	1	X	X	X	X	1	X	X	1	0
0	1	1	1	0	X	X	X	X	0	X	X	0	1
0	1	1	1	1	X	X	X	X	1	X	X	1	0
1	X	X	X	X	X	X	X	X	X	X	X	1	1

351

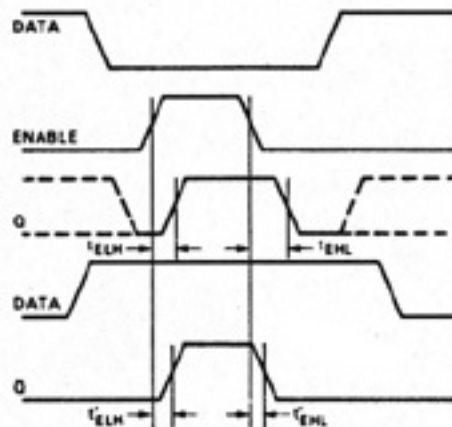
Enable	S ₀	S ₁	D ₀	D ₁	D ₂	D ₃	Q
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	0	X	0	X	0
0	1	0	1	X	1	X	1
0	0	1	0	X	X	0	0
0	0	1	1	X	X	1	1
0	1	1	0	X	X	X	0
0	1	1	1	X	X	X	1
1	X	X	X	X	X	X	0

Switching Time Waveforms

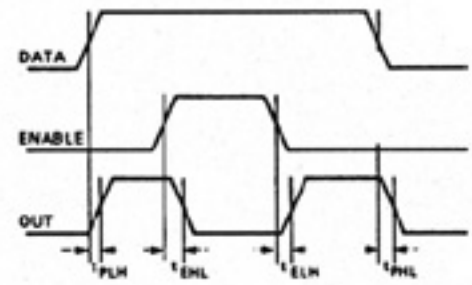
350



350



351



Specifications

I_{CC} (Worst Case) 33mA @ 13V, 40mA @ 16V

350

Parameter	Maximum
t _{PLH}	450ns
t _{PHL}	200ns
t' _{PLH}	400ns
t' _{PHL}	250ns

With enable input at low logic voltage.

350

Parameter	Maximum
t _{ELH}	400ns
t _{EHL}	250ns
t' _{ELH}	400ns
t' _{EHL}	250ns

High on enable input sets both Q and $\bar{Q}$ to high.

351

Parameter	Maximum
t _{PLH}	400ns
t _{PHL}	150ns
t _{ELH}	500ns
t _{EHL}	160ns

High on enable input sets output low.

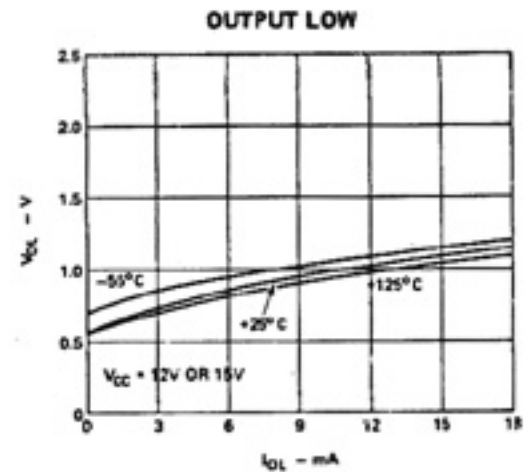
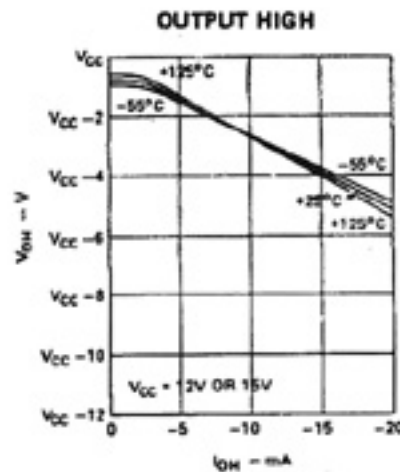
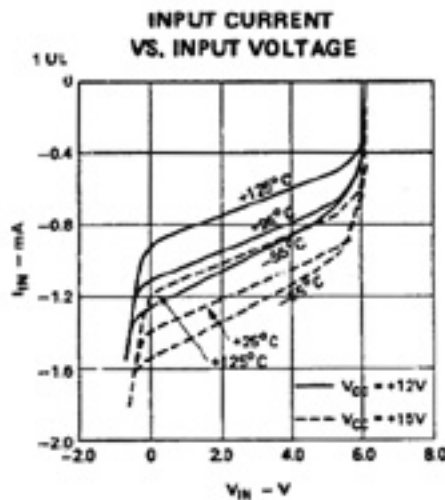
See page 12 for electrical summary data.

Loading Table

350, 351

PIN	LOADING
Input Select, All Data Inputs and Enable	1 UL
Output (Q or $\bar{Q}$)	8 UL

Typical Performance Characteristics



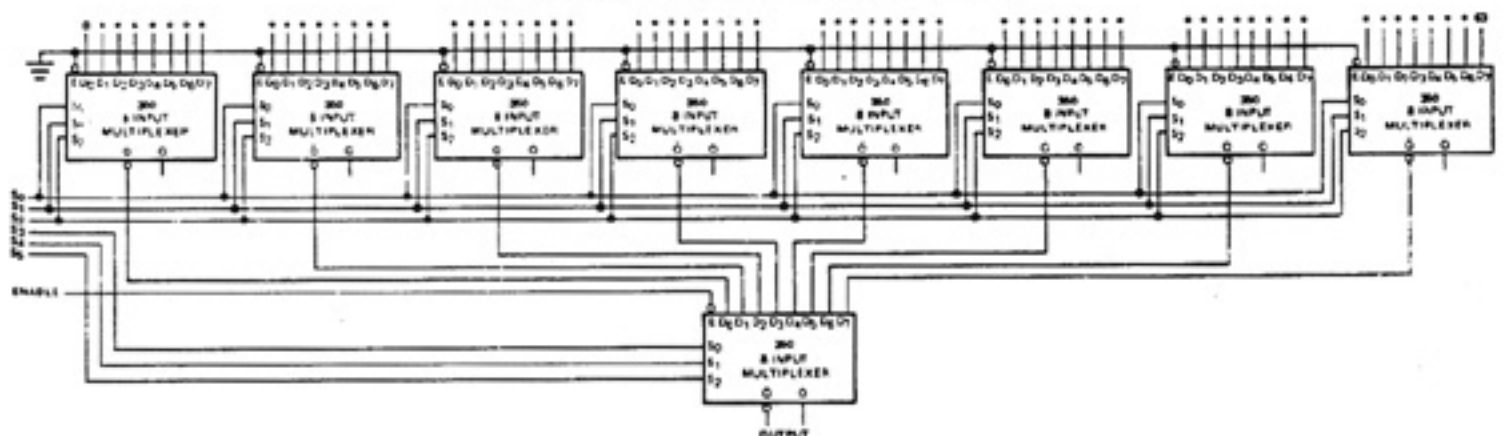
Typical Applications

The 350 8-Bit Multiplexer is the electronic equivalent of a single-pole eight-position switch. It can serve as an 8-Bit parallel to serial converter, but differs from a shift register in that each input is selected by a 3-Bit binary number. High logic levels on the various input select lines S_0 , S_1 , and S_2 , determine the active input. An active enable input expands the multifunctional capabilities of the device and allows inhibit operation.

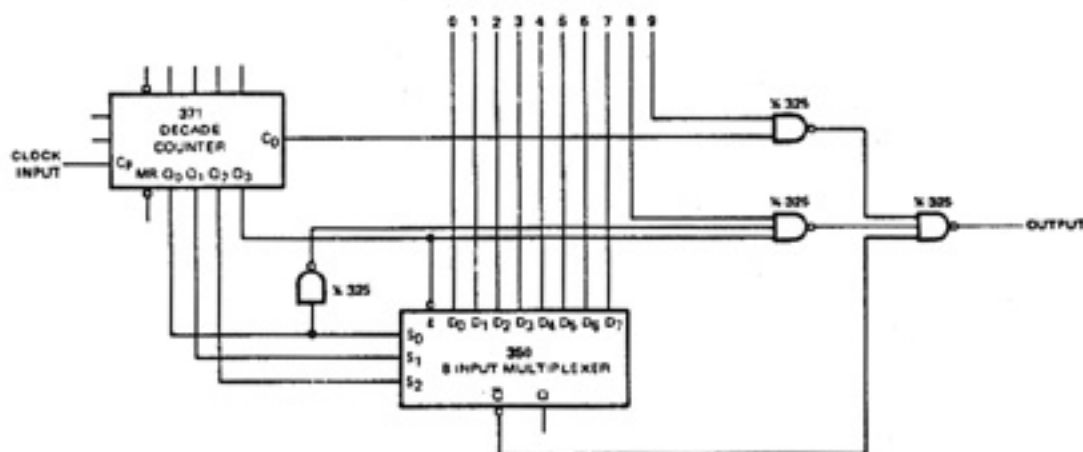
Complementary outputs are provided for greater logic flexibility.

The 351 Dual 4-bit Multiplexer is essentially an electronic two-pole four-position switch whose output is determined by the logic state of the two input select lines, S_0 and S_1 . It features common input select lines and independent output enables for two-phase operation.

64 INPUT DIGITAL MULTIPLEXING SCHEME



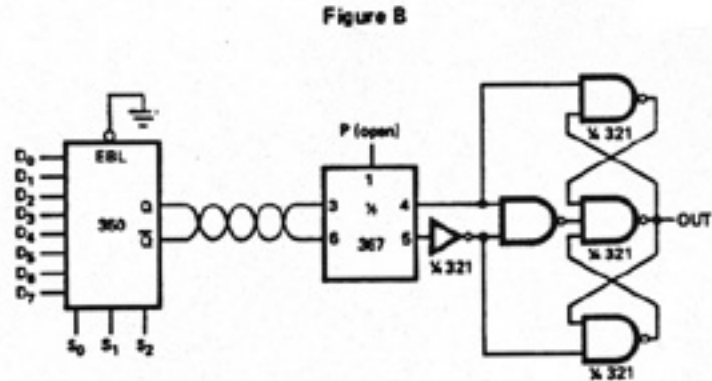
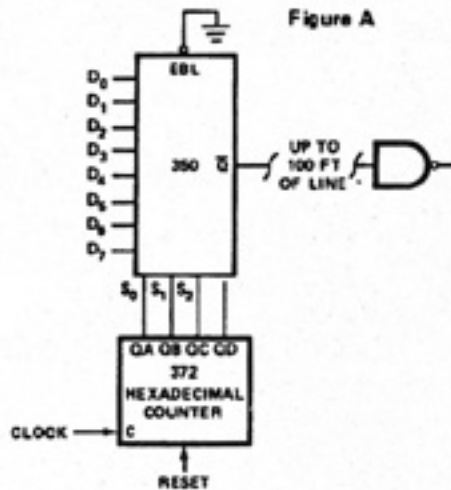
DECADE MULTIPLEXER



Typical Applications (contd.)

REMOTE PARALLEL TO SERIAL DATA TRANSMISSION

The high output current (I_{OH}) of the 350/351 makes them ideal line driver circuits — no special drivers are required.



MULTI-CHANNEL DATA BUS

The enable function of the 350 (a low on ENABLE sets both Q and $\bar{Q}$ to logic "1") allows data busing of N channels of data to a single output. The 301 has expandable inputs and each additional input requires only the addition of a discrete diode on expanded input (i.e., 1N4148).

MINTERM GENERATION WITH 350 8 BIT MULTIPLEXER

The 350 and 351 Multiplexers resemble read-only memories in their basic functioning (i.e., the input select word, and data inputs can be considered an address generating some specific output). This similarity makes these devices practical in such applications as minterm generators or sequencers.

