PHAST-3N
STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator with Telecom Bus Interface
TXC-06103

DATA SHEET

FEATURES

- Byte-parallel SDH/SONET line interface
  - Parity detection/generation with optional frame pulse input
- Section, line, and path overhead byte processing
  - RAM access for overhead bytes
  - Line AIS, REI (FEBE) and RDI detection
  - B2 and B3 byte BIP detection with BER measurement
  - J0 byte TIM or single-byte comparison
  - S1 byte change in synchronization status
  - J1 byte TIM or 64-byte LF/CR alignment
  - C2 byte PSL, unequipped, PDI detection
  - G1 byte RDI (single-bit or three-bit), path REI (FEBE) detection
  - H4 byte multiframe detection with optional V1 pulse generation
- Section, line and path overhead byte insertion
  - From RAM, interfaces, terminal, ring (mate device) or receive side (e.g., RDI)
- Supports 1+1 or 1:N APS applications
- N1 byte tandem connection processing (STM-1 VC-4 format)
- Interfaces
  - TOH (RSOH & MSOH) bytes with programmable marker pulse
  - K1/K2 APS bytes, E1 and E2 order wire bytes
  - Section data communication (D1-D3) bytes
  - Line data communication (D4-D12) bytes
  - POH bytes (for VC-4 or each STS-1)
  - Alarm Indication Port (AIP) for line/path ring operation
  - Scan and drive leads (two each)
- Telecom Bus terminal interface
  - Clock, byte data, parity, C1J1V1, SPE, POH byte, AIS indication, bus active indication
- Tributary unequipped/AIS generation for TUG-3, TU-2/VT6, TU-12/VT2 and TU-11/VT1.5
- Telecom Bus terminal interface source timing mode
  - Transmit timing for downstream devices from reference clock and frame pulse
- Receive and transmit pointer rejustification to receive and transmit reference clock and frame pulse
- Receive pointer tracking
  - AIS, LOP, NDF and false pointer detection,
- Receive and transmit line/path AIS generation
- Motorola or Intel microprocessor interface for memory access
- Boundary scan, loopbacks, and optional PRBS generator/detector
- Single +3.3 volt, ±5% power supply; 5 volt tolerant inputs
- 256-lead, 27 mm x 27 mm, plastic ball grid array package
- Device driver:
  - Insulates application from register access details
  - Driver APIs configure and manage the PHAST-3N device
  - Default configurations are provided within the driver
  - One command configures all the control registers
  - Driver can download the firmware code into PHAST-3N
  - Similar architecture to other device drivers, such as the TL3M

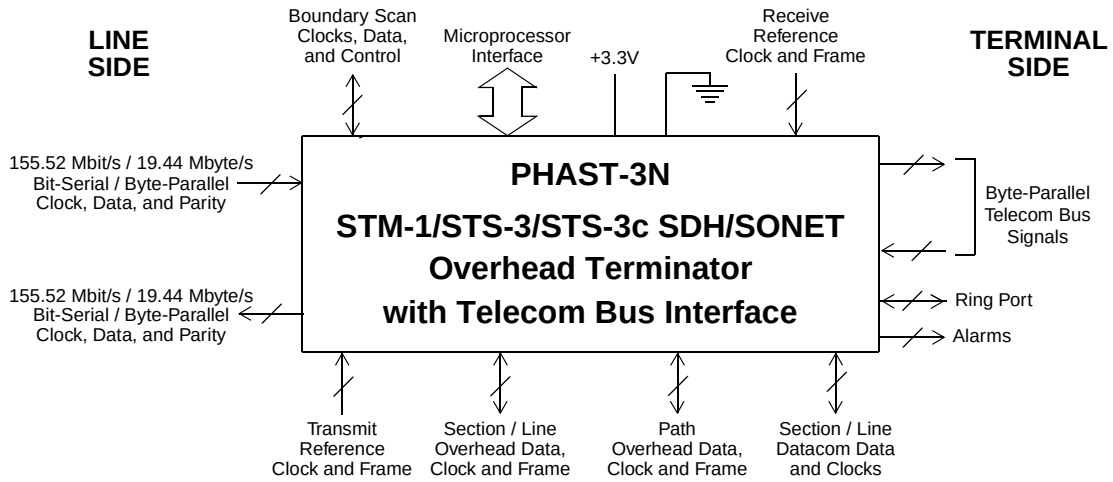
DESCRIPTION

The TranSwitch PHAST-3N (TXC-06103) is an STM-1/STS-3/STS-3c section, line and path overhead termination device that provides a terminal side Telecom Bus interface. The PHAST-3N device provides either a serial or parallel interface on the line side. The serial interface provides 155 MHz clock recovery and clock synthesis. Line and section overhead bytes are processed. The PHAST-3N performs pointer tracking, and receive and transmit pointer justification. The PHAST-3N also performs POH byte processing. TOH (RSOH and MSOH) and POH bytes are written into RAM locations for microprocessor access or provided via interfaces for external access. In the transmit direction, the PHAST-3N will either interface to downstream timing or provide the timing signals. The transmit POH bytes can be inserted from RAM, a serial POH interface, a mate PHAST-3N device for path and line ring applications, or directly from the terminal side.

The PHAST-3N can generate line and path AIS in the receive and transmit directions. For testing, the device provides boundary scan, a PRBS generator and analyzer, B2 and B3 byte BER measurements, programmable BIP error mask generation, line and terminal loopback, and STS-1 terminal loopback. The device provides either Motorola or Intel microprocessor access. Performance counters can be configured to be saturating or roll-over. The interrupts, with mask bits, can be programmed for activation on positive, negative, or positive and negative alarm transitions, or positive levels. A software polling register is also provided.

APPLICATIONS

- Telecom Bus applications for TU/VT mappers
- Line and path ring applications
- Add/drop multiplexers
- Cross connect systems
- Data communications systems



Document Number:
PRELIMINARY TXC-06103-MB
Ed. 5, May 2002

TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

TABLE OF CONTENTS

Section **Page**

List of Figures 3
List of Tables 4
Overview 5
Features 7
Block Diagram 12
Block Diagram Description 13
Lead Diagram 18
Lead Descriptions 19
Absolute Maximum Ratings and Environmental Limitations 38
Thermal Characteristics 38
Power Requirements 38
Input, Output and Input/Output Parameters 39
Timing Characteristics 42
Operation 68
- SDH/SONET Formats 68
- Path Modes of Operation 71
- Transmit Timing Modes 72
- Reference Retiming 72
- Alarm Structure 74
- Interrupt Structure 75
- Performance Counters 78
- Pseudo-ECL Termination 79
- Clock Recovery 80
- Clock Synthesis 82
- Disabling of Scrambler and Descrambler in Serial Mode 82
- Disabling of SONET Transport Overhead and SDH Section Overhead Byte Processing 83
- Receive Pointer Tracking 84
- Receive J0 and J1 Byte Processing 88
- Receive C2 Bytes 90
- Receive Terminal Side AIS Generation 92
- Receive Terminal Interface Bus 96
- Transmit Terminal Interface Bus 99
- Tandem Connection Operation 100
- Transmit G1 Byte REI and RDI Insertion 105
- Transmit H4 Byte 111
- Transmit Path AIS Generation 113
- VC-4 and STS-1 Unequipped Status Generation 113
- TU-N/VTN Tributary Unequipped Status and AIS Generation 114
- Transmit Line REI (FEBE) 116
- Transmit Line RDI 116
- Transmit Line AIS 117
- Stuff Column Insertion 118
- Ring Applications 119
- POH Byte Interfaces 122
- B2 BER Measurement 123
- B3 BER Measurement 124
- BIP Error Mask Generation 124
- Loopbacks 126
- High Impedance Test Mode 127
- Pseudo-Random Test Generator and Analyzer 128

TABLE OF CONTENTS (cont.)

Section **Page**

Boundary Scan 130
Internal Processor Initialization 132
Power-Up and Initialization 136
Access of Registers Located in RAM 139
Memory Maps and Bit Descriptions 140
Common Memory Map Segments 141
Transmit Side Memory Map Segments 157
Transmit Common Registers 157
Transmit Registers Per STM-1 VC-4 or STS-3 STS-1 No. n 180
Receive Side Memory Map Segments 191
Receive Common Registers 191
Receive Registers Per STM-1 VC-4 or STS-3 STS-1 No. n 220
Transmit and Receive ACE Processor Access 239
Package Information 242
Application Diagram 243
Ordering Information 244
Related Products 244
Standards Documentation Sources 245
List of Data Sheet Changes 247
Documentation Update Registration Form* 249

* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

Figure **Page**

1 PHAST-3N TXC-06103 Block Diagram 12
2 PHAST-3N TXC-06103 Lead Diagram 18
3 Receive Serial Interface Timing 42
4 Receive Parallel Interface Timing 43
5 Receive Terminal Interface Timing 44
6 Receive TOH Interface Timing 45
7 Receive Section Data Communication Interface Timing (D1-D3 Bytes) 46
8 Receive Line Data Communication Interface Timing (D4-D12 Bytes) 46
9 Receive Alarm Indication Port (AIP) Interface Timing 47
10 Receive APS, E1 and E2 Interface Timing 48
11 Receive POH Interface Timing 49
12 Transmit Serial Interface Timing 51
13 Clock Synthesis Timing 52
14 Transmit Parallel Interface Timing 53
15 Transmit Terminal Interface Normal Timing 54
16 Transmit Terminal Interface Source Timing 55
17 Transmit TOH Interface Timing 57
18 Transmit Section Data Communication Interface Timing (D1-D3 Bytes) 58
19 Transmit Line Data Communication Interface Timing (D4-D12 Bytes) 58

LIST OF FIGURES (cont.)

Figure **Page**

20 Transmit Alarm Indication Port (AIP) Interface Timing 59
21 Transmit APS, E1 and E2 Interface Timing 60
22 Transmit POH Interface Timing 61
23 Intel Microprocessor Interface Read Cycle Timing 63
24 Intel Microprocessor Interface Write Cycle Timing 64
25 Motorola Microprocessor Interface Read Cycle Timing 65
26 Motorola Microprocessor Interface Write Cycle Timing 66
27 Boundary Scan Timing 67
28 Transmit Clocking Scheme - Serial Mode 73
29 Termination of Pseudo-ECL Leads 79
30 Connection of an Unused P-ECL Lead 80
31 Clock Recovery Jitter Tolerance 81
32 Clock Recovery External Component Connections 81
33 Clock Synthesis External Component Connections 82
34 Pointer Tracking State Machine 85
35 IEC Processing 101
36 IEC Insertion 102
37 H4 Byte Functions in Source Timing Mode 111
38 H4 Byte Functions in Normal Timing Mode 112
39 Transmit Line REI Count in M1 Byte Logic Diagram 116
40 Loopbacks 127
41 Boundary Scan Schematic 131
42a Firmware Download Procedure Phase 1: Boot RAM Load 133
42b Firmware Download Procedure Phase 2: Rx IRAM Load 134
42c Firmware Download Procedure Phase 3: Tx IRAM Load 135
43 PHAST-3N TXC-06103 256-Lead Plastic Ball Grid Array Package 242
44 Mux of three STS 1 to/from one STS-3 243
45 Bidirectional add/drop Fiber Multiplexer 243

LIST OF TABLES

Table **Page**

1 TOH Bytes - SONET Transport Overhead Byte Assignment 69
2 SOH Bytes - SDH STM-1 Section Overhead Byte Assignment 69
3 STS-3 STS-1 POH Byte Assignment 70
4 STM-1 VC-4 POH Byte Assignment 70
5 Parity Control Bit Selection 96
6 Receive Terminal Side E1/E2 Byte Utilization 97
7 Normal Timing Mode Parity Control Bit Selection 99
8 Source Timing Mode Parity Control Bit Selection 99
9 ETSI Tandem Connection Message Structure 100
10 ETSI Tandem Connection Message N1 (Z5) Byte, Bits 7 and 8 Utilization 100
11 B2 Bit Error Rate Measurement Settings 123
12 B3 Bit Error Rate Measurement Settings 124
13 Initialization State of Configurable Control & Mask Registers 136

OVERVIEW

The PHAST-3N provides a section, line and path overhead byte termination for a STM-1 AU-4 (STS-3c), or STS-3 (STM-1 AU-3) format. Upstream line access to the PHAST-3N is provided by either a serial 155.52 MHz pseudo-ECL interface or a 19.44 MHz byte-parallel interface. The serial interface is equipped with an optional 155.52 MHz to 19.44 MHz Clock Recovery block. For incoming parallel byte data, byte boundary alignment and frame pattern detection are performed according to ITU-T (formerly CCITT) G.783 and Bellcore GR-253-CORE. An option for scrambling/descrambling is also provided. The incoming TOH (RSOH and MSOH) bytes are checked for line RDI, line AIS, and other related TOH (RSOH and MSOH) functions. All TOH (RSOH and MSOH) section and line bytes are written into RAM locations in the memory map for microprocessor access. The section and line bytes are also provided at interfaces for external access. In addition to a TOH (RSOH and MSOH) byte interface, the APS bytes K1 and K2, the order wire bytes E1 and E2, section data communication bytes D1 through D3, and line data communication bytes D4 through D12, have separate interfaces. An option is provided to place the K1/K2 and E1/E2 bytes on the receive terminal interface data bus.

The PHAST-3N provides pointer tracking for the STM-1 AU-4, STS-3c, three STM-1 AU-3s, and STS-3 STS-1 formats. The pointer tracking state machine has been implemented based on the requirements found in ETSI documents. Both positive and negative pointer movements are counted. In addition to the various alarms provided by this state machine, false concatenation is detected and the size bits can be programmed or disabled.

The POH bytes are monitored and checked, and are passed through the PHAST-3N to the receive terminal interface. Processing of the POH bytes includes: J1 byte TIM comparisons, three-bit or single-bit RDI detection, and other related POH functions. A B3 byte bit error rate (BER) measurement circuit and tandem connection processing for the N1 byte are also provided. The tandem connection circuit supports ETSI message processing only (the ANSI format is not supported). The ETSI format is fully supported, including a 16-byte TIM comparison. The N1 byte may be terminated with B3 byte compensation, or passed through to the receive terminal interface. The POH bytes are also provided at a POH interface for external access.

The PHAST-3N provides optional pointer justification against a reference clock and frame pulse. Both positive and negative pointer justification events are counted. The H1/H2 byte pointer generation circuit conforms to the state machine specified in ITU-T/ETSI standards. In addition, the size bits in the H1/H2 bytes, and the s-bits in the Y bytes (STM-1 AU4 or STS-3c format) are programmable.

The PHAST-3N provides the ability to generate line AIS, path AIS, or a TranSwitch-defined path AIS format at the receive terminal side. Enable bits are used to control the generation of the AIS signal when an alarm is declared. In addition, the microprocessor can control the generation of the various AIS signals.

The receive terminal interface is compatible with the Telecom Bus that TranSwitch uses in its other SDH/SONET products. The receive terminal interface consists of byte-wide data and signals which identify the locations of the POH and payload (SPE) and the C1 (J0) and J1 bytes. In addition, an internal H4 byte multiframe detector/generator can insert a V1 pulse into the C1J1 signal in order to identify the locations of the V1/V2 bytes in the tributary signals for downstream circuits. Other options provided at the terminal interface include a parity bit, a fail indication (AIS) bit, bus activity indication bit, the ability to force the data bus to a tristate condition, programmable even or odd parity, the ability to invert the output clock, and a POH/STUFF byte marker signal.

Although the PHAST-3N terminates the TOH (RSOH and MSOH) bytes, options are provided for generating and inserting a fixed A1/A2 frame pattern or a microprocessor-written pattern, and passing through the K1/K2 and E1/E2 bytes to the receive data bus. In addition, the device can be configured to provide an in-band AIS/RDI indication in the E1 bytes.

In the transmit direction, the PHAST-3N can be configured to provide a normal timing mode or a source timing mode. In normal timing mode, the downstream device or circuit provides the input timing and data signals. In the source timing mode, the PHAST-3N provides the timing signals for the downstream device or circuits, with data provided as an input. A data adjustment delay circuit is provided for offsetting the round-trip delay between the downstream circuit and the PHAST-3N.

The PHAST-3N provides the choice of controlling the insertion of the POH bytes in the STM-1 VC-4 (STS-3c) and individual STM-1 AU-3 (STS-3 STS-1) formats. Individual POH byte control is provided. The insertion of POH bytes into the VC-4 (SPE) or each of the VC-3s (STS-1s) can be bypassed or configured for a path terminating mode. In the bypassed mode, the POH bytes are transmitted in line side format without processing. One exception is made for the N1 byte, which may be used for tandem connection applications. The other mode, path terminating mode, enables the PHAST-3N to insert the POH bytes into the VC-4 or each of the VC-3 (STS-1) formats from either memory map locations, a POH interface, the local receive side, or a mate PHAST-3N in a ring configuration. Tandem connection capability is also provided, including the ability to insert a 16-byte message and frame, and other signals, for ETSI applications. The ability to generate TCODI, TCRDI, etc., from receive side alarms is also provided, with enable bits for the various alarms.

Optional pointer justification and generation is provided relative to a reference clock and frame pulse. Both positive and negative pointer justification events are counted. A 16-bit pointer leak register is provided for the FIFO. The s-bits in the Y bytes and the values of the size bits within the H1/H2 pointer are programmable.

The ability to generate an unequipped, or a supervisory unequipped, format for the VC-4 and for each of the STS-1s is provided. The PHAST-3N can also be programmed to generate a tributary TU/VT (TU-3, TU-2/VT6, TU-12/VT2, or TU-11/VT1.5) unequipped format. An option is provided in which an external signal can generate a tributary AIS signal in place of the tributary unequipped format. The PHAST-3N can also generate line AIS or path AIS based on transmit alarms or under microprocessor control.

Section and line overhead bytes can be inserted from memory map locations, interfaces, the receive side (e.g., line RDI), or from a mate PHAST-3N when configured for ring applications. The TOH (RSOH and MSOH) bytes, either individually or as groups, are programmable for their source selection.

The line interface can be configured as a pseudo-ECL serial interface or as a parallel interface. The selection is common with the receive side. The serial interface is provided with an optional Clock Synthesis block, in which a 155.52 MHz clock signal is derived from a 19.44 MHz clock reference.

The microprocessor interface is selectable for either Intel or Motorola devices. A hardware interrupt and a global software polling register are provided. The software polling register enables the microprocessor to determine the location of the alarm. The interrupt structure uses mask bits for enabling/disabling the individual alarms. The latched bits for controlling the interrupt can be programmed to occur on a positive level, positive transition, negative transition, or both positive and negative transitions. Performance counters can be configured to either roll over to zero or saturate when the count reaches all ones. The BIP/REI (FEBE) performance counters can be configured to count bit errors either individually or as blocks.

Testing capabilities include boundary scan, forcing all output leads to tristate, BIP error mask with programmable frames in error, B2 and B3 byte BER measurement circuits, line loopbacks, terminal loopback including looping back individual STS-1s (retiming feature must be enabled), and a PRBS generator and analyzer.

The PHAST-3N is equipped with two internal processors, one for the receive side and the other for the transmit side. The purpose of the internal processors is to perform many of the TOH (RSOH and MSOH)/POH processes. For example, controlling the alarms that will generate path RDI, and implementing the J1 trail trace message comparisons.

The PHAST-3N software driver has the same architecture as some other TranSwitch device drivers, such as the TL3M driver, and is meant to be easily integrated with them. The application software calls the driver functions to configure, control and manage the PHAST-3N device. The device driver insulates the application from the internal details of the device register usage and provides a higher level of abstraction. Particularly powerful are the default configurations provided within the driver that allow one single command to bring the device to operational mode. The device driver will also take care of downloading the firmware code into the PHAST-3N.

FEATURES

The following is a list of features supported by the PHAST-3N:

- Modes of operation
  - STM-1 AU-4 (STS-3c)
    - TOH (RSOH and MSOH) byte termination
    - POH byte termination with transmit pass-through option
  - STS-3 (STM-1 AU-3)
    - TOH (RSOH and MSOH) byte termination
    - POH byte termination with transmit pass-through option for each AU-3 or STS-1
- Line interface
  - Pseudo-ECL bit-serial interface features
    - Loss of signal detection (per ITU-T or ANSI standards)
    - Loss of clock detection
    - Receive clock reference 8 kHz generation
    - Frame alignment (OOF and LOF per standards)
    - Clock recovery and synthesis
    - Receive clock reference 19.44 MHz generation
  - Byte-parallel interface features
    - Byte-wide data at 19.44 MHz
    - Optional frame pulse
    - Loss of clock detection
    - Parity detection (even or odd)
    - Receive clock reference 8 kHz generation
    - Receive clock reference 19.44 MHz generation
- TOH (RSOH and MSOH) and POH byte external access
  - TOH (RSOH and MSOH) byte interface with byte marker selection
    - Markers for J0, D1-D3, D4-D12, E1, E2, K1/K2, F1 bytes
  - APS (K1 and K2 bytes) interface
  - E1 byte interface
  - E2 byte interface
  - Section data communication (D1 - D3 bytes) interface
  - Line data communication (D4 - D12 bytes) interface
  - POH byte interface
- Reference timing interfaces
  - 19.44 MHz clock and frame derived from transmit clock in the serial mode only
  - Transmit retiming input (clock and data)
  - Source timing input (clock and data)
  - Receive retiming input (clock and data)
  - Input clocks monitored for loss of clock

- Terminal side interface
  - Telecom Bus standard (interface for SDH/SONET mappers)
    - Plus parity, POH, bus active, and fail (AIS) indicators
    - Receive TOH (RSOH and MSOH) byte insertion option
      - A1/A2 bytes (fixed or microprocessor-written)
      - E1/E2 (AIS/RDI or order wire) bytes
      - K1/K2 APS bytes
    - Transmit options
      - Normal timing mode
        - Timing and data signals are inputs
      - Source timing mode
        - Timing signals are outputs
        - Data signals are inputs
- Alarm Indication Port (AIP) for APS ring applications
  - 81-bit frame with CRC-4 loss of frame and loss of clock detection
    - with CRC-4 error insertion check
  - Line RDI, new APS byte, new K3 byte, debounced K1/K2 and K3 bytes, B2 byte errors, line REI (FEBE), B3 byte errors, path REI (FEBE), path RDI, SDH/SONET loss of signal alarm, SDH/SONET loss of frame alarm and CRC-4 loss of frame alarm
  - Write to local counters option for AIP interface: B2, B3, path and line REI (FEBE)
- TOH (RSOH and MSOH) byte termination
  - J0 byte mismatch detection
    - 16-byte trail trace message
    - Single-byte (ANSI)
    - No comparison
  - Scrambling/descrambling (option)
  - B1/B2 BIP bytes
    - B2 byte BER detection - programmable
    - 16-bit counter
    - Disable B1 byte BIP option, with option to count external B1 byte errors
  - Sync byte (S1 byte) debounce indication (bits 5-8)
  - Write TOH (RSOH and MSOH) bytes to RAM locations
  - K1/K2 byte processing
    - Line RDI (K2 = 110)
    - Line AIS (K2 = 111)
    - New APS (three K1 bytes and first five bits of K2 byte)
    - Inconsistent APS byte (three out of 12)
    - K1/K2 bytes debounced (three frames)
  - Line REI (FEBE) counter (16-bit)
  - Disable TOH (RSOH and MSOH) byte processing option
    - Higher order mutiplexer applications
    - Designated lead

- Pointer tracking
  - ETSI (ETS 300 417 document state machine)
  - Programmable size bits or disable
  - False concatenation detection
  - Option for AIS/LOP transition bypass
  - LOP, AIS, and NDF alarms
- POH byte termination
  - Receive direction
    - Write to RAM locations in memory map
    - Monitor POH bytes for various alarms
    - Process (e.g., AIS generation) with individual enable bits
    - Pass through POH bytes to terminal
  - Transmit direction
    - Insert into POH bytes
      - From terminal interface
        - With tandem connection option
      - From RAM locations in memory map (i.e., microprocessor-written values)
      - From POH interface
      - From receive side (e.g., RDI)
      - From Alarm Indication Port (e.g., RDI)
- POH bytes
  - J1 byte mismatch detection
    - 16-byte trail trace comparison
    - 64-byte (ANSI) with CR/LF alignment
    - No comparison
  - H4 byte
    - Bypass option
    - V1 reference generation
    - Detection and generation
    - LOM and OOF feature of detection (per G.783)
  - C2 byte
    - Signal label mismatch
    - Unequipped detection and generation
    - VC AIS detection
    - PDI (ANSI) detection
  - G1 byte
    - Single-bit or three-bit RDI detection
    - Alarm enable bits plus microprocessor control
    - REI (path FEBE) counter
    - Bit 8 control

- Tandem connection byte (N1/Z5) for STM-1 VC4 format
  - Receive and transmit
    - Separate enable control options
  - ETSI format (TIM/TCODI/TCRDI etc.)
  - B3 byte compensation upon termination option
  - Receive and transmit IEC counters
- B3 byte BIP
  - B3 byte BER detection - programmable
  - 16-bit error counters

- Retiming and pointer generation
  - Receive and transmit FIFOs
    - Automatic or microprocessor-controlled recentering capability
    - PJ and NJ counters
  - Programmable size bit selection
  - Programmable Y byte bits
  - Bypass option

- Test features
  - JTAG boundary scan (IEEE 1149.1)
  - BIP error mask with control of number of frames sent
  - Line loopback
    - Transmit to receive
    - Receive to transmit, serial mode only
  - Terminal loopback
    - VC-4 or individual STS-1s
  - Set all output leads to high impedance state, except boundary scan output (High-Z)
  - Pattern generator and analyzer
    - 2^{23}-1 per O-151
    - 16-bit error counter for PRBS analyzer

- Other features
  - VC-4/AU-3/STS-1 unequipped (force all bytes to zeros)
    - Supervisory unequipped option (J1, G1, and B3 bytes valid with 522 pointer value)
    - Tributary unequipped generation
    - Option to generate AIS
      - Three TUG-3s in VC-4
      - Any TU-2/VT6, TU-12/VT2, TU-11/VT1.5
  - Receive and transmit AIS generation
    - Line AIS
    - Path AIS
      - With TranSwitch-defined receive path AIS generation

- Options
  - Microprocessor control
  - Alarms with enable bits
  - External lead option
  - E1 byte in-band indication generation
  - Transmit terminal detection
    - E1 byte
    - H1/H2 bytes

- Alarm and interrupts
  - Latched and unlatched alarms
    - Individual mask bits
  - Software polling register
  - Programmable interrupt transition
    - Positive level
    - Positive transition
    - Negative transition
    - Positive/Negative transitions

- Counters
  - Bit or block (selection for section, line and path)
  - Roll-over or saturation (with interrupt)

- Microprocessor bus
  - Split address/data buses
  - Selectable Intel or Motorola microprocessor interface compatibility

BLOCK DIAGRAM

The functional block diagram for the PHAST-3N is shown in Figure 1 below:

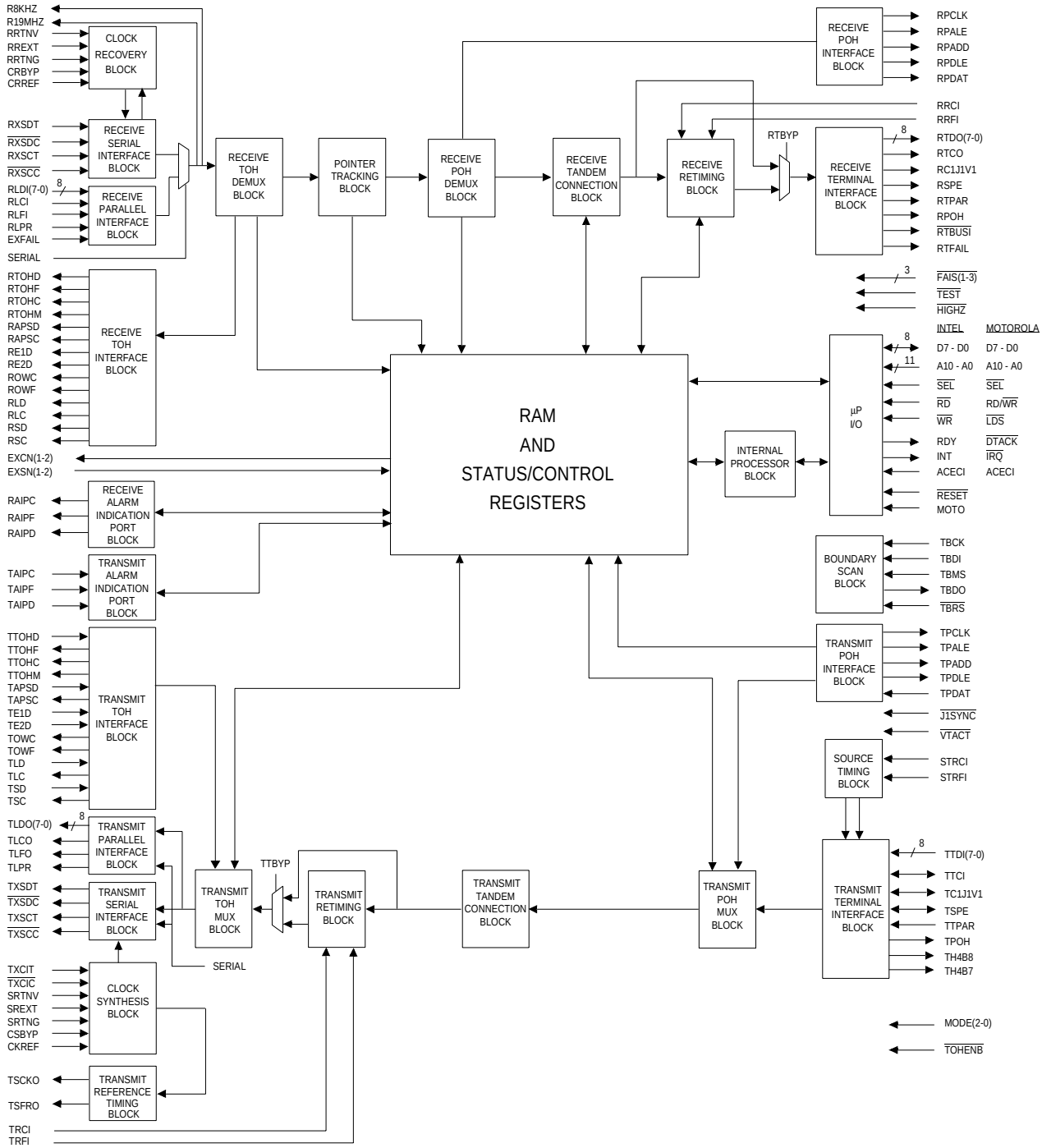


Figure 1. PHAST-3N TXC-06103 Block Diagram

BLOCK DIAGRAM DESCRIPTION

The receive line side interface consists of a Receive Parallel Interface block and a Receive Serial Interface block. The parallel interface consists of a byte-wide data interface RLDI(7-0), an optional frame pulse RLFI, clock input RLCI, a parity lead RLPR, and an external signal fail indicator EXFAIL. When the frame pulse is not provided by the upstream circuitry, the PHAST-3N will perform a search of the incoming data bits for the A1/A2 bytes. The search mechanism is the same one used when the serial interface is selected. The parity calculation can be selected to be either odd or even, calculated over the data byte or data byte plus frame pulse. Other than providing an indication for the microprocessor, a parity error will have no effect on the operation of the PHAST-3N. However, a bit error in the data may cause a BIP error in addition to a parity error. The external signal fail indication can be used for supplying a loss of frame and/or loss of signal indication from an upstream device or circuit. The action taken for this indication will be the same as that for a loss of signal alarm when the serial interface is selected. The parallel data signal is also monitored for loss of signal when the descrambler is enabled. An alarm occurs when no transitions are detected in the parallel data for 125 microsecond period. The input clock signal (TLOC) is also monitored for a stuck high or low condition.

The pseudo-ECL bit-serial interface is selected by placing a high on the SERIAL lead. This interface is provided with an optional Clock Recovery block which may be bypassed by placing a high on the CRBYP lead. When enabled, a 155.52 MHz clock is recovered from the pseudo-ECL data leads. A 19.44 MHz clock reference (CRREF) is required for the clock recovery block. This clock lead may be connected to the CKREF lead in non-looped timing applications. A loss of signal detector is provided which has an option to configure the loss of signal detector parameters to ANSI or ETSI requirements. The serial interface searches for the A1/A2 byte pattern. Out of frame and loss of frame detection are performed.

For both interfaces, the internal 19.44 MHz clock that is derived from the 155.52 MHz or 19.44 MHz clock is checked for stuck high or low states. A 8 kHz clock reference signal is derived and provided on the R8KHZ lead. A 19.44 MHz clock reference signal is also derived and provided on the R19MHZ lead. The 19.44 MHz clock reference signal is derived from the 155.52 MHz clock when the clock recovery block is bypassed, from the clock recovery block when it is enabled, or from the 19.44 MHz parallel clock input (RLCI).

The Receive TOH Demultiplexer block is responsible for interfacing the section and line bytes to the Receive TOH Interface block, writing the bytes into RAM locations in the memory map for microprocessor access, and for processing the various TOH (RSOH and MSOH) bytes according to standards. The processing functions performed by this block include: J0 byte mismatch detection for either a single byte (ANSI) or 16 bytes (ETSI), B1 byte parity check, de-scrambling, B2 byte parity check with a programmable BER measurement, line REI (FEBE) count, K1 and K2 byte APS byte processing and debouncing, line RDI and AIS detection, and change in synchronization in the S1 byte. K1 and K2 byte processing includes APS byte failure detection and change in APS status detection. The B1 byte parity detection feature can be disabled and the counter configured to count the number of bits set to 1 in the B1 block. Likewise, the descrambler can be disabled.

The Receive TOH Interface block provides an interface to all of the TOH (RSOH and MSOH) bytes, K1 and K2 APS bytes, E1 byte, E2 byte, section data communications bytes D1-D3 and line data communications bytes D4-D12. The Receive TOH Interface block also provides a programmable marker pulse RTOHM for selected TOH (RSOH and MSOH) bytes. This will enable external circuitry to identify the location of TOH (RSOH and MSOH) bytes in the serial bit stream.

The PHAST-3N also provides an option to disable processing of the TOH (RSOH and MSOH) bytes by placing a high on the $\overline{\text{TOHENB}}$ lead. It is useful for applications in which the PHAST-3N is configured in a higher order multiplexer system where TOH byte processing is performed in the preceding device.

The Pointer Tracking block determines the start of the J1 byte and the payload by processing the pointer bytes H1 and H2. Three pointer tracking state machines are provided for the AU-3 and STS-1 formats. The size bits can be disabled or programmed for the state machine. This block also provides a false concatenation detector to determine if the incoming format matches the format selected by the microprocessor. Positive and negative pointer movements are counted. Three alarms are provided: loss of pointer, path AIS, and new pointer indication.

The Receive POH Demultiplexer block performs POH byte processing. This includes a 16-byte J1 byte TIM comparison, B3 byte BIP check and BER measurement, C2 byte mismatch, unequipped, VC AIS and PDI detection, G1 byte REI (FEBE) and single-bit or three-bit RDI detection, H4 byte multiframe detection and generation with a V1 pulse option, and K3 byte debouncing and alarm indication when the STM-1 AU-4 format is *selected. All POH bytes are written into RAM locations in the memory map for microprocessor access and provided at the POH interface.

The Receive POH Interface block formats the POH bytes into a serial bit stream for external access. Depending upon the mode of operation, up to three sets of POH bytes will be provided, for each of the AU-3s or STS-1s. The POH interface consists of a clock RPCLK, address enable signal RPALE, address signal RPADD, data enable signal RPDLE, and data signal RPDAT.

The Receive Tandem Connection block is responsible for processing the N1 byte, when enabled. The PHAST-3N supports only ETSI tandem connection format. The PHAST-3N will count the OEI and REI (FEBE) values as well as perform message frame alignment, a 16-byte TIM comparison against a microprocessor-written message, TC RDI and TC ODI detection, and provide access to the spare bits in the multiframe structure. In addition, the PHAST-3N can perform IEC processing, terminate the N1 byte and compensate the B3 byte, or provide the N1 byte intact to downstream circuitry without B3 compensation.

The receive Alarm Indication Port (AIP) block provides receive alarms, debounced K1, K2 and K3 bytes, path and line REI (FEBE) and RDI status. A CRC-4 is also calculated on the data.

The Receive Retiming block provides payload justification to an external clock RRCI and frame pulse RRFI using FIFOs. For STS-3 operation, three FIFOs are provided. The retiming block can be bypassed when required. Three measurements are taken, i.e., slow, fast and immediate on each side of center. An internal TranSwitch developed algorithm is used to control the leak rate. When the FIFO limits are exceeded, it can be reset automatically or by the microprocessor. The pointer is recalculated and inserted into the outgoing bit stream. The size bits and the s-bits in the Y bytes are programmable. Positive and negative justification movements against the reference are counted. The reference clock is also monitored for stuck high and low conditions.

The Receive Terminal Interface block generates line AIS, path AIS, or a TranSwitch-defined path AIS when a receive alarm is declared. A majority of the alarms have enable/disable bits by which an alarm can be prevented from causing the AIS signal downstream. AIS can also be forced using the external leads $\overline{\text{FAIS3}}$, $\overline{\text{FAIS2}}$ and $\overline{\text{FAIS1}}$, when enabled. The same leads can be used to send RDI when enabled. Output signals are data RTDO(7-0), clock RTCO, SPE signal RSPE, timing signal RC1J1V1, POH indication signal RPOH, parity bit RTPAR, AIS indication RTFAIL, and a bus activity signal $\overline{\text{RTBUSI}}$. The output bus can also be forced to a tristate condition if required. A clock inversion feature is provided which enables the PHAST-3N to clock the bus signals out on the opposite clock edge. Although the TOH (RSOH and MSOH) bytes are normally terminated within the device, the PHAST-3N can regenerate the A1/A2 bytes or insert a microprocessor-written value. The line side K1/K2 APS bytes may also be provided as an output on the bus. An option is provided in which the E1/E2 bytes placed on the bus may be either the line side order wire bytes or bytes used as an in-band AIS indication.

In the transmit direction, the Transmit Terminal Interface block provides a byte data interface to downstream circuitry. In the normal timing mode, data TTDI(7-0), clock TTCI, SPE indicator TSPE, timing signal TC1J1V1 and parity TTPAR are input signals. When the source timing mode is enabled, the clock TTCI, SPE indicator TSPE, timing signal TC1J1V1 POH column indicator TPOH, and H4 multiframe indicators TH4B7 and TH4B8 are output signals and the data TTDI(7-0) and parity TTPAR are input signals. The source timing mode is used in applications that require the PHAST-3N to provide the timing signals for downstream circuitry. Control bits are provided to compensate for delays between data and timing signals.

The Source Timing block generates the transmit terminal bus timing signals using an external reference clock STRCI and reference frame pulse STRFI. The clock is monitored for a stuck high or low state.

The Transmit POH Multiplexer Interface block inserts the POH bytes into the transmitted STM-1 VC-4 (STS-3c), or three STS-3 STS-1 (STM-1 AU-3) formats. Two general modes of operation are provided, a pass-through mode and a termination mode. In the pass-through mode, all POH bytes are transferred transparently through this block without processing. Options are provided to select any of the three STS-1s (AU-3s). Thus, one or more STS-1s can be transferred transparently through the PHAST-3N. In path terminating mode, several options are available: the individual bytes may be inserted from a POH interface, from RAM locations in the memory map, from the local receive side for path RDI and REI (FEBE) indications, or by using RDI and REI (FEBE) indicators from an Alarm Indication Port for path protected ring applications.

Unequipped or supervisory unequipped generations are provided. The PHAST-3N can also be programmed to generate an unequipped format for TU-3s, TU-2 (VT6)s, TU-12 (VT2)s, or TU-11 (VT1.5)s. Using an external pulse $\overline{\text{VTACT}}$ for the columns of the TU (VT) selected, a tributary AIS condition can be generated instead.

The Transmit POH Interface block provides timing output signals needed for clocking in up to three sets of POH bytes. The POH interface consists of a clock TPCLK, address enable signal TPALE, address signal TPADD, data enable signal TPDLE, and input data signal TPDAT.

The Transmit Tandem Connection block is used for monitoring terminal side IEC errors and inserting tandem connection bit information into the N1 byte, when enabled. The PHAST-3N inserts the TC REI (FEBE) and TC OEI value, constructs the multiframe message structure, inserts a microprocessor-written 16-byte TIM message and TC RDI/ODI states, and provides control of the spare bits in the frame. In addition, the PHAST-3N can also generate a tandem connection AIS indication.

The Transmit Retiming block provides payload justification to an external clock TRCI and frame pulse TRFI using a FIFO. The retiming block can be bypassed when required. Three measurements are taken, i.e., slow, fast and immediate on each side of center. When the FIFO limits are exceeded, it can be reset automatically or by the microprocessor. The pointer is recalculated and inserted into the transmit bit stream. The size bits and the s-bits in the Y bytes are programmable. Positive and negative justification movements against the reference are counted. The reference clock is also monitored for stuck high and low conditions.

The Transmit TOH Multiplexer block inserts the TOH (RSOH and MSOH) bytes into the transmitted format from either RAM locations in the memory map, the TOH (RSOH and MSOH) byte interface, the receive side (line REI (FEBE) and RDI) or the Alarm Indication Port for ring applications. The insertion control options are divided up according to function, such as the line data communication bytes. The ability to generate a line AIS on selected transmit alarms is also provided.

The Transmit TOH Interface block provides an interface to all of the TOH (RSOH and MSOH) bytes, K1 and K2 APS bytes, E1 byte, E2 byte, line data communication bytes, and section data communication bytes. The TOH (RSOH and MSOH) interface also provides a programmable marker pulse TTOHM for selected TOH (RSOH and MSOH) bytes. This enables external circuitry to identify the location of a TOH (RSOH and MSOH) byte for the serial bit stream.

The transmit Alarm Indication Port (AIP) block provides the alarm and status information for inserting the line and path REI (FEBE), line RDI and RDI for the G1 bytes in the transmitted frame.

The transmit line side interface consists of a Transmit Parallel Interface block and a Transmit Serial Interface block. The parallel interface consists of a byte-wide data interface TLDO(7-0), frame pulse TLFO, clock TLCO, and a parity bit TLPR. Even or odd parity may be selected in addition to calculated parity for the data bytes only or for the data bytes and the frame pulse.

The pseudo-ECL serial interface is selected by placing a high on the SERIAL lead. The selection is common with the receive side. The serial interface is provided with a Clock Synthesis block which may be bypassed by placing a high on the CSBYP lead. When enabled, a 155.52 MHz clock is derived from a 19.44 MHz clock signal CKREF The 155.52 MHz pseudo-ECL clock is used for clocking out the pseudo-ECL data.

The Transmit Reference Timing block is used to derive a 19.44 MHz clock reference TSCKO and frame pulse reference TSFRO when either the serial or byte-parallel line side interface is selected.

All of the control registers, performance counters, status and alarm indications, and internal processors are accessed through the Microprocessor Input/Output Interface block. The PHAST-3N supports either an Intel-compatible or a Motorola-compatible microprocessor bus interface, with some signal leads performing different functions according to the type of interface selected via the MOTO lead.

When MOTO is low, the Intel microprocessor bus interface is selected and its signal leads consist of: an 8-bit bidirectional data bus D(7-0), an 11-bit address input bus A(10-0), a select input $\overline{SEL}$, a read input $\overline{RD}$, a write input $\overline{WR}$, an interrupt request output INT, and a ready output RDY. D0 and A0 are defined as the least significant bits.

When MOTO is high, the Motorola microprocessor bus interface is selected and its signal leads consist of: an 8-bit bidirectional data bus D(7-0), an 11-bit address input bus A(10-0), a select input $\overline{SEL}$, an active low LDS signal $\overline{LDS}$ for 68302 operation, a read/write input RD/$\overline{WR}$, an interrupt request output $\overline{IRQ}$, and a data transfer acknowledgment output $\overline{DTACK}$. D0 and A0 are defined as the least significant bits.

An external clock ACECI, asynchronous with respect to the other clocks connected to the PHAST-3N, is used for the ACE Internal Processor block and for internal RAM arbitration (i.e., internal processor read/write operations versus external microprocessor read/write operations). This clock should be operated at a frequency of 48 MHz ±2% and with a duty cycle of (50±10)%.

The alarm reporting structure consists of unlatched and latched (event) alarm bit positions. The unlatched alarm bit positions will reflect the current status of the detection circuit (e.g., C2 mismatch detection). A latched alarm (event bit) may be selected to latch on either a positive level, positive transition, negative transition or both transitions of the associated current status bit. A latched bit position, and all other latched bit positions in a register, are cleared during a microprocessor read cycle for that register.

The latched (event) bits are used to activate a hardware interrupt, when enabled. The PHAST-3N provides both a hardware indication INT/$\overline{IRQ}$ and software polling register indications. The software polling register provides a way to have the microprocessor read a register in memory to detect the alarm(s) that caused the interrupt, or the alarms that are set, without having to read all the alarm registers until the active alarms are found.

All counters are capable of counting events as either bits or blocks, unless otherwise specified. All 16-bit performance counters have a special 16-bit read operation which will allow uninterrupted access, without the danger of one byte changing while the other byte is read. All the performance counters can be configured to be either saturating or non-saturating. When a performance counter is configured to be saturating, the counter stops at its all-ones maximum count. A saturating counter is always reset on a microprocessor read cycle. When a counter is configured to be non-saturating, it is not cleared on a microprocessor read cycle but continues to count, and it rolls over to all zeros on the count following all ones. Counts that occur during the read cycle are held, with the counter being updated afterwards. All the performance counters can be reset simultaneously by writing to a reset control bit.

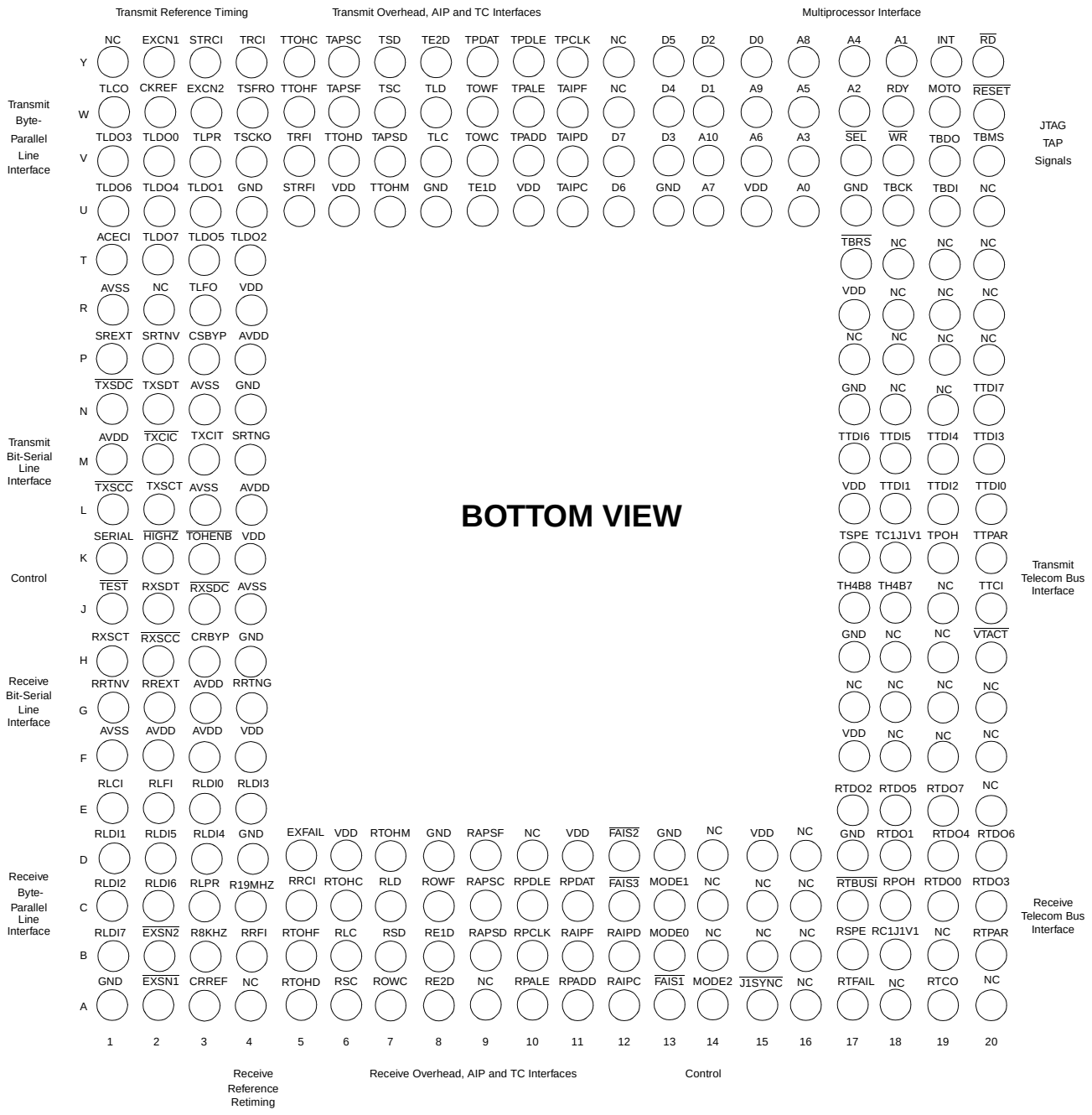
The PHAST-3N supports the following boundary scan test instructions as specified in IEEE 1149.1 documents: EXTEST, SAMPLE, and BYPASS. The boundary scan test bus interface has four input signals: a test clock TBCK, test mode select TBMS, test data input TBDI, and test reset $\overline{TBRS}$. There is one output signal, test data output TBDO.

A lead designated as $\overline{HIGHZ}$ is provided for customer testing. An active low placed on this lead sets all output leads, except the boundary scan TBDO output lead, the receive terminal clock output RTCO, the transmit terminal H4 byte generation indication output TH4B7, the transmit terminal path overhead bytes indication TPOH, and the pseudo-ECL leads, to the high impedance state for board testing.

In addition to five loopback modes, the PHAST-3N provides a test generator and analyzer that uses the PRBS sequence 2^{23}-1, which is defined by the ITU-T O.151 recommendation.

Please note that the PHAST-3N has separate 3.3 volt power and ground leads for the (analog) clock recovery and clock synthesis blocks, in addition to the power and ground leads provided for the other blocks. It is recommended that separate planes and bypass networks be used for connecting the VDD and AVDD power leads on the PHAST-3N to +3.3 volts. Furthermore, each power supply lead should have a 0.1 microfarad capacitor to its corresponding ground.

LEAD DIAGRAM



Notes:

1. This is the bottom view. The leads are solder balls. See Figure 43 for package information. This view is rotated relative to the bottom view in Figure 43.
2. Some lead symbols are shown abbreviated. Lead symbols are described in the "Lead Descriptions" section.

Figure 2. PHAST-3N TXC-06103 Lead Diagram

LEAD DESCRIPTIONS

In the I/O/P column of the following tables, I = Input, O = Output, P = Power, T = Tristateable. Entries in the Type column are defined in the Input, Output and Input/Output Parameters section.

POWER SUPPLY, GROUND, AND NO CONNECT LEADS

Symbol	Lead No.	I/O/P	Name/Function
VDD	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	P	**VDD:** +3.3 volt power supply, ±5%
GND	A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, U17	P	**Ground:** Zero volts reference
AVDD	F2, F3, G3, L4, M1, P4	P	**Analog VDD:** +3.3 volt power supply, ±5%, for clock recovery and synthesis blocks.
AVSS	F1, J4, L3, N3, R1	P	**Analog Ground:** Zero volts reference for clock recovery and synthesis blocks.
NC	A4, A9, A16, A18, A20, B14, B15, B16, B19, C14, C15, C16, D10, D14, D16, E20, F18, F19, F20, G17, G18, G19, G20, H18, H19, J19, N18, N19, P17, P18, P19, P20, R2, R18, R19, R20, T18, T19, T20, U20, W12, Y1, Y12		**No Connect:** These leads are not to be connected, and must be left floating. Connection of an NC lead may impair performance or cause damage to the device. NC leads that are currently unused may be assigned functions in a future version of the device, affecting its usability in applications which have not left them floating.

TRANSMIT BIT-SERIAL LINE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TXSDT	N2	O	P-ECL	**Transmit Serial Data Output True (Pseudo-ECL):** This output, with its complement $\overline{\text{TXSDC}}$ signal, is used to output the 155.52 Mbit/s serial data. Data is clocked out on falling edges of TXSCT. This lead requires a 50 ohm termination, which is shown in Figure 29 on page 79.
$\overline{\text{TXSDC}}$	N1	O	P-ECL	**Transmit Serial Data Output Complement (Pseudo-ECL):** This output requires a 50 ohm termination, which is shown in Figure 29 on page 79.
TXSCT	L2	O	P-ECL	**Transmit Serial Clock Output True (Pseudo-ECL):** This output, with its complement $\overline{\text{TXSCC}}$ signal, is the 155.52 MHz transmit clock. This lead requires a 50 ohm termination, which is shown in Figure 29 on page 79.
$\overline{\text{TXSCC}}$	L1	O	P-ECL	**Transmit Serial Clock Output Complement (Pseudo-ECL):** This output requires a 50 ohm termination, which is shown in Figure 29 on page 79.

TRANSMIT CLOCK SYNTHESIS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
CSBYP	P3	I	LVTTL-5p	**Clock Synthesis Block Bypass:** A high on this lead bypasses the Clock Synthesis block. When the Clock Synthesis block is bypassed in the serial interface mode, an external 155.52 MHz clock reference must be connected to the TXCIT and $\overline{\text{TXCIC}}$ leads. The 155.52 MHz clock reference is used to derive the pseudo-ECL transmit output clocks TXSCT and $\overline{\text{TXSCC}}$, a 19.44 MHz reference clock (TSCKO), and a frame timing signal (TSFRO). A low on this lead enables the Clock Synthesis block. A 19.44 MHz clock must be applied to the CKREF lead. This clock signal is used to synthesize a 155.52 MHz clock, which in turn is used to derive the pseudo-ECL transmit output clocks TXSCT and $\overline{\text{TXSCC}}$, a 19.44 MHz reference clock (TSCKO) and a frame timing signal (TSFRO). This lead has an internal pull-up resistor.
TXCIT	M3	I	P-ECL	**Transmit Clock In True (Pseudo-ECL):** This input, with its complement lead $\overline{\text{TXCIC}}$, provides the 155.52 MHz clock reference input when the Clock Synthesis block is bypassed (CSBYP lead is high). When enabled, the clock reference is used to derive the pseudo-ECL transmit output clock and data, and the reference clock and frame timing signals. This lead requires a 50 ohm termination, which is shown in Figure 29 on page 79. If this lead is not used, it should It should be connected to VDD through a 180Ω resistor as shown in Figure 30 on page 80.
$\overline{\text{TXCIC}}$	M2	I	P-ECL	**Transmit Clock In Complement (Pseudo-ECL):** This input requires a 50 ohm termination, which is shown in Figure 29. If this lead is not used it should be connected to ground through a 180Ω resistor as shown in Figure 30 on page 80.
CKREF	W2	I	LVTTL-5d	**19.44 MHz Transmit Synthesis Reference Clock:** This input clock signal is used to provide a clock reference for the 155.52 MHz Clock Synthesis block. This clock should have a stability of +/- 20 ppm. This lead has an internal pull-down resistor.
SRTNV SREXT SRTNG	P2 P1 M4	I		**Clock Synthesis Block External Components:** These leads are used to connect an external filter to the internal clock synthesis circuit. When clock synthesis is enabled (CSBYP = 0), these pins must be connected as shown in Figure 33 on page 82. When clock synthesis is disabled (CSBYP =1) SRTNV and SRTNG must be left unconnected (floating); SREXT should be grounded.

TRANSMIT REFERENCE GENERATION TIMING

Symbol	Lead No.	I/O/P	Type	Name/Function
TSCKO	V4	O	LVCMOS 4 mA	**Transmit Serial Clock Reference Output:** This lead provides a 19.44 MHz clock which is derived from the pseudo-ECL TXCIT and $\overline{\text{TXCIC}}$ clock signals, or from the internal Clock Synthesis block when the serial interface is enabled. When the parallel interface is enabled and the clock synthesis block is bypassed, this signal is derived from the TXCIT and $\overline{\text{TXCIC}}$ clock signals. When the parallel interface and clock synthesis blocks are enabled this reference is not provided. This clock would normally be connected to the Transmit Reference Clock Input (TRCI) signal when the transmit retiming block is used in normal timing mode or the Source Timing Reference Clock Input (STRCI) signal when the transmit retiming block is bypassed in source timing mode. See Figure 28 on page 73.
TSFRO	W4	O	LVCMOS 4 mA	**Transmit Serial Frame Reference Output:** This lead provides an 8 kHz one clock cycle-wide frame pulse which is derived from the pseudo-ECL TXCIT and $\overline{\text{TXCIC}}$ clock signals, or from the internal Clock Synthesis block when the serial interface is enabled. When the parallel interface is enabled and the clock synthesis block is bypassed, this signal is derived from the TXCIT and $\overline{\text{TXCIC}}$ clock signals. When the parallel interface and clock synthesis blocks are enabled this reference is not provided. This frame pulse would normally be connected to the Transmit Reference Frame Input (TRFI) signal when the transmit retiming block is used in normal timing mode or the Source Timing Reference Frame Input (STRFI) signal when the transmit retiming block is bypassed in source timing mode. See Figure 28 on page 73.

RECEIVE BIT-SERIAL LINE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RXSDT	J2	I	P-ECL	**Receive Serial Data In True (Pseudo-ECL):** This input, with its complement $\overline{\text{RXSDC}}$ when enabled, is used to input 155.52 Mbit/s serial data into the PHAST-3N. Data is clocked in on rising edges of RXSCT. This lead requires a 50 ohm termination, which is shown in Figure 29 on page 79.
$\overline{\text{RXSDC}}$	J3	I	P-ECL	**Receive Serial Data In Complement (Pseudo-ECL):** This input requires a 50 ohm termination, which is shown in Figure 29 on page 79.

Symbol	Lead No.	I/O/P	Type	Name/Function
RXSCT	H1	I	P-ECL	**Receive Serial Clock In True (Pseudo-ECL):** This input is required when the Clock Recovery block is bypassed (CRBYP lead is high). With its complement $\overline{\text{RXSCC}}$, it is the 155.52 MHz receive input clock for the PHAST-3N. When the Clock Recovery block is enabled, these leads are disabled. This lead requires a 50 ohm termination, which is shown in Figure 29 on page 79. If this lead is not used it should be connected to VDD through a 180Ω resistor as shown in Figure 30 on page 80.
$\overline{\text{RXSCC}}$	H2	I	P-ECL	**Receive Serial Clock In Complement (Pseudo-ECL):** This input requires a 50 ohm termination, which is shown in Figure 29 on page 79 If this lead is not used it should be connected to ground through a 180Ω resistor as shown in Figure 30 on page 80.

CLOCK RECOVERY INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RRTNV REXT RRTNG	G1 G2 G4	I	Analog	**Clock Recovery Block External Components:** These leads are used to connect an external filter to the internal clock recovery circuit. When clock recovery is enabled (CRBYP = 0), these pins must be connected as shown in Figure 32 on page 81. When clock recovery is disabled (CRBYP = 1), RRTNV and RRTNG must be left unconnected (floating); RREXT should be grounded.
CRBYP	H3	I	LVTTL-5p	**Clock Recovery Block Bypass:** A high on this lead disables the Clock Recovery block. When the Clock Recovery block is bypassed, an external pseudo-ECL clock is required (RXSCT and $\overline{\text{RXSCC}}$). This clock signal is used to clock data in and is used to derive an internal 19.44 MHz clock. This lead has an internal pull-up resistor.
CRREF	A3	I	LVTTL-5d	**19.44 MHz Receive Clock Recovery Reference Clock:** This input clock signal is used to provide a clock reference for the 155.52 MHz Clock Recovery block. This lead may be connected to the clock synthesis reference clock lead (CKREF) for non-looped timing applications. This clock should have a stability of +/- 20 ppm. This lead has an internal pull-down resistor.

TRANSMIT BYTE-PARALLEL LINE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TLDO (7-0)	T2, U1, T3, U2, V1, T4, U3, V2	O	LVCMOS 4 mA	**Transmit Line Data Out:** Byte-wide data is clocked out on falling edges of the transmit line clock (TLCO). The data present on the TLDO7 lead (lead T2) is the first bit transmitted to the line for the byte interface. TLDO0 is the LSB and the last bit transmitted in the byte.
TLCO	W1	O	LVCMOS 4 mA	**Transmit Line Clock Out:** Byte-wide data (TLDO(7-0)) and a positive frame signal (TLFO) are clocked out of the PHAST-3N on falling edges of this 19.44 MHz clock. TLCO is derived from either the TRCI clock (normal or source timing modes with transmit retiming enabled), TTCI clock (normal timing mode with transmit retiming bypassed), or the STRCI clock (source timing mode with transmit retiming bypassed).
TLFO	R3	O	LVCMOS 4 mA	**Transmit Line Frame Out:** A positive, one (TLCO) clock cycle-wide pulse, that occurs during the third A2 byte time.
TLPR	V3	O	LVCMOS 4 mA	**Transmit Line Parity Out:** A selectable parity signal, even or odd. It is calculated over the data, or over the data and frame pulse.

RECEIVE BYTE-PARALLEL LINE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RLDI (7-0)	B1, C2, D2, D3, E4, C1, D1, E3	I	LVTTL-5	**Receive Line Data In:** Byte-wide data. The data present on RLDI7 (lead B1) is the MSB and the first bit received from the line in the SDH/SONET format. RLDI0 is the LSB and the last bit received in the byte. The byte need not be on byte boundaries when the frame pulse RLFI is disabled because internal circuitry will establish byte and frame boundaries.
RLCI	E1	I	LVTTL-5	**Receive Line Clock In:** Byte-wide data (RLDI(7-0)) and the frame signal (RLFI) are clocked into the PHAST-3N on rising edges of this clock. The clock rate is 19.44 MHz.
RLFI	E2	I	LVTTL-5d	**Receive Line Frame Pulse In:** An optional active high, one (RLCI) clock cycle-wide frame pulse marking the last A2 byte (A23), which establishes the start of the frame for the parallel interface. When the PHAST-3N is optioned to operate without the frame pulse, the internal OOF and LOF circuit searches for and synchronizes to the A1/A2 byte frame pattern. This lead has an internal pull-down resistor.
RLPR	C3	I	LVTTL-5	**Receive Line Parity:** A parity input signal. Parity, selectable as even or odd, is calculated over the data or over the data and frame signal internally, and compared to the value on this lead.

Symbol	Lead No.	I/O/P	Type	Name/Function
EXFAIL	D5	I	LVTTL-5d	**External Failure Indication:** Enabled when the parallel interface is selected. An active high input indicates an external failure condition (e.g., LOS, LOF) in the upstream circuitry. This signal is used by the PHAST-3N to inhibit TOH and POH processing, and may be used to generate path AIS and RDI when enabled. This input should not be used for an Out Of Frame (OOF) alarm. This lead has an internal pull-down resistor.
R19MHZ	C4	O	LVCMOS 4 mA	**Receive 19.44 MHz Synchronization Signal:** This 19.44MHz, 50% duty cycle clock output signal is derived from the 155.52 MHz input clock signal (RXSCT/$\overline{\text{RXSCC}}$) when the clock recovery block is disabled, from the clock recovery block when enabled, or from the 19.44 MHz clock input (RLCI) when the parallel interface is enabled. When clock recovery is disabled, this output will not be present if Receive Serial Data Input (RXSDT/$\overline{\text{RXSDC}}$) is not present.
R8KHZ	B3	O	LVCMOS 4 mA	**Receive 8 kHz Synchronization Signal:** This 8 kHz, 50% duty cycle clock output signal is derived from the 155.52 MHz input clock (RXSCT, $\overline{\text{RXSCC}}$) when the clock recovery block is disabled, from the clock recovery block when enabled, or from the 19.44 MHz clock input (RLCI) when the parallel interface is enabled. When clock recovery is disabled, this output will not be present if Receive Serial Data Input (RXSDT/$\overline{\text{RXSDC}}$) is not present.

TRANSMIT REFERENCE TIMING

Symbol	Lead No.	I/O/P	Type	Name/Function
TRFI	V5	I	LVTTL-5d	**Transmit Reference Line Frame Pulse In:** An optional active high one (TRCI) clock cycle-wide frame pulse that must occur every 125 microseconds. This frame pulse is used to establish the transmit line frame reference when the transmit pointer justification circuit is enabled. This lead has an internal pull-down resistor.
TRCI	Y4	I	LVTTL-5d	**Transmit Reference Line Clock In:** A 19.44 MHz input clock that must be present for transmit retiming when the transmit justification circuit is enabled. The active high frame pulse (TRFI) is clocked in on rising edges of this clock. This lead has an internal pull-down resistor.
STRFI	U5	I	LVTTL-5d	**Transmit Reference Source Timing Frame Pulse In:** An optional active high one (STRCI) clock cycle-wide frame pulse that must occur every 125 microseconds. This frame pulse is used to establish the transmit source frame and timing reference. This lead has an internal pull-down resistor.
STRCI	Y3	I	LVTTL-5d	**Transmit Reference Source Timing Clock In:** A 19.44 MHz input clock that is used to derive the timing signals needed for transmit source timing mode. The active high frame pulse (STRFI) is clocked in on rising edges of this clock. This lead has an internal pull-down resistor.

RECEIVE REFERENCE TIMING

Symbol	Lead No.	I/O/P	Type	Name/Function
RRFI	B4	I	LVTTL-5d	**Receive Reference Frame Pulse In:** An optional active high one (RRCI) clock cycle-wide frame pulse that must occur every 125 microseconds. This frame pulse is used to establish the receive terminal side frame starting location reference when the receive pointer justification circuit is enabled. This lead has an internal pull-down resistor.
RRCI	C5	I	LVTTL-5d	**Receive Reference Clock In:** A 19.44 MHz input clock that must be present when the justification circuit is enabled. The frame pulse (RRFI) is clocked in on rising edges of this clock. This lead has an internal pull-down resistor.

TERMINAL SIDE RECEIVE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RTDO (7-0)	E19, D20, E18, D19, C20, E17, D18, C19	O(T)	LVCMOS 8 mA	**Receive Terminal Data Out:** Byte-wide data output for the STM-1 AU-4 (STS-3c) and STS-3 (STM-1 AU-3) frames. Data is clocked out on falling edges of the clock (RTCO). The data present on the lead RTDO7 is the MSB and the first bit received from the line for the byte interface. RTDO0 is defined as the LSB and the last bit received in the byte. Data will be present for the A1 and A2 frame bytes, the pointer bytes H1 and H2, the VC-4 or STS-3 SPE (POH and payload bytes), and optionally the K1/K2 and E1/E2 bytes. During other byte times (i.e., inactive byte times), the data bus will be either tristated or forced to zero. The data bus may be forced to a high Z state by writing a 1 to control bit RBHZE (bit 2 in register 402H).
RTCO	A19	I/O	LVTTL-5p/ LVCMOS 4 mA	**Receive Terminal Clock Out:** In normal operation this signal is an output. It is a 19.44 MHz output clock which is derived from the receive reference clock (RRCI) when the pointer justification circuit is enabled. When the justification is bypassed, this clock is derived from the SDH/SONET serial or parallel line clock. This clock is also used to clock out the terminal receive signals on its falling edges. The bus signals may be clocked out on its rising edges by writing a 1 to control bit RTCIV. For TranSwitch testing, this signal becomes an input with an internal pull-up resistor.
RC1J1V1	B18	O	LVCMOS 8 mA	**Receive Terminal C1, J1 and Optional V1 Indications:** Composite active high timing signal that carries STM-1 AU-4 and STS-3 starting frame and SPE byte location information. This signal functions in conjunction with the RSPE signal. The C1 pulse identifies the location of the first C1 (J0) byte in the SONET/SDH frame when RSPE is low. A J1 pulse identifies the starting location of the J1 byte for the STM-1 VC-4 signal. For STS-3 operation, three J1 pulses identify the starting locations of the three J1 bytes for each of the three STS-1 signals when RSPE is high. One or more V1 pulses may be generated, depending upon the H4 multiframe generator/detector options selected.

Symbol	Lead No.	I/O/P	Type	Name/Function
RSPE	B17	O	LVCMOS 8 mA	**Receive Terminal SPE Indication:** An active high signal that occurs during each byte of the AU-4 VC-4/STS-3 SPE (POH bytes and payload) and for each STS-3 STS-1 SPE. This signal is low during Transport Overhead byte times.
RTPAR	B20	O(T)	LVCMOS 8 mA	**Receive Terminal Parity:** Odd or even parity is calculated over each clock cycle of RTCO for the data (RTDO(7-0)), SPE (RSPE) and C1, J1 and V1 (RC1J1V1) signals, or for the data bus (RTDO(7-0)) only. An option is provided which enables the RPOH signal to be included in the output parity bit calculation. The parity bit may be forced to a high Z state by writing a 1 to control bit RBHZE (bit 2 in register 402H).
$\overline{\text{RTBUSI}}$	C17	O	LVCMOS 8 mA	**Receive Terminal Bus Indicator:** This signal is high during unused TOH byte times, that is, TOH byte times other than A1, A2, H1, H2, and optionally E1, E2, K1, and K2, otherwise, $\overline{\text{RTBUSI}}$ is low. It may be used to control bus drivers. See also control bit RTUBZ (register 402H, bit1) and control bits RTK1BE, RTE1CH, and RTE1BE (register 445H, bits 6-4).
RTFAIL	A17	O	LVCMOS 8 mA	**Receive Terminal Failure Indication:** An active high indication signal that is generated when path AIS or line AIS is generated. For an STS-3 signal, the indication will be present for each of the STS-1s.
RPOH	C18	O	LVCMOS 8 mA	**Receive Terminal Path Overhead Bytes Indication:** This signal is high for the first column (POH column) in the STM-1 VC-4 format. For the STS-3 format, it high for the first column (POH column) and for the two stuff columns (30 and 59) in each STS-1. During other byte times this signal is low.

TERMINAL SIDE TRANSMIT INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TTDI (7-0)	N20, M17, M18, M19, M20, L19, L18, L20	I	LVTTL-5p	**Transmit Terminal Data In:** Byte-wide data input for the STM-1 AU-4 VC-4 (STS-3c SPE) and STS-3 STS-1 frames. The data present on the TTDI7 lead is the MSB and the first bit transmitted to the line for the byte interface. TTDI0 is the LSB and the last bit transmitted in the byte. This lead has an internal pull-up resistor.
TTCI	J20	I/O	LVTTL-5p/ LVCMOS 4 mA	**Transmit Terminal Clock:** In the normal timing mode, this 19.44 MHz input clock is used for clocking in the data byte (TTDI(7-0)), the C1J1V1 (TC1J1V1) signal, the SPE (TSPE) signal, and parity (TTPAR) signals. These signals are clocked in on rising edges of the clock. When control bit TTCIV is a 1, the input signals are clocked in falling edges of this clock. This lead has an internal pull-up resistor. For the source timing mode, this clock becomes an output. The TC1J1V1, TSPE, TPOH, TH4B7 and TH4B8 signals are clocked out on rising edges of this clock. The data (TTDI(7-0)) and parity (TTPAR) signals are clocked into the PHAST-3N on falling edges of this clock, when control bit TTCIV (bit 3 in register 022H) is a 1 and clocked in on the rising edges when TTCIV is 0.

Symbol	Lead No.	I/O/P	Type	Name/Function
TC1J1V1	K18	I/O	LVTTL-5/ LVCMOS 8 mA	**Transmit Terminal C1, J1 and Optional V1 Indications:** In the normal timing mode, this signal is an input. Composite active high input timing signal that carries STM-1 or STS-3 starting frame, J1 byte location information. This timing signal functions in conjunction with the TSPE signal. The C1 (J0) pulse identifies the location of the first C1 (J0) byte in the SONET/SDH frame when TSPE is low. A J1 pulse identifies the starting location of the J1 byte for the AU-4 VC-4 signal or three J1 pulses identify the starting location of the three J1 bytes for the STS-1 signals in the STS-3 signal when TSPE is high. One or more V1 pulses may be present for asynchronous VT/TU mappings to determine the starting location of the V1 byte. In the source timing mode, this signal becomes an output.
TSPE	K17	I/O	LVTTL-5p/ LVCMOS 4 mA	**Transmit Terminal SPE Indication:** For the normal timing mode, this signal is an input. The signal is high for each byte of the AU-4 VC-4/STS-3 SPE (POH bytes and payload) and high for each STS-3 STS-1 SPE. This signal is low during Transport Overhead byte times. This lead has an internal pull-up resistor. In the source timing mode, this signal is an output and it will be high for STM-1 VC-4 (STS-3c SPE) times (POH bytes and payload), and for the STS-3 STS-1 times.
TTPAR	K20	I	LVTTL-5d	**Transmit Terminal Parity:** An input for odd or even parity. Odd or even parity, as selected, will be calculated over each clock cycle of TTCI for the data (TTDI(7-0)), SPE (TSPE), and the C1, J1 and V1 (TC1J1V1) signals, or for the data signals only. The internal parity calculation is compared against this lead. This lead has an internal pull-down resistor.
TPOH	K19	I/O	LVTTL-5d/ LVCMOS 4 mA	**Transmit Terminal Path Overhead Bytes Indication:** For normal operation this signal is an output. For TranSwitch Testing this signal becomes an input with an internal pull-down resistor. This signal is provided for the source timing mode only. This signal is high during STM-1 VC-4 (STS-3c) POH byte times, and for each of the POH times and stuff bytes associated with each of the STS-3 STS-1 signals. During other times this signal is low.
TH4B7	J18	I/O	LVTTL-5d/ LVCMOS 8 mA	**Transmit Terminal H4 Byte Generator Indication:** For normal operation these signals are outputs. Enabled in the source timing mode only (pin MODE0 = 1). A two-bit H4 multiframe sequence is provided (equivalent to bits 7 and 8 in the H4 byte). The sequence will change states (in sequence 00, 01, 10, and 11) at the start of a new frame (A1 byte). For other timing modes, these output leads are forced to the zero state. The TH4B7 and TH4B8 outputs correspond to bits 7 and 8 in the H4 byte. For TranSwitch testing, TH4B7 becomes an input with an internal pull-down resistor.
TH4B8	J17	O	LVCMOS 8 mA	

RECEIVE SONET TRANSPORT OVERHEAD AND SDH SECTION OVERHEAD BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RTOHD	A5	O	LVCMOS 4 mA	**Receive TOH Interface Data Out.** This is a serial bit stream that carries the contents of all of the receive SONET Transport Overhead and SDH Section Overhead bytes (81 bytes). This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RTOHC	C6	O	LVCMOS 4 mA	**Receive TOH Interface Clock Out:** This clock is derived from the receive line side clock. Serial data (RTOHD), the byte indication (RTOHM), and the frame pulse (RTOHF) are clocked out on falling edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RTOHF	B5	O	LVCMOS 4 mA	**Receive TOH Interface Frame Pulse Out:** An active high, one (RTOHC) clock cycle-wide frame pulse, that identifies the first bit (the MSB) in the first A1 byte present at the RTOHD interface. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RTOHM	D7	O	LVCMOS 4 mA	**Receive TOH Byte Indication:** An active high indication for the selected bytes in the RTOHD signal. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

RECEIVE APS, E1 AND E2 BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RAPSD	B9	O	LVCMOS 4 mA	**Receive APS Interface Data Out:** This is a serial bit stream that carries the K1 and K2 APS bytes. The K1 and K2 bytes are clocked out by the receive APS clock RAPSC. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RAPSC	C9	O	LVCMOS 4 mA	**Receive APS Clock Out:** Serial APS data (RAPSD) and the frame pulse (RAPSF) are clocked out on falling edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RAPSF	D9	O	LVCMOS 4 mA	**Receive APS Frame Pulse Out:** A positive one (RAPSC) clock cycle-wide frame pulse that identifies the starting location of the first bit (bit 1) in the K1/K2 APS data stream. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RE1D	B8	O	LVCMOS 4 mA	**Receive E1 Interface Data Out:** This is a serial bit stream that carries the E1 byte. The E1 byte is clocked out by the receive order wire clock ROWC. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RE2D	A8	O	LVCMOS 4 mA	**Receive E2 Interface Data Out:** This is a serial bit stream that carries the E2 byte. The E2 byte is clocked out by the receive order wire clock ROWC. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
ROWF	C8	O	LVCMOS 4 mA	**Receive Order Wire Frame Pulse:** A one (ROWC) clock cycle-wide positive frame pulse that identifies the starting location of bit 8 or bit 1 (programmable) in the E1 and E2 byte data streams. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

Symbol	Lead No.	I/O/P	Type	Name/Function
ROWC	A7	O	LVCMOS 4 mA	**Receive Order Wire Clock Out:** The serial order wire bytes, E1 (RE1D) and E2 (RE2D), and frame pulse (ROWF) are clocked out on either falling or rising edges (programmable) of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

RECEIVE SECTION DATA BYTES (D1-D3) INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RSD	B7	O	LVCMOS 4 mA	**Receive Section Data Bytes (D1-D3) Interface Data Out:** This is a serial bit stream that carries the D1-D3 section data communication bytes. The D1-D3 bytes are clocked out by the receive section data bytes clock RSC. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RSC	A6	O	LVCMOS 4 mA	**Receive Section Data Bytes Clock Out:** Serial data communication bytes D1-D3 are clocked out on falling edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

RECEIVE LINE DATA BYTES (D4-D12) INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RLD	C7	O	LVCMOS 4 mA	**Receive Line Data Bytes (D4-D12) Interface Data Out:** This is a serial bit stream that carries the D4-D12 line data communication bytes. The D4-D12 bytes are clocked out by the receive line data bytes clock RLC. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
RLC	B6	O	LVCMOS 4 mA	**Receive Line Data Bytes Clock Out:** Serial data communication bytes D4-D12 are clocked out on falling edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

TRANSMIT SONET TRANSPORT OVERHEAD AND SDH SECTION OVERHEAD BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TTOHD	V6	I	LVTTL-5p	**Transmit TOH Interface Data In:** This is a serial bit stream that carries the programmable contents of the transmit SONET Transport Overhead and SDH Section Overhead bytes. The following TOH bytes, as shown in Tables 1 and 2, are not available via this interface: U (Xn) bytes, NU(n) bytes, Z1(n) bytes, Z2(n) bytes, MDB1-MDB6 bytes, and all unassigned bytes. These bytes are transmitted from RAM locations. This lead has an internal pull-up resistor.

Symbol	Lead No.	I/O/P	Type	Name/Function
TTOHC	Y5	O	LVCMOS 4 mA	**Transmit TOH Interface Clock Out:** This clock is derived from the transmit reference clock (TRCI). Serial data (TTOHD) is clocked in on rising edges of this clock, and the frame pulse (TTOHF) and the byte indication (TTOHM) are clocked out on falling edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
TTOHF	W5	O	LVCMOS 4 mA	**Transmit TOH Interface Frame Pulse Out:** An active high, one (TTOHC) clock cycle-wide frame pulse that identifies the first bit (the MSB) in the first A1 byte present at the TTOHD interface. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
TTOHM	U7	O	LVCMOS 4 mA	**Transmit TOH Byte Indication:** An active high indication for the selected bytes in the TTOHD signal. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

TRANSMIT APS, E1 AND E2 BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TAPSD	V7	I	LVTTL-5p	**Transmit APS Interface Data In:** This is a serial bit stream that carries the K1 and K2 bytes. The K1 and K2 bytes are clocked in by the transmit APS clock TAPSC. This lead has an internal pull-up resistor.
TAPSC	Y6	O	LVCMOS 4 mA	**Transmit APS Clock Out:** The serial APS data (TAPSD) is clocked in on rising edges of this clock. The serial APS frame pulse (TAPSF) is clocked out on the falling edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
TAPSF	W6	O	LVCMOS 4 mA	**Transmit APS Frame Pulse Out:** A positive one (TAPSC) clock cycle-wide frame pulse that identifies the location of the first bit (bit 1) in the K1/K2 byte. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
TE1D	U9	I	LVTTL-5p	**Transmit E1 Interface Data In:** This is a serial bit stream that carries the E1 byte. The E1 byte is clocked in by the transmit order wire clock TOWC. This lead has an internal pull-up resistor.
TE2D	Y8	I	LVTTL-5p	**Transmit E2 Interface Data In:** This is a serial bit stream that carries the E2 byte. The E2 byte is clocked in by the transmit order wire clock TOWC. This lead has an internal pull-up resistor.
TOWC	V9	O	LVCMOS 4 mA	**Transmit Order Wire Clock Out:** Serial E1 data (TE1D) and E2 data (TE2D) are clocked in on rising or falling edges of this clock. The frame pulse (TOWF) is clocked out on falling or rising edges of the clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.
TOWF	W9	O	LVCMOS 4 mA	**Transmit Order Wire Frame Pulse Out:** A one (TOWC) clock cycle-wide positive frame pulse that identifies the starting location of bit 1 or bit 8 (programmable) in the E1 and E2 order wire bytes. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

TRANSMIT SECTION DATA COMMUNICATION (D1-D3) BYTES INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TSD	Y7	I	LVTTL-5p	**Transmit Section Data Bytes (D1-D3) Interface Data In:** This is a serial bit stream that carries the D1-D3 section data communication bytes. The D1-D3 bytes are clocked in by the transmit section data bytes clock TSC. This serial interface, TTOHD, or RAM locations may be used to transmit the D1-D3 bytes. This lead has an internal pull-up resistor.
TSC	W7	O	LVCMOS 4 mA	**Transmit Section Data Bytes Clock Out:** Serial section data communication bytes D1-D3 are clocked in on rising edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

TRANSMIT LINE DATA COMMUNICATION BYTES (D4-D12) INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TLD	W8	I	LVTTL-5p	**Transmit Line Data Bytes (D4-D12) Interface Data In:** This is a serial bit stream that carries the serial D4-D12 line data communication bytes. The D4-D12 bytes are clocked in by the transmit line data bytes clock TLC. This lead has an internal pull-up resistor.
TLC	V8	O	LVCMOS 4 mA	**Transmit Line Data Bytes Clock Out:** Serial line data communication bytes D4-D12 are clocked in on rising edges of this clock. This lead is forced low when lead $\overline{\text{TOHENB}}$ is high.

RECEIVE PATH OVERHEAD (POH) BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RPCLK	B10	O	LVCMOS 4 mA	**Receive POH Interface Clock:** The receive POH address (RPADD), address latch enable (RPALE), data (RPDAT), and data latch enable (RPDLE) signals are clocked out on falling edges of this clock.
RPALE	A10	O	LVCMOS 4 mA	**Receive POH Interface Address Latch Enable:** A positive 12 (RPCLK) clock cycle-wide pulse that indicates a valid address present on RPADD.
RPADD	A11	O	LVCMOS 4 mA	**Receive POH Interface Address:** The states present on this lead during address latch enable time indicate the POH byte and the SDH/SONET format.
RPDLE	C10	O	LVCMOS 4 mA	**Receive POH Interface Data Latch Enable:** A positive 8 (RPCLK) clock cycle-wide pulse that indicates valid data present on RPDAT.
RPDAT	C11	O	LVCMOS 4 mA	**Receive POH Interface Data:** The states present on this lead during data latch enable time are the byte data selected by the address.

TRANSMIT PATH OVERHEAD (POH) BYTE INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TPCLK	Y11	O	LVCMOS 4 mA	**Transmit POH Interface Clock:** The transmit POH address (TPADD), address latch enable (TPALE) and the data latch enable (TPDLE) are clocked out on falling edges of this clock. Data (TPDAT) is clocked in on rising edges of this clock.
TPALE	W10	O	LVCMOS 4 mA	**Transmit POH Interface Address Latch Enable:** A positive 12 (TPCLK) clock cycle-wide pulse that indicates a valid address present on TPADD.
TPADD	V10	O	LVCMOS 4 mA	**Transmit POH Interface Address:** The states present on this lead during address latch enable time indicate the POH byte and the SONET/SDH format.
TPDLE	Y10	O	LVCMOS 4 mA	**Transmit POH Interface Data Latch Enable:** A positive 8 (TPCLK) clock cycle-wide pulse that indicates the valid data time for TPDAT.
TPDAT	Y9	I	LVTTL-5	**Transmit POH Interface Data:** The states present on this lead during data latch enable time are the byte data selected by the address.

RECEIVE ALARM INDICATION PORT (AIP) INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
RAIPD	B12	O	LVCMOS 4 mA	**Receive Alarm Indication Port Data Out:** This is a serial bit stream that provides the status of local receive alarms for the mate PHAST-3N in a line or path protected ring configuration. This signal is clocked out on falling edges of the receive AIP Interface clock (RAIPC). The data format is transmitted once per frame. In a ring configuration, this lead is connected to the TAIPD input lead of the mate PHAST-3N.
RAIPC	A12	O	LVCMOS 4 mA	**Receive Alarm Indication Port Clock Out:** In a line or path protected ring configuration, this lead will be connected to the transmit AIP clock input lead (TAIPC) of the mate PHAST-3N. Data (RAIPD) and the frame signal (RAIPF) are clocked out on falling edges of this clock.
RAIPF	B11	O	LVCMOS 4 mA	**Receive Alarm Indication Port Frame Pulse Out:** In a line or path protected ring configuration, this lead will be connected to the transmit AIP frame pulse input lead (TAIPF) of the mate PHAST-3N. An active high, one (RAIPC) clock cycle-wide, frame pulse that identifies the first bit position in the receive AIP serial data bit stream.

TRANSMIT ALARM INDICATION PORT (AIP) INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TAIPD	V11	I	LVTTL-5	**Transmit Alarm Indication Port Data In:** In a line or path protected ring configuration, this lead will be connected to the receive AIP data output lead (RAIPD) of the mate PHAST-3N.
TAIPC	U11	I	LVTTL-5	**Transmit Alarm Indication Port Clock In:** In a line or path protected ring configuration, this clock is connected to the receive AIP clock output lead (RAIPC) of the mate PHAST-3N. Data (TAIPD) and the frame signal (TAIPF) are clocked in rising edges of this clock.
TAIPF	W11	I	LVTTL-5	**Transmit Alarm Indication Port Frame In:** In a line or path protected ring configuration, this lead will be connected to the receive AIP frame pulse output lead (RAIPF) of the mate PHAST-3N. This signal is an active high, one (TAIPC) clock cycle-wide, frame pulse that identifies the first bit position in the serial AIP data bit stream.

CONTROLS

Symbol	Lead No.	I/O/P	Type	Name/Function
SERIAL	K1	I	LVTTL-5d	**Bit-Serial Interface Enable:** A high enables the pseudo-ECL receive bit-serial interface (RXSDT, $\overline{\text{RXSDC}}$, RXSCT and $\overline{\text{RXSCC}}$), and pseudo-ECL transmit bit-serial interface (TXCIT, $\overline{\text{TXCIC}}$, TXSDT, $\overline{\text{TXSDC}}$, TXSCT, and $\overline{\text{TXSCC}}$). A low enables the receive byte-parallel interface (RLDIn, RLFI and RLCI), and transmit byte-parallel interface (TLDOn, TLFO, and TLCO). When the Clock Recovery and Clock Synthesis blocks are enabled, the RXSCT, $\overline{\text{RXSCC}}$, TXCIT and $\overline{\text{TXCIC}}$ leads are disabled. This lead has an internal pull-down resistor.
EXCN1	Y2	O	LVCMOS 4 mA	**External Control Out 1:** An optional control signal generated by the microprocessor, (see TDRV1, bit 1 in register 010H) that can be used for controlling an external device.
EXCN2	W3	O	LVCMOS 4 mA	**External Control Out 2:** An optional control signal generated by the microprocessor, (see TDRV2, bit 2 in register 010H) that can be used for controlling an external device.
$\overline{\text{EXSN1}}$	A2	I	LVTTL-5p	**External Scan In 1:** An active low signal from external circuitry provided for a microprocessor read cycle (see SCAN1 alarm, bit 2 in registers 01C, 01DH) and an interrupt indication when enabled. The pulse width of this input must be greater than two ACECI clock periods.This lead has an internal pull-up resistor.
$\overline{\text{EXSN2}}$	B2	I	LVTTL-5p	**External Scan In 2:** An active low signal from external circuitry provided for a microprocessor read cycle (see SCAN2 alarm, bit 3 in registers 01C, 01DH) and an interrupt indication when enabled. The pulse width of this input must be greater than two ACECI clock periods.This lead has an internal pull-up resistor.

Symbol	Lead No.	I/O/P	Type	Name/Function
MODE2 MODE1 MODE0	A14 C13 B13	I	LVTTL-5p	**Mode Selection:** The following table shows how these leads can be used to select the operating modes of the PHAST-3N. These leads have internal pull-up resistors. MODE2 MODE1 MODE0 Operating Mode Low Low Low Normal Timing Low Low High Source Timing Please note: the other states are not used.
$\overline{\text{TOHENB}}$	K3	I	LVTTL-5p	**TOH Byte Processing Enable:** In normal operation this pin is low; a low enables SONET (TOH) and SDH (RSOH and MSOH) processing, while a high disables the processing of these bytes. A high also forces the TOH byte interface output signals to zero. This lead has an internal pull-up resistor.
$\overline{\text{FAIS1}}$	A13	I	LVTTL-5p	**Generate Receive Path AIS and Transmit an RDI Indication for STM-1 AU-4 (STS-3c) or STS-3 STS-1 No. 1:** An active low input for controlling the generation of path AIS and transmit RDI for STM-1 AU-4 (STS-3c) or STS-3 STS-1 No. 1, when enabled. This lead has an internal pull-up resistor.
$\overline{\text{FAIS2}}$	D12	I	LVTTL-5p	**Generate Receive Path AIS and Transmit an RDI Indication for STS-3 STS-1 No. 2:** An active low input for controlling the generation of path AIS and transmit RDI for STS-3 STS-1 No. 2, when enabled. This lead has an internal pull-up resistor.
$\overline{\text{FAIS3}}$	C12	I	LVTTL-5p	**Generate Receive Path AIS and Transmit an RDI Indication for STS-3 STS-1 No. 3:** An active low input for controlling the generation of path AIS and transmit RDI for STS-3 STS-1 No. 3, when enabled. This lead has an internal pull-up resistor.
$\overline{\text{J1SYNC}}$	A15	I	LVTTL-5p	**J1 Byte Optional Synchronization Pulse:** This input lead is used for test purposes. When an active low pulse having a minimum pulse width of one 19.44 MHz clock period is applied to this lead the three transmit J1 counter addresses are reset. The next J1 byte transmitted for a STM-1 (STS-3c) or for the three STS-3 STS-1s will start at the same time. This lead has an internal pull-up resistor.
$\overline{\text{VTACT}}$	H20	I	LVTTL-5p	**Transmit VT AIS Enable:** When control bit VTACT is a 1, an active low placed on this lead will generate an AIS signal for the VT selected instead of an unequipped signal. The active low must be present for the tributary byte times in order for this feature to function. The Add bus indication output provided by TranSwitch mapper devices may be used for this purpose. This lead has an internal pull-up resistor.

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{HIGHZ}}$	K2	I	LVTTL-5p	**High Impedance Select:** A low forces all output leads, except the PECL-type outputs, the boundary scan data output TBDO, the receive terminal clock output RTCO, the transmit terminal H4-byte generation indication output TH4B7, and the transmit terminal path overhead bytes indication TPOH to the high impedance state for testing purposes. The TPOH and TH4B7 outputs are pulled down and the RTCO output is pulled up. This lead has an internal pull-up resistor.
$\overline{\text{TEST}}$	J1	I	LVTTL-5p	**TranSwitch Test Select:** Used for TranSwitch testing. Although this lead has an internal pull-up resistor it should be tied to VDD through a pullup resistor to assure that it is not activated during normal operation.
$\overline{\text{RESET}}$	W20	I	LVTTL-5p	**Reset:** A low pulse on this lead for a minimum of 250 ns causes the device to halt all processing and puts it in a state in which the firmware MUST be downloaded as shown in the Firmware Download Procedure on page 132. Once the firmware download is complete the internal FIFOs will be reset to preset values, internal logic and counters are preset to defined values. All configurable control and mask registers are reset/preset to values defined in the Power-Up and Initialization section as shown on page 136. Performance Counters are all reset to zero. Counters will start in rollover mode since control bit CROV (bit 0 in register 00BH) defaults to zero after a hardware reset. This lead has an internal pull-up resistor.

MICROPROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
MOTO	W19	I	LVTTL-5	**Motorola/Intel Microprocessor Select:** A high selects the Motorola microprocessor compatible bus interface (Motorola Mode). A low selects the Intel microprocessor compatible bus interface (Intel Mode).
A(10-0)	V14, W15, Y16, U14, V15, W16, Y17, V16, W17, Y18, U16	I	LVTTL-5	**Address Bus:** These leads are active high address line inputs that are used by the microprocessor for accessing a memory map location for a read/write cycle. A10 is the most significant bit in the location's address.
D(7-0)	V12, U12, Y13, W13, V13, Y14, W14, Y15	I/O	LVTTL-5/ LVCMOS 8 mA	**Data Bus:** Bidirectional data lines used for transferring data between the PHAST-3N and the microprocessor. D7 is the most significant bit.
$\overline{\text{SEL}}$	V17	I	LVTTL-5p	**Select:** A low enables data transfers between the microprocessor and the PHAST-3N memory map during a read/write cycle. This lead has an internal pull-up resistor.

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{RD}$ or RD/$\overline{WR}$	Y20	I	LVTTL-5	**Read (Intel mode) or Read/Write (Motorola mode):** Intel Mode - An active low signal generated by the microprocessor for reading the PHAST-3N memory map locations. Motorola Mode - An active high signal generated by the microprocessor for reading the PHAST-3N memory map locations. An active low signal is used to write to the memory map locations.
$\overline{WR}$ or $\overline{LDS}$	V18	I	LVTTL-5	**Write (Intel mode) or LDS (Motorola mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the PHAST-3N memory map locations. Motorola Mode - An active low Data Strobe (DS) signal for 68xxx (e.g., 68302) operation. For 68xxx microprocessors, if the $\overline{LDS}$ signal is not present this input should be connected to $\overline{SEL}$.
RDY or $\overline{DTACK}$	W18	O	LVCMOS 8 mA	**Ready (Intel mode) or Data Transfer Acknowledge (Motorola mode):** Intel Mode - A high is an acknowledgment from the addressed memory location that the transfer can be completed. A low indicates that the PHAST-3N cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low indicates the information on the data bus is valid. During a write bus cycle, a low acknowledges the acceptance of data.
INT or $\overline{IRQ}$	Y19	O	LVCMOS 4 mA	**Interrupt (Intel mode) or Interrupt Request (Motorola mode):** This lead is enabled when control bit HINT (bit 0 in register 010H) is equal to 1. Intel Mode - A high on this output lead signals an interrupt request to the microprocessor. Motorola Mode - A low on this output lead signals an interrupt request to the microprocessor.

INTERNAL PROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
ACECI	T1	I	LVTTL-5	**Internal Processor Clock Input:** An asynchronous clock input used for the internal ACE processors and also for internal memory map arbitration. This clock must be present in order for the PHAST-3N to function. This clock should have a frequency of 48 MHz ±2% with a (50±10)% duty cycle.

TEST PORT FOR BOUNDARY SCAN (IEEE STANDARD 1149.1)

Symbol	Lead No.	I/O/P	Type	Name/Function
TBCK	U18	I	LVTTL-5	**Test Boundary Scan Clock:** This signal is used to shift data into TBDI on its rising edge and out of TBDO on its falling edge. The maximum clock frequency is 10 MHz.
TBDI	U19	I	LVTTL-5p	**Test Boundary Scan Data Input:** Serial test instructions and data are clocked into this lead on the rising edge of TBCK. This lead has an internal pull-up resistor.

Symbol	Lead No.	I/O/P	Type	Name/Function
TBDO	V19	O	LVCMOS 4 mA	**Test Boundary Scan Data Output:** Serial data test instructions and data are clocked out of this lead on the falling edge of TBCK. When inactive, this lead goes to a high impedance state.
TBMS	V20	I	LVTTL-5p	**Test Boundary Scan Mode Select:** This input lead is sampled on the rising edge of TBCK. It is used to place the Test Access Port controller into various states, as defined in IEEE 1149.1. An internal pull-up holds this lead high during normal operation. This lead has an internal pull-up resistor.
$\overline{\text{TBRS}}$	T17	I	LVTTL-5p	**Test Boundary Scan Reset:** An active low signal that asynchronously resets the Test Access Port controller. The reset must be present for a minimum of 250 ns. This lead has an internal pull-up resistor.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	5.5	V	Notes 1, 3
Storage temperature range	T_S	-40	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification, HBM (Human Body Model)	ESD	Absolute value 2000		V	Note 4
Latch up	LU				Meets JEDEC Standard 78

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. All input signal leads accept 5 volt signals.
4. Absolute value tested per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			25.0	$^oC/W$	0 ft/min linear airflow.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}		430	492	mA	STS3 Mode, ACECI = 48 MHz, Clock recovery and clock synthesis both enabled; Maximum power is at minimum operating temperature.
Power Dissipation, P_{DD}		1419	1700	mW	

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR P-ECL (DIFFERENTIAL INPUT, PSEUDO-ECL)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.17		4.0	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}	1.45	1.7	1.82	V	$3.15 \le V_{DD} \le 3.45$
$V_{diff} = V_{IH} - V_{IL}$	0.35		1.1	V	$3.15 \le V_{DD} \le 3.45$
Vcm (common mode)	1.6		2.9	V	$3.15 \le V_{DD} \le 3.45$
Input Leakage Current	-10			µA	$V_{in} = V_{SS}$; $V_{DD} = 3.45$
Input Leakage Current			10	µA	$V_{in} = V_{DD}$; $V_{DD} = 3.45$.

INPUT PARAMETERS FOR LVTTL-5 (LOW VOLTAGE TTL, 5 VOLT TOLERANT)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.5	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	-10		10	µA	$V_{DD} = 3.45$, $V_{SS} \le V_{IN} \le 5.5$
Input capacitance		5		pF	

INPUT PARAMETERS FOR LVTTL-5p (LOW VOLTAGE TTL, 5 VOLT TOLERANT, PULL-UP RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.5	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	-100		0	µA	$V_{DD} = 3.45$; $V_{IN} = V_{SS}$
Input capacitance		5		pF	

INPUT PARAMETERS FOR LVTTL-5d (LOW VOLTAGE TTL, 5 VOLT TOLERANT, PULL-DOWN RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.5	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	0		100	µA	$V_{DD} = 3.45$; $V_{IN} = 5.5$
Input capacitance		5		pF	

OUTPUT PARAMETERS FOR P-ECL (DIFFERENTIAL OUTPUT, PSEUDO-ECL, 50 OHMS)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.25	2.40	4.0	V	R_T = 50 ohms, VT = 1.7 V
V_{OL}	1.45	1.70	1.82	V	R_T = 50 ohms, VT = 1.7 V
I_{OZL} (output leakage current)	-10			µA	V_{DD} = 3.45, V_{IN} = V_{SS}
I_{OZH} (output leakage current)			10	µA	V_{DD} = 3.45, V_{IN} = V_{DD} Not 5V tolerant
I_{OH} (pull-up outgoing current)			-13	mA	R_T = 50 ohms, VT = 1.7 V
V_T		1.70		V	Termination voltage

OUTPUT PARAMETERS FOR LVCMOS 4mA (LOW VOLTAGE CMOS, 4mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}			4.0	mA	V_{OL} = 0.4
I_{OH}			-4.0	mA	V_{OH} = 2.4
I_{OZ}			±10	µA	V_{DD}=3.45, $V_{SS} \le V_{IN} \le 5.5$

OUTPUT PARAMETERS FOR LVCMOS 8mA (LOW VOLTAGE CMOS, 8mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	V_{OL} = 0.4
I_{OH}			-8.0	mA	V_{OH} = 2.4
I_{OZ}			±10	µA	V_{DD}=3.45, $V_{SS} \le V_{IN} \le 5.5$

INPUT/OUTPUT PARAMETERS FOR LVTTL INPUT AND LVCMOS OUTPUT 8mA (LOW VOLTAGE TTL/CMOS, 5 VOLT TOLERANT 8mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input Capacitance		9.0		pF	
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	V_{OL} = 0.8
I_{OH}			-8.0	mA	V_{OH} = 2.0
I_{OZ}			±10	µA	V_{DD}=3.45, $V_{SS} \le V_{IN} \le 5.5$

INPUT/OUTPUT PARAMETERS FOR LVTTL-5d INPUT AND LVCMOS OUTPUT 8mA (LOW VOLTAGE TTL/CMOS, 5 VOLT TOLERANT, 8mA WITH PULL-DOWN RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input Capacitance		9.0		pF	
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	V_{OL} = 0.8
I_{OH}			-8.0	mA	V_{OH} = 2.0
I_{OZ}	0		100	µA	V_{DD}=3.45, V_{IN} = 5.5

INPUT/OUTPUT PARAMETERS FOR LVTTL-5d INPUT LVCMOS OUTPUT 4mA (LOW VOLTAGE TTL/CMOS, 5 VOLT TOLERANT, 4ma WITH PULL-DOWN RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input Capacitance		9.0		pF	
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}			4.0	mA	V_{OL} = 0.8
I_{OH}			-4.0	mA	V_{OH} = 2.0
I_{OZ}	0		100	µA	V_{DD}=3.45, V_{IN} = 5.5

INPUT/OUTPUT PARAMETERS FOR LVTTL-5p INPUT, LVCMOS OUTPUT 4mA (LOW VOLTAGE TTL/CMOS, 5 VOLT TOLERANT, 4ma WITH PULL-UP RESISTOR)

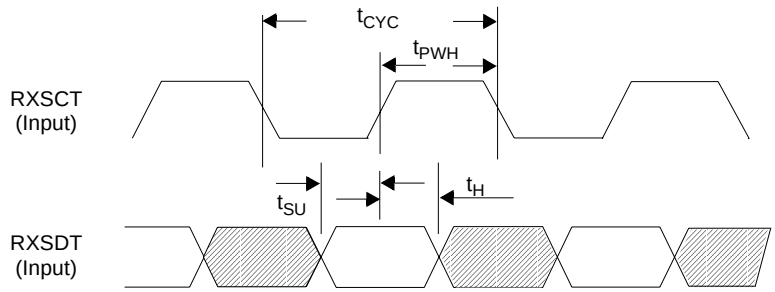
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input Capacitance		9.0		pF	
V_{OH}	2.4		V_{DD}	V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}	0		0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}			4.0	mA	V_{OL} = 0.8
I_{OH}			-4.0	mA	V_{OH} = 2.0
I_{OZ}	-100		0	µA	V_{DD}=3.45, V_{IN}=V_{SS}

TIMING CHARACTERISTICS

Detailed timing diagrams for the PHAST-3N device are illustrated in Figures 3 through 27 with values of the timing parameters tabulated below each waveform diagram. All outputs are measured with a maximum load capacitance of 25 pF unless otherwise stated. Timing parameters are measured at the voltage levels of $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$ for output and input signals, respectively.

RECEIVE SIDE TIMING

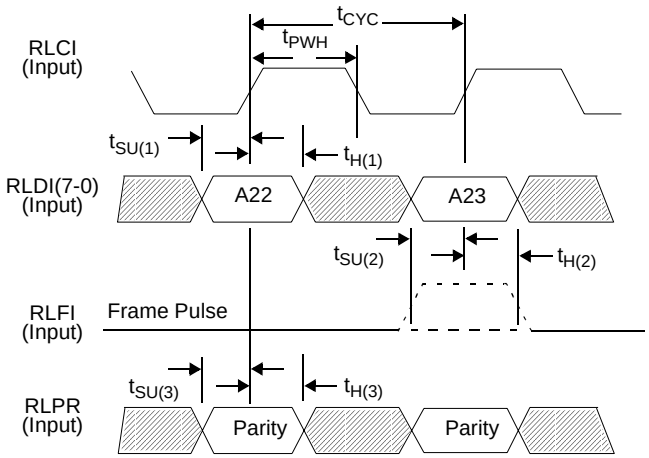
Figure 3. Receive Serial Interface Timing



Note: The waveforms are shown for the true pseudo-ECL signal inputs only. There are also complement clock ($\overline{RXSCC}$) and data ($\overline{RXSDC}$) pseudo-ECL signals. RXSCT is shown for the clock recovery circuit bypass situation (CRBYP lead set high). When the clock recovery circuit is enabled (CRBYP is set low), the RXSCT and $\overline{RXSCC}$ signals are ignored if they are present.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYC}	RXSCT clock period		6.43		ns
	RXSCT duty cycle t_{PWH}/t_{CYC}	45		55	%
t_{SU}	RXSDT data setup time to RXSCT ↑	2.0			ns
t_H	RXSDT data hold time after RXSCT ↑	1.0			ns

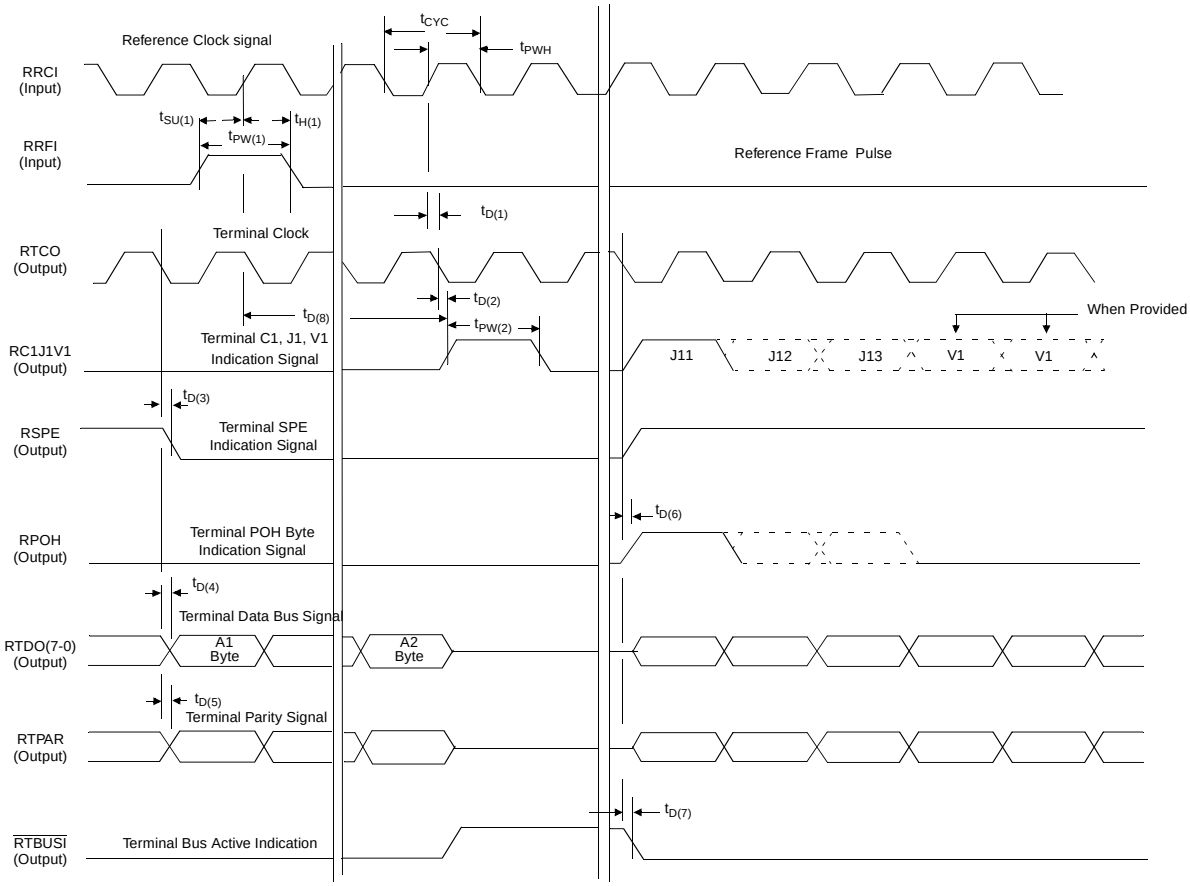
Figure 4. Receive Parallel Interface Timing



Note: The use of the frame pulse is optional and is enabled when control bit RFRME (bit 7 in register 400H) is a 1. Parity may be calculated for the data, or the data and the frame pulse, and it may be even or odd, depending upon control bits RLPDO and RLPRE (register 403H, bits 6 and 7), and control bit RFRME.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYC}	RLCI clock period		51.44		ns
	RLCI duty cycle, t_{PWH}/t_{CYC}	45		55	%
$t_{SU(1)}$	RLDI(7-0) setup time to RLCI ↑	8.0			ns
$t_{H(1)}$	RLDI(7-0) hold time after RLCI ↑	1.0			ns
$t_{SU(2)}$	RLFI setup time to RLCI ↑	8.0			ns
$t_{H(2)}$	RLFI hold time after RLCI ↑	1.0			ns
$t_{SU(3)}$	RLPR setup time to RLCI ↑	8.0			ns
$t_{H(3)}$	RLPR hold time after RLCI ↑	1.0			ns

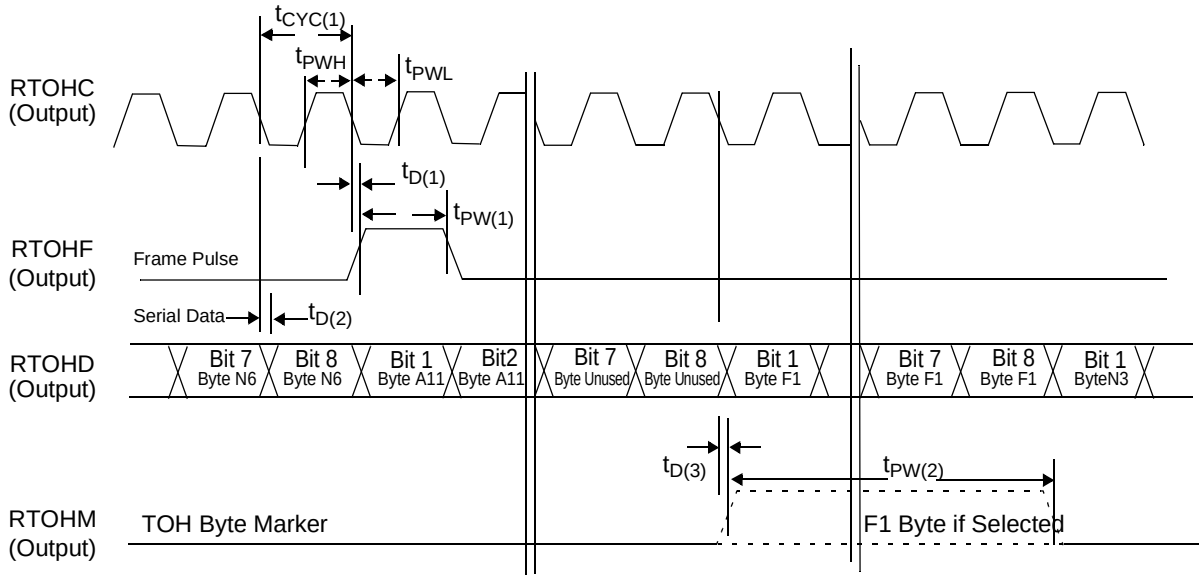
Figure 5. Receive Terminal Interface Timing



Note: The waveforms shown correspond to control bit RTCIV (bit 3 in register 402H) set to 0. RTCIV controls the polarity of the output clock. When this control bit is set to 1, the terminal signals will be clocked out on rising edges of the clock. The delay from the RRCI ↑ which samples RRFI to RC1J1V1 (C1 pulse) ↑ is one RRCI clock period added to $t_{D(1)}$ and $t_{D(2)}$. This is shown as $t_{D(8)}$ in the table below. When control bit RBHZE (bit 2 in register 402H) is set to 1, data RTDO (7-0) and the parity signal RTPAR are forced to a high impedance state. Not shown is the RTFAIL signal, which will be active high for line AIS and path AIS times. The first bit (MSB) in a byte is RTDO7. Unused TOH bytes are forced to a tristate level when control bit RTUBZ is set to 1 (bit 1 in register 402H), and to 0 when control bit RTUBZ is set to 0. Note that for STM-1 operation, the optional V1 pulse occurs three RTCO clock periods after the J1 pulse although the earliest a V1 byte can occur is six clocks after the V1 pulse.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYC}	RRCI clock period		51.44		ns
	RRCI duty cycle, t_{PWH}/t_{CYC}	45		55	%
$t_{SU(1)}$	RRFI setup time to RRCI ↑	3.0			ns
$t_{H(1)}$	RRFI hold time after RRCI ↑	3.0			ns
$t_{D(1)}$	RTCO ↓ delay from RRCI ↑	4.5		17.0	ns
$t_{D(2)}$	RC1J1V1↑ delay from RTCO ↓	1.0		8.0	ns
$t_{D(3)}$	RSPE ↓ delay from RTCO ↓	1.0		8.0	ns
$t_{D(4)}$	RTDO(7-0) delay from RTCO ↓	0.0		8.0	ns
$t_{D(5)}$	RTPAR ↓ delay from RTCO ↓	0.0		8.0	ns
$t_{D(6)}$	RPOH ↑ delay from RTCO ↓	0.0		6.0	ns
$t_{D(7)}$	$\overline{RTBUSI}$ ↓ delay from RTCO ↓	0.0		7.0	ns
$t_{D(8)}$	RC1J1V1 ↑ delay from RRCI ↑clocking in RRFI	56.9		76.4	ns
$t_{PW(1)}$	RRFI pulse width	40		51.4	ns
$t_{PW(2)}$	RC1J1V1 pulse width	51.4		308.4	ns

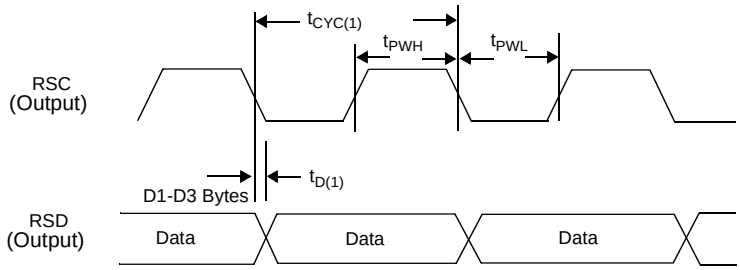
Figure 6. Receive TOH Interface Timing



Note: The RTOHM signal indicates the location of a programmable TOH byte using control bits TOHS2, TOHS1, and TOHS0. The following TOH byte locations are programmable: J0, D1-D3, D4-D12, E1, E2, K1/K2, F1, and no selection. The control bits are also shared for the transmit side.

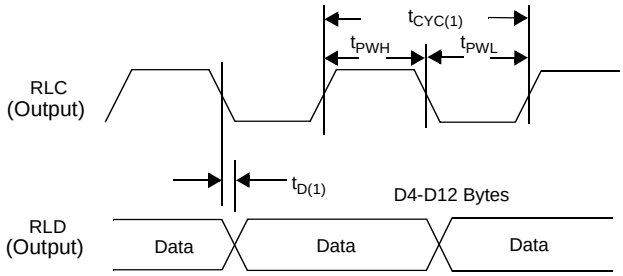
Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	RTOHC clock period	154.3		205.8	ns
t_{PWH}	RTOHC high time	51.4		102.9	ns
t_{PWL}	RTOHC low time		102.9		ns
$t_{D(1)}$	RTOHF delay from RTOHC ↓	-1.0		3.0	ns
$t_{D(2)}$	RTOHD delay from RTOHC ↓	0.0		3.0	ns
$t_{D(3)}$	RTOHM delay from RTOHC ↓	-1.0		3.0	ns
$t_{PW(1)}$	RTOHF pulse width		205.8		ns
$t_{PW(2)}$	RTOHM pulse width		1543		ns

Figure 7. Receive Section Data Communication Interface Timing (D1-D3 Bytes)



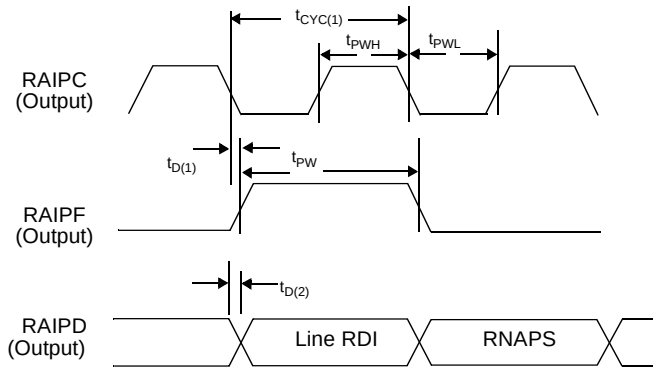
Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	RSC clock period	5.0		5.2	µs
t_{PWH}	RSC high time	2.5		2.6	µs
t_{PWL}	RSC low time	2.5		2.6	µs
$t_{D(1)}$	RSD delay from RSC ↓	-1.0		2.0	ns

Figure 8. Receive Line Data Communication Interface Timing (D4-D12 Bytes)



Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	RLC clock period	1.7		1.8	µs
t_{PWH}	RLC high time	823.0		874.5	ns
t_{PWL}	RLC low time	823.0		874.5	ns
$t_{D(1)}$	RLD delay from RLC ↓	-1.0		2.0	ns

Figure 9. Receive Alarm Indication Port (AIP) Interface Timing

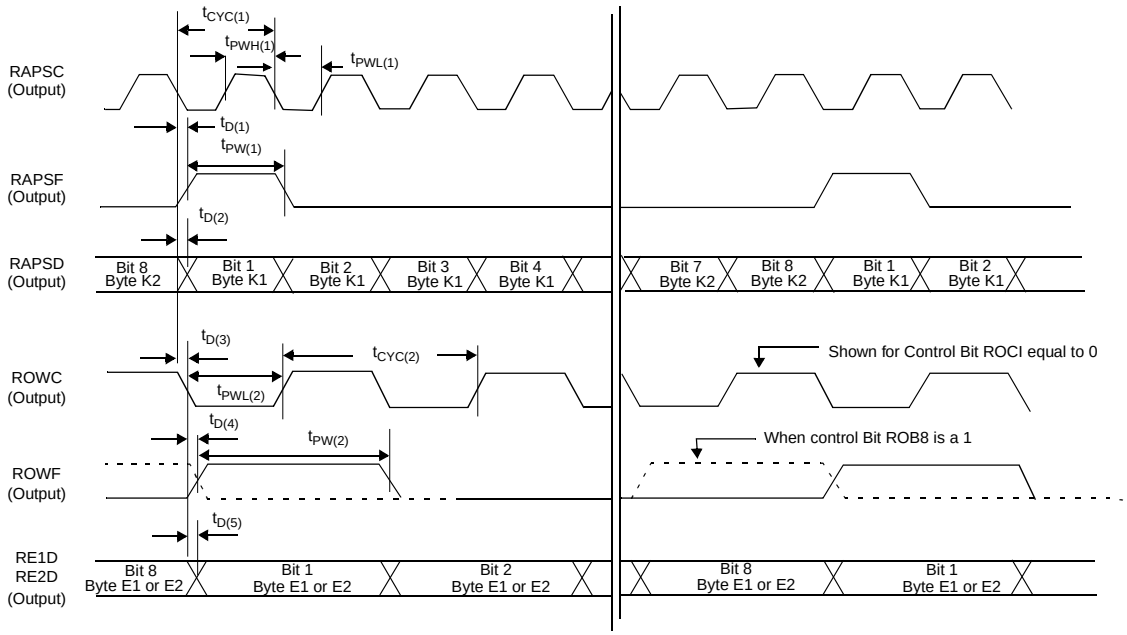


Note: The serial data format consists of 81 bits. The first bit in a frame is designated to carry the line AIS status alarm. The last four bits of the frame (bits 78, 79, 80 and 81) are designated to carry a CRC-4.

.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	RAIPC clock period		1.5		µs
t_{PWH}	RAIPC high time		771.6		ns
t_{PWL}	RAIPC low time		771.6		ns
$t_{D(1)}$	RAIPF ↑ delay from RAIPC ↓	-2.0		2.0	ns
$t_{D(2)}$	RAIPD delay from RAIPC ↓	-1.0		2.0	ns

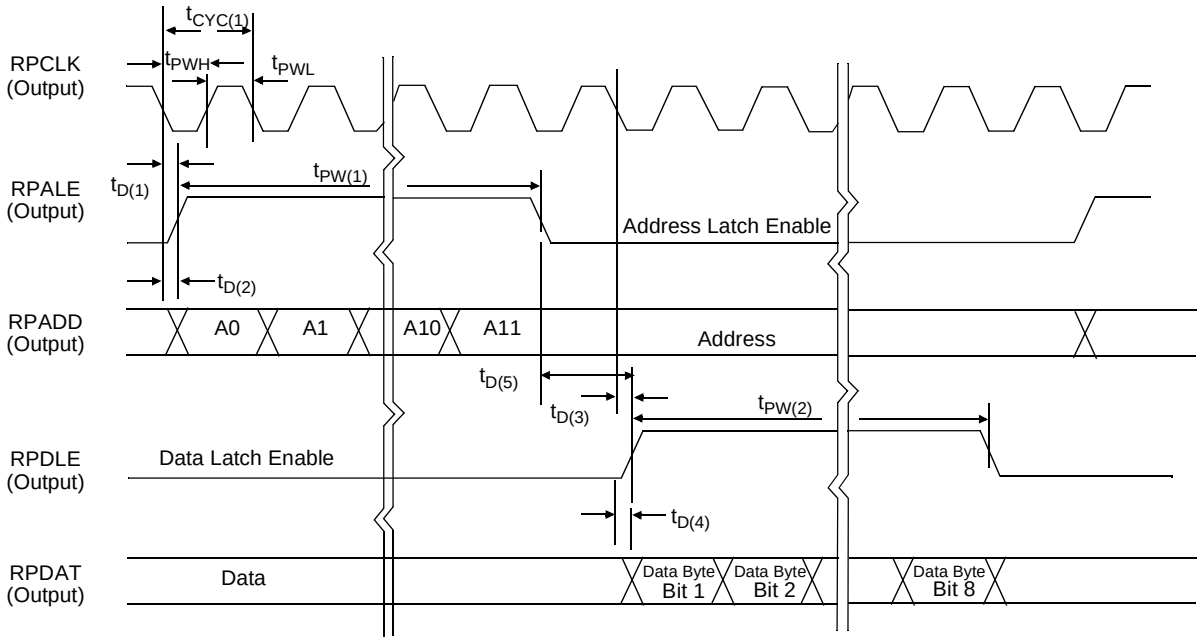
Figure 10. Receive APS, E1 and E2 Interface Timing



Note: The waveforms shown correspond to control bit ROB8 equal to 0 (bit 2 in register 400H). When control bit ROB8 is a 1, the frame pulse will be shifted to bit 8 for RE1D and RE2D. The waveforms also correspond to control bit ROCI equal to 0 (bit 3 in register 400H). When control bit ROCI is a 1, RE1D, RE2D and ROWF will clocked out on rising edges of ROWC.

Parameter	Description	Min	Typ	Max	Unit
$t_{CYC(1)}$	RAPSC clock period	7.8			µs
$t_{PWH(1)}$	RAPSC high time	4.1			µs
$t_{PWL(1)}$	RAPSC low time		3.7		µs
$t_{D(1)}$	RAPSF ↑ delay after RAPSC ↓	-1.0		3.0	ns
$t_{pw(1)}$	RAPSF pulse width		7.8		µs
$t_{D(3)}$	ROWC ↓ delay after RAPSC ↓	0.0		2.0	ns
$t_{CYC(2)}$	ROWC clock period	15.5		15.6	µs
$t_{PWL(2)}$	ROWC low time	7.7		7.8	µs
$t_{D(4)}$	ROWF delay after ROWC ↓	-2.0		3.0	ns
$t_{PW(2)}$	ROWF pulse width	15.5		15.6	µs
$t_{D(5)}$	RE1D, RE2D delay after ROWC ↓	-1.0		3.0	ns

Figure 11. Receive POH Interface Timing



The address field has the following format:

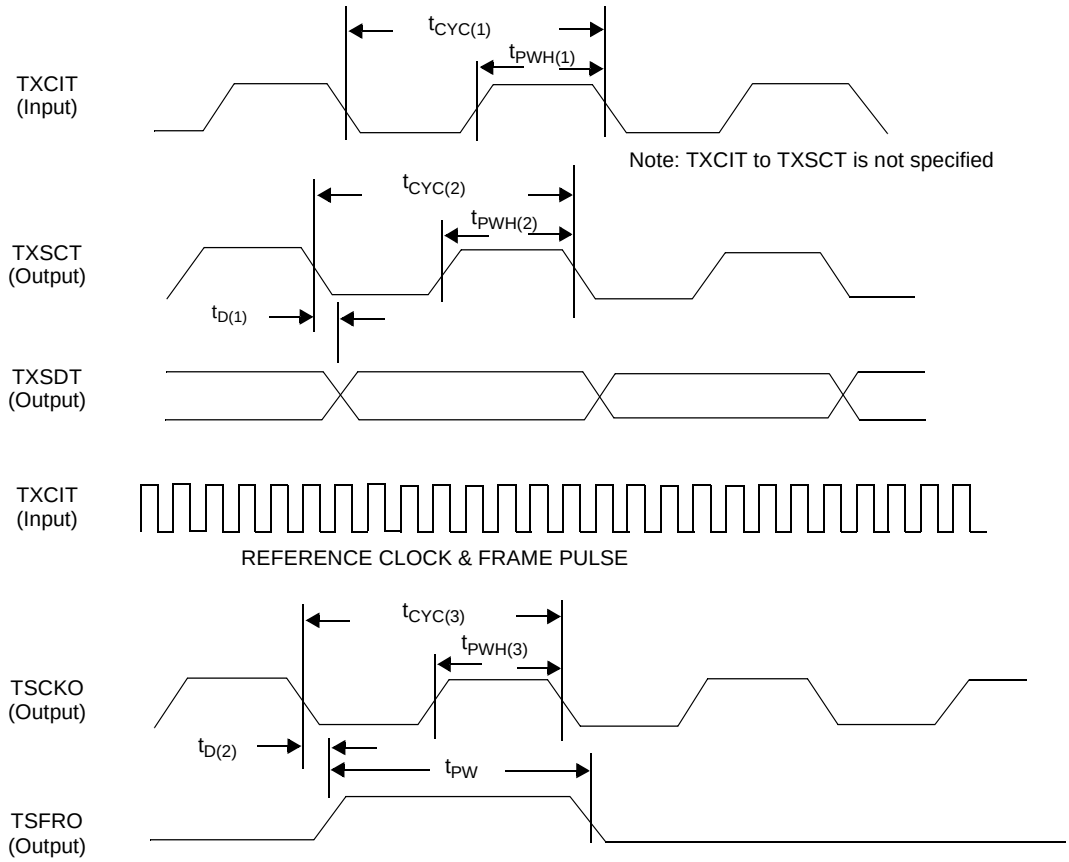
A0 - A5	A6	A7	A8	A9	A10	A11	Format and POH Byte
Not Used Equal to 0s	0	0	X	X	X	X	STS-1 No. 1
	0	1	X	X	X	X	STS-1 No. 2
	1	0	X	X	X	X	STS-1 No. 3
	1	1	X	X	X	X	STM-1/VC-4
	X	X	0	0	0	0	J1 Byte
	X	X	0	0	0	1	B3 Byte
	X	X	0	0	1	0	C2 Byte
	X	X	0	0	1	1	G1 Byte
	X	X	0	1	0	0	F2 Byte
	X	X	0	1	0	1	H4 Byte
	X	X	0	1	1	0	F3 Byte
	X	X	0	1	1	1	K3 Byte
	X	X	1	0	0	0	N1 (Z5) Byte

(continued on next page)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	RPCLK clock period		154.3		ns
t_{PWL}	RPCLK low time		102.9		ns
t_{PWH}	RPCLK high time		51.4		ns
$t_{D(1)}$	RPALE ↑ delay from RPCLK ↓	-1.0		3.0	ns
$t_{PW(1)}$	RPALE pulse width		1.9		µs
$t_{D(2)}$	RPADD delay from RPCLK ↓	-1.0		3.0	ns
$t_{D(3)}$	RPDLE ↑ delay from RPCLK ↓	-1.0		3.0	ns
$t_{PW(2)}$	RPDLE pulse width		1.2		µs
$t_{D(4)}$	RPDAT delay from RPCLK ↓	-1.0		3.0	ns
$t_{D(5)}$	RPDLE ↑ delay from RPALE ↓	150.0	154.3	160.0	ns

TRANSMIT SIDE TIMING

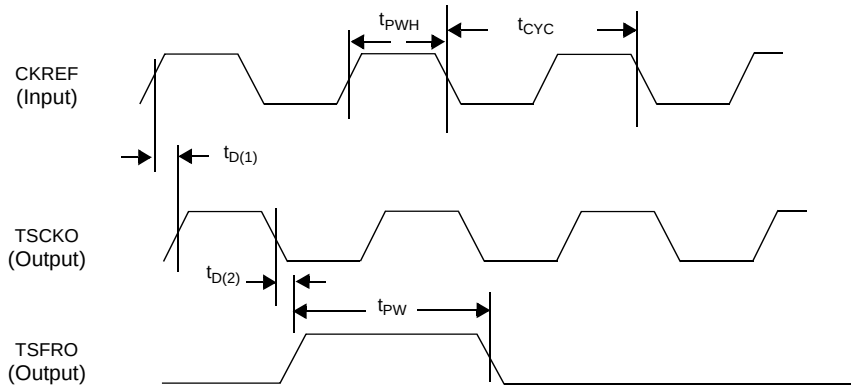
Figure 12. Transmit Serial Interface Timing



When the Clock Synthesis block is disabled (CSBYP lead is high), the pseudo-ECL clock signals TXCIT and $\overline{\text{TXCIC}}$ are required to derive the pseudo-ECL transmit clock signals TXSCT and $\overline{\text{TXSCC}}$.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TXCIT clock period		6.43		ns
	TXCIT duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	45		55	%
$t_{CYC(2)}$	TXSCT clock period		6.43		ns
	TXSCT duty cycle $t_{PWH(2)}/t_{CYC(2)}$	45		55	%
$t_{D(1)}$	TXSDT output delay from TXSCT ↓	0.0		2.0	ns
$t_{CYC(3)}$	TXSCKO clock period		51.44		ns
	TXSCKO duty cycle $t_{PWH(3)}/t_{CYC(3)}$	45		55	%
t_{PW}	TSFRO pulse width		51.44		ns
$t_{D(2)}$	TSFRO ↑ output delay from TSCKO ↓	-1.0		3.0	ns

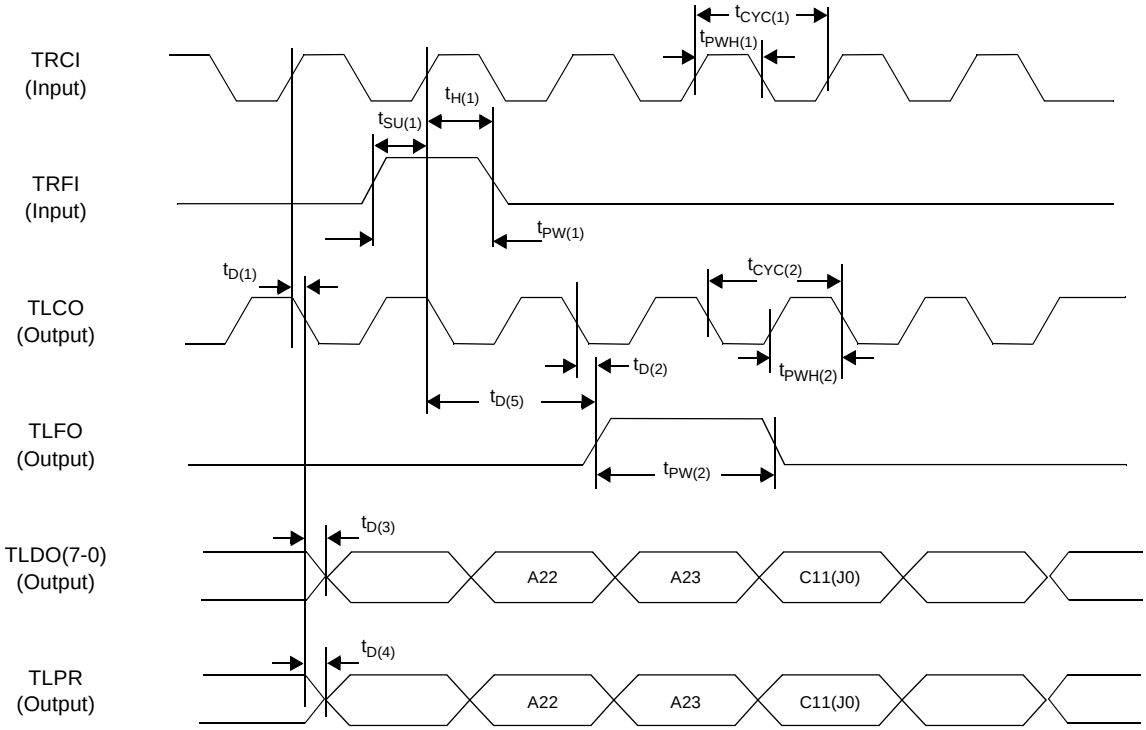
Figure 13. Clock Synthesis Timing



Note: When the Clock Synthesis block is enabled (CSBYP lead is low), the pseudo-ECL clock signals TXCIT and $\overline{\text{TXCIC}}$ are not required. Instead, a 19.44 MHz clock reference input signal (CKREF) is used to derive the pseudo-ECL transmit clock signals TXSCT and $\overline{\text{TXSCC}}$.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYC}	CKREF clock period		51.44		ns
	CKREF duty cycle t_{PWH}/t_{CYC}	45		55	%
$t_{D(1)}$	TSCKO ↑ output delay from CKREF ↑	0.0		2.0	ns
$t_{D(2)}$	TSFRO ↑ output delay from CKREF ↓	-1.0		3.0	ns
t_{PW}	TSFRO pulse width	40	51.44		ns

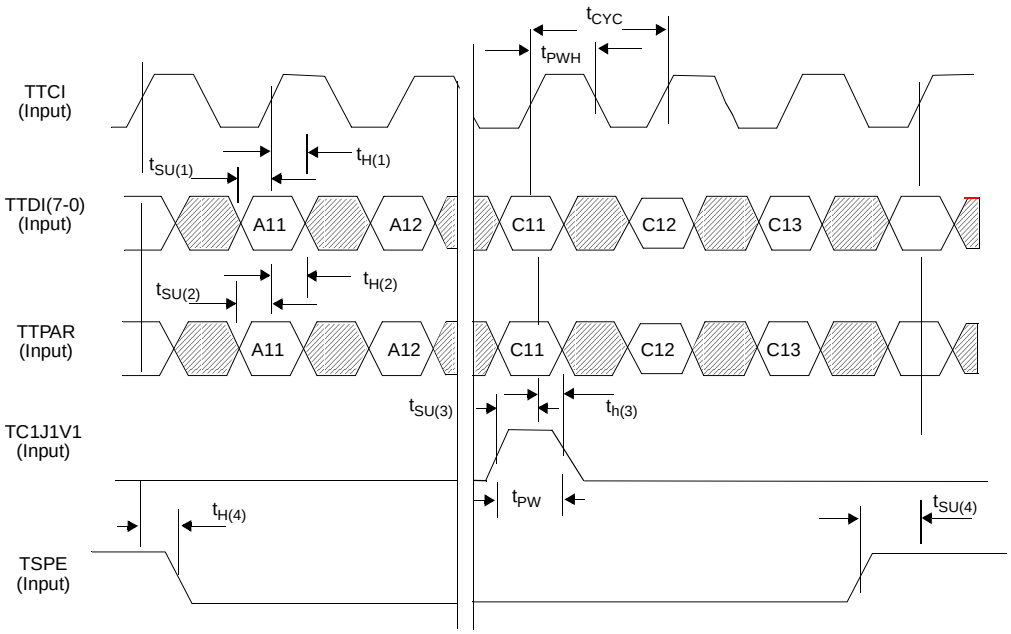
Figure 14. Transmit Parallel Interface Timing



Note: TLCO is derived from either TRCI (normal or source timing mode, Tx retiming enabled), TTCI (normal mode, Tx retiming bypassed), or STRCI (source timing mode, Tx retiming bypassed). Clock synthesis does not function when the parallel interface is selected, and should be bypassed. When clock synthesis is bypassed, TSCKO and TSFRO are derived from the 155 MHz TXCIT/C inputs.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TRCI clock period		51.44		ns
	TRCI duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	40		60	%
$t_{SU(1)}$	TRFI setup time to TRCI ↑	2.0			ns
$t_{H(1)}$	TRFI hold time after TRCI ↑	6.0			ns
$t_{CYC(2)}$	TLCO clock period		51.44		ns
	TLCO duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	40		60	%
$t_{D(1)}$	TLCO ↓ output delay from TRCI ↑	0.0		20	ns
$t_{D(2)}$	TLFO ↑ delay from TLCO ↓	-1.0		2.0	ns
$t_{D(3)}$	TLDO(7-0) delay from TLCO ↓	0.0		3.0	ns
$t_{D(4)}$	TLPR delay from TLCO ↓	-1.0		2.0	ns
$t_{D(5)}$	TLFO ↑ delay from TRCI ↑ that clocks in TRFI	51.44		81.4	ns
$t_{PW(1)}$	TRFI pulse width		51.44		ns
$t_{PW(2)}$	TLFO pulse width		51.44		ns

Figure 15. Transmit Terminal Interface Normal Timing



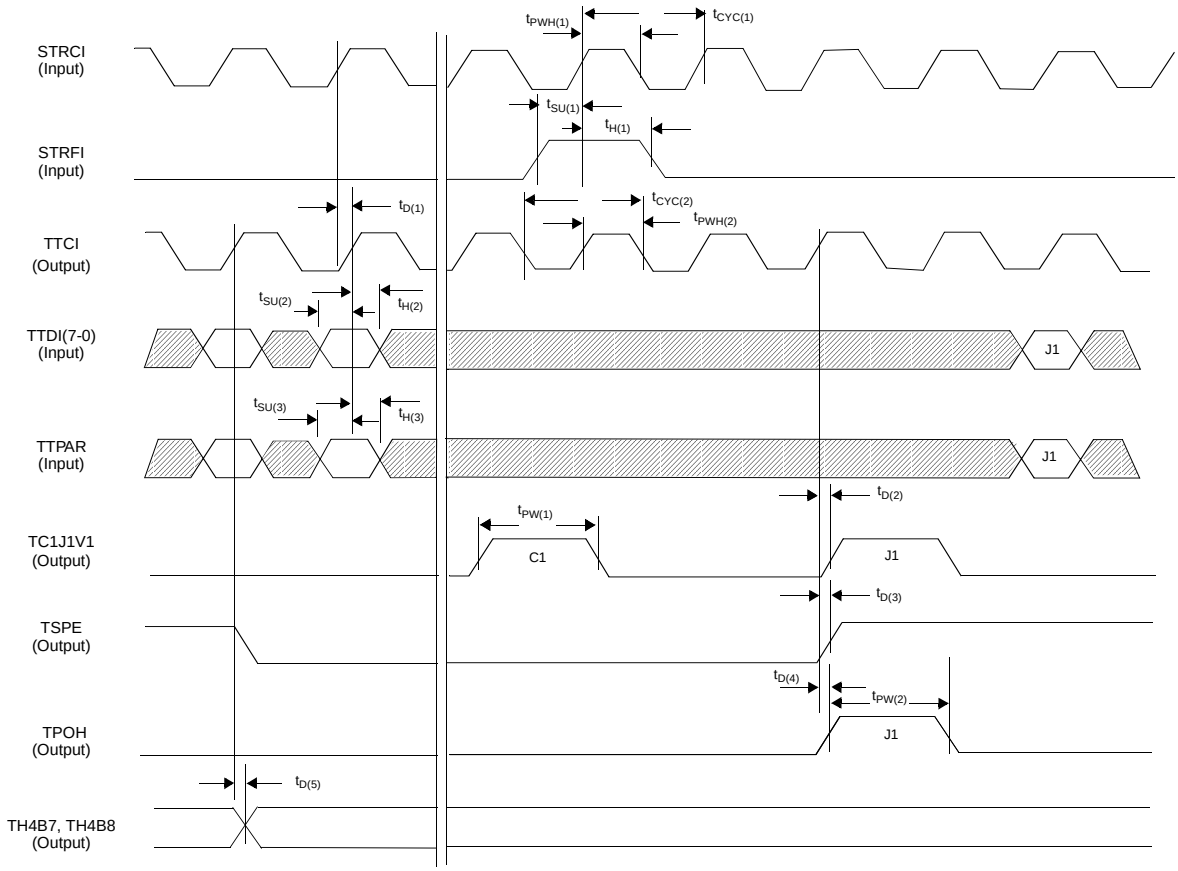
Note: The H1/H2 pointer bytes (including the concatenation pointer bytes in STM-1 mode) must be present at the transmit terminal interface when the retiming block is bypassed and normal timing is selected.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYC}	TTCI clock period		51.44		ns
	TTCI duty cycle t_{PWH}/t_{CYC}	40		60	%
$t_{SU(1)}$	TTDI setup time to TTCI ↑	5.5			ns
$t_{H(1)}$	TTDI hold time after TTCI ↑	1.0			ns
$t_{SU(2)}$	TTPAR setup time to TTCI ↑	4.0			ns
$t_{H(2)}$	TTPAR hold time after TTCI ↑	1.0			ns
$t_{SU(3)}$	TC1J1V1 setup time to TTCI ↑	7.0			ns
$t_{H(3)}$	TC1J1V1 hold time after TTCI ↑	1.0			ns
t_{PW}	TC1J1V1 pulse width		51.44		ns
$t_{SU(4)}$	TSPE setup time to TTCI ↑	7.0			ns
$t_{H(4)}$	TSPE hold time after TTCI ↑	1.0			ns

The Signal TC1J1V1 (input) is shown going active during the C1 time for the first STS-1 of the STS-3 signal. The signal is also active for the J1 byte (3 J1s in an STS-3 signal) and for the V1 byte(s) if so configured. The C1 pulse occurs once per frame, and J1 pulses occur once per frame per STS-1 (once in STS-3c or STM-1 mode, or 3 times in STS-3 mode). The V1 pulse(s) occur once every four frames when enabled.

For STM-1 operation, the V1 pulse must occur three TTCI clock periods after the J1 pulse (same as STS-3 mode) although the earliest a V1 byte can occur is six clocks after the V1 pulse.

Figure 16. Transmit Terminal Interface Source Timing



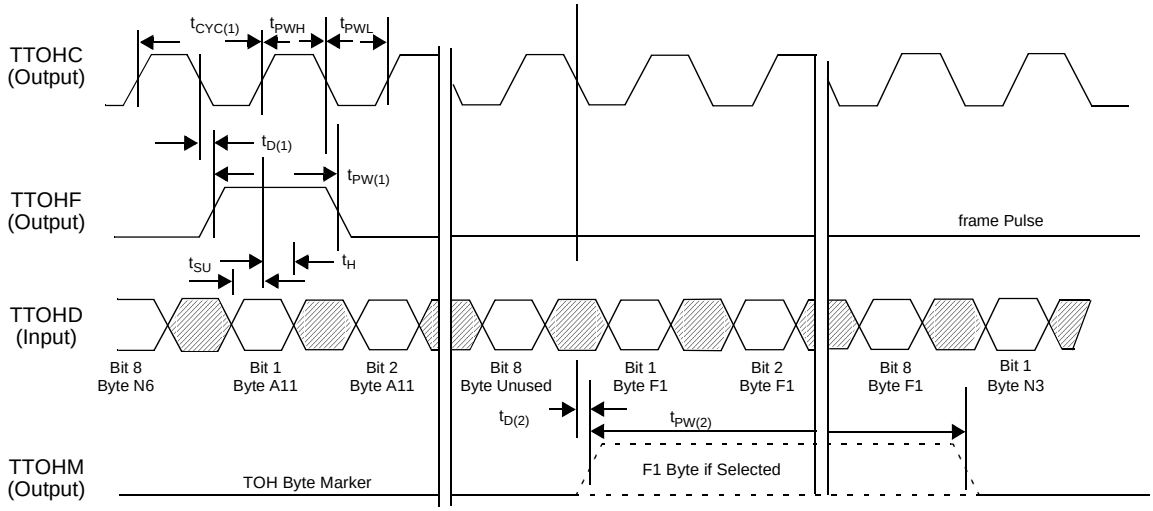
Note: The input data TTDI (7-0) and parity TTPAR are shown for control bits TTCIV (bit 3 in register 022H) and TTOS1/0 (bits 2 and 1 in register 022H) set to 000. Data and parity will be clocked in on positive edges of TTCI two clocks after the output signals (TC1J1V1, TSPE). When TTCIV and TTOS1/0 are set to 100, the delay between the output signals and the input data is 1.5 clock cycles. Data and parity will be clocked in on negative edges of TTCI when control bit TTCIV is set to 1. The V1 pulse occurs three clock cycles after the J1 pulse. For STM-1 VC-4 (STS-3c) operation, one J1 pulse and one optional V1 pulse is present. For STS-3 operation, three J1 pulses and three optional V1 pulses will be present.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	STRCI clock period		51.44		ns
	STRCI duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	45		55	%
$t_{SU(1)}$	STRFI setup time to STRCI ↑	2.0			ns
$t_{H(1)}$	STRFI hold time after STRCI ↑	8.0			ns
$t_{D(1)}$	TTCI ↑ delay from STRCI ↑	3.0		13.5	ns
$t_{CYC(2)}$	TTCI clock period	0.0	51.4		ns
	TTCI duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	45		55	%
$t_{SU(2)}$	TTDI(7-0) setup time to TTCI ↑	17.5			ns

(continued on next page)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{H(2)}$	TTDI(7-0) hold time after TTCI ↑	-2.0			ns
$t_{SU(3)}$	TTPAR setup time to TTCI ↑	17.5			ns
$t_{H(3)}$	TTPAR hold time after TTCI ↑	-2.0			ns
$t_{D(2)}$	TC1J1V1↑ after TTCI ↑	3.5		11.5	ns
$t_{PW(1)}$	TC1J1V1 pulse width		51.4	154.3	ns
$t_{D(3)}$	TSPE ↑ delay from TTCI ↑	3.5		11.5	ns
$t_{D(4)}$	TPOH ↑ delay from TTCI ↑	3.1		11.0	ns
$t_{D(5)}$	TH4B7, TH4B8 delay from TTCI ↑	3.2		11.5	ns
$t_{PW(2)}$	TPOH pulse width		51.4	154.3	ns

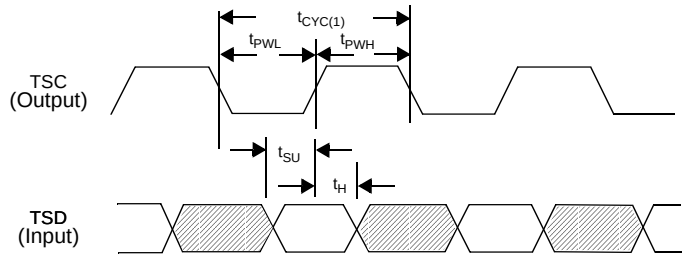
Figure 17. Transmit TOH Interface Timing



Note: The TTOHM signal indicates the location of a programmable TOH byte using control bits TOHS2, TOHS1, and TOHS0. The following TOH byte locations are programmable using control bits TOHS2, TOHS1 and TOHS0 (bits 4, 3 and 2 in register 00CH): J0, D1-D3, D4-D12, E1, E2, K1/K2, F1, and no selection. The control bits are also shared for the receive side.

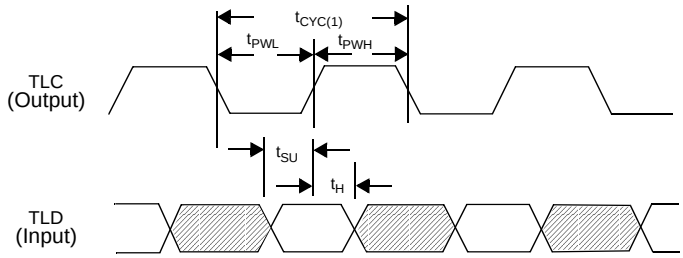
Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TTOHC clock period	154.3		205.8	ns
t_{PWH}	TTOHC high time		102.9		ns
t_{PWL}	TTOHC low time	51.4		102.9	ns
$t_{D(1)}$	TTOHF ↑ delay from TTOHC ↓	-1.0		2.0	ns
$t_{D(2)}$	TTOHM ↑ delay from TTOHC ↓	-2.0		2.0	ns
$t_{PW(1)}$	TTOHF pulse width		154.3		ns
$t_{PW(2)}$	TTOHM pulse width		1543		ns
t_{SU}	TTOHD setup time to TTOHC ↑	25.0			ns
t_H	TTOHD hold time after TTOHC ↑	0.0			ns

Figure 18. Transmit Section Data Communication Interface Timing (D1-D3 Bytes)



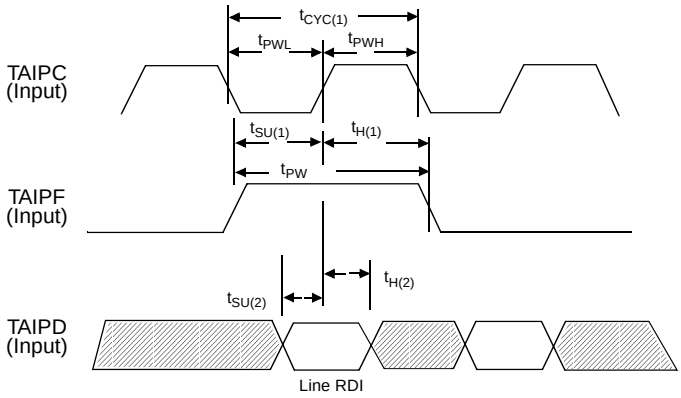
Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TSC clock period	5.0		5.2	µs
t_{PWH}	TSC high time	2.5		2.6	µs
t_{PWL}	TSC low time	2.5		2.6	µs
t_{SU}	TSD setup time to TSC ↑	8.0			ns
t_H	TSD hold time after TSC ↑	2.0			ns

Figure 19. Transmit Line Data Communication Interface Timing (D4-D12 Bytes)



Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TLC clock period	1.7		1.8	µs
t_{PWH}	TLC high time	823.0		874.5	ns
t_{PWL}	TLC low time	823.0		874.5	ns
t_{SU}	TLD setup time to TLC ↑	25.0			ns
t_H	TLD hold time after TLC ↑	0.0			ns

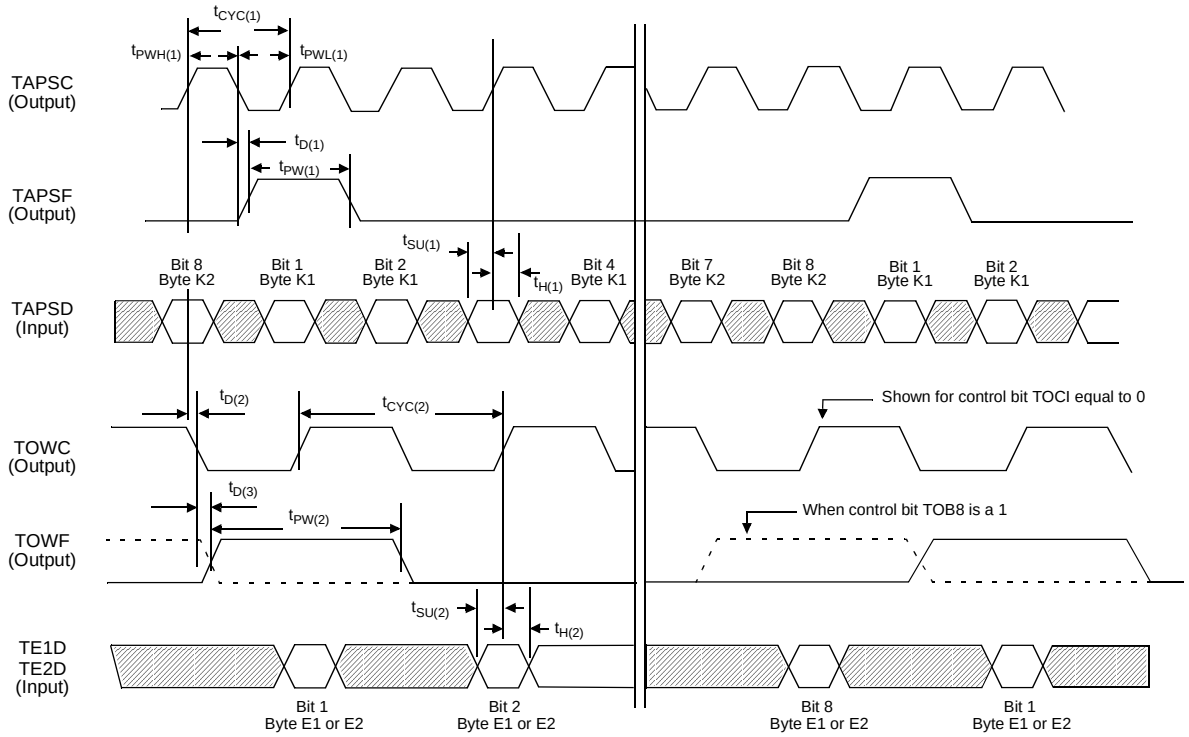
Figure 20. Transmit Alarm Indication Port (AIP) Interface Timing



Note: The TAIPC lead is normally connected to the RAIPC lead of the mate PHAST-3N. The TAIPF and TAIPD leads are normally connected to the RAIPF and RAIPD leads of the mate PHAST-3N, respectively.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TAIPC clock period		1.5		µs
t_{PWH}	TAIPC high time		771.6		ns
t_{PWL}	TAIPC low time		771.6		ns
$t_{SU(1)}$	TAIPF setup time to TAIPC ↑	5.0			ns
$t_{H(1)}$	TAIPF hold time after TAIPC ↑	2.0			ns
t_{PW}	TAIPF pulse width		1.5		µs
$t_{SU(2)}$	TAIPD setup time to TAIPC ↑	5.0			ns
$t_{H(2)}$	TAIPD hold time after TAIPC ↑	2.0			ns

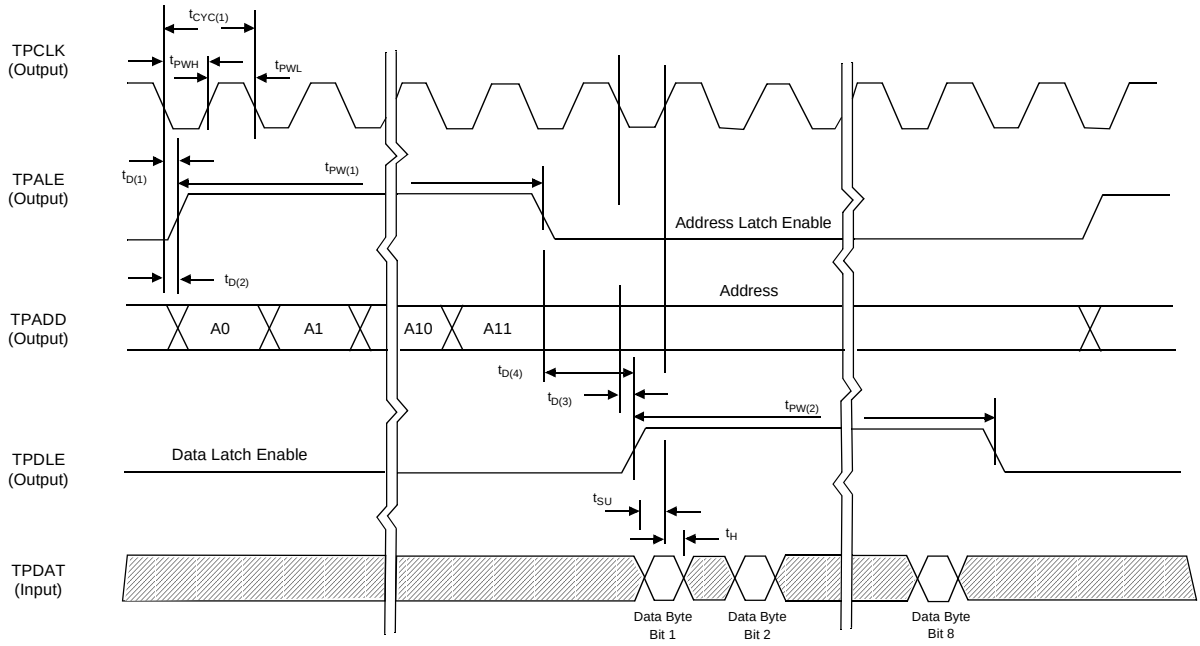
Figure 21. Transmit APS, E1 and E2 Interface Timing



Note: The solid-line TOWF, TE1D and TE2D waveforms shown correspond to control bit TOB8 equal to 0 (bit 2 in register 020H). When control bit TOB8 is a 1, the frame pulse will be shifted to bit 8 for TE1D and TE2D. The waveforms also correspond to control bit TOCI (bit 3 in register 020H) equal to 0 (TOWF clocked out on falling edges of TOWC and TE1D, TE2D clocked in on rising edges of TOWC). When control bit TOCI is a 1, TOWF will be clocked out on rising edges of TOWC and TE1D, TE2D will be clocked in on falling edges of TOWC.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TAPSC clock period	7.7		7.8	µs
$t_{PWH(1)}$	TAPSC high time		3.7		µs
$t_{PWL(1)}$	TAPSC low time	4.1		4.2	µs
$t_{D(1)}$	TAPSF ↑ delay from TAPSC ↓	-1.0		3.0	ns
$t_{SU(1)}$	TAPSD setup time to TAPSC ↑	25.0			ns
$t_{H(1)}$	TAPSD hold time after TAPSC ↑	0.0			ns
$t_{PW(1)}$	TAPSF pulse width	7.7		7.8	µs
$t_{PW(2)}$	TOWF pulse width	15.5		15.6	µs
$t_{D(2)}$	TOWC ↓ delay from TAPSC ↑	0.0		3.0	ns
$t_{D(3)}$	TOWF ↑ delay from TOWC ↓	-1.0		3.0	ns
$t_{CYC(2)}$	TOWC clock period	15.5		15.6	µs
$t_{SU(2)}$	TE1D, TE2D setup time to TOWC ↑	25.0			ns
$t_{H(2)}$	TE1D, TE2D hold time after TOWC ↑	0.0			ns

Figure 22. Transmit POH Interface Timing



The address field has the following format:

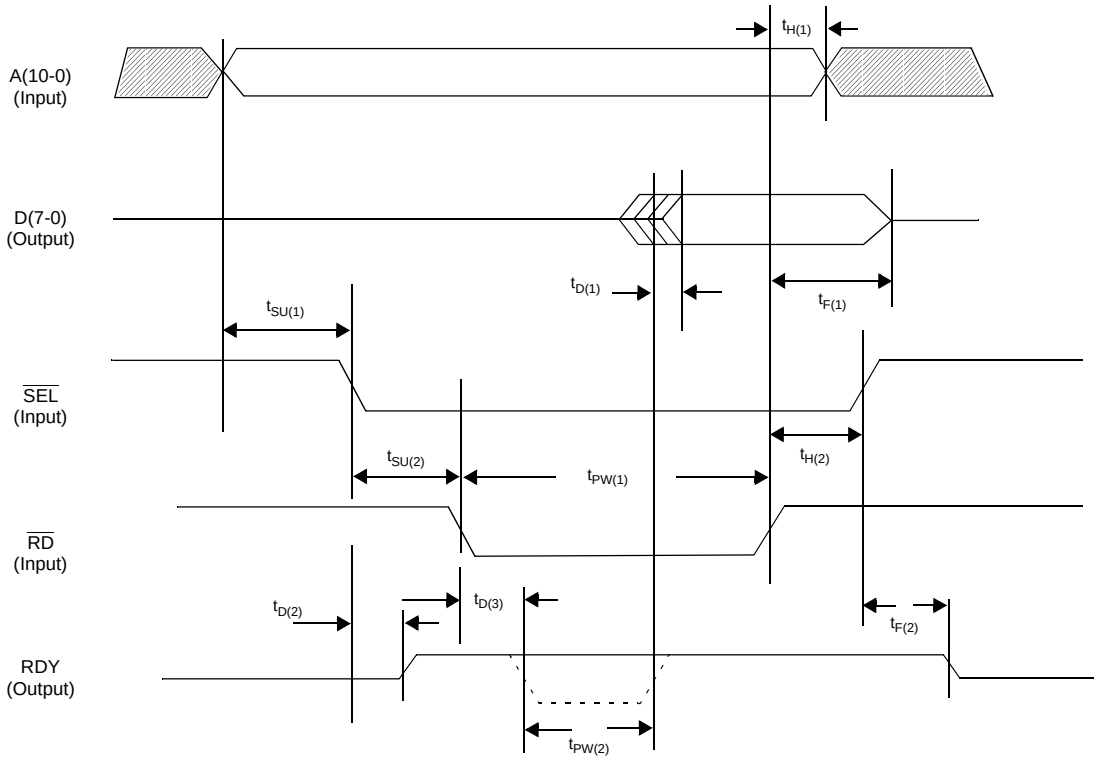
A0 - A5	A6	A7	A8	A9	A10	A11	Format and POH Byte
Not Used Equal to 0s	0	0	X	X	X	X	STS-1 No. 1
	0	1	X	X	X	X	STS-1 No. 2
	1	0	X	X	X	X	STS-1 No. 3
	1	1	X	X	X	X	STM-1/VC-4
	X	X	0	0	0	0	J1 Byte
	X	X	0	0	0	1	B3 Byte
	X	X	0	0	1	0	C2 Byte
	X	X	0	0	1	1	G1 Byte
	X	X	0	1	0	0	F2 Byte
	X	X	0	1	0	1	H4 Byte
	X	X	0	1	1	0	F3 Byte
	X	X	0	1	1	1	K3 Byte
	X	X	1	0	0	0	N1 (Z5) Byte

(continued on next page)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYC(1)}$	TPCLK clock period		154.3		ns
t_{PWH}	TPCLK high time		102.9		ns
t_{PWL}	TPCLK low time		51.4		ns
$t_{D(1)}$	TPALE ↑ delay from TPCLK ↓	-2.0		2.0	ns
$t_{PW(1)}$	TPALE pulse width		1.9		µs
$t_{D(2)}$	TPADD delay from TPCLK ↓	-1.0		2.0	ns
$t_{D(3)}$	TPDLE ↑ delay from TPCLK ↓	-2.0		2.0	ns
$t_{PW(2)}$	TPDLE pulse width		1.2		µs
t_{SU}	TPDAT setup time to TPCLK ↑	25.0			ns
t_{H}	TPDAT hold time after TPCLK ↑	0.0			ns
$t_{D(4)}$	TPDLE ↑ delay from TPALE ↓	150.0	154.3	160.0	ns

MICROPROCESSOR TIMING

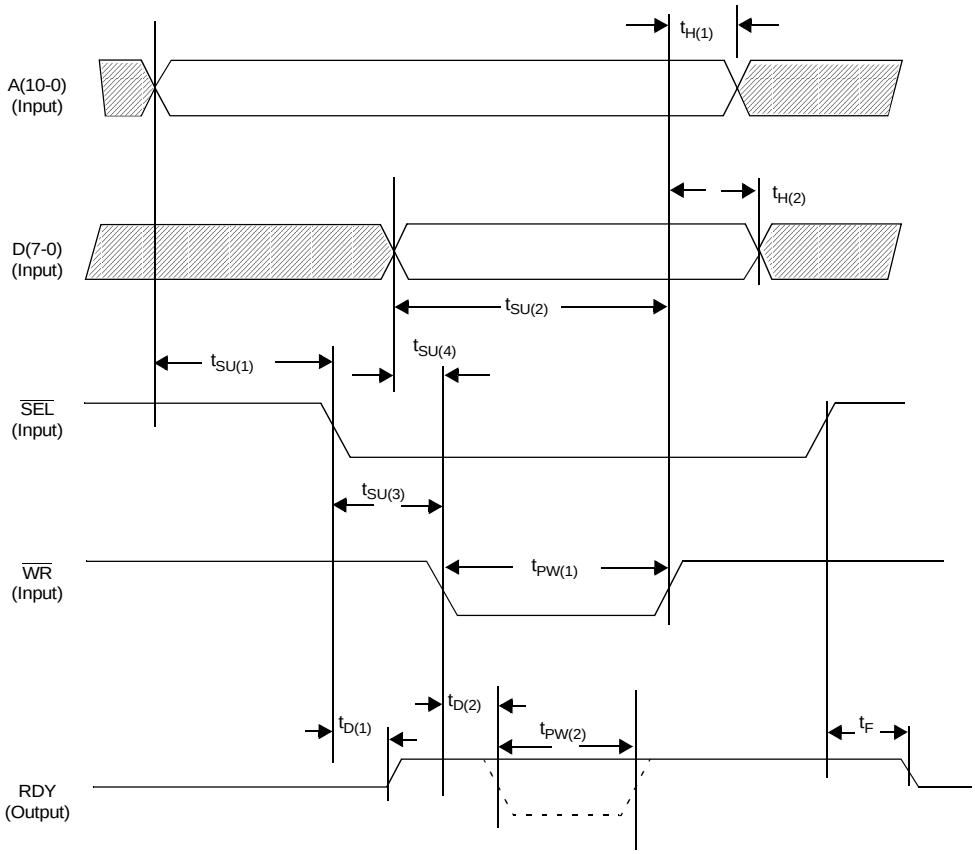
Figure 23. Intel Microprocessor Interface Read Cycle Timing



Symbol	Parameter		Min	Typ	Max	Unit
$t_{SU(1)}$	A(10-0) address setup time to $\overline{SEL}$ ↓		5.0			ns
$t_{H(1)}$	A(10-0) address hold time after $\overline{RD}$ ↑		8.0			ns
$t_{D(1)}$	D(7-0) data valid delay from RDY ↑		5.0			ns
$t_{F(1)}$	D(7-0) data float time after $\overline{RD}$ ↑		10			ns
$t_{SU(2)}$	$\overline{SEL}$ ↓ setup time to $\overline{RD}$ ↓		5.0			ns
$t_{PW(1)}$	$\overline{RD}$ pulse width		40			ns
$t_{H(2)}$	$\overline{SEL}$ ↓ hold time after $\overline{RD}$ ↑		7.0			ns
$t_{D(2)}$	RDY ↑ delay from $\overline{SEL}$ ↓				0.0	ns
$t_{D(3)}$	RDY ↓ delay from $\overline{RD}$ ↓		0.0		16	ns
$t_{F(2)}$	RDY float time after $\overline{SEL}$ ↑		0.0		15	ns
$t_{PW(2)}$	RDY pulse width	Hardware register access (Note 1)	3*ACE_{cyc}		40*ACE_{cyc}	ns
		RAM register access (Note 2)	34*ACE_{cyc}		50*ACE_{cyc}	ns
		RAM register access (Note 3)	34*ACE_{cyc}		324*ACE_{cyc}	ns

Note 1: The ACE clock (ACECI) frequency is 48 MHz and one ACE cycle (ACE_{cyc}) is 20.83 ns.
Note 2: When the relevant Busy bit = 0. TBUSY (bit 1 in register 017H) for accessing Transmit RAM or RBUSY (bit 0 in register 017H) for accessing Receive RAM.
Note 3: When the relevant Busy bit = 1.
Please refer to “Access of Registers Located in Ram” on page 139.

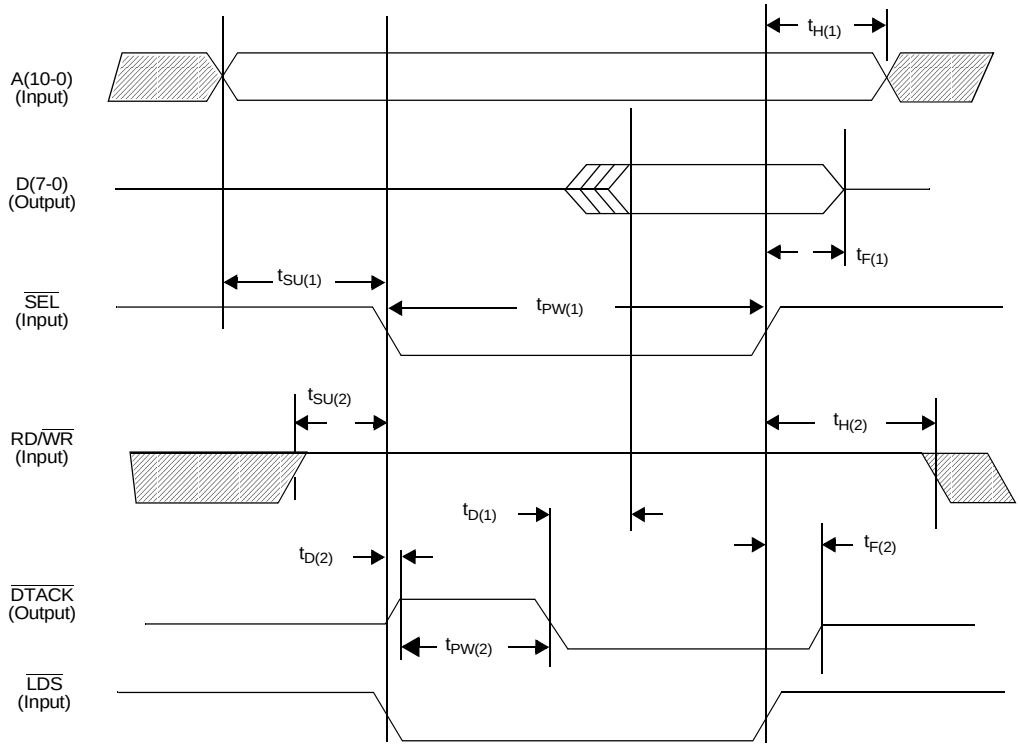
Figure 24. Intel Microprocessor Interface Write Cycle Timing



Symbol	Parameter		Min	Typ	Max	Unit
$t_{SU(1)}$	A(10-0) address setup time to $\overline{SEL}$ ↓		5.0			ns
$t_{H(1)}$	A(10-0) address hold time after $\overline{WR}$ ↑		8.0			ns
$t_{SU(2)}$	D(7-0) data valid setup time to $\overline{WR}$ ↑		5.0			ns
$t_{H(2)}$	D(7-0) data hold time after $\overline{WR}$ ↑		10			ns
$t_{SU(3)}$	$\overline{SEL}$ ↓ setup time to $\overline{WR}$ ↓		5.0			ns
$t_{PW(1)}$	$\overline{WR}$ pulse width		40			ns
$t_{D(1)}$	RDY ↑ delay from $\overline{SEL}$ ↓				0.0	ns
$t_{D(2)}$	RDY ↓ delay from $\overline{WR}$ ↓				16	ns
$t_{PW(2)}$	RDY pulse width	Hardware register access (Note 1)	0.0		40*ACE_{cyc}	ns
		RAM register access (Note 2)	0.0		50*ACE_{cyc}	ns
		RAM register access (Note 3)	0.0		324*ACE_{cyc}	ns
$t_{SU(4)}$	RAM cycle data valid setup time to $\overline{WR}$ ↓		0.0			ns
t_F	RDY float time after $\overline{WR}$ ↑				15	ns

Note 1: The ACE clock (ACECI) frequency is 48 MHz and one ACE cycle (ACE_{cyc}) is 20.83 ns.
Note 2: When the relevant Busy bit = 0. TBUSY (bit 1 in register 017H) for accessing Transmit RAM or RBUSY (bit 0 in register 017H) for accessing Receive RAM.
Note 3: When the relevant Busy bit = 1.
Please refer to “Access of Registers Located in Ram” on page 139.

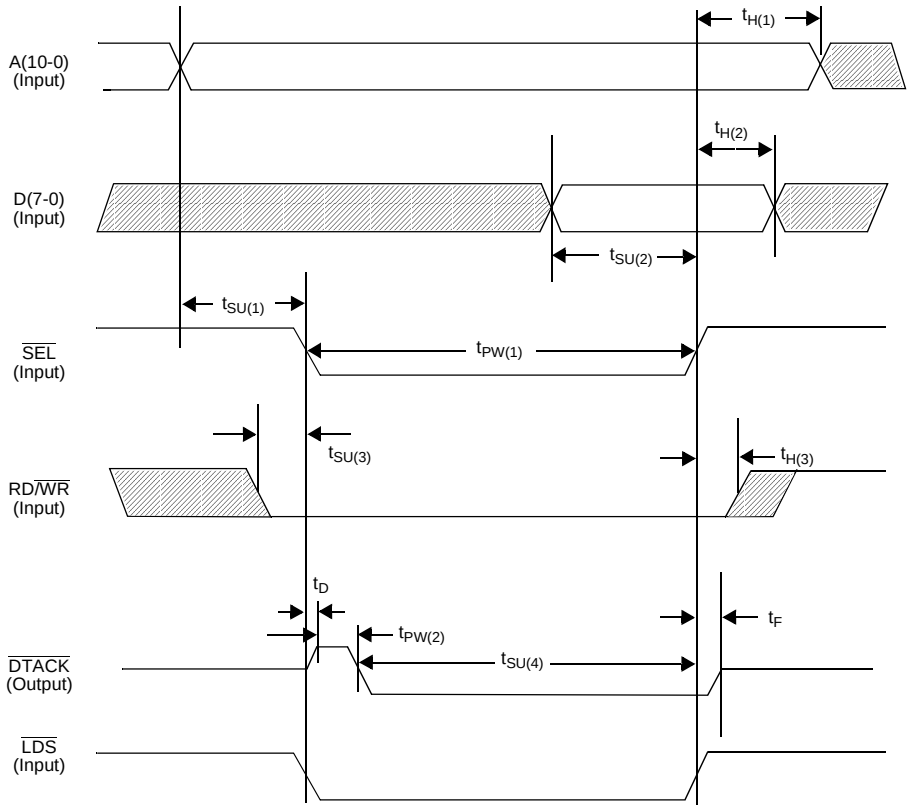
Figure 25. Motorola Microprocessor Interface Read Cycle Timing



Symbol	Parameter		Min	Typ	Max	Unit
$t_{SU(1)}$	A(10-0) address valid setup time to $\overline{SEL}$ ↓, $\overline{LDS}$ ↓ (see Note 1)		5.0			ns
$t_{H(1)}$	A(10-0) address hold time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		8.0			ns
$t_{D(1)}$	D(7-0) data valid delay from $\overline{DTACK}$ ↓				7.0	ns
$t_{F(1)}$	D(7-0) data float time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)				15	ns
$t_{PW(1)}$	$\overline{SEL}$ or $\overline{LDS}$ pulse width		40			ns
$t_{SU(2)}$	RD/$\overline{WR}$ ↑ setup time to $\overline{SEL}$ ↓, $\overline{LDS}$ ↓ (see Note 1)		5.0			ns
$t_{H(2)}$	RD/$\overline{WR}$ ↓ hold time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		7.0			ns
$t_{D(2)}$	$\overline{DTACK}$ ↑ delay from $\overline{SEL}$ ↓, $\overline{LDS}$ ↓ (see Note 1)		6.0		17	ns
$t_{PW(2)}$	$\overline{DTACK}$ pulse width	Hardware register access (Note 3)	3*ACE_{cyc}		40*ACE_{cyc}	ns
		RAM register access (Note 4)	34*ACE_{cyc}		50*ACE_{cyc}	ns
		RAM register access (Note 5)	34*ACE_{cyc}		324*ACE_{cyc}	ns
$t_{F(2)}$	$\overline{DTACK}$ float time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑, (see Note 2)		5.0		13	ns

Note 1: Measured with respect to the later of $\overline{LDS}$ or $\overline{SEL}$ falling edge.
Note 2: Measured with respect to the earlier of $\overline{LDS}$ or $\overline{SEL}$ rising edge.
Note 3: The ACE Clock (ACECI) frequency is 48 MHz and one ACE cycle (ACE_{cyc}) is 20.83 ns.
Note 4: When the relevant Busy bit = 0. TBUSY (bit 1 in register 017H) for accessing Transmit RAM or RBUSY (bit 0 in register 017H) for accessing Receive RAM.
Note 5: When the relevant Busy bit = 1.
Please refer to “Access of Registers Located in Ram” on page 139.

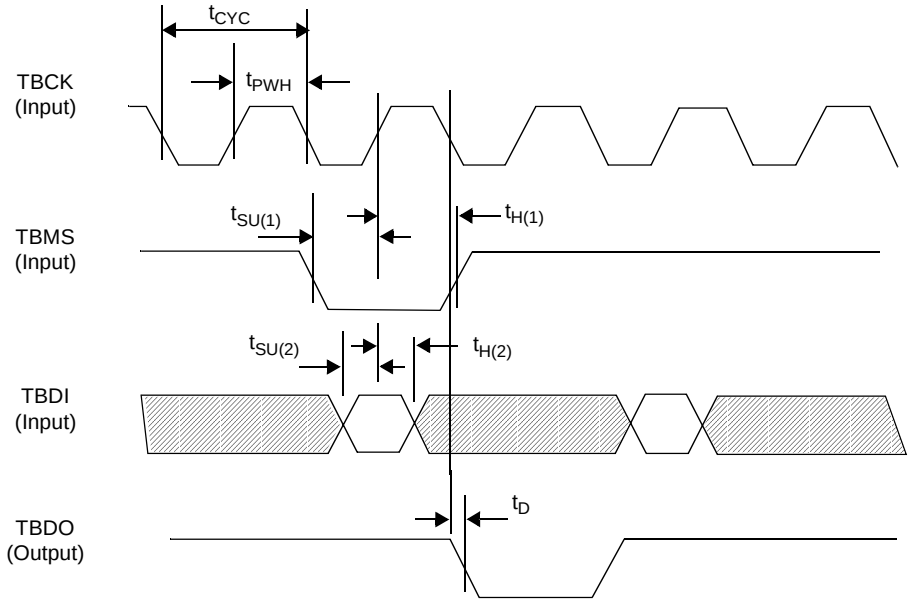
Figure 26. Motorola Microprocessor Interface Write Cycle Timing



Symbol	Parameter		Min	Typ	Max	Unit
$t_{SU(1)}$	A(10-0) address setup time to $\overline{SEL}$ ↓, $\overline{LDS}$ ↓ (see Note 1)		5.0			ns
$t_{H(1)}$	A(10-0) address hold time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		8.0			ns
$t_{SU(2)}$	D(7-0) data valid setup time to $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		5.0			ns
$t_{H(2)}$	D(7-0) data hold time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		10			ns
$t_{PW(1)}$	$\overline{SEL}$ or $\overline{LDS}$ pulse width		40			ns
$t_{SU(3)}$	RD/$\overline{WR}$ ↓ setup time to $\overline{SEL}$ ↓, $\overline{LDS}$ ↓ (see Note 1)		5.0			ns
$t_{H(3)}$	RD/$\overline{WR}$ ↓ hold time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		5.0			ns
t_D	$\overline{DTACK}$ ↑ delay from $\overline{SEL}$ ↓, $\overline{LDS}$ ↓ (see Note 1)		6.0		17	ns
$t_{PW(2)}$	$\overline{DTACK}$ pulse width	Hardware register access (Note 3)	0.0		40*ACE_{cyc}	ns
		RAM register access (Note 4)	0.0		50*ACE_{cyc}	ns
		RAM register access (Note 5)	0.0		324*ACE_{cyc}	ns
t_F	$\overline{DTACK}$ float time after $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		5.0		13	ns
$t_{SU(4)}$	$\overline{DTACK}$ low setup time to $\overline{SEL}$ ↑, $\overline{LDS}$ ↑ (see Note 2)		5.0			ns

Note 1: Measured with respect to the later of $\overline{LDS}$ or $\overline{SEL}$ falling edge.
Note 2: Measured with respect to the earlier of $\overline{LDS}$ or $\overline{SEL}$ rising edge.
Note 3: The ACE Clock (ACECI) frequency is 48 MHz and one ACE cycle (ACE_{cyc}) is 20.83 ns.
Note 4: When the relevant Busy bit = 0. TBUSY (bit 1 in register 017H) for accessing Transmit RAM or RBUSY (bit 0 in register 017H) for accessing Receive RAM.
Note 5: When the relevant Busy bit = 1.
Please refer to “Access of Registers Located in Ram” on page 139.

Figure 27. Boundary Scan Timing

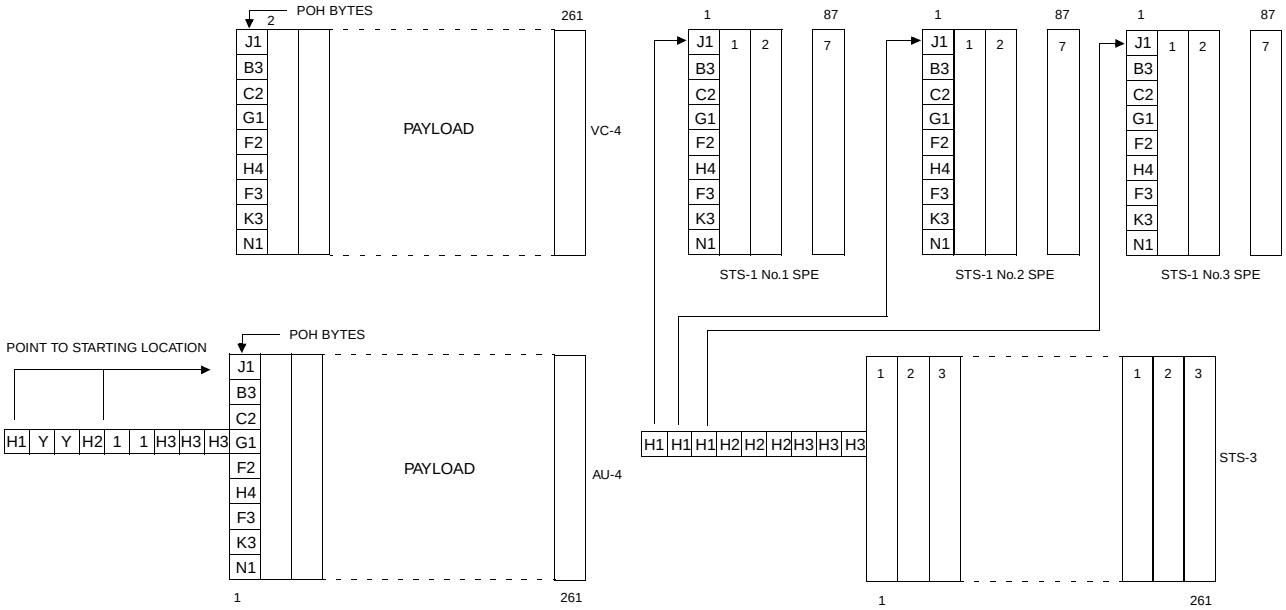


Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	TBCK clock cycle time	100			ns
	TBCK duty cycle, t_{PWH}/t_{CYC}	40	50	60	%
$t_{SU(1)}$	TBMS setup time to TBCK ↑	2.0			ns
$t_{H(1)}$	TBMS hold time after TBCK ↑	5.0			ns
$t_{SU(2)}$	TBDI setup time to TBCK ↑	2.0			ns
$t_{H(2)}$	TBDI hold time after TBCK ↑	5.0			ns
t_D	TBDO delay from TBCK ↓	6.0		17.0	ns

OPERATION

SDH/SONET FORMATS

The PHAST-3N terminates either an STM-1 AU-4 (STS-3c), or an STS-3 (STM-1 AU-3) format. The two formats, STM-1 AU-4 (STS-3c) and STS-3 (STM-1 AU-3), and their pointer relationships are shown in the diagram below.



STM-1 AU-4 (STS-3c) Format **STS-3 (STM-1 AU-3) Format**

The STM-1 AU-4 (STS-3c) format carries a Virtual Container-4 (VC-4). The VC-4 format consists of one column of POH bytes and a payload. Depending on the payloads assigned to the VC-4, the second and third columns may be designated as stuff columns. An STS-3c is defined as the SPE, concatenation pointer, and the other TOH bytes. The SPE consists of one column of POH bytes and a payload. The SPE in the STS-3c is usually assigned to carry ATM cells or packet data. The STM-1 VC-4 is usually assigned to carry TUG-3s. It can also be assigned to carry ATM cells and PPP frames, as required. The TUG-3 can be further assigned to carry TUG-2s which in turn may carry TU-12s and TU-11s. Please note that the PHAST-3N does not terminate the POH bytes that are assigned to TUG-3s carrying E3 or DS3 formats.

Each STS-3 (STM-1 AU-3) consists of an STS-1 (VC-3) plus its individual pointer bytes. Each STS-1 (VC-3) consists of one column of POH bytes and its payload. Each STS-1 is labeled 1, 2 and 3, while each AU-3 is labeled A, B and C. The primary difference between the AU-3 and the STS-1 formats is in the pointer bytes. The AU-3 requires the detection in the pointer tracking state machine of the SS-bits (size bits), while in the STS-1 pointer bytes, the SS-bits are not defined and are normally set to zero. Please note that recent changes in the ITU-T standards no longer require the detection of the size bits in the receive direction for both the STM-1 AU-3 and AU-4 formats. However, they must be generated in the transmit direction in order to be backwards compatible with existing systems in the network.

Transport Overhead and Section Overhead Bytes Structure

The transport overhead and section overhead bytes defined for the SONET STS-3 and SDH STM-1 structures are shown in the tables below. The SONET STS-3 designations are according to ANSI T1.105 - 1995 while the SDH STM-1 designations are according to draft ITU-T G.707- 11/95.

	Transport Overhead Bytes (9 columns)								
Section OH bytes	A1	A1	A1	A2	A2	A2	J0	Z0	Z0
	B1	MDB1	MDB2	E1	MDB3		F1	U (X1)	U (X2)
	D1	MDB4	MDB5	D2	MDB6		D3	U (X3)	U (X4)
Line OH Bytes	H1	H1	H1	H2	H2	H2	H3	H3	H3
	B2	B2	B2	K1			K2		
	D4			D5			D6		
	D7			D8			D9		
	D10			D11			D12		
	S1	Z1(2)	Z1(3)	Z2(1)	Z2(2)	M1	E2	U (X5)	U (X6)

Where: The U (Xn), Z1(n) and Z2(n) bytes are reserved.
The blank byte locations in the table indicate that these bytes are undefined at this time.

Table 1. TOH Bytes - SONET Transport Overhead Byte Assignment

	Transport Overhead Bytes (9 columns)								
Regenerator Section Overhead (RSOH)	A1	A1	A1	A2	A2	A2	J0	NU(1)	NU(2)
	B1	MDB1	MDB2	E1	MDB3		F1	NU(3)	NU(4)
	D1	MDB4	MDB5	D2	MDB6		D3		
AU Pointer	H1	Y	Y	H2	1*	1*	H3	H3	H3
Multiplex Section Overhead (MSOH)	B2	B2	B2	K1			K2		
	D4			D5			D6		
	D7			D8			D9		
	D10			D11			D12		
	S1					M1	E2	NU(5)	NU(6)

Where: NU (SDH) are bytes reserved for national use.
MDB (SDH) are media dependent bytes.
1* = all ones byte (FFH).
The blank byte locations in the table indicate that these bytes are undefined at this time.

Table 2. SOH Bytes - SDH STM-1 Section Overhead Byte Assignment

Path Overhead (POH) Bytes and Payload Structure

The POH bytes and payload bytes defined for the STS-3 STS-1 format are shown in the table below:

Path Overhead Bytes and payload (87 columns)

1	2 29	30	31 58	59	60 87
J1	Payload	Fixed Stuff	Payload	Fixed Stuff	Payload
B3					
C2					
G1					
F2					
H4					
Z3					
Z4					
Z5					

Table 3. STS-3 STS-1 POH Byte Assignment

The POH bytes and payload bytes defined for the STM-1 VC-4 format are shown in the table below:

Path Overhead Bytes and payload (261 columns)

1	2 261
J1	Payload
B3	
C2	
G1	
F2	
H4	
F3	
K3	
N1	

Table 4. STM-1 VC-4 POH Byte Assignment

PATH MODES OF OPERATION

In the receive direction, the path overhead bytes in the VC-4 or the path overhead bytes in the three STS-1s are monitored for operation. All POH bytes are provided intact at the receive terminal interface. However, an exception is made for the N1 and B3 bytes when the tandem connection feature is enabled. The N1 byte may be terminated by the PHAST-3N, in which case the B3 byte is recalculated before it is provided at the terminal interface.

The POH bytes are also provided at a POH interface and are written into RAM locations in the memory map for microprocessor access. The subsequent actions taken by receive events such as path level alarms or BIP errors are controlled by AIS and RDI enable control bits. Thus, it possible to have a path level alarm and not generate AIS downstream or RDI upstream.

Two path termination modes (i.e., for handling of the POH bytes) are provided for in the transmit direction: a non-terminating mode and a terminating mode.

Path Non-Terminating Mode

When a 0 is written to control bit(s) PTEn (bit 7 in register X42H where n corresponds to STS-1 No. 1, 2 or 3 and X = 1, 2 or 3), the PHAST-3N transmit section is configured in the path non-terminating mode. All POH bytes are transmitted transparently through the PHAST-3N without processing, except for the Tandem Connection feature (the N1 byte) which may be enabled. For the STM-1 AU-4 (STS-3c) format, control bit PTE1 is enabled. Control bits PTE2 and PTE3 are disabled except with respect to stuff column insertion. For the STS-3 (STM-1 AU-3) format, all three PTE control bits (PTEn) are enabled. Thus, each STS-1/AU-3 can be individually selected for path non-terminating mode.

Path Terminating Mode

When a 1 is written to control bit(s) PTEn, the PHAST-3N transmit section is configured for the path terminating mode. For the STM-1 AU-4 (STS-3c) format, control bit PTE1 is enabled. Control bits PTE2 and PTE3 are disabled except with respect to stuff column insertion. For the STS-3 (STM-1 AU-3) format, all three control bits (PTEn) are enabled. Thus, each STS-1/AU-3 can be individually selected for path terminating mode.

When a path terminating mode is enabled, any POH byte present at the transmit terminal interface is ignored (with the exception of the H4 byte which can be programmed to be transmitted from the transmit terminal interface). All transmit POH bytes (nine bytes) are inserted into the STM-1 VC-4 (STS-3c SPE), or STS-3 STS-1 SPE (STM-1 AU-3) formats by the PHAST-3N. In general these bytes are inserted from either RAM locations or the POH interface. Some bytes can also be inserted from other sources, e.g., the G1 byte from the Alarm Indication Port interface or the B3 byte from internal logic. POH byte source selection is on a per byte basis.

TRANSMIT TIMING MODES

The PHAST-3N provides two transmit timing modes: normal timing, and source timing. The timing mode is selected via the MODE(2-0) leads.

The normal timing mode is used in applications where downstream devices connected to the transmit terminal interface provide timing signals to the PHAST-3N. Byte data TTDI(7-0), the C1, J1 and V1 signal TC1J1V1, the SPE signal TSPE, parity TTPAR, and clock TTCI are input signals. The C1, J1 and V1 signal identifies the locations of the C1 (J0) byte, the J1 byte in the POH column, and the V1 bytes in the tributaries. The V1 pulse is optional. When provided, the V1 pulse is used to synchronize an internal transmit H4 multiframe generator for generating the H4 multiframe sequence. The SPE signal identifies the locations of the POH bytes and payload bytes. In this mode, when the transmit retiming block is bypassed and the STM-1 mode is selected, the concatenation pointer bytes must be input at the transmit terminal interface.

The source timing mode is used in applications where the PHAST-3N is required to provide timing signals for downstream devices connected to the transmit terminal interface. The PHAST-3N provides the C1, J1 and V1 signal TC1J1V1, the SPE signal TSPE, the POH indication TPOH, the clock TTCI, and a two-bit multiframe H4 sequence TH4B7 and TH4B8 as output signals at the transmit terminal interface. Input signals required at the terminal interface are byte data TTDI(7-0) and parity TTPAR. For timing delay flexibility, the relationship between the input data and the output timing signals is programmable, ranging from 1.5 to 5 clock cycles of delay.

This mode also enables an optional V1 pulse to be generated and placed in the C1, J1 and V1 signal when required. In addition, the multiframe sequence in the H4 byte is generated and transmitted independently for each STS-1. The H4 output sequence generator (TH4B7 and TH4B8) enables an external circuit to identify the multiframe sequence for determining the V1 byte location without actually having to use the V1 pulse reference in the C1, J1 and V1 signal. The H4 multiframe sequence is generated on a per frame basis. The timing signals for the terminal side for this timing mode are derived from the source reference frame and clock timing signals, STRFI and STRCI. For added reference timing flexibility, the source reference timing is provided as separate inputs. When required, the reference output clock TSCKO and frame pulse TSFRO may be connected to the source input clock STRCI and frame input STRFI. When the retiming block is bypassed, the pointer (H1/H2 bytes) offset value will be fixed to 522.

REFERENCE RETIMING

Receive Direction

In the receive direction, the RRCI and RRFI input signals are used for pointer justification of the STM-1 AU-4, STM-1 AU-3, or STS-3 formats. The pointer justification and pointer generation circuit is enabled when control bit RTBYP (bit 4 in register 402H) is set to 1. In addition to the calculation and insertion of the pointer bytes, and the alignment of the VC-4, STS-1s or AU-3s to the new pointer, the RRCI and RRFI reference signals are also used to derive the timing signals for the receive terminal interface. The RRCI reference is monitored for loss of clock (clock stuck high or low).

When the pointer justification circuit is bypassed, the terminal interface signals are derived from the line interface signals. The H1/H2 pointer values and POH/payload byte locations remain intact.

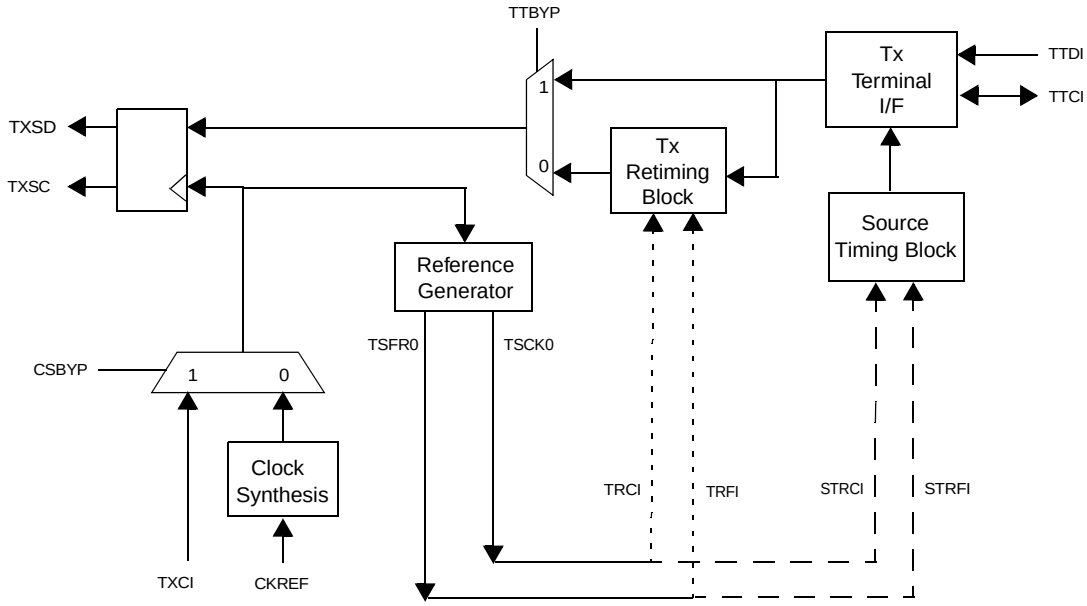
Transmit Direction

In the transmit direction, the pseudo-ECL transmit input clock (TXCIT, $\overline{\text{TXCIC}}$) or the clock synthesis circuit (via CKREF) is used to derive a 19.44 MHz transmit reference output clock TSCKO and frame pulse TSFRO when the serial interface is enabled. These signals are provided as a system reference and are normally used for the transmit retiming circuit. When used, the output clock TSCKO and frame pulse TSFRO are connected to leads for the transmit input reference retiming clock input TRCI and frame input TRFI. See Figure 28 below.

The TRCI and TRFI input signals are used for pointer justification of the incoming STM-1 AU-4, STM-1 AU-3, or STS-3 formats based on the C1J1 and SPE signals, and the calculation and insertion of the H1/H2 pointer bytes. The pointer justification and pointer generation circuit is enabled when control bit TTBYP (bit 3 in register 021H) is set to 0. The TRCI signal is monitored for loss of clock (clock stuck high or low).

When the pointer justification circuit is bypassed, the terminal line signals are fixed to the terminal side timing signals. The H1/H2 pointer bytes (including the concatenation pointer bytes in STM-1 mode) must be present at the terminal interface when the transmit retiming block is bypassed except in source timing mode when the device inserts the pointer value 522.

Figure 28. Transmit Clocking Scheme - Serial Mode



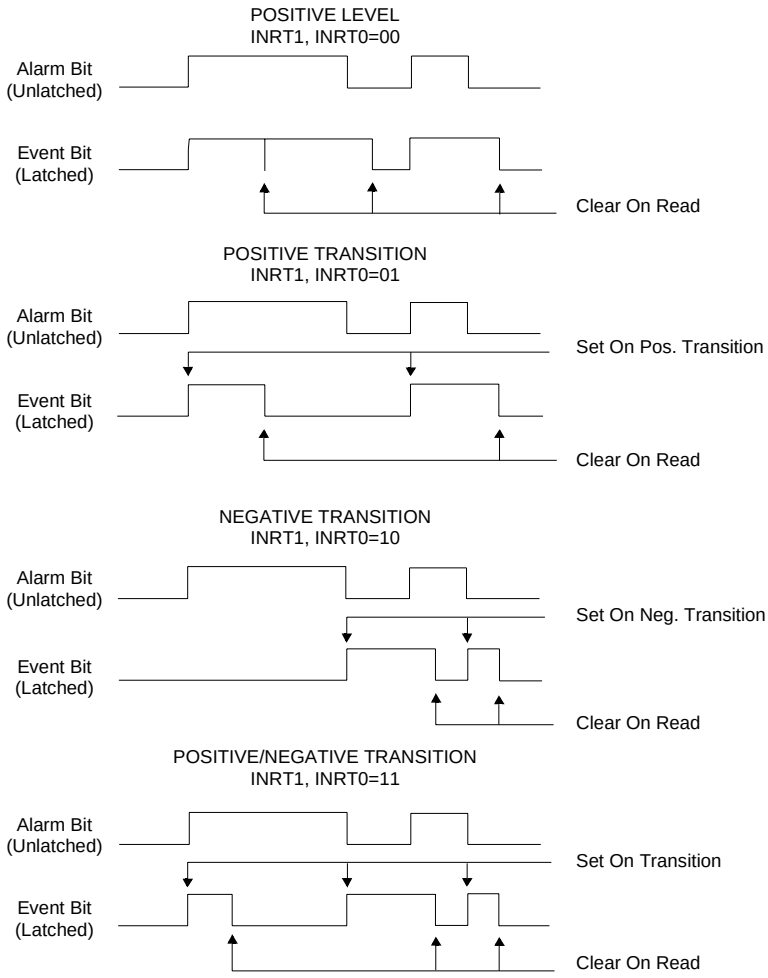
Tx Retiming Block enabled (TTBYP=0), Normal timing mode => dotted connection

Tx Retiming Block bypassed (TTBYP=1), Source timing mode => dashed connection

Tx Retiming Block bypassed (TTBYP=1), Normal timing mode => H1 H2 must be inserted from terminal side

ALARM STRUCTURE

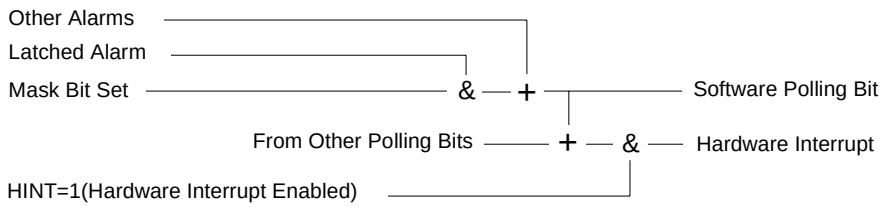
The alarm reporting structure within the PHAST-3N consists of unlatched and latched (event) alarm register bit positions. The unlatched alarm bit positions reflect the current status of a detection circuit (e.g., C2 mismatch detection). A latched alarm (event) bit latches upon the occurrence of unlatched bit conditions defined by setting the control bit INRT(1-0) states, as shown in the following diagram.



As shown in the above diagram there are four possible alarm latching configurations: positive level, positive transition, negative transition, or positive/negative transition. For example, assume that control bits INRT1 and INRT0 (bits 1 and 0 in register 00CH) are equal to 01. This configures the latched alarm circuits to set on positive transitions (0 to 1) of an alarm. The positive transition of an alarm causes the corresponding event (latched) bit to set to 1. The latched bit will remain set until the register containing the latched bit position is read by the microprocessor, at which time the latched bit positions in this register will be reset to 0. Even though the alarm (unlatched) remains active, it will not cause a latched state to recur. The latched bit will remain reset to 0 until another positive alarm (unlatched) transition occurs to set it to 1.

INTERRUPT STRUCTURE

The latched (event) bits are used for activating the hardware interrupt, when enabled. The PHAST-3N provides both a hardware indication (INT/$\overline{IRQ}$) and software polling interrupt indication, when enabled by the corresponding interrupt mask bit. The hardware interrupt capability must first be enabled by writing a 1 into the control bit HINT (bit 0 in register 010H). A software polling bit and the hardware interrupt indication (if enabled by writing a 1 to HINT) occur when one or more interrupt mask bit locations are written with a 1, and any corresponding latched alarm occurs. Please note that setting of a mask bit to 1 enables the actions by an alarm. The following is a simplified view of the logic diagram used for setting the software polling bits and the hardware interrupt (where & is an “and” function, and + is an “or” function).



The software polling interrupt register at address 019H provides a way to have the microprocessor poll a register in the memory map (provided the proper interrupt mask bits are set to 1) to point to the alarms that caused the interrupt. The software polling register has the following structure. Please note these bits follow the state of the latched alarm and when the latched alarm is cleared, the corresponding bit in the polling register will be reset to zero.

Bit	7	6	5	4	3	2	1	0
019H	SINTR	SINTT	SINTA	SINTG	SINTP1	SINTP2	SINTP3	SINTF

A SINTR indication occurs (as a 1) when one or more of the following latched alarms occurs if the corresponding mask bit is set to 1:

- Receive Loss Of Signal (RLOS),
- Receive Line Loss Of Clock (RLLOC),
- Receive Out Of frame (ROOF),
- Receive Loss Of Frame (RLOF),
- External SDH/SONET Line Failure (SLFAIL),
- Receive J0 Loss Of Lock (J0LOL),
- Receive J0 Trace Mismatch (J0TIM),
- B2 Bit Error Rate exceeded (B2BER),
- Receive Line AIS (RLAIS),
- Receive APS (RAPS),
- Receive New APS (RNAPS),
- Receive Line RDI (RLRDI),
- Alarm Indication Port Loss Of Frame alarm (APLOF),
- Alarm Indication Port Loss Of Signal alarm (APLOS),
- Alarm Indication Port Line RDI indication (APLRDI),
- Alarm Indication Port New APS alarm (APNAPS),
- Receive False Concatenation (RFHID),
- Receive Line Parity Error (RLPERR),

- External Scan Alarm 1 (SCAN1),
- External Scan Alarm 2 (SCAN2),
- Change In Synchronization Indication - S1 Byte (SSMBC),
- Receive Clock Recovery Loss Of Data Alarm (RDOOL),
- Receive Clock Recovery Frequency Alarm (RROOL),
- Test Pattern Out Of Lock alarm (TPOOL).

A SINTT indication occurs (as a 1) when one or more of the following latched alarms occurs if the corresponding mask bit is set to 1, where n is equal to 1 for the STM-1 (STS-3c) format and STS-3 STS-1 No.1, n is equal to 2 for STS-3 STS-1 No. 2, and n is equal to 3 for STS-3 STS-1 No. 3:

- Transmit Loss Of Clock (TLOC),
- Transmit Loss Of Signal (TLOS),
- Transmit Parity Error (TPERR),
- Transmit E1 Byte AIS Indication (TE1nAIS),
- Transmit H4 Out Of Multiframe (TnOOM),
- Transmit H4 Loss Of Multiframe (TnLOM),
- Transmit H1/H2 AIS Indication (THnAIS).

A SINTA indication occurs (as a 1) when one or more of the following latched alarms occurs if the corresponding mask bit is set to 1, where n is equal to 1 for the STM-1 AU-4 (STS-3c) format and STS-3 STS-1 No.1, n is equal to 2 for STS-3 STS-1 No. 2, and n is equal to 3 for STS-3 STS-1 No. 3:

- Receive Reference Loss Of Clock (RRLOC),
- Transmit Reference Loss Of Clock (TRLOC),
- Alarm Indication Port Interface Loss Of Clock (APLOC),
- Alarm Indication Port Interface CRC-4 Error (APCRC),
- Counter saturating at maximum count (COUNT).

A SINTG indication occurs (as a 1) when one or more of the following latched alarms occurs if the corresponding mask bit is set to 1, where n is equal to 1 for the STM-1 AU-4 (STS-3c) format and STS-3 STS-1 No.1, n is equal to 2 for STS-3 STS-1 No. 2, and n is equal to 3 for STS-3 STS-1 No. 3. SINTG is a software polling indication for the tandem connection alarms.

When the ETSI TC feature is enabled:

- Tandem Connection Loss Of Frame (TCLOF),
- Tandem Connection Loss Of Lock (TCLOL),
- Tandem Connection Trace Mismatch (TCTIM),
- Tandem Connection RDI (TCRDI),
- Tandem Connection ODI (TCODI),
- Tandem Connection Unequipped (TCUQ),
- Receive Tandem Connection AIS indication (RTCAIS).

A SINTPn indication occurs (as a 1) when one or more of the following latched alarms occurs if the corresponding mask bit is set to 1, where n is equal to 1 for the STM-1 AU-4 (STS-3c) format and STS-3 STS-1 No.1, n is equal to 2 for STS-3 STS-1 No. 2, and n is equal to 3 for STS-3 STS-1 No. 3:

- Receive path AIS (RnPAIS),
- Receive Loss Of Pointer (RnLOP),
- Receive New Pointer (RnNPTR),
- Receive Single-Bit RDI (RnOLD),
- Receive Remote Server Defect Indication (RnSVD),
- Receive Remote Payload Defect Indication (RnPYD),
- Receive Remote Connectivity Defect Indication (RnCND),
- Receive J1 Loss Of Lock (J1nLOL),
- Receive J1 Trace Mismatch (J1nTIM),
- B3 Bit Error Rate Exceeded (B3nBER),
- C2 Mismatch (C2nMM),
- C2 PDI (C2nPDI),
- VC AIS (VCnAIS),
- Unequipped Status (UNEQn),
- Receive Out Of Multiframe (RnOOM),
- Receive Loss Of Multiframe (RnLOM),
- Receive New K3 Byte (RPAPS) for SINTP1 only (K3 APS byte, STM-1 and STS-3 STS-1 No.1),
- Alarm Indication Port New K3 Byte (APPAPS) for SINTP1 only (K3 APS byte, STM-1 and STS-3 STS-1 No.1),
- Alarm Indication Port RDI (Server, Connectivity, Payload) indication (APRDIn).

A SINTF indication occurs (as a 1) when one or more of the following latched alarms occurs if the corresponding mask bit is set to 1, where n is equal to 1 for the STM-1 AU-4 (STS-3c) format and STS-3 STS-1 No.1, n is equal to 2 for STS-3 STS-1 No. 2, and n is equal to 3 for STS-3 STS-1 No. 3:

- Receive FIFO (RnFIFO),
- Transmit FIFO (TnFIFO).

PERFORMANCE COUNTERS

All 16-bit performance counters within the PHAST-3N have a special 16-bit read operation which allows “snap-shot” access, without the danger of one 8-bit segment changing its value after the other has been read. To perform a 16-bit read, the low order byte is read first followed by a read of the high order byte. Do not read another low order byte until after reading the high order byte. Reading the low order byte causes the high order byte of the count to be frozen, while a shadow counter continues recording in the background so that counts are not lost.

All the performance counters can be configured to be either saturating or non-saturating. When a 0 is written to control bit CROV (bit 0 in register 00BH), the performance counters are configured to be saturating, with the counters stopping at their maximum count. A saturating counter is reset to 00H on a microprocessor read cycle.

When a 1 is written to control bit CROV, the performance counters are configured to be non-saturating, and roll over to 0 on the next count after the maximum count is reached (i.e., all ones). In this mode, the counters do not clear on a microprocessor read cycle, but continue to count.

All performance counters may be reset simultaneously by writing a 1 to control bit RESETC (bit 6 in register 00AH). This bit resets the performance counters, with the counters starting to count after the clearing operation. This reset bit is self-clearing. In the saturating mode, the performance counters are reset to zero. In the non-saturating mode, 8-bit counters are reset to the value FEH, while 16-bit counters are reset to the value FEFFH. These values were chosen for test purposes. In addition, a performance counter can be cleared by writing the value of 00H to the low byte at address n, immediately followed by writing 00H to address n+1. The n+1 address location contains the high order byte of the 16-bit performance counter.

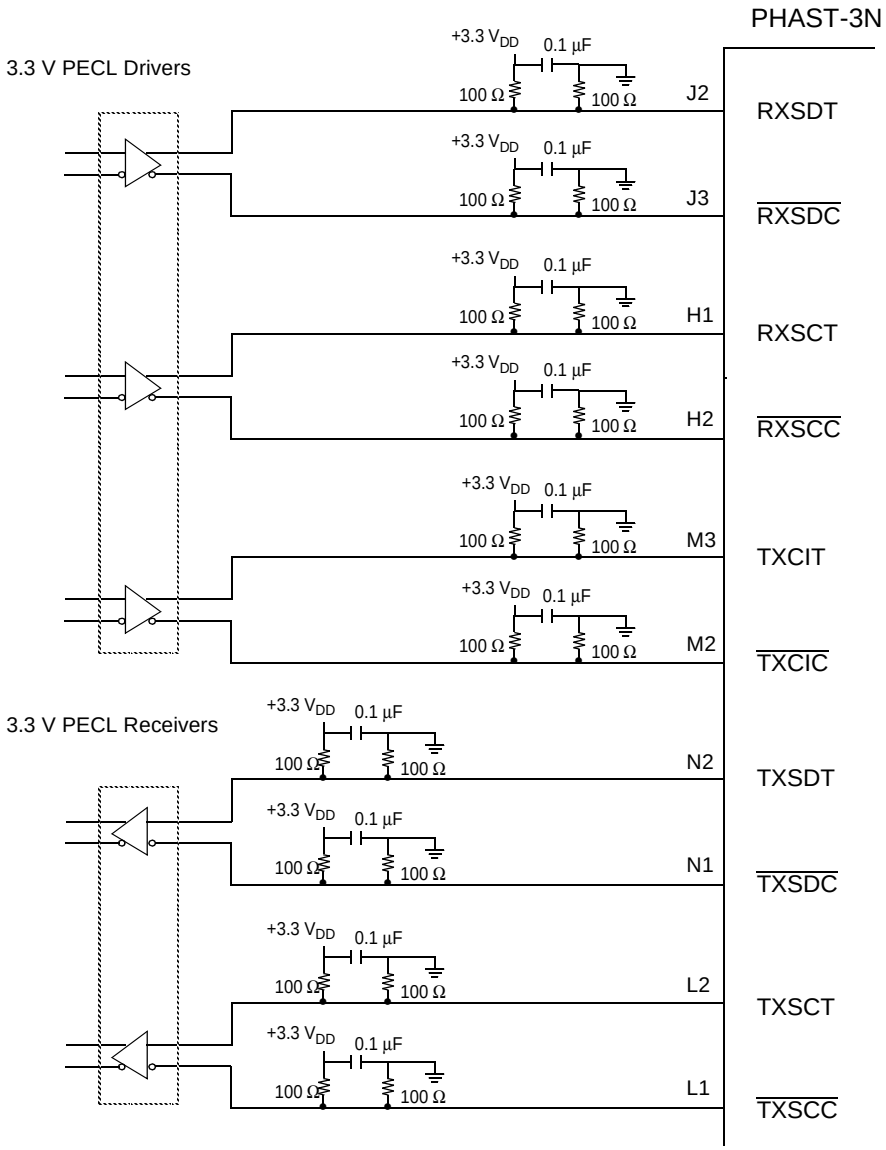
A status alarm bit COUNT (bit 0 in register 01CH/01DH), with an associated interrupt mask bit CNTM (bit 0 in register 01AH), is also provided. The COUNT status bit will be set when any of the performance counters has reached its maximum value in either the saturating mode or non-saturating modes of operation.

All BIP and REI performance counters are capable of counting events as either bits or blocks, unless otherwise specified. When a 1 is written to control bit BLKS (bit 4 in register 00BH), the B1 counter counts one or more B1 parity errors per frame as a single block error. When a 0 is written into control bit BLKS, the B1 counter counts individual errors. When a 1 is written to control bit BLKL (bit 3 in register 00BH), the B2 and line REI (FEBE) counters count one or more B2 or line REI errors per frame as a single block error. When a 0 is written into control bit BLKL, the B2 and line REI counters count individual errors. When a 1 is written to control bit BLKP (bit 2 in register 00BH), the B3 and path REI (FEBE) counters count one or more B3 or path REI errors per frame as a single block error. When a 0 is written into control bit BLKP, the B3 and path REI counters count individual errors.

PSEUDO-ECL TERMINATION

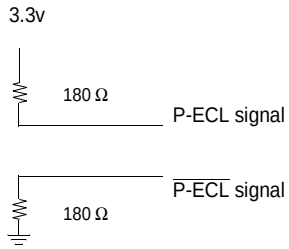
At 155.52 Mbit/s, all interface leads should be treated as transmission lines and must be terminated correctly to avoid problems. The pseudo-ECL leads must be terminated into 50 ohm loads. Figure 29 shows the method of terminating the pseudo-ECL leads. For optimum performance, the termination networks should be located as close as possible to the destination end of the trace. A suggested reference for PCB design information can be found in the Motorola MECL System Design Handbook.

Figure 29. Termination of Pseudo-ECL Leads



The figure shown below illustrates the circuit that should be used for on unused P-ECL terminations.

Figure 30. Connection of an Unused P-ECL Lead



CLOCK RECOVERY

The Clock Recovery block is bypassed when control lead CRBYP is high. In this mode of operation, the receive pseudo-ECL serial interface will consist of the following input signals: a true and complement receive clock (RXSCT and $\overline{\text{RXSCC}}$) which has a clock rate of 155.52 MHz, and true and complement receive data (RXSDT and $\overline{\text{RXSDC}}$). Data (RXSDT) is clocked into the PHAST-3N on rising edges of the clock (RXSCT).

The Clock Recovery block is enabled when control lead CRBYP is low. The pseudo-ECL serial interface will consist of the following input signals: true and complement receive data (RXSDT and $\overline{\text{RXSDC}}$). A 19.44 MHz clock will be recovered from the RXSDT and $\overline{\text{RXSDC}}$ signal leads. The RXSCT and $\overline{\text{RXSCC}}$ leads must be left floating.

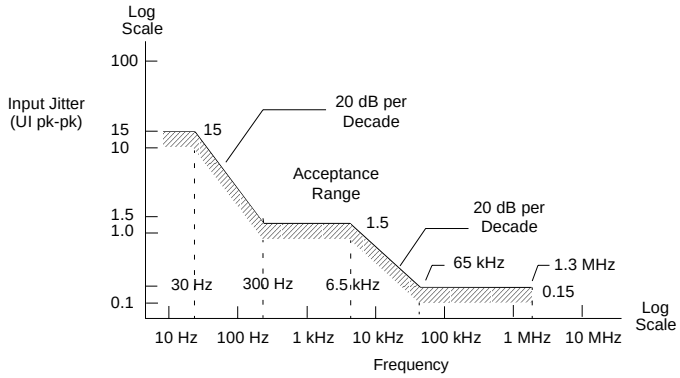
The Clock Recovery block has the following leads in addition to the P-ECL data leads: RRTNV, REXT and RRTNG. These leads are used to connect an external bias resistor and de coupling capacitor to the internal PLL as shown in Figure 32 on page 81.

The clock recovery circuit operates in two modes. In frequency acquisition mode the recovery PLL is locked to a reference 19.44 MHz clock source. The clock reference is connected to lead CRREF. This clock may be connected to the clock synthesis block reference clock (CKREF) for non-looped timing applications. Once near the correct frequency, the PLL enters the data recovery mode in which the PLL phase locks to the incoming data pattern at 155.52 MHz. The frequency acquisition mode is forced if the VCO frequency is more than 1000 ppm from the reference frequency (RROOL alarm, bit 2 in register 01E/01FH). The data recovery mode is forced when the VCO frequency is within 250 ppm of the reference frequency.

The clock recovery circuit has been designed to acquire lock with an average transition density of four bit intervals and to hold the data acquisition mode over 128-bit data intervals with no transitions (RDOOL alarm, bit 3 in register 01E/01FH).

The Clock Recovery block will meet the input jitter requirements shown in the following diagram.

Figure 31. Clock Recovery Jitter Tolerance

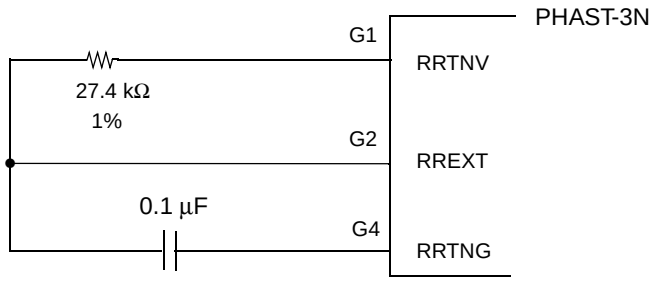


Frequency Range		Tolerated Input Jitter
Low	High	
10 Hz	30 Hz	15.0 UI (UI=1/155.52 MHz or 6.43 ns)
300 Hz	6.5 kHz	1.5 UI
65 kHz	1.3 MHz	0.15 UI

Clock Recovery External Component Connections

The following diagram shows the external connections required for the Clock Recovery block.

Figure 32. Clock Recovery External Component Connections



Note: Locate the above external components as close as possible to the leads.

CLOCK SYNTHESIS

The Clock Synthesis block is bypassed when control lead CSBYP is high. In this mode of operation, the transmit pseudo-ECL serial interface will consist of the following signals: a true and complement transmit input clock (TXCIT and $\overline{\text{TXCIC}}$), output clock (TXSCT and $\overline{\text{TXSCC}}$), and output data (TXSDT and $\overline{\text{TXSDC}}$). Data (TXSDT) is clocked out of the PHAST-3N on falling edges of the clock (TXSCT).

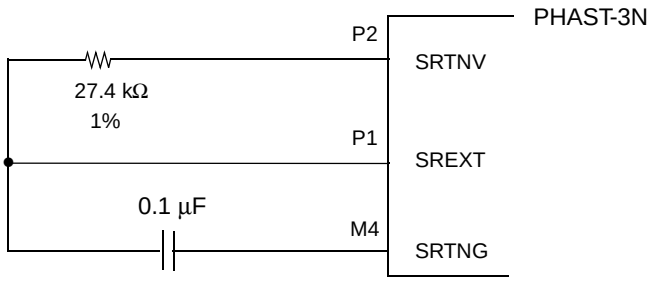
The Clock Synthesis block is enabled when control lead CSBYP is low. The pseudo-ECL serial interface will consist of the following signals: true and complement output data (TXSDT and $\overline{\text{TXSDC}}$), and true and complement output clock (TXSCT and $\overline{\text{TXSCC}}$). The pseudo-ECL clock will be synthesized from a 19.44 MHz clock that is applied to the CKREF lead. This clock may tied together with the clock recovery 19.44 MHz reference (CRREF) for non-looped timing applications. See Figure 28 on page 73.

The Clock Synthesis block has the following leads in addition to the P-ECL data leads: SRTNV, SREXT, and SRTNG. These leads are used to connect an external bias resistor and de coupling capacitor to the internal PLL, as shown in Figure 32.

Clock Synthesis External Component Connections

The following diagram shows the external connections required for the Clock Synthesis block.

Figure 33. Clock Synthesis External Component Connections



Note: Locate the above external components as close as possible to the leads.

DISABLING OF SCRAMBLER AND DESCRAMBLER IN SERIAL MODE

This mode is intended to support STS-3/STM-1 switching back planes, where 155.52 MHz data and clock are present. It is enabled when SCRMD (bit 7, register 00CH) is a 1 and SERIAL (Lead No. K1) is set to a high state.

On the line side, the PHAST-3N has the capability to transmit and receive an unscrambled serial SDH/SONET signal. A scrambled signal guarantees a high density of transitions for the loss of signal detection circuit and the clock recovery circuit. When SCRMD =1, and the descrambler is disabled, then the loss of signal detection circuit is automatically disabled (no RLOS indication possible) and the clock recovery circuit must be bypassed by setting CRBYP (Lead No. H3) to a high state. Both data (RXSDT and $\overline{\text{RXSDC}}$) and 155.52 MHz clock (RXSCT and $\overline{\text{RXSCC}}$) must be provided.

Items to note:

1. The receive loss of clock (RLOC) detection circuit is still active and monitors the status of the 155.52 MHz clock (RXSCT and $\overline{\text{RXSCC}}$).
2. Always apply a RESETS (bit 7, register 00AH) after setting SCRMD to a 1 to clear out any RLOS alarm that may have been present.

DISABLING OF SONET TRANSPORT OVERHEAD AND SDH SECTION OVERHEAD BYTE PROCESSING

There may be applications in which the PHAST-3N will be configured in a higher order SDH/SONET multiplexer system. In those applications the higher order multiplexer will perform the TOH/SOH processing (B2 BIP check and generation, etc.). When a high is placed on the input lead $\overline{\text{TOHENB}}$, the following actions are taken within the PHAST-3N:

In the receive direction the following TOH/SOH byte processes are disabled:

- J0 alarms and processing forced off
- B1 counter turned off
- B2 counter and BER measurement turned off
- TOH/SOH RAM locations except H1/H2 are disabled. The A1/A2 locations are forced to F628H while all other TOH/SOH locations are forced to 00H.
- Line REI counter turned off
- Descrambling can be enabled or disabled through the control bit SCRMD (bit 7, register 00CH)

The following TOH/SOH byte interfaces are forced low:

- TOH/SOH interface leads (RTOHD, RTOHF, RTOHM and RTOHC)
- APS interface leads (RAPSD, RAPSC and RAPSF)
- E1 interface leads (RE1D, ROWC and ROWF)
- E2 interface leads (RE2D, ROWC and ROWF)
- Section Data Communication interface leads (RSD and RSC)
- Line Data Communication interface leads (RLD and RLC)

The TOH/SOH Bytes present in the AIP interface are turned off:

- The TOH/SOH bytes are forced to 0

At the receive terminal interface:

- The H1/H2 bytes are present
- The A1/A2 bytes are forced to F628H
- All other TOH/SOH bytes are forced to 00H

Please note: The A1/A2 byte frame pattern bytes must be present for the serial interface to function properly. The RLFI frame pulse must be present for the parallel interface to function properly. The H1/H2 bytes must be present for path level processing.

In the transmit direction the following actions are taken:

- Insertion of bytes from the TOH/SOH RAM locations into the transmit frame is disabled.
- Scrambling can be enabled or disabled through the control bit SCRMD (bit 7, register 00CH).
- Other than the frame pattern and the H1/H2 bytes, the TOH bytes are transmitted as zeros.
- Insertion of states from the AIP is disabled.
- Insertion of line AIS and line RDI is disabled.

The following TOH/SOH byte interfaces are forced low:

- TOH/SOH Interface (TTOHD disabled, TTOHF, TTOHM, and TTOHC)
- APS Interface (TAPSD disabled, TAPSC and TAPSF)
- E1 Byte Interface (TE1D disabled, TOWF and TOWC)
- E2 Byte Interface (TE2D disabled, TOWF and TOWC)
- Section Data Communication Interface (TSD disabled, and TSC forced low)
- Line Data Communication Interface (TLD disabled, and TLC forced low)

RECEIVE POINTER TRACKING

The H1 and H2 bytes in the STM-1 AU-4 (STS-3c) format are used to determine the starting location of the J1 byte and the payload bytes in the VC-4 (SPE) format. In the STS-3 (STM-1 AU-3) format there are three H1/H2 bytes which are used to determine the location of the individual J1 bytes in each of the three STS-1s (AU-3s).

The STM-1 AU-4 (STS-3c) pointer byte sequence is shown below:

H1	Y	Y	H2	1*	1*	H3	H3	H3

Y = 1001ss11, where ss-bits in Y are normally equal to 00.
1* = all ones byte (FFH)

The STS-3 (STM-1 AU-3) pointer byte sequence is shown below:

H11	H12	H13	H21	H22	H23	H31	H32	H33

H11 and H21 correspond to STS-1 Number 1 (or AU-3 A)
H12 and H22 correspond to STS-1 Number 2 (or AU-3 B)
H13 and H23 correspond to STS-1 Number 3 (or AU-3 C)

The pointer value has a binary number with the range 0 to 782 Decimal. The pointer value indicates the offset value, in three-byte increments, between the pointer and the first byte of the VC-4, or STS-1. For example, for an STM-1 AU-4 format, a pointer value of 0 indicates that the VC-4 starts in the byte location that immediately follows the H3 byte, whereas an offset value of 87 indicates that the VC-4 starts three bytes after the K2 byte.

H1 Byte								H2 Byte							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
N	N	N	N	S	S	I	D	I	D	I	D	I	D	I	D

I = Increment bit
D = Decrement bit
N = New Data Flag bit (1001= enabled, 0110 = disabled)
SS = Size bits

The received H1 and H2 bytes are interpreted for:

- Receive Loss Of Pointer
- Receive path AIS
- Receive new pointer
- Pointer decrements and increments
- False concatenation

Three pointer tracking state machines are provided in the PHAST-3N for the three STS-1s (AU-3s). For STM-1 AU-4 (STS-3c) operation one state machine is enabled. The output of the pointer tracking state machine(s) is a single J1 pulse and SPE indication for an STM-1 VC-4 signal, or three J1 pulses and three SPE indications for each of the three AU-3s/STS-3 STS-1s. In addition, the pointer bytes are forwarded to the pointer justification block for calculating a new pointer.

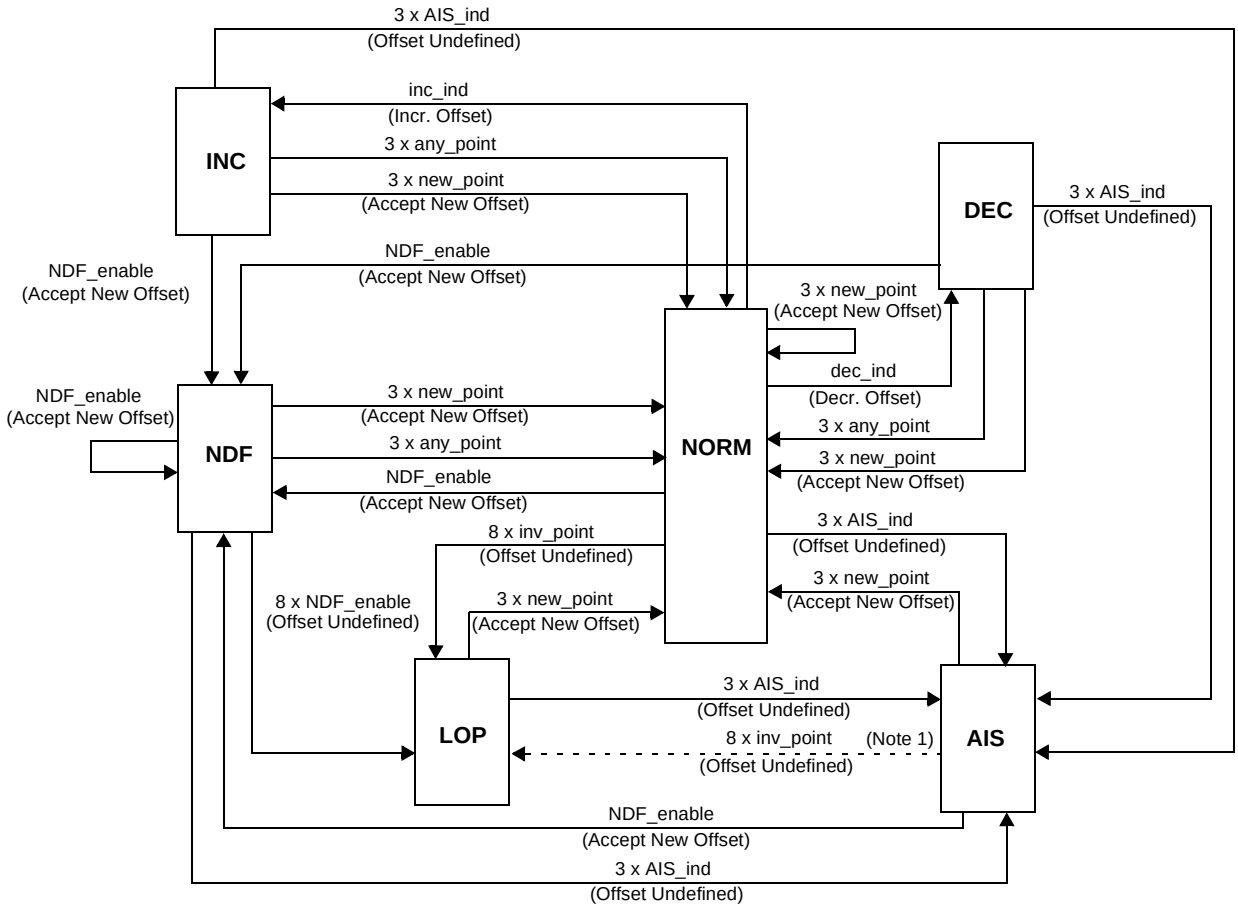
When the PHAST-3N is programmed to interface with the STM-1 AU-4 (STS-3c) format, the concatenation indications, consisting of the Y bytes and 1s bytes, will be monitored (i.e., in the pointer row) for a false concat-

enation indication. A Y and 1s byte-pair value not equal to 1001ss11 11111111 and 1001ss11 11111111 for both occurrences in four or more consecutive frames will result in a false concatenation indication (RFHID). Recovery will occur when values equal to 1001ss11 11111111 and 1001ss11 11111111 are detected for four or more consecutive frames. This alarm indicates that the incoming format is an STS-3 format, and not an STM-1 AU-4 (STS-3c) format. Please note that the ss bits are undefined in the ITU-T recommendation and are assumed to be set to 00.

When the PHAST-3N is programmed to interface with an STS-3 (STM-1 AU-3) format a value equal to 10010011 11111111 in the H12 and H22 locations or 10010011 11111111 in the H13 and H23 locations will result in a receive LOP alarm for STS-1 No. 2 and STS-1 No. 3. When the two LOP alarms are detected, the H12, H22, H13 and H23 bytes will be checked. If the H12, H22, H13 and H23 bytes are equal to 1001ss11 11111111 1001ss11 11111111, a false concatenation indication (RFHID) will be declared. Recovery occurs when LOP has recovered. This alarm indicates that the incoming format is an STM-1 AU-4 (STS-3c) format, and not an STS-3 format. Please note that the ss bits are undefined in ITU-T Recommendations and are assumed to be set to 00 for the STM-1 format.

The pointer tracking state machine shown in Figure 34 is implemented within the PHAST-3N. This state machine is the state machine specified in the ETS 300 417 document.

Figure 34. Pointer Tracking State Machine



Note: The AIS to LOP transition is enabled by control bit PTALE (bit 4 of register 401H)

Pointer Tracking State Machine States Definition

Event	Definition
norm_point	Disabled NDF (0110, 1110, 0010, 0100, 0111) AND match of SS-bits when enabled AND receive pointer offset value equal to active offset value.
NDF_enable	NDF enabled (1001, 0001, 1101, 1011, 1000) AND match of SS-bits when enabled AND received pointer offset value in range.
AIS_ind	pointer = 11111111 11111111 (FF Hex, FF Hex)
inc_ind	NDF disabled (0110, 1110, 0010, 0100, 0111) AND match of SS-bits when enabled AND a match of 8 or more of the 10 I and D bits. Please note that this requirement differs from the majority of I bits inverted and no majority of D bits received.
dec_ind	NDF disabled (0110, 1110, 0010, 0100, 0111) AND match of SS-bits when enabled AND a match of 8 or more of the 10 I and D bits. Please note that this requirement differs from the majority of D bits inverted and no majority of I bits received.
inv_point	Not norm_point AND NOT NDF_enable AND NOT AIS_ind AND NOT {(inc_ind or dec_ind) AND norm_state}.
8 x NDF_enable	8 consecutive NDF_ enable.
3 x AIS_ind	3 consecutive AIS_ind.
3 x any_point	3 x NOT NDF_enable AND NOT 3 x AIS_ind AND NOT 3 x new_point.
new_point	Disabled NDF (0110, 1110, 0010, 0100, 0111) AND match of SS-bits when enabled AND receive pointer offset value in range but not equal to the active offset value.
3 x new_point	3 consecutive new_point received.

Notes:

1. The active offset value is defined as the accepted current phase of the VC-4/STS-1s in the state norm_state and is undefined in other states.
2. NDF Enabled is defined as one of the following bit patterns: 1001, 0001, 1101, 1011, 1000.
3. NDF Disabled is defined as one of the following bit patterns: 0110, 1110, 0010, 0100, 0111.
4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100 and 1111) result in an inv_point indication. The NDF code 1111 does not result in an inv_point indication if it is part of an AIS_ind.
5. Note that the new_point is also an inv_point.
6. 3 x new_point takes precedence over other events.
7. The second and third offset value received in 3 x new_point must be identical with the first.
8. The consecutive new_point counter is reset to 0 on a change of state, except for transitions occurring among the INC, DEC, NDF and NORM states.
9. The consecutive inv_point counter can be incremented in all states. The consecutive inv_point counter is not reset on a change of state.
10. The consecutive AIS_ind counter is not reset on a change of state.
11. The consecutive NDF_enable counter is reset to zero on a change of AIS to NDF state. Otherwise the counter is not reset.
12. Inc_ind/dec_ind causes the active offset value to be incremented/decremented, respectively. The subsequent detection of a 3 x new_point with an offset value equal to the offset value caused by inc_ind/dec_ind will not cause the new pointer flag (RnNPTR) to assert.

The values of the size (SS)-bits used in the pointer tracking state machine detection circuitry, and the resulting actions, are shown in the following table. Please note that the ITU-T position regarding the use of the size bits in the state machine has changed. They are no longer required. However, the PHAST-3N provides a number of options for using the size bits in the state machine. The following table lists the various options that are available.

PSBEN (bit 7, 401H)	**SBIT1** (bit 6, 401H)	**SBIT0** (bit 5, 401H)	**Action**
0	X	X	SS-bit check in pointer tracking state machine(s) is disabled. Pointer tracking state machine(s) ignore(s) the SS-bits in the transition state definitions.
1	0	0	SS-bit check in pointer tracking state machine(s) is enabled. Pointer tracking state machine(s) include(s) the SS-bits in the transition state definitions. The SS-value will be 00.
1	0	1	SS-bit check in pointer tracking state machine(s) is enabled. Pointer tracking state machine(s) include(s) the SS-bits in the transition state definitions. The SS-value will be 01.
1	1	0	SS-bit check in pointer tracking state machine(s) is enabled. Pointer tracking state machine(s) include(s) the SS-bits in the transition state definitions. The SS-value will be 10.
1	1	1	SS-bit check in pointer tracking state machine(s) is enabled. Pointer tracking state machine(s) include(s) the SS-bits in the transition state definitions. The SS-value will be 11.

SS-bit Control Bit Selection

A control bit (PTALE) is also provided for enabling/disabling the AIS to LOP transition.

PTALE (bit 4, 401H)	**Action**
0	The AIS to LOP transition is disabled.
1	The AIS to LOP transition is enabled.

Pointer Tracking State Machine Control Bit Selection

RECEIVE J0 AND J1 BYTE PROCESSING

The PHAST-3N provides several options for processing the J0 and J1 bytes. The J0 byte can be assigned to carry either a single-byte (ANSI applications) or a 16-byte message as specified in ETSI/ITU-T documents. The programming options available for the J0 byte are shown in the following table.

J0AEN (bit 7, 440H)	**J0S16** (bit 6, 00CH)	**Action**
0	0	The received J0 byte is written into the receive TOH RAM and the first byte of a 16-byte RAM segment for microprocessor read access. The mismatch (J0TIM and J0LOL) alarms are disabled.
1	0	The received J0 byte is written into the receive TOH RAM and compared against the fist byte of the microprocessor-written 16-byte message. The mismatch is reported as a mismatch (J0TIM) alarm.
0	1	The received J0 bytes are written into a 16-byte RAM segment on a rotating basis with an arbitrary starting address for microprocessor read access. The Loss of Lock (J0LOL) and Mismatch (J0TIM) alarms are disabled.
1	1	The received J0 bytes are valid in a 16-byte RAM segment after it has been aligned to the multiframe pattern (100....). A comparison between the aligned message and the microprocessor-written 16 byte message is performed. The first byte of the microprocessor-written message is written into the starting location for the 16-byte message. The Loss of Lock (J0LOL) and Mismatch (J0TIM) alarms are enabled. Please note that the PHAST-3N does not calculate a CRC-7.

J0 (C1) Receive Byte Selection

The programming options available for the J1 byte are shown in the following table. For STM-1 AU-4 (STS-3c) operation, n is equal to 1. The control bits for n equal to 2 and 3 are disabled. For the STS-3/STM-1 AU-3 format n corresponds to 1, 2 or 3, which corresponds to the like-numbered STS-1 or AU-3 A, B and C.

J1nS1 (bit 7, 00EH)	**J1nS0** (bit 6, 00EH)	**Action**
0	0	J1 segment is configured for a 64-byte message. Received bytes are written into the assigned RAM segment on a rotating basis, starting with an arbitrary address, for microprocessor read access. No comparison is performed. The J1 alarms (J1nLOL and J1nTIM) are disabled.
0	1	J1 segment is configured for a 64-byte message. Reception of an ASCII CR/LF sequence will synchronize an internal counter so that the next J1 byte after the last LF is written into the starting address location of the RAM segment. No microprocessor comparison is performed. The J1 alarms (J1nLOL and J1nTIM) are disabled.
1	0	J1 segment is configured for a 16-byte message. Received bytes are written into their assigned 16-byte segment on a rotating basis, starting with an arbitrary address, for microprocessor read access. The J1 alarms (J1nLOL and J1nTIM) are disabled.
1	1	J1 segment is configured for a 16-byte message and comparison. The received message is valid in a 16-byte RAM segment after it has been aligned to the multiframe pattern (100....). A comparison between the aligned message and the microprocessor-written 16 byte message is performed. The first byte of the microprocessor-written message is written into the starting location for the 16-byte message. The Loss of Lock and mismatch (J1nLOL and J1nTIM) alarms are enabled. Please note that the PHAST-3N does not calculate a CRC-7.

J1 Message Selection

The 16-byte message consists of an alignment signal of (10000000 00000000) in the most significant bit (bit 1) of each byte. The rest of the first byte carries a CRC-7. The remaining seven bits in each subsequent byte carry a data message, as illustrated in the diagram below. Please note that the PHAST-3N does not perform the CRC-7 calculation.

Bit	1	2	3	4	5	6	7	8
1	CRC-7							
0	J0 or J1 Message							
0								
0								
0								
0								
0								
0								
0								
0								
0								
0								
0								
0								
0								

J0/J1 Message Format

The J0/J1 16-byte message comparison works according to the following steps:

1. Assume that the J0/J1 detectors are out of lock and there is no mismatch alarm
2. A 16-byte J0/J1 TIM message is written into the applicable microprocessor-written compare segment.
3. The incoming multiframe pattern is searched for by the J0/J1 comparison circuits.
4. The multiframe pattern is found.
5. The received 16-byte message is then checked for three consecutive 16-byte message repeats.
6. If an error is detected before step 5 has been completed, the sequence repeats, starting with step 3.
7. If the incoming 16-byte message repeats three times in a row after the multiframe pattern is detected, without an error, an in-lock condition exists and the J0/J1 loss of lock alarm is reset. Note that the received J0/J1 segment (460H-46FH for J0; X70H-X7FH for J1) is valid only after lock is achieved.
8. This receive segment is compared against the microprocessor-written message, byte for byte, for 16 bytes. If they match, a match is declared. The mismatch alarm is reset. If they do not compare, a mismatch alarm is declared.
9. If the microprocessor writes a new byte, a J0/J1 mismatch alarm will occur (J0/J1TIM) because the receive message is stable but there is a mismatch between the two segments.
10. If the receive message changes for three consecutive 16-byte messages, an out of lock alarm is declared, and the mismatch alarm is reset.
11. The sequence repeats.

RECEIVE C2 BYTES

The received value of the C2 byte in the VC-4 format and the values of the three C2 bytes in the STS-3/AU-3 format are monitored for a C2 mismatch alarm, an unequipped alarm, PDI, a payload defect indication (ANSI) and a VC AIS status (ETSI).

Mismatch and PDI Detection

For STM-1 AU-4 (STS-3c) operation, the received C2 value is compared against a microprocessor-written value in register X58H. Also included in the mismatch detection is the option to select PDI detection and the fixed value equal to 01H. The PDI codes are defined as EYH or FXH (where Y = 1 to F and X = 0 to C). The following table defines the control bit states for mismatch and PDI detection. The value of n is equal to 1 for the STM-1 VC-4 (STS-3c SPE) format, and it is equal to 1, 2 or 3 for the STS-3 STS-1 (STM-1 AU-3) format.

C2CID (bit 3, 440H)	C2PID (bit 2, 440H)	Action
0	0	The received C2 byte is compared against the microprocessor-written value in register X58H and the 01H, EYH and FXH values. The mismatch alarm C2nMM is set if a match to 01H or the microprocessor-written value is not detected in five or more consecutive comparisons. The PDI alarm C2nPDI is set if the incoming C2 value matches the PDI codes of EYH or FXH in five or more consecutive comparisons. In either case, recovery occurs when five or more consecutive comparisons do not indicate the alarm conditions.
0	1	The received C2 byte is compared against the microprocessor-written value and the 01H value. The mismatch alarm C2nMM is set if a match to 01H or the microprocessor-written value is not detected in five or more consecutive comparisons. The PDI alarm C2nPDI is disabled. C2nMM alarm recovery occurs when five or more consecutive comparisons do not indicate the alarm conditions.
1	0	The received C2 byte is compared against the microprocessor-written value and the EYH and FXH values. The mismatch alarm C2nMM is set if a match to the microprocessor-written value is not detected in five or more consecutive comparisons. The PDI alarm C2nPDI is set if the incoming C2 value matches the PDI codes of EYH or FXH in five or more consecutive comparisons. In either case, recovery occurs when five or more consecutive comparisons do not indicate the alarm conditions.
1	1	The received C2 byte is compared against the microprocessor-written value. The mismatch alarm C2nMM is set if a match to this value is not detected in five or more consecutive comparisons. The PDI alarm C2nPDI is disabled. C2nMM alarm recovery occurs when five or more consecutive comparisons do not indicate the alarm conditions.

C2 Mismatch and PDI Detection Control Bit Selection

The 01H value represents an equipped-nonspecific payload code, while the EYH and FXH codes represent PDI codes defined in the Bellcore documents. Other than reporting the C2nPDI alarm, no action is taken by the PHAST-3N. It is the responsibility of the microprocessor to read the C2 byte when a C2nPDI alarm has occurred to determine the PDI value.

The C2 mismatch and C2 PDI detection circuits are inhibited (except as noted) when:

- All ones are received (used for VC AIS detection) - Note: does not apply for C2 PDI detection
- The unequipped status alarm UNEQn is active for n - Note: does not apply for C2 PDI detection
- The receive loss of signal alarm RLOS is active
- The receive loss of frame alarm RLOF is active
- The external SDH/SONET line failure alarm SLFAIL is active
- The receive line AIS alarm RLAIS is active
- The receive path AIS alarm RnPAIS is active
- The receive loss of pointer alarm RnLOP is active

Unequipped Detection

The C2 byte is checked for an unequipped status indication. An unequipped status alarm UNEQn occurs when the received C2 byte is equal to 00H for five or more consecutive frames. This alarm is terminated when five or more consecutive values that are not equal to 00H are received. The unequipped status detection circuit is inhibited when:

- The receive loss of signal alarm RLOS is active
- The receive loss of frame alarm RLOF is active
- The external SDH/SONET line failure alarm SLFAIL is active
- The receive line AIS alarm RLAIS is active
- The receive path AIS alarm RnPAIS is active
- The receive loss of pointer alarm RnLOP is active

VC AIS Detection

The C2 byte is checked for a VC AIS indication. A VC AIS alarm VCnAIS occurs when the received C2 byte is equal to FFH for five or more consecutive frames. This alarm is terminated when five or more consecutive values that are not equal to FFH are received. The VC AIS detection circuit is inhibited when:

- The receive loss of signal alarm RLOS is active
- The receive loss of frame alarm RLOF is active
- The external SDH/SONET line failure alarm SLFAIL is active
- The receive line AIS alarm RLAIS is active
- The receive path AIS alarm RnPAIS is active
- The receive loss of pointer alarm RnLOP is active

Receive H4 Byte Loss of Multiframe Detection and Generation

The H4 byte is used to identify the location of the V1/V2 pointer bytes for low order tributaries (e.g., TU-11s/VT1.5s), as shown in the following table. In the receive direction, the states of bits 1 through 6 are passed through the PHAST-3N to the terminal without further processing.

	Bit	1	2	3	4	5	6	7	8	Action
Frame	n	X	X	X	X	X	X	0	0	Generate V1 pulse in frame n+1
	n+1	X	X	X	X	X	X	0	1	
	n+2	X	X	X	X	X	X	1	0	
	n+3	X	X	X	X	X	X	1	1	

RECEIVE TERMINAL SIDE AIS GENERATION

The PHAST-3N provides the ability to generate a terminal side line AIS, path AIS, or a TranSwitch-defined path AIS, using local alarms, when enabled, or the microprocessor. The generation of receive line AIS and path AIS will use the receive line clock signal RLCI or the internal derived 19.44 MHz clock when the receive retiming circuit is bypassed (control bit RTBYP, bit 4 in register 402H, is a 1) or the RRCI clock when the receive retiming circuit is enabled (control bit RTBYP is a 0).

The generation of path AIS is programmable for each of the STS-1s (STM-1 AU-3s). The generation of AIS downstream is accomplished in a hierarchical fashion. At the top of the hierarchy, the microprocessor can generate line AIS, or path AIS (and a TranSwitch-defined path AIS if selected), at any time, independent of the alarms. The following microprocessor control bits determine the generation of AIS:

- Control bit SLAIS (bit 3 register 445H); a 1 written by the microprocessor generates line AIS
- Control bit SnPAIS (bit 3 register X40H); a 1 written by the microprocessor generates path AIS for the numbered STS-3 STS-1 selected or the STM VC-4.

In the next level of the hierarchy, global control bits are provided that enable specified alarms when they are enabled (i.e., mask bits turned off) to generate line AIS, path AIS, or a TranSwitch defined path AIS. The following table is a summary of those global AIS enable bits, where X = don't care (representing either the 0 or 1 states), n is equal to 1 for the STM-1 AU-4 (STS-3c) format, and n is equal to 1, 2 or 3 for each of the STS-1s in the STS-3 format. The control bits for n equal to 2 and 3 are disabled (don't care) for the STM-1 AU-4 (STS-3c) format.

RLAISE (bit 0, 441H)	PnAISE (bit 2, X01H)	RnAISE (bit 1, X01H)	Action		
			Line AIS	Path AIS	TranSwitch Defined Path AIS
0	0	0	**---**	**---**	**---**
1	0	0	**enabled**	**---**	**---**
0	1	X	**---**	**enabled**	**---**
0	0	1	**---**	**---**	**enabled**
1	1	X	**enabled**	**enabled**	**---**
1	0	1	**enabled**	**---**	**enabled**

--- = disabled

Summary of AIS Global Enable Bits

At the bottom of the hierarchy are the individual alarms. Most, but not all, alarms are also provided with enable AIS control bits. Thus, an individual alarm may be disabled from generating line or path AIS downstream, even through a global control bit for the AIS generation may be enabled. In all cases, the microprocessor has full control over the generation of the AIS type.

Receive Line AIS Generation

Line AIS is generated by forcing all line overhead bytes (H1, H2, H3, B2, K1, K2, D4-D12, Z1, Z2, E2 and all unused bytes) and the bytes in the VC-4/STS-1s SPE (POH and payload bytes) to an all ones state. The data will be provided unscrambled at the terminal interface. When line AIS is generated, the C1J1V1 indication and SPE indication will remain fixed to the states they were in before line AIS was generated.

The following conditions or alarms will generate line AIS. In addition, an out-of-band AIS indication on lead RTFAIL is provided.

- When the line AIS enable control bit (RLAISE) is a 1 and any of the following conditions occur:
  - Receive loss of frame alarm (RLOF)
  - Receive loss of signal alarm (RLOS)
  - Receive loss of clock alarm (RLOC) when control bit RTBYP is a 0
  - External SDH/SONET Line Failure (SLFAIL) alarm
  - Receive B2 bit error alarm (B2BER) when control bit B2AISE is a 1
  - Receive J0 loss of lock alarm (J0LOL) when control bit J0AISE is a 1
  - Receive J0 Trace ID Message (J0TIM) when control bit J0AISE is a 1
  - Microprocessor writes a 1 to send line AIS control bit (SLAIS)
- When the line AIS enable control bit (RLAISE) is a 0 and any of the following conditions occur:
  - Microprocessor writes a 1 to send line AIS control bit (SLAIS)

Receive Path AIS Generation

Receive path AIS is defined as all ones carried in the H1/H2 pointer bytes, the POH bytes, and the payload bytes. Path AIS is generated for the VC-4 when n is equal to 1, and for any one or more of the three STS-1s (where n is equal to 1, 2 or 3 for the like-numbered STS-1) for the alarms that are specified below. Upon release of a receive path AIS, an NDF will be sent followed by the previous value of the pointer, provided a new pointer has not been received. Note: the J1 pulse, SPE indication, and SPE will remain fixed, and will not jump to a new location when receive path AIS is enabled. Upon release of the path AIS, the J1 pulse, SPE indication and SPE are allowed to assume a new pointer location.

The conditions for sending a path AIS, and for providing a receive terminal fail indication (RTFAIL) are:

- When the path AIS enable control bit (PnAISE) is a 1:
  - Receive loss of signal alarm (RLOS)
  - Receive loss of frame alarm (RLOF)
  - Receive line AIS alarm (RLAIS)
  - External SDH/SONET line failure (SLFAIL) alarm
  - Receive J0 loss of lock alarm (J0LOL) when J0AISE is a 1
  - Receive J0 Trace ID Message (J0TIM) when J0AISE is a 1
  - Receive B2 bit error alarm (B2BER) when B2AISE is a 1
  - Receive loss of pointer alarm (RnLOP)
  - Receive path AIS alarm (RnPAIS)
  - Receive FIFO alarm (RnFIFO) when FRENB and RFAISE are a 1 (path AIS will be generated for a minimum of 3 frames)
  - Control bits RFnRST and RFAISE are a 1 (path AIS will be generated for a minimum of 3 frames)
  - Externally generated AIS/RDI indication ($\overline{\text{FAIS}}$n lead is low) and control bit EXTAIS is a 1
  - Receive loss of multiframe alarm (RnLOM) when control bit H4AISE is a 1
  - Receive C2 mismatch alarm (C2nMM) when control bit C2AISE is a 1
  - Receive Unequipped alarm (UNEQn) when control bit UQAISE is a 1
  - Receive VC AIS alarm (VCnAIS) when control bit VCAISE is a 1
  - Receive J1 Loss Of Lock alarm (J1nLOL) when control bit J1AISE is a 1
  - Receive J1 Trace ID Mismatch alarm (J1nTIM) when control bit J1AISE is a 1
  - Receive B3 bit error alarm (B3nBER) when control bit B3AISE is a 1
  - Receive TC AIS alarm (RTCAIS) when control bit TCAISE is a 1
  - Receive TC loss of frame alarm (TCLOF) when control bit TCMSAE is a 1
  - Receive TC unequipped alarm (TCUQ) when control bit TCMSAE is a 1
  - Receive TC message loss of lock alarm (TCLOL) when control bit TCTSAE is a 1
  - Receive TC message mismatch alarm (TCTIM) when control bit TCTSAE is a 1
  - Microprocessor writes a 1 to send path AIS control bit (SnPAIS)
- When path AIS enable control bit (PnAISE) is a 0:
  - Microprocessor writes a 1 to send path AIS control bit (SnPAIS)

TranSwitch-Defined Path AIS Generation

The TranSwitch-defined path AIS signal consists of the pointer bytes, H1 and H2, being equal to 522, zeros in the H3 byte, and ones in the entire payload, including the POH bytes, except for the H4 byte. The contents of the H4 byte will contain the two-bit H4 count from the internal H4 tracking machine. The RPOH signal will be forced low, and the fail indicator (RTFAIL) will not be active during the H4 times and H1/H2 byte times. The intent of this signal is to generate the “skeleton” of a payload with sufficient timing information after an input failure. When the AIS condition is released, NDF is sent once, followed by a normal pointer (same as if no pointer movement took place). The J1 pulse will jump when internal AIS is selected, and will jump back to the normal pointer location after the release of path AIS.

When the TranSwitch-defined path AIS occurs, the H4 byte at the terminal interface will continue to run (free-wheel). There is no guarantee that the H4 byte value will be the next value in the multiframe sequence. The H4 byte value at the terminal interface is derived from a multiframe generator, which is locked to the input H4. The conditions for sending this AIS are described below:

- When the receive AIS enable control bit (RnAISE) is a 1 and the path AIS enable control bit (PnAISE) is a 0:
  - Receive loss of signal alarm (RLOS)
  - Receive loss of frame alarm (RLOF)
  - Receive line AIS alarm (RLAIS)
  - External SDH/SONET line failure (SLFAIL) alarm
  - Receive J0 loss of lock alarm (J0LOL) when J0AISE is a 1
  - Receive J0 Trace ID Message (J0TIM) when J0AISE is a 1
  - Receive B2 bit error alarm (B2BER) when B2AISE is a 1
  - Receive loss of pointer alarm (RnLOP)
  - Receive path AIS alarm (RnPAIS)
  - Receive FIFO alarm (RnFIFO) when RFAISE=1
  - Externally generated AIS/RDI indication ($\overline{\text{FAISn}}$ lead is low) and control bit EXTAIS is a 1
  - Receive loss of multiframe alarm (RnLOM) when control bit H4AISE is a 1.
  - Receive C2 mismatch alarm (C2nMM) when control bit C2AISE is a 1
  - Receive Unequipped alarm (UNEQn) when control bit UQAISE is a 1
  - Receive VC AIS alarm (VCnAIS) when control bit VCAISE is a 1
  - Receive J1 Loss Of Lock alarm (J1nLOL) when control bit J1AISE is a 1
  - Receive J1 Trace ID Mismatch alarm (J1nTIM) when control bit J1IASE is a 1
  - Receive B3 bit error alarm (B3nBER) when control bit B3AISE is a 1
  - Receive TC AIS alarm (RTCAIS) when control bit TCAISE is a 1
  - Receive TC loss of frame alarm (TCLOF) when control bit TCMSAE is a 1
  - Receive TC unequipped alarm (TCUQ) when control bit TCMSAE is a 1
  - Receive TC message loss of lock alarm (TCLOL) when control bit TCTSAE is a 1
  - Receive TC message mismatch alarm (TCTIM) when control bit TCTSAE is a 1
  - Microprocessor writes a 1 to send internal path AIS (SnIAIS)
- When the receive AIS enable control bit (RnAISE) is a 0 and the path AIS enable (PnAISE) control bit is a 0:
  - Microprocessor writes a 1 to send internal path AIS control bit (SnIAIS) and the path AIS control bit (SnPAIS) is a 0.

RECEIVE TERMINAL INTERFACE BUS

The terminal-side Telecom Bus bus interface consists of the following output leads:

- Data byte RTDO(7-0),
- Clock RTCO,
- SPE active signal RSPE,
- Composite timing signal RC1J1V1,
- POH indicator signal RPOH,
- Parity bit RTPAR,
- Failure indication (RTFAIL), and a
- Receive bus active indicator signal ($\overline{\text{RTBUSI}}$).

Several bus features are provided, including:

- Ability to force data bus and parity to a high impedance state
- Ability to force TOH unused bytes to 0 or tristate
- Invert the output clock
- Provide the following TOH bytes (A1/A2, H1/H2, and optionally both K1/K2, and E1/E2)

The function of the POH indication pulse is to provide an indication (i.e., marker) for the POH columns, and stuff columns. For the VC-4 format, the POH indication signal (RPOH) is active for the first column, assuming that the J1 byte aligned to a pointer value of 522. For the STS-3 format, the POH indication is active for the first column (POH column) and for the two stuff columns that are designated as columns 30 and 59 in each STS-1, assuming that the STS-1 is aligned to a pointer value of 522.

Parity (RTPAR lead) is calculated according to the states given in the Table below. The receive bus indicator signal ($\overline{\text{RTBUSI}}$) and the failure indication (RTFAIL) are not included in the parity calculation.

RPREV (bit 7, 402H)	**RPRDO** (bit 6, 402H)	**RPPOH** (bit 5, 402H)	**Action**
0	0	0	Odd parity calculated over the RTDO (7-0), RSPE and RC1J1 signals.
0	0	1	Odd parity calculated over the RTDO (7-0), RSPE and RPOH signals.
0	1	X	Odd parity calculated over the RTDO (7-0) and RSPE signals only.
1	0	0	Even parity calculated over the RTDO (7-0), RSPE and RC1J1 signals.
1	0	1	Even parity calculated over the RTDO (7-0), RSPE, RC1J1 and RPOH signals.
1	1	X	Even parity calculated over the RTDO (7-0) signals only.

Table 5. Parity Control Bit Selection

When control bit RBHZE (bit 2 in register 402H) is a 1, the RTDO(7-0) signals and parity RTPAR are forced to the high impedance state. When control bit RBHZE is a 0, the data bus signals and parity are enabled.

An active high failure indication (RTFAIL) output signal lead is provided. This signal provides an out of band line or path AIS indication (including an internal AIS indication) for the alarms and the conditions that caused the AIS state.

An bus indicator signal ($\overline{\text{RTBUSI}}$) is provided. This signal is active low for the bytes (i.e., time slots) that are active on the bus. This signal may be used for controlling bus drivers.

The ability to invert the output clock (RTCO) is provided. A 1 written to control bit RTCIV (bit 3 in register 402H) causes the receive terminal signals to be clocked out on positive transitions of the clock instead of negative transitions.

The following TOH bytes are provided at the receive terminal interface: the A1 and A2 frame bytes, the H1/H2 pointer bytes, and optionally the K1 and K2 bytes and the E1/E2 bytes. The other TOH bytes (unused, including K1/K2 or E1/E2 when not enabled) are either tristated or set to zero depending upon control bit RTUBZ (bit 1 of register 402H). When RTUBZ is a 1, the data bus and parity are set to a high impedance state for the unused byte positions present on the receive terminal interface.

The PHAST-3N generates the F6F6F6282828H frame pattern for the three A1 and A2 bytes when control bit RTABE (bit 7 in register 445H) is written with a 0. When control bit RTABE is written with a 1, the three A1 and A2 bytes are the values written into memory locations 447H (A1) and 448H (A2) by the microprocessor.

The K1 and K2 bytes may be used by downstream circuitry for APS applications. When control bit RTK1BE (bit 6 in register 445H) is a 1, the line side K1 and K2 bytes are provided as terminal side bytes. When control bit RTK1BE is a 0, the K1/K2 bytes are tristated or forced to zero, as controlled by the RTUBZ control bit.

The receive terminal E1/E2 bytes may be forced to either a tristate or zero level, or contain the line side E1/E2 orderwire bytes. Additionally, the receive terminal E1n bytes can indicate an AIS/RDI status. Control bits RTE1CH (bit 5 of register 445H), RTE1BE (bit 4 of register 445H), and RTUBZ control the operation of the E1/E2 bytes.

RTE1CH (bit 5, 445H)	**RTE1BE** (bit 4, 445H)	**Action**
0	X	The E1 and E2 TOH bytes are either tristated or forced to zero (unless line AIS is generated), depending upon control bit RTUBZ.
1	0	The SONET/SDH line side E1 and E2 orderwire bytes are inserted into the receive terminal side data bit stream. The E12, E13, E23, and E33 byte locations are forced to 0 independent of control bit RTUBZ.
1	1	AIS/RDI indications are sent via the E1n bytes. Path AIS for STS-1 no. 1 and the VC-4 are sent in the E11 byte location. Path AIS for STS-1 no. 2 is sent in the E12 byte location, etc. The E2 byte locations are either tristated or forced to 0, depending upon control bit RTUBZ.

Table 6. Receive Terminal Side E1/E2 Byte Utilization

The bit assignment for the three E1n bytes when assigned to carry alarm information is shown below:

Bit	1(MSB)	2	3	4	5
	LFAULT	E1nPAIS	E1nRAIS	LRDI	LFAULT or E1nPAIS or E1nRAIS or PRDIn

(cont.) Bit	6	7	8(LSB)
	LFAULT or E1nPAIS or E1nRAIS		

LRDI (Line RDI status) is equal to:

- Line RDI alarm (LRDI)

PRDIn (Path RDI status) is equal to:

- Receive Path RDI Old (RnOLD)
- Receive Payload RDI ANSI (RnPYD)
- Receive Server RDI ANSI (RnSVD)
- Receive Connectivity RDI ANSI (RnCND)

LFAULT (Line Fault Failure) is equal to (when control bit RLAISE is a 1):

- Receive loss of signal alarm (RLOS)
- Receive loss of frame alarm (RLOF)
- Receive line AIS alarm (RLAIS)
- External SDH/SONET Line Failure (SLFAIL) alarm when the parallel interface is selected
- Receive J0 loss of lock alarm (J0LOL) when J0AISE is a 1
- Receive J0 Trace ID Message (J0TIM) when J0AISE is a 1
- Receive B2 bit error alarm (B2BER) when B2AISE is a 1
- Control bit SLAIS is a 1 (independent of the control bit RLAISE)

E1nPAIS (Pointer Tracking alarms) is equal to (when control bit PnAISE is a 1 or when PnAISE is a 0 and RnAISE is a 1)

- Receive loss of pointer alarm (RnLOP)
- Receive path AIS alarm (RnPAIS)
- Control bit SnPAIS is a 1 (independent of the enable control bits PnAISE and RnAISE)
- Control bits SnIAIS is a 1 and SnPAIS is a 0 (independent of enable control bits PnAISE and RnAISE)

E1nRAIS (Path alarms) is equal to (when control bit PnAISE is a 1 or when PnAISE is a 0 and RnAISE is a 1)

- Receive FIFO alarm (RnFIFO)
- External Generate AIS/RDI indication ($\overline{\text{FAIS}}$n lead is low) and EXTAIS is a 1
- Receive loss of multiframe alarm (RnLOM) when control bit H4AISE is a 1
- Receive C2 mismatch alarm (C2nMM) when control bit C2AISE is a 1
- Receive Unequipped alarm (UNEQn) when control bit UQAISE is a 1
- Receive J1 Loss Of Lock alarm (J1nLOL) when control bit J1IASE is a 1
- Receive J1 Trace ID Mismatch alarm (J1nTIM) when control bit J1IASE is a 1
- Receive B3 bit error alarm (B3nBER) when control bit B3AISE is a 1
- Receive TC AIS alarm (RTCAIS) when control bit TCAISE is a 1
- Receive TC loss of frame alarm (TCLOF) when control bit TCMSAE is a 1
- Receive TC message loss of lock alarm (TCLOL) when control bit TCTSAE is a 1
- Receive TC message mismatch alarm (TCTIM) when control bit TCTSAE is a 1
- Receive TC unequipped alarm (TCUQ) when control bit TCMSAE is a 1
- Control bit SnPAIS is a 1 (independent of PnAISE and RnAISE)
- Control bit SnIAIS is a 1 and SnPAIS is a 0 (independent of PnAISE and RnAISE)

TRANSMIT TERMINAL INTERFACE BUS

The terminal-side Telecom Bus bus interface consists of the following leads for the normal timing mode. This timing mode is selected using the MODE leads. The normal timing mode enables the Telecom Bus signals as inputs to the PHAST-3N.

- Data byte TTDI(7-0),
- Clock TTCI,
- SPE active signal TSPE,
- Composite timing signal TC1J1V1,
- Parity bit TTPAR.

The Source timing mode is used in applications in which the PHAST-3N provides the timing signals for down-stream circuitry. An external clock (STRCI) and frame reference (STRFI) must be applied. The terminal-side Telecom Bus bus interface consists of the following leads for the source timing mode:

- Data byte input TTDI(7-0),
- Clock output TTCI,
- SPE active output signal TSPE,
- Composite output timing signal TC1J1V1,
- Parity input bit TTPAR,
- POH byte output indication TPOH,
- H4 byte Output Generator.

The POH byte indication is active for the POH times and also for the stuff columns associated with each The H4 byte generator provides a multiframe H4 sequence each frame.

Parity for the normal timing mode is calculated according to the states given in the Table below.

TPREV (bit 7, 022H)	**TPRDO** (bit 6, 022H)	**Action**
0	0	Odd parity calculated over the TTDI (7-0), TSPE and TC1J1 signals.
0	1	Odd parity calculated over the TTDI (7-0) signals.
1	0	Even parity calculated over the TTDI (7-0), TSPE and TC1J1 signals.
1	1	Even parity calculated over the TTDI (7-0) signals

Table 7. Normal Timing Mode Parity Control Bit Selection

Parity for the source timing mode is calculated according to the states given in the Table below. X can be either state.

TPREV (bit 7, 022H)	**TPRDO** (bit 6, 022H)	**Action**
0	X	Odd parity calculated over the TTDI (7-0) signals.
1	X	Even parity calculated over the TTDI (7-0) signals.

Table 8. Source Timing Mode Parity Control Bit Selection

TANDEM CONNECTION OPERATION

The PHAST-3N supports tandem connection operation via the N1 (Z5) byte for ETSI applications. The G.707 Annex D method (STM-1 VC-4) is supported. The ETSI format is shown below:

ETSI Format

VC-4

1	2	3	4	5	6	7	8
IEC				TC REI	TC OEI	TRACE ID TC RDI TC ODI	

Table 9. ETSI Tandem Connection Message Structure

IEC is defined as the Incoming Error Count

TC REI is defined as the tandem connection remote error indication (errored TC block indication)

TC OEI is defined as the VC tandem connection outgoing error indication

TC RDI is defined as the tandem connection remote defect indication

TC ODI is defined as the VC tandem connection outgoing defect indication request

Bits 7 and 8 in the N1 (Z5) byte have the following structure in frames 1 through 76:

ETSI Message Structure		
Frame No.	**N1 (Z5) Byte, Bits 7 and 8 Definition**	
1 - 8	Frame Alignment Signal 1111 1111 1111 1110	
9 - 12 13 - 16 17 - 20 21 - 64 65 - 68 69 - 72	TC Trace ID Byte No. 1 (1 CRC-7) TC Trace ID Byte No. 2 (0 X X X X X X X) TC Trace ID Byte No. 3 (0 X X X X X X X) TC Trace ID Bytes No. 4 - 14 (0 X X X X X X X) TC Trace ID Byte No. 15 (0 X X X X X X X) TC Trace ID Byte No. 16 (0 X X X X X X X)	
73	Reserved (default = 0)	TC RDI
74	TC ODI	Reserved (default = 0)
75	Reserved (default = 0)	Reserved (default = 0)
76	Reserved (default = 0)	Reserved (default = 0)

Table 10. ETSI Tandem Connection Message N1 (Z5) Byte, Bits 7 and 8 Utilization

The tandem connection (TC) feature is controlled independently in the transmit and receive directions, using control bit RTCEN (bit 0 in register 445H) for the receive direction and control bit TTCEN (bit 7 in register 064H) for the transmit direction.

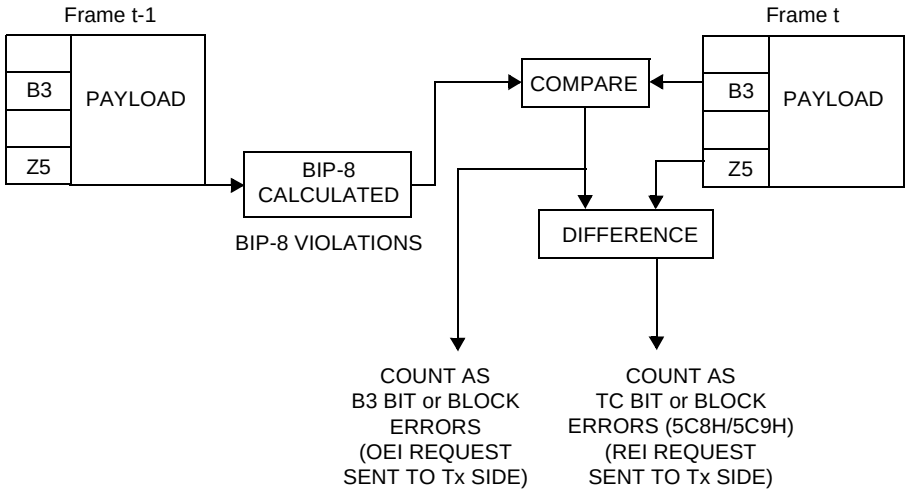
Receive Direction

The tandem connection feature is inhibited when any of the following alarm conditions or control states occurs:

- The receive loss of signal alarm RLOS is active
- The receive loss of frame alarm RLOF is active
- The external SDH/SONET line failure alarm SLFAIL is active
- The receive line AIS alarm RLAIS is active
- The receive path AIS alarm R1PAIS is active
- The receive loss of pointer alarm R1LOP is active
- The control bit RTCEN is a 0.

In the receive direction, the Incoming Error Count (IEC) is checked, and the incoming errors counted when the tandem connection feature is enabled. An IEC value of 0000 is equal to zero errors, 0001 is equal to 1 error in binary, with the maximum value being 1000 or 8. The values of 9 through 15 are interpreted as zero incoming errors. The value of 1110 is used to indicate a TC AIS state, which is detected. A TC AIS indication is indicated by setting the RTCAIS alarm bit (bit 7 in register 5F4H).

Figure 35. IEC Processing



The magnitude of the difference between the calculated number of B3 BIP-8 errors and the number of errors carried in the IEC field is counted a in 16-bit counter at locations 5C8H and 5C9H.

The message/TC REI/TC OEI bits are carried in bits 5 through 8 of the N1 (Z5) byte. These bits are monitored and processed when control bit TCDL (bit 5 in register 00DH) is a 1.

The ETSI-formatted bit message processing performs the following functions:

- Count the number of REI bits received as equal to 1 in bit 5 (TC REI)
- Count the number of OEI bits received as equal to 1 in bit 6 (TC OEI)
- Message frame alignment in bits 7 and 8
- Tandem connection 16-byte TIM comparison against a microprocessor-written value (see Note)
- Tandem Connection Remote Detect Indication (TC RDI indication) detection

Note: TIM comparison and its effects can be disabled using control bits TCTIME, TCTSAE, and TCTLME.

- Tandem Connection Outgoing Detect Indication (TC ODI indication) detection
- Tandem connection unequipped detection (all bits in the N1 byte)
- Access to spare bits in frames 73, 74, 75, and 76.

For downstream circuitry, when the tandem connection feature is enabled, the PHAST-3N will provide the N1 (Z5) byte(s) at the terminal side transparently without B3 compensation when control bit RTCTZ (bit 1 in register 445H) is a 0, or force the N1 byte(s) to 0 with B3 compensation when control bit RTCTZ is a 1. This feature enables the PHAST-3N to act as a monitor for the tandem connection or to terminate the tandem connection before forwarding the N1 byte downstream.

Transmit Direction

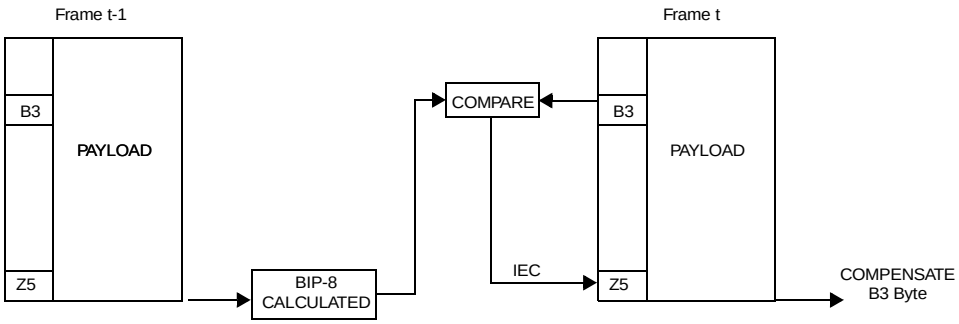
The transmit tandem connection capability is enabled independently of the receive side. The PHAST-3N may be configured as a tandem connection source, defined for path terminating equipment (e.g., connected to a TranSwitch L4M device), or for line terminating equipment. The difference is that when the PHAST-3N is configured as path terminating equipment for originating a tandem connection, the tandem connection IEC field does not have to be calculated, and the IEC field in the N1 (Z5) byte can be set equal to 0. In this configuration, the data field may be carrying a TC bit message protocol. Because the PHAST-3N is operating as a path terminating device, the B3 byte does not require B3 compensation.

When the PHAST-3N is configured in line terminating equipment for originating a tandem connection, the POH bytes are mapped transparently from the terminal side to the line side, and as a result, the PHAST-3N will calculate the IEC field, insert the TC message, and then compensate the B3 byte prior to transmission.

The PHAST-3N may also be configured for monitoring the tandem connection. In this application, the receive side monitors the tandem connection link for IEC errors and the TC message and alarms. In the transmit direction the tandem connection feature is disabled, and the POH bytes are mapped transparently from terminal to line.

Tandem connection IEC errors are checked when enabled. The terminal side TC errors that are detected are then inserted into the outgoing (line side) IEC field of the N1 (Z5) byte.

Figure 36. IEC Insertion



For line terminating equipment, since the BIP-8 parity check is calculated over the VC-4 (including the incoming N1 (Z5) byte), writing into the N1 (Z5) byte will affect the path parity calculation. Unless this is compensated for, a device which monitors the path parity within the tandem connection (a bridging or non-intrusive monitor) may incorrectly count errors. For this reason, the B3 byte must always be consistent with the current state of the VC-4. Therefore, whenever the N1 (Z5) byte is written (with the IEC or message/TC REI/TC OEI), the B3 byte is recalculated.

The number of IEC errors in the N1 byte at the transmit terminal interface are counted in a 16-bit performance counter (registers 1C2H and 1C3H) as bit or block errors. The selection of a bit or block count is common with the receive IEC performance counters.

The message/TC REI/TC OEI bits are carried in bits 5 through 8 in the N1 (Z5) byte. The ability to insert the ETSI message/TC REI/TC OEI is controlled by TCDL (bit 5 in register 00DH). When the insertion in the ETSI format is disabled (TCDL bit equal to 0), the states of bits 5 through 8 are controlled by the values present at the terminal side, POH interface, or POH RAM location. When the ETSI format is enabled (TCDL bit equal to 1), the following functions are performed:

- Tandem Connection Remote Error Indication (TC REI) bit generation
- Tandem Connection Outgoing Error Indication (TC OEI) bit generation
- Tandem connection frame alignment pattern generation (bits 7 and 8)
- Insertion of a 16-byte microprocessor-written message
- Tandem Connection Remote Defect Indication (TC RDI) generation
- Tandem Connection Outgoing Defect Indication (TC ODI) generation
- Control spare bits in frames 73, 74, 75, and 76.

TC REI is sent when control bits RTCEN, TTCEN and TCDL are all a 1, and the receive side has detected a difference between the number of BIP-8 errors in the B3 byte and the IEC value in the N1 byte.

TC OEI is sent when control bits RTCEN, TTCEN and TCDL are all a 1, and the receive side has detected BIP-8 errors in the B3 byte.

Bit 8 in frame 73 is designated as the TC RDI bit. A TC RDI is sent when either of the following conditions is met:

- Control bit TCRDIE is a 0, TTCEN is a 1, and TCDL is a 1 and any of the following conditions occurs:
    - Control bit Transmit Tandem Connection RDI (TTRDI) is a 1.

- Control bits TCRDIE, TTCEN, and TCDL are all a 1, and any of the following conditions occurs:
    - Receive Loss Of Signal alarm (RLOS)
    - Receive Loss Of Frame alarm (RLOF)
    - External SDH/SONET Line Failure (SLFAIL) alarm
    - Receive Line AIS alarm (RLAIS)
    - Receive Loss of Pointer alarm (R1LOP)
    - Receive Path AIS alarm (R1PAIS)
    - External AIS/RDI indication ($\overline{\text{FAIS1}}$ lead is low) and control bit ETCRDI is a 1
    - Receive B3 alarm (B31BER) when control bit B3SDIE is a 1
    - Receive B3 alarm (B31BER) when control bit B3CDIE is a 1
    - Receive Loss Of Multiframe alarm (R1LOM) when control bit H4PDIE is a 1
    - Receive C2 Mismatch alarm (C21MM) when control bit C2PDIE is a 1
    - Receive VCAIS alarm (VC1AIS) when control bit VCSDIE is a 1
    - Receive J1 Loss Of Lock alarm (J11LOL) when control bit J1CDIE is a 1
    - Receive J1 Trace ID Mismatch alarm (J11TIM) when control bit J1CDIE is a 1
    - Receive Unequipped alarm (UNEQ1) when control bit UQCDIE is a 1
    - Receive TC Loss Of Frame alarm (TCLOF) when control bit TCTLME is a 1
    - Receive TC Loss Of Lock alarm (TCLOL) when control bit TCTLME is a 1
    - Receive TC Trace ID Mismatch alarm (TCTIM) when control bit TCALME is a 1
    - Receive TC Unequipped alarm (TCUQ) when control bit TCUQE is a 1
    - Control bit Transmit Tandem Connection RDI (TTRDI) is a 1.

Bit 7 in frame 74 is designated as the TC ODI bit. A TC ODI is sent when either of the following conditions is met.

- Control bit TCODIE is a 0, TTCEN is a 1, and TCDL is a 1, and any of the following conditions occurs:
  - Control bit Transmit Tandem Connection ODI (TTODI) is a 1.

- Control bits TCODIE, TTCEN, and TCDL are all a 1, and any of the following conditions occurs:
  - Receive Loss Of Signal alarm (RLOS)
  - Receive Loss Of Frame alarm (RLOF)
  - External SDH/SONET Line Failure (SLFAIL) alarm
  - Receive Line AIS alarm (RLAIS)
  - Receive Loss of Pointer alarm (R1LOP)
  - Receive Path AIS alarm (R1PAIS)
  - External generate AIS/RDI indication ($\overline{\text{FAIS1}}$ lead is low) and control bit ETCRDI is a 1.
  - Receive B3 alarm (B31BER) when control bit B3SDIE is a 1
  - Receive B3 alarm (B31BER) when control bit B3CDIE is a 1
  - Receive Loss Of Multiframe (R1LOM) when control bit H4PDIE is a 1
  - Receive C2 mismatch alarm (C21MM) when control bit C2PDIE is a 1
  - Receive VCAIS alarm (VC1AIS) when control bit VCSDIE is a 1
  - Receive J1 Loss Of Lock alarm (J11LOL) when control bit J1CDIE is a 1
  - Receive J1 Trace ID Mismatch alarm (J11TIM) when control bit J1CDIE is a 1
  - Receive Unequipped alarm (UNEQ1) when control bit UQCDIE is a 1
  - Receive TC AIS detected (TC1AIS)
  - Receive TC Loss Of Frame alarm (TCLOF) when control bit TCTLME is a 1
  - Receive TC Loss Of Lock alarm (TCLOL) when control bit TCTLME is a 1
  - Receive TC Trace ID Mismatch alarm (TCTIM) when control bit TCALME is a 1
  - Receive TC Unequipped alarm (TCUQ) when control bit TCUQE is a 1
  - Control bit Transmit Tandem Connection ODI (TTODI) is a 1.

The PHAST-3N provides a single byte in the memory map allocated for writing the reserved bit states in the ETSI-formatted message, as shown below. Bits 8 and 7 in frames 73 and 74 (TC RDI and TC ODI) are controlled by local alarms and control bits. The transmit location is 071H. In the receive direction the bits are written into register 449H for microprocessor access.

Bit	7	6	5	4	3	2	1	0
	Frame 73		Frame 74		Frame 75		Frame 76	
	Bit 7	Bit 8	Bit 7	Bit 8	Bit 7	Bit 8	Bit 7	Bit 8
	Set 0	-	-	Set 0	Set 0	Set 0	Set 0	Set 0

TC Message Spare Bit State Selection

The PHAST-3N can also generate a tandem connection AIS: A tandem connection AIS has the following properties.

- Valid pointer (H1 and H2 bytes) that is set equal to 522 Decimal
- An IEC field equal to 1110 in the N1 (Z5) byte
- A valid TC trace ID message in the N1 (Z5) byte
- The complement of the N1 (Z5) byte is written into the B3 byte

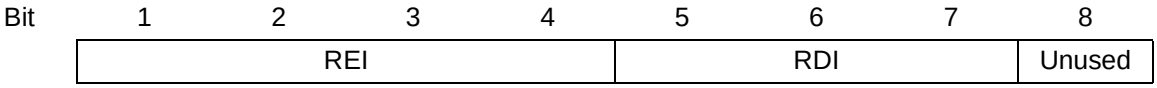
- All ones in the remaining bytes of the SPE (payload bytes and POH bytes) except the N1 (Z5) and B3 bytes

Please note that an unequipped status or transmit path AIS (when enabled) can override tandem connection AIS. The tandem connection AIS is generated when:

- Control bit TTAEN is a 1 and any of the following conditions occurs:
  - Transmit Terminal Loss Of Clock alarm (TTLOC)
  - Transmit Terminal Loss Of Signal alarm (TTLOS)
  - Control bit Transmit Tandem Connection AIS (STCAIS) is set to a 1
  - Transmit Terminal side E11 byte has a majority of ones, and E1AISE and TSAISE are both a 1.

TRANSMIT G1 BYTE REI AND RDI INSERTION

The transmit G1 byte for the VC-4 and for each of the STS-1s has the following bit assignments.



Remote Error Indication Insertion

The REI (FEBE) value (bits 1, 2, 3 and 4) transmitted in the G1 byte represents the number of B3 BIP-8 errors detected locally or from a mate device when the PHAST-3N is configured in a path-protected ring configuration. Bit 4 is the least significant bit. The only values allowed to be transmitted are the counts of 0 through 8. Other count values are transmitted as zero. A check of legal REI values is performed for the error count derived from the local B3 byte BIP-8 or the path REI input from the Alarm Indication Port (path-protected ring). The RAM location value or POH interface, when enabled, will not be checked. This allows a false path REI value to be transmitted for testing. To prevent missed counts from being transmitted due to phase differences between the receive and transmit clocks, a synchronization circuit is provided.

The generation and transmission of REI in the G1 byte is caused by any of the following conditions:

- Terminal REI count when control bit PTEn (bit 7 of register X42H) is a 0
- The REI count is equal to 0 when control bit PTEn is a 1 and control bits G1nM2, G1nM1 and G1nM0 are 000
- Local REI count is sent when control bit PTEn is a 1 and control bits G1nM2, G1nM1 and G1nM0 are 001, 010, 011 or 101
- Path ring AIP REI count is sent when control bit PTEn is a 1 and control bits G1nM2, G1nM1 and G1nM0 are 111
- POH interface REI count is sent (any value) when control bit PTEn is a 1 and control bits G1nM2, G1nM1 and G1nM0 are 110
- RAM REI count is sent (any value) when control bit PTEn is a 1 and control bits G1nM2, G1nM1 and G1nM0 are 100
- Path ring AIP REI count is equal to 0 when control bit PTEn is a 1, control bits G1nM2, G1nM1 and G1nM0 are 111, and AIP interface loss of clock alarm APLOC is detected.

Remote Defect Indication Insertion

Three bits (bits 5, 6 and 7) are assigned for either three-bit RDI or single-bit RDI. Bit RDIO (bit7, 067H) at 1 configures single bit RDI, while a 0 sets three bit RDI.

- Three-bit RDI - Remote Server Defect Indication (RSDI) - bits 5, 6 and 7 equal to 101
- Three-bit RDI - Remote Connectivity Defect Indication (RCDI) - bits 5, 6 and 7 equal to 110
- Three-bit RDI - Remote Payload Defect Indication (RPDI) - bits 5, 6 and 7 equal to 010
- Single-bit RDI (bits 5, 6 and 7 equal to 100)

The states 000, and 001, in bits 5, 6 and 7 indicate no defect indication (off state) for single-bit RDI three-bit RDI respectively. In addition, for three-bit RDI the request to generate two or more types of remote defect indications because of multiple simultaneous alarms or a simultaneous alarm and microprocessor request will result in the transmission of the highest priority defect indication. The priority is remote server defect indication, followed by remote connectivity indication, followed by remote payload indication. For example, for the local alarm or microprocessor controlled mode (G1nM2, G1nM1, G1nM0 = 010), if a local alarm occurs which requests a remote payload defect while the microprocessor control bit which requests a remote connectivity defect is set (TnRCDI), the remote connectivity defect code will be transmitted. If simultaneous alarms occur which request remote server and remote connectivity defect codes be transmitted, the remote server defect code is transmitted. A local alarm is defined as a defect detected on the incoming receive side signal (I.E. LOS, LOF, Line AIS...) that would cause an upstream RDI (or downstream AIS) to be sent.

When control bit PTEn is a 0 the terminal interface RDI value is transmitted. Control bit RDIO (bit 7 in register 067H) enables single-bit RDI when set to 1. The G1nM(2-0) control bits (bits 7, 6 and 5 in register X40H) define the insertion source of RDI, for example, external POH interface. RDI insertion is defined by the text subsections A through G presented below.

A. The local alarms generate RDI in the following manner:

- When control bits are set such that PTEn is a 1, RDIO is a 0, and G1nM2, G1nM1, and G1nM0 are equal to 010, and any of the following conditions occurs, the remote server defect indication (101) is generated. RDI is transmitted for a minimum of 20 frames.
    - Receive Loss of Signal alarm (RLOS)
    - Receive Loss of Frame alarm (RLOF)
    - External SDH/SONET Line Failure (SLFAIL) alarm
    - Receive Line AIS alarm (RLAIS)
    - Receive Loss Of Pointer alarm (RnLOP)
    - Receive FIFO alarm (RnFIFO) when control bit RFRDIE is a 1
    - Receive Path AIS alarm (RnPAIS)
    - External generate AIS/RDI indication ($\overline{\text{FAISn}}$ lead is low) and control bit ERSDIE is a 1
    - Receive B3 alarm (B3nBER) when control bit B3SDIE is a 1
    - Receive VC AIS alarm (VCnAIS) when control bit VCSDIE is a 1
    - Microprocessor writes a 1 to control bit TnRSDI
- When control bits are set such that PTEn is a 1, RDIO is a 0, and G1nM2, G1nM1, and G1nM0 are equal to 010, and any of the following conditions occurs, the remote connectivity defect indication (110) is generated. RDI is transmitted for a minimum of 20 frames.
    - Receive Unequipped alarm (UNEQn) when control bit UQCDIE is a 1
    - Receive B3 bit error alarm (B3nBER) when control bit B3CDIE is a 1
    - Receive J1 Loss Of Lock alarm (J1nLOL) when control bit J1CDIE is a 1
    - Receive J1 Trace ID Mismatch alarm (J1nTIM) when control bit J1CDIE is a 1
    - External generate AIS/RDI indication ($\overline{\text{FAISn}}$ lead is low) and control bit ERCDIE is a 1
    - Microprocessor writes a 1 to control bit TnRCDI
- When control bits are set such that PTEn is a 1, RDIO is a 0, and G1nM2, G1nM1, and G1nM0 are equal to 010, and any of the following conditions occurs, the remote payload defect indication (010) is generated. RDI is transmitted for a minimum of 20 frames.
    - Receive Loss of Multiframe alarm (RnLOM) when control bit H4PDIE is a 1
    - Receive C2 Mismatch alarm (C2nMM) when control bit C2PDIE is a 1
    - External generate AIS/RDI indication ($\overline{\text{FAISn}}$ lead is low) and control bit ERPDIE is a 1
    - Microprocessor writes a 1 to control bit TnRPDI

- When control bits are set such that PTEn and RDIO are a 1, and G1nM2, G1nM1, and G1nM0 are equal to 010, and any of the following conditions occurs, the single-bit RDI (100) is generated. RDI is transmitted for a minimum of 20 frames.
  - Receive Loss of Signal alarm (RLOS)
  - Receive Loss of Frame alarm (RLOF)
  - External SDH/SONET Line Failure (SLFAIL) alarm
  - Receive Loss of Pointer alarm (RnLOP)
  - Receive FIFO alarm (RnFIFO) when control bit RFRDIE is a 1
  - Receive Path AIS alarm (RnPAIS)
  - Receive Line AIS alarm (RLAIS)
  - Receive C2 Mismatch alarm (C2nMM) when control bit C2PDIE is a 1
  - Receive Unequipped alarm (UNEQn) when control bit UQCDIE is a 1
  - Receive VC AIS alarm (VCnAIS) when control bit VCSDIE is a 1
  - Receive J1 Loss Of Lock alarm (J1nLOL) when control bit J1CDIE is a 1
  - Receive J1 Trace ID Mismatch alarm (J1nTIM) when control bit J1CDIE is a 1
  - External generate AIS/RDI indication ($\overline{\text{FAISn}}$ lead is low) and control bit ERSDIE is a 1
  - Receive B3 alarm (B3nBER) when control bit B3SDIE is a 1
  - Receive Loss Of Multiframe (RnLOM) when H4PDIE is a 1
  - Microprocessor writes a 1 to control bit TnRSDI
- When none of the above conditions occurs in the local alarm RDI mode, the 3-bit RDI no-defect code (001) is transmitted (when RDIO=0) or the single-bit RDI no-defect code (000) is transmitted (when RDIO=1).

B. The microprocessor generates RDI in the following manner

- When control bits are set such that PTEn is a 1, RDIO is a 0, and G1nM2, G1nM1, and G1nM0 are equal to 001, and any of the following conditions occurs. There is no control regarding the minimum number of frames RDI is transmitted.
  - Microprocessor writes a 1 to control bit TnRSDI, TnRCDI, or TnRPDI. For all other combinations of these three control bits, the no-defect code is transmitted (001). See the RDI Generation Using Microprocessor Control table on page 109.
- When control bits are set such that PTEn is a 1 RDIO is a 1, and G1nM2, G1nM1, and G1nM0 are equal to 001, and the following condition occurs. There is no control regarding the minimum number of frames RDI is transmitted.
  - Microprocessor writes a 1 to control bits TnRSDI. The no-defect code (000) is transmitted for all other combinations of TnRSDI, TnRCDI, and TnRPDI. See the RDI Generation Using Microprocessor Control table on page 109.

C. The Terminal Side RDI value is sent when control bit PTEn is a 0.

D. The POH RAM RDI value (G1 byte, bits 5, 6 and 7) is sent:

- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 100. There is no control regarding the minimum number of frames RDI is transmitted.
  - Bits in RAM control bits 5, 6 and 7 of the G1 byte (any value).

E. The POH Interface RDI value (G1 byte, bits 5, 6 and 7) is sent for the following conditions:

- When control bit PTEn is a 1, control bit RDIO is a 0, and control bits G1nM2, G1nM1, and G1nM0 are equal to 101. RDI is transmitted for a minimum of 20 frames.
  - Bits 5, 6 and 7 in the G1 byte are equal to the POH interface G1 byte RDI value (in bit 5, 6 and 7) for 101 (RSDI), 110 (RCDI), or 010 (RPDI). All other codes sent as 001 (no-defect).
  - Microprocessor writes a 1 to control bit TnRPDI, TnRCDI or TnRSDI. See the RDI Generation using Microprocessor Control table on page 109.

- When control bit PTEn is a 1, control bit RDIO is a 1, and control bits G1nM2, G1nM1, and G1nM0 are equal to 101. RDI is transmitted for a minimum of 20 frames.
    - Bits 5, 6 and 7 of the G1 byte are equal to the POH interface G1 byte RDI value (in bits 5, 6 and 7) for 100 (single-bit RDI). All other codes sent as 000 (no-defect).
    - Microprocessor writes a 1 to control bit TnRSDI. See the RDI Generation using Microprocessor Control table on page 109.
- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 110. There is no control regarding the minimum number of frames RDI is transmitted.
    - Bits 5, 6 and 7 of the G1 byte are controlled by the POH interface (any value).

F. The Path-Protected Ring Mode RDI value is sent from the Alarm Indication Port for the following conditions:

- When control bit PTEn is a 1, control bit RDIO is a 0, and control bits G1nM2, G1nM1, and G1nM0 are equal to 111, RDI is transmitted for a minimum of 20 frames.
    - AIP bits 5, 6 and 7 of the G1 byte equal to 101 (RSDI), 110 (RCDI), or 010 (RPDI). All other codes sent as 001 (no-defect).
    - Microprocessor writes a 1 to control bit TnRPDI, TnRCDI or TnRSDI. See the RDI Generation using Microprocessor Control table on page 109.
    - Remote server Defect Indication (bits 5, 6 and 7 set to 101) is sent during APLOC alarm.
- When control bit PTEn is a 1, control bit RDIO is a 1, and control bits G1nM2, G1nM1 and G1nM0 are equal to 111. RDI is transmitted for a minimum of 20 frames.
    - AIP bits 5, 6 and 7 of the G1 byte equal to 100. All other codes sent as 000 (no-defect).
    - Microprocessor writes a 1 to control bit TnRSDI. See the RDI Generation using Microprocessor Control table on page 109.
    - Single-bit RDI Indication (bits 5, 6 and 7 set to 100) is the sent during APLOC alarm.

Note: The same alarm conditions shown in the local mode (G1nM2, G1nM1, and G1nM0 are equal to 010) in subsection A, also cause the corresponding RDI code to be output onto the receive AIP port when the ring mode is selected. This allows correct operation when two PHAST-3N devices are used in a ring application.

G. The Test Mode RDI value is sent:

- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 011.
    - Bits 5, 6 and 7 of the G1 byte are equal to 100, independent of alarms and control bits

Bit 8 of the G1 byte

Bit 8 of the G1 byte is undefined at this time. However, control bit TG1nB8 controls the state of Bit 8 as follows:

- When control bit PTEn is a 0
    - Bit 8 is determined by the terminal side G1 byte.
- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 000
    - Bit 8 is equal to 0.
- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 001, 010 or 011.
    - Control bit TG1nB8 determines the bit 8 state.
- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 101 or 110
    - POH port determines bit 8 value
- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 100
    - RAM determines bit 8 value

- When control bit PTEn is a 1 and control bits G1nM2, G1nM1, and G1nM0 are equal to 111
    - Alarm Indication Port determines bit 8 value (bit 8 is sent as 0 for an APLOC alarm)

RDI Generation using Microprocessor Control

The following table lists the RDI that is generated using the microprocessor control bits. The table applies to all modes in which microprocessor control is enabled.

PTEn (bit 7, X42H)	**TnRSDI** (bit 3, X40H)	**TnRPDI** (bit 1, X40H)	**TnRCDI** (bit 2, X40H)	**RDIO** (bit 7, 067H)	**RDI Transmitted When enabled G1 Byte Bits 5, 6, 7**
1	0	0	0	0	001 - Three-bit RDI, No RDI Defect
1	0	0	1	0	110 - Three-bit RDI, Remote Connectivity Defect
1	0	1	0	0	010 - Three-bit RDI, Remote Payload Defect
1	0	1	1	0	001 - Three-bit RDI, No RDI Defect
1	1	0	0	0	101 - Three-bit RDI, Remote Server Defect
1	1	0	1	0	001 - Three-bit RDI, No RDI Defect
1	1	1	0	0	001 - Three-bit RDI, No RDI Defect
1	1	1	1	0	001 - Three-bit RDI, No RDI Defect
1	0	0	0	1	000 - Single-bit RDI, No RDI Defect
1	0	0	1	1	000 - Single-bit RDI, No RDI Defect
1	0	1	0	1	000 - Single-bit RDI, No RDI Defect
1	0	1	1	1	000 - Single-bit RDI, No RDI Defect
1	1	0	0	1	100 - Single-bit RDI, Remote Defect Indication
1	1	0	1	1	000 - Single-bit RDI, No RDI Defect
1	1	1	0	1	000 - Single-bit RDI, No RDI Defect
1	1	1	1	1	000 - Single-bit RDI, No RDI Defect

Summary of Control Bits for G1 Byte

The following table is a summary of the control bits associated with the transmitted G1 byte. Control bit PTEn must be set to 1 to enable these control bits. When control bit PTEn is a 0, the control bits can be set to any state since the G1 byte is transmitted transparently. When PTEn is a 0 the G1 byte is also written into the POH RAM for a microprocessor read cycle.

Control Bits			Transmit G1 Byte is Derived from:		
G1nM2 (bit 7, X40H)	**G1nM1 (bit 6, X40H)**	**G1nM0 (bit 5, X40H)**	**Path REI Value (G1 bits 1-4)**	**Path RDI Value (G1 bits 5-7)**	**Unused bit (G1 bit 8)**
0	0	0	Send 0000	• Send 000	Send 0
0	0	1	Rx B3 errors	• Microprocessor control only • Local alarms disabled • No priority check • No 20 frame minimum transmission	TG1nB8
0	1	0	Rx B3 errors	• Microprocessor control or Local alarms • Priority check • 20 frame minimum transmission	TG1nB8
0	1	1	Rx B3 errors	• Send Single-bit RDI (100) • Microprocessor control and local alarms disabled • No priority check • No 20 frame minimum transmission	TG1nB8
1	0	0	POH RAM (any value)	• POH RAM location (any value) • No priority check • No 20 frame minimum transmission • Microprocessor control and local alarms disabled	POH RAM
1	0	1	Rx B3 errors	• POH interface (RDI codes only) or microprocessor control • Priority check • 20 frame minimum transmission • Local alarms disabled	POH Interface
1	1	0	POH interface (any value)	• POH interface (any value) • No priority check • No 20 frame minimum transmission • Microprocessor control and local alarms disabled	POH Interface
1	1	1	AIP interface (0000 for APLOC)	• AIP interface (RDI codes only) or microprocessor control • Priority check • 20 frame minimum transmission • Local alarms disabled	AIP Interface

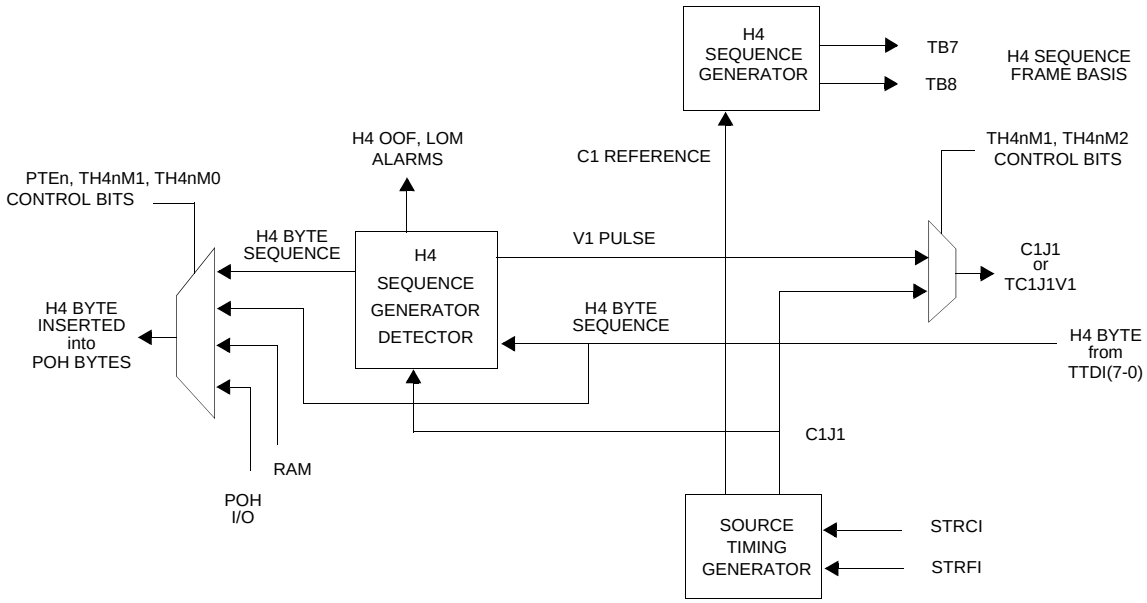
G1n Byte Options Summary

TRANSMIT H4 BYTE

Telecom Bus Interface - Source Timing Mode

The following diagram is a simplified view of the implementation of the H4 byte in the Source Timing mode.

Figure 37. H4 Byte Functions in Source Timing Mode



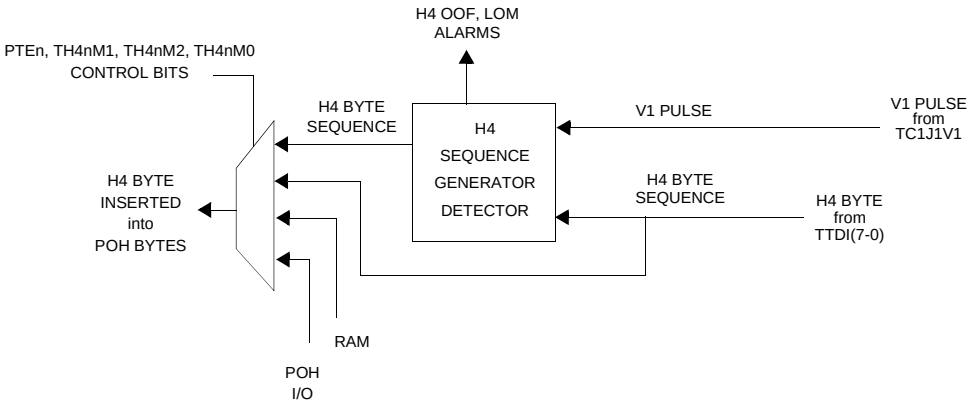
The following table provides a summary of the various options for the H4 byte in path terminating mode using source timing. X can be either state. Control bit PTEn must be set to 1 (path terminating mode). When control bit PTEn is a 0 (non-path terminating mode), these control bits can be set to any state. In the non-path terminating mode the terminal-side H4 bytes are transmitted transparently. The H4 multiframe detector/generator (and alarm) are disabled. The transmit terminal side H4 bytes are written into the H4 RAM location each frame.

TH4nM1 (bit 6, X42H)	**TH4nM0** (bit 5, X42H)	**EXnH4** (bit 4, X41H)	**H4 Byte**
0	0	0	H4 Byte is transmitted from the assigned RAM location. The RAM location value is written by the microprocessor. The H4 multiframe detector/generator (and alarm) is disabled.
0	1	0	H4 Byte is transmitted from the terminal interface and also written into the assigned RAM location. The H4 multiframe detector/generator (and alarm) is disabled.
1	0	0	The multiframe generator H4 byte sequence is transmitted, locked to the input H4 byte multiframe sequence from the terminal interface. The H4 byte is also written into a RAM location. The terminal side H4 byte is monitored for out of multiframe, and loss of multiframe. Bits 1 through 6 are equal to 1s, while bits 7 and 8 carry the H4 sequence.
1	1	0	The multiframe generator H4 byte sequence is transmitted, locked to the output V1 pulse (in the C1J1V1 signal). Bits 1 through 6 are equal to 1, while bits 7 and 8 carry the H4 sequence.
X	X	1	The H4 byte is transmitted from the POH interface. The H4 byte is also is written into the RAM location each frame. The H4 multiframe detector/generator (and alarm) are disabled.

Telecom Bus Interface - Normal Timing Mode

The following diagram is a simplified view of the functions that are provided for the H4 byte in the Normal Timing Mode.

Figure 38. H4 Byte Functions in Normal Timing Mode



The following table provided a summary of the various options for the H4 byte in path terminating mode using normal timing. X can be either state. Control bit PTEn must be set to 1 (path terminating mode). When control bit PTEn is a 0 (non-path terminating mode), these control bits can be set to any state. In the non-path terminating mode, the terminal-side H4 bytes (and all POH bytes) are transmitted transparently. The H4 multiframe detector/generator (and alarm) is disabled. The transmit terminal side H4 bytes are written into the H4 RAM location each frame.

TH4nM1 (bit 6, X42H)	**TH4nM0** (bit 5, X42H)	**EXnH4** (bit 4, X41H)	**H4 Byte**
0	0	0	The H4 Byte is transmitted from RAM. The microprocessor is responsible for writing the value of the H4 byte. The H4 multiframe detector/generator (and alarm) is disabled.
0	1	0	The H4 Byte is transmitted from the terminal interface, and is also written into the assigned RAM location. The H4 multiframe detector/generator (and alarm) is disabled.
1	0	0	The multiframe generator H4 byte sequence is transmitted, locked to the input H4 byte multiframe from the terminal interface. The H4 byte is also written into a RAM location. The terminal side H4 byte is monitored for out of multiframe, and loss of multiframe. Bits 1 through 6 are equal to 1s, while bits 7 and 8 carry the H4 sequence.
1	1	0	The multiframe generator H4 byte sequence is transmitted, locked to the input V1 pulse (in the C1J1V1 signal). Bits 1 through 6 are equal to 1s, while bits 7 and 8 carry the H4 sequence.
X	X	1	The H4 byte is transmitted from the POH interface. The external POH interface byte is written into the RAM location each frame. The H4 multiframe detector/generator (and alarm) are disabled.

TRANSMIT PATH AIS GENERATION

Path AIS is defined as all ones in the POH, the payload, and the H1 and H2 pointer bytes. Please note that an NDF is generated upon Path AIS exit. A transmit Path AIS is generated for either the STM-1 AU-4 VC-4 or for each of the three STS-1s for the following conditions. Please note that transmit Path AIS overrides unequipped status and supervisory unequipped status when enabled, and the tandem connection feature, if enabled.

- When control bit TnPAISE is a 1 and:
  - Control bit TRnPAIS is a 1
  - Transmit FIFO alarm (TnFIFO) and FRENB and TFAISE are a 1 (path AIS will be transmitted for a minimum of three frames)
  - Control bits TFnRST and TFAISE are a 1 (path AIS will be transmitted for a minimum of three frames)
  - Transmit loss of signal alarm (TLOS)
  - Transmit loss of clock alarm (TLOC) when transmit retiming is enabled (TTBYP=0)
  - Transmit terminal E1n byte has a majority of 1s and control bits E1AISE and TSAISE are a 1
  - H1/H2 byte AIS alarm (THnAIS) and control bits HAISE and TSAISE are a 1
- When control bit TnPAISE is a 0 and
  - Control bit TRnPAIS is a 1

VC-4 AND STS-1 UNEQUIPPED STATUS GENERATION

The PHAST-3N can generate an unequipped status channel, or a supervisory unequipped channel, for the VC-4 and for each of the STS-1s, according to the following table.

UQnEN (bit 7, X43H)	**POHnE** (bit 6, X43H)	**Action**
0	X	**Normal Operation**.
1	0	Unequipped Status Generation. The path termination enable control bit (PTEn) must be set to 1 for this mode. When an unequipped status channel is generated, the payload bytes are forced to zero, and except for the B3 byte, all other POH bytes and payload bytes are transmitted as zero. The B3 byte will be a valid BIP-8. The pointer bytes and payload are transmitted with a pointer value equal to 522. An unequipped status channel overrides the tandem connection feature, if enabled.
1	1	Supervisory Unequipped Status Generation. The path termination enable control bit (PTEn) must be set to 1 in this mode. When an unequipped supervisory status channel is generated, the payload bytes are forced to zero, the J1 and G1 bytes are valid, and the C2 byte will be equal to 00 Hex. The B3 byte will have a valid BIP-8. The pointer bytes and payload are transmitted with a pointer value equal to 522. An unequipped supervisory status channel overrides the tandem connection feature, if enabled.

TU-N/VTN TRIBUTARY UNEQUIPPED STATUS AND AIS GENERATION

The PHAST-3N will provide the capability of generating a tributary unequipped status channel or an AIS for a TUG-3, TU-2 (VT6), TU-12 (VT2) and TU-11 (VT1.5). Please note: In order to send a TU-2 (VT6), TU-12 (VT2) or TU-11 (VT1.5) unequipped channel (or AIS), in both STS-3 and VC-4 formats, it is necessary to:

- Enable the H4 detector and generator: The multiframe sequence in bits 7 and 8 in the H4 byte defines the starting location of the V1/V2 pointer bytes within the tributaries.
- Disable the TUG-3 tributary that includes the chosen VT (i.e., set control bits TUG3A, TUG3B or TUG3C to 0).

A TU or VT AIS condition may be substituted for a tributary unequipped status when control bit VTACT (bit 0 in register 020H) is a 1, and an active low is placed on the $\overline{\text{VTACT}}$ input lead for the byte times (rows and columns within the payload) that correspond to the tributary payload. The location of the byte times corresponds to the generated active low signal using the Add indication output provided by TranSwitch mapper devices such as the QE1M.

When the VC-4 format is selected, an unequipped status (or AIS) is generated for a TUG-3 when control bit T3AUE (bit 2 in register 027H) for TUG-3 A or STS-1 No. 1, T3BUE (bit 2 in register 02FH) for TUG-3 B or STS-1 No. 2, or T3CUE (bit 2 in register 037H) for TUG-3 C or STS-1 No. 3, is written with a 1, when enabled. A TUG-3 is enabled by writing a 1 to control bit TUG3m (bit 7 in registers 027H, 02FH and 037H), where m is equal to A, B or C. An unequipped TUG-3 will have TU-3 H1/H2 pointer bytes equal to normal NDF, size bits equal to 10, and a pointer equal to 522. The TU-3 H1/H2 pointer bytes are carried in rows 1 and 2 in columns 4 (TU-3 A), 5 (TU-3 B), or 6 (TU-3 C) of the VC-4. All other bytes (payload and POH) will be assigned the value of 00H.

There are seven TU-2s (VT6s) that are mapped into their corresponding TUG-2s, which in turn are mapped into each of the three TUG-3s or into three STS-1s (VC-3s). The TUG-2 will be configured to carry a TU-2 unequipped status (or AIS) by setting one or more of the seven pairs of TUG-2 control bits (TGm2ny1 and TGm2ny0, where m is either A, B or C, and n is 1 through 7) to 01. The unequipped status format is generated for the TU-2 by setting control bit TUnm1 to a 1, where m is equal to A, B or C.

An unequipped status TU-2 is defined as having a valid pointer (V1/V2 bytes with a normal NDF, size bits=00, pointer=321), and the other bytes within the TU-2 equal to 00 Hex.

There are three TU-12s (VT2s) which can map into seven TUG-2s, which in turn are mapped into each of the three TUG-3s or into three STS-1s (VC-3s). The TUG-2 will be configured to carry a TU-12 unequipped status (or AIS) by setting one or more of the seven pairs of TUG-2 control bits (TGm2ny1 and TGm2ny0) to 00. The unequipped status format is generated for one or more of the three TU-12s within a TUG-2 by setting control bits TUnmx to a 1, where m is equal to A, B or C, and x is equal to 1, 2, or 3.

An unequipped status TU-12 is defined as having a valid pointer (V1/V2 bytes with a normal NDF, size bits=10, pointer=105), and the other bytes within the TU-12 equal to 00 Hex.

There are four TU-11s (VT1.5s) which can map into seven TUG-2s, which in turn are mapped into each of the three TUG-3s or into three STS-1s (VC-3s). The TUG-2 will be configured to carry a TU-11 unequipped status by setting one or more of the seven pairs of TUG-2 control bits (TGm2ny1 and TGm2ny0) to 11. The unequipped status format is generated for one or more of the four TU-11s within a TUG-2 by setting control bits TUnmx to a 1, where m is equal to A, B or C, and x is equal to 1, 2, 3 or 4.

An unequipped status TU-11 is defined as having a valid pointer (V1/V2 bytes with a normal NDF, size bits=11, pointer=78), and the other bytes within the TU-11 equal to 00 Hex.

For example, assume the format is a VC-4, and TUG-3 A is carrying a TU-3, TUG-3B is carrying 21 TU-12s, and TUG-3C is carrying 28 TU-11s. We want to send an unequipped status channel for the TU-3 in TUG-3 A, an unequipped for the No. 1 and No. 3 TU-12s in the TUG-2 No. 3 in TUG-3 B, and an unequipped status channel for the No. 2 and No. 4 TU-11s in TUG-2 No. 7 in TUG-3 C. The following control bits in the memory map would be set to configure the channels for unequipped:

For the VC-4:

Set bits TUG3A (bit 7 in register 027H) to 1 (TUG-3), TUG3B (bit 7 in register 02FH) to 0 (TUG-2), and TUG3C (bit 7 in register 037H) to 0 (TUG-2)

Set bits TGB231/TGB230 (bits 3 and 2 in register 028H) to 00 (TUG-2 No. 3 in TUG-3 B),

Set bits TGC271/TGC270 (bits 3 and 2 in register 039H) to 11 (TUG-2 No. 7 in TUG-3 C)

For the TUG-3, TU-11s and TU-12s:

Set bit T3AUE (bit 2 in register 027H) for TUG-3 A.

Set bits TU3B1 (bit 5 in register 032H) and TU3B3 (bit 5 in register 034H) for TU-12s No.1 and 3 in TUG-2 No. 3 for TUG-3 B

Set bits TU7C2 (bit 1 in register 03BH) and TU7C4 (bit 1 in register 03DH) for TU-11s No.2 and 4 in TUG-2 No. 7 for TUG-3 C

For another example, assume the format in an STS-3 and in STS-1 No. 1 is carrying 28 VT1.5s, STS-1 No. 2 is carrying 21 VT2s, and STS-1 No. 3 is carrying 28 VT1.5s. We want to send an unequipped status channel for STS-1 No. 1 VT1.5 No. 28, STS-1 No. 2 VT2 No. 1, and for STS-1 No. 3 a VT1.5 No. 2. The following control bits in the memory map would be set to configure the channels for unequipped:

Set bit TUG3A (STS-1 No. 1) (bit 7 in register 027H) to 0

Set bit TUG3B (STS-1 No. 2) (bit 7 in register 02FH) to 0

Set bit TUG3C (STS-1 No. 3) (bit 7 in register 037H) to 0

Set bits TGA271 and TGA270 (bits 3 and 2 in register 029H) to 11 (four VT1.5s in Group 7)

Set bits TGB211 and TGB210 (bits 7 and 6 in register 030H) to 00 (three VT2s in Group 1)

Set bits TGC261 and TGC260 (bits 5 and 4 in register 039H) to 11 (for VT1.5 in Group 1)

Set bit TU7A4 (bit 1 in register 02DH) to 1 (send unequipped status for VT1.5 No. 28)

Set bit TU1B1 (bit 7 in register 032H) to 1 (send unequipped status for VT2 No. 1)

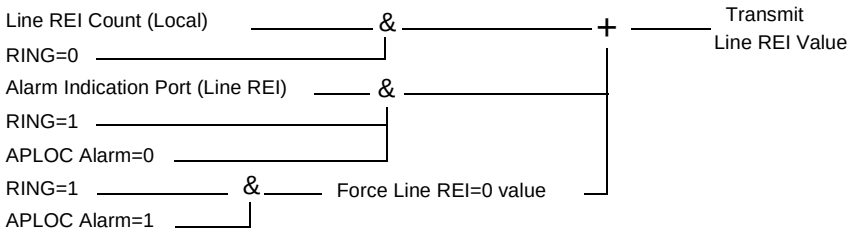
Set bit TU2C1 (bit 6 in register 03AH) to 1 (send unequipped status for VT1.5 No. 2)

TRANSMIT LINE REI (FEBE)

The M1 byte is designated to carry the line REI (FEBE) count. The value sent in M1 is equal to the number of bits in error detected in the three received B2 bytes (BIP-24) for the previous frame (which is the line REI count). The error count (between 0 and 24) is inserted into bits 4 (MSB) through 8 (LSB). Only the values 0 through 24 are valid. Other values are sent as 0 errors. Bits 1 through 3 are transmitted as zeros. For example, a received line REI count of 24 is transmitted as 0001 1000 in the M1 byte. To prevent missed counts from being transmitted due to phase differences between the receive and transmit clocks, a synchronization circuit is provided on the transmit side. When the M1 byte is optioned to be transmitted from the TOH interface, any value for REI may be transmitted. The M1 byte value is also written into the assigned TOH RAM location prior to being transmitted.

The logic diagram for sending line REI is shown below for both the STM-1 AU-4 (STS-3c) and STS-3 (STM-1 AU-3) formats, where + represents a logical “or” function, and & represents a logical “and” function.

Figure 39. Transmit Line REI Count in M1 Byte Logic Diagram



TRANSMIT LINE RDI

The insertion of line RDI is enabled when lead $\overline{\text{TOHENB}}$ is low. Line RDI (FERF) is defined as the value of 110 in bits 6, 7 and 8 of the transmitted K2 byte. The conditions and alarms for sending line RDI are described below. The line RDI state will be transmitted for a minimum of 20 frames. The generation of Line RDI overrides the value that may be present in bits 6, 7, and 8 in the K2 byte.

- When control bit TLRDIE is a 1 and control bit RING is a 0 and any of the following conditions occurs:
  - Receive Loss of Signal alarm (RLOS)
  - Receive Loss of Frame alarm (RLOF)
  - External SDH/SONET Line Failure alarm (SLFAIL) when the SERIAL lead is low
  - Receive Line AIS alarm (RLAIS)
  - Receive J0 Loss of Lock alarm (J0LOL) when control bit J0RDIE is a 1
  - Receive J0 Trace Mismatch alarm (J0TIM) when control bit J0RDIE is a 1
  - B2 Bit Error Rate exceeded (B2BER) when control bit B2RDIE is a 1
  - Control bit TRLRDI is a 1
- When control bits TLRDIE and RING are 0 and
  - Control bit TRLRDI is a 1
- When control bits TLRDIE and RING are a 1 and any of the following conditions occurs:
  - LRDI status via the Alarm Indication Port
  - AIP Loss of Clock alarm (APLOC)
  - Control bit TRLRDI is a 1
- When control bit TLRDIE is a 0 and control bit RING is a 1 and
  - Control bit TRLRDI is a 1

Bits 6, 7, 8 of the K2 byte in the Tx TOH RAM location are not overwritten by the Line RDI value when the K2 byte source is the Tx TOH RAM location. When the K2 byte source is either the APS or TOH interface, Line RDI overwrites bits 6, 7, 8 of the Tx TOH RAM K2 byte.

TRANSMIT LINE AIS

The insertion of line AIS is enabled when lead $\overline{\text{TOHENB}}$ is low. Line AIS is defined as normal section overhead bytes (A1, A2, C1, B1, E1, F1, D1-3) and a scrambled all ones in the remainder of the Transport Overhead bytes and in the entire payload. Line AIS overrides an unequipped channel, path AIS generation, the PRBS generator and the tandem connection feature. Please note that an NDF is generated upon the Line AIS exit. The conditions for sending a line AIS are described below:

- When control bit TLAISE is a 1 and:
  - Transmit terminal side E11 byte has a majority of 1s (five out of eight) and control bits E1AISE and TSAISE are a 1
  - Transmit loss of signal alarm (TLOS)
  - Transmit loss of clock alarm (TLOC) when transmit retiming is enabled (control bit TTBYP is a 0)
- When control bit TRLAIS is a 1

The Line/Section overhead Tx TOH RAM locations are not overwritten by Line AIS.

STUFF COLUMN INSERTION

When the STM-1 AU-4 (STS-3c) format is selected, the first column in the VC-4 is assigned to carry POH bytes, while the second and third columns may designated as fixed stuff, depending upon the payload being carried. When the VC-4 is assigned to carry three TUG-3s, any of the TUG-3s may be assigned to carry seven TUG-2s. In this mapping format (TUG-3 carrying TUG-2s), the three TUG-3s will carry fixed stuff in columns 4 and 7 (n=1), 5 and 8 (n=2), and 6 and 9 (n=3). The starting location for the VC-4 (SPE) is based on the location of the J1 byte, which is determined by the J1 pulse in the TC1J1V1 signal.

In the STS-3 (STM-1 AU-3) format, the three AU-3/STS-1s may be assigned to carry VC-3s, which may be carrying TU-11s/VT1.5s or TU-12s/VT2s. For STS-3 format, the fixed stuff columns for each STS-1 are defined as columns 30 and 59. The starting location of each of the STS-1s (i.e., the J1 byte) is determined by the three J1 pulses in the TC1J1V1 signal.

The following table shows a summary of control bits for generating fixed stuff columns for the STM-1 AU-4 VC-4 (STS-3c) format when PTE1 is a 1 (path terminating mode). When control bit PTE1 is a 0 (non-path terminating mode), the POH bytes, stuff columns bytes, and payload bytes are mapped from terminal side to the line side transparently.

TFSV4 (bit 7, 020H)	**TFSy** (020H)	**Action**
0	0	No action is taken on the incoming columns. They are transmitted transparently from the terminal side to the line side.
0	1	Causes a fixed stuff value of 0 to be transmitted for the columns specified, otherwise the columns are transmitted intact from the terminal side, where: y=1 (bit 6, 020H) for columns 4 and 7, y=2 (bit 5, 020H) for columns 5 and 8, and for y=3 (bit 4, 020H) for columns 6 and 9. Columns 2 and 3 are transmitted intact from the terminal side to the line side.
1	0	Columns 2 and 3 in the VC-4 are transmitted as zero. Other columns are transmitted intact from the terminal side.
1	1	Columns 2 and 3 in the VC-4 are transmitted as zero. This is followed by a fixed stuff value of 0 transmitted for the columns specified for TFSy (bits 6, 5 and 4 in 020H). y=1 for columns 4 and 7, y=2 for columns 5 and 8, and y=3 for columns 6 and 9.

Stuff Column Control Bit Selection for STM-1 VC-4 Format

The following table shows a summary of control bits for generating a fixed stuff for the STS-3 format when PTEn is a 1 (path terminating mode). When PTEn is a 0 (non-path terminating mode), the POH bytes, stuff column bytes, and payload bytes for the corresponding STS-1, are mapped from the terminal side to the line side transparently. Note that control bit TFSV4 must be set to zero for the STS-3 format.

TFSV4 (bit 7, 020H)	**TFSy** (020H)	**Action**
0	0	No action taken on the incoming columns in the SPEs. They are transmitted transparently from the terminal side to the line side.
0	1	A 1 causes the specified columns for the selected STS-1 to be transmitted as zeros, where: y = 1 (bit 6, 020H) for columns 30 and 59 for STS-1 No. 1, y = 2 (bit 5, 020H) for STS-1 No. 2, and y = 3 (bit 4, 020H) for STS-1 No. 3.

Stuff Column Control Bit Selection for STS-3 (STM-1 AU-3) Format

RING APPLICATIONS

Receive-side alarms and performance monitoring signals are provided at the PHAST-3N Alarm Indication Port for use in protected ring applications. In the receive direction, the signals at this interface consist of a data output (RAIPD), clock output (RAIPC) and frame indication output (RAIPF). In the transmit direction, the Alarm Indication Port signals consist of a data input (TAIPD), clock input (TAIPC), and frame input (TAIPF). The receive side signals are connected to the transmit side Alarm Indication Port of the mate PHAST-3N. Similarly, the mate's receive Alarm Indication Port is connected to the PHAST-3N Transmit Alarm Indication Port.

Synchronization circuits are provided for inserting the line REI (FEBE) and path REI (FEBE) values into the transmit frame to prevent the transmitter from losing counts.

The signal assignment in the Alarm Indication Port frame is shown in the following table. The serial interface will support 81 bits, of which 73 bits are assigned to carry status information. The 81-bit format was selected in order to provide a symmetric clock (81 bits ÷ 648 kbit/s = 125 µs, and 155.52 Mbit/s ÷ 648 kbit/s = 240).

No. of Bits	Indication
1	Line RDI alarm indication. This bit reflects the state of the local line RDI indication which is generated by specific alarms. See the TRANSMIT LINE RDI paragraph in the OPERATION section.
1	Received RNAPS (New TOH APS byte) alarm. This bit is the same as the RNAPS indication at address 4FAH, bit 5.
1	Received RPAPS (New POH K3 APS byte) alarm (STM-1 AU-4 or STS-3 STS-1 No. 1). This bit is the same as the RPAPS indication at address 4FAH, bit 2.
8	Bits 1 to 8 Debounced received K1 byte
8	Bits 1 to 8 Debounced received K2 byte
8	Bits 1 to 8 Debounced received K3 byte (STM-1 and STS-3 STS-1 No. 1)
5	B2 errors converted to a line REI (FEBE) value to be transmitted (5-bit value). This field is forced to zero during the RLOF, RLOS, and SLFAIL alarm states.
5	Received line REI (FEBE) value (5-bit value), bits 4 to 8 in the Z23 byte. This field is forced to zero during the RLOF, RLOS, SLFAIL, and RLAIS alarm states.
4	B3 errors converted to a REI (FEBE) value (four bits) for transmit path REI for STM-1 AU-4 or STS-3 STS-1 No. 1. This field is forced to zero during the RLOF, RLOS, SLFAIL, RLAIS, R1PAIS, and R1LOP alarm states.
4	Received path REI (FEBE), bits 1 to 4 in the G1 byte for STM-1 AU-4 or STS-3 STS-1 No. 1. This field is forced to zero during the RLOF, RLOS, SLFAIL, RLAIS, R1PAIS, and R1LOP alarm states.
3	Path RDI to be transmitted in bits 5 to 7 in the G1 byte for STM-1 AU-4 or STS-3 STS-1 No. 1
1	Bit 8 in the G1 byte for STM-1 AU-4 or STS-3 STS-1 No. 1
4	B3 errors converted to a REI (FEBE) value (four bits) for transmit path REI for STS-3 STS-1 No. 2. This field is forced to zero during the RLOF, RLOS, SLFAIL, RLAIS, R2PAIS, and R2LOP alarm states.
4	Received path REI (FEBE) value, bits 1 to 4 in the G1 byte for STS-3 STS-1 No. 2. This field is forced to zero during the RLOF, RLOS, SLFAIL, RLAIS, R2PAIS, and R2LOP alarm states.
3	Path RDI to be transmitted in bits 5 to 7 in the G1 byte for STS-3 STS-1 No. 2
1	Bit 8 in the G1 byte for STS-3 STS-1 No. 2
4	B3 errors converted to a REI (FEBE) value (four bits) for transmit path REI for STS-3 STS-1 No. 3. This field is forced to zero during the RLOF, RLOS, SLFAIL, RLAIS, R3PAIS, and R3LOP alarm states.
4	Received path REI (FEBE), bits 1 to 4 in the G1 byte for STS-3 STS-1 No. 3. This field is forced to zero during the RLOF, RLOS, SLFAIL, RLAIS, R3PAIS, and R3LOP alarm states.

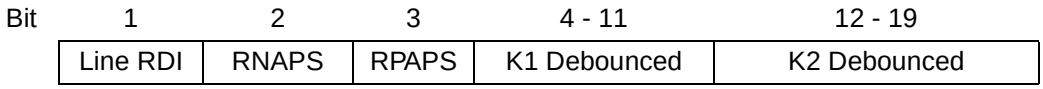
No. of Bits	Indication
3	Path RDI to be transmitted in bits 5 to 7 in the G1 byte for STS-3 STS-1 No. 3
1	Bit 8 in the G1 byte for STS-3 STS-1 No. 3
1	Loss Of Signal Indication for received line (RLOS or SLFAIL)
1	Loss Of Frame Indication (RLOF)

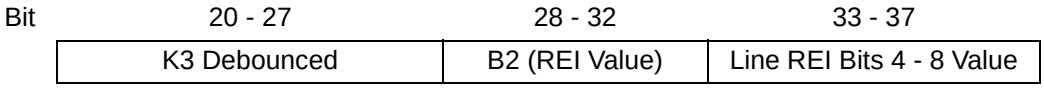
AIP Interface Data Lead Signal Content Definition

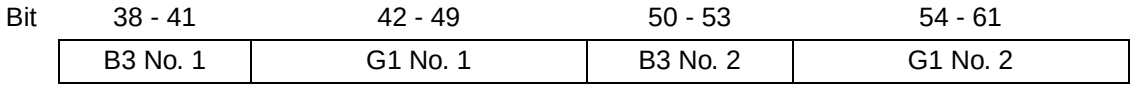
Please note: The TOH alarm states are forced to 0 when lead $\overline{\text{TOHENB}}$ is high.

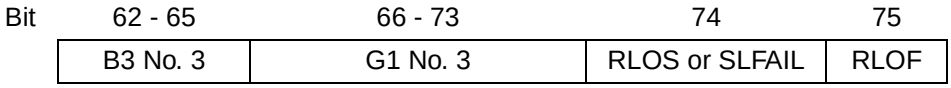
The following is the bit assignment within the 81-bit frame:

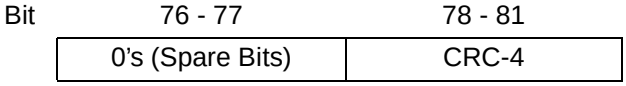
.











AIP Frame Bit Assignment

The transmit clock (TAIPC) is monitored for operation. When enabled, a transmit AIP loss of clock alarm (APLOC) will result in transmitting a line REI value of zero, a path REI value equal to 0, and a path RDI remote server defect indication. A line RDI indication is transmitted when lead $\overline{\text{TOHENB}}$ is low.

The CRC-4 generating polynomial is $x^4 + x + 1$. A CRC-4 is calculated and compared against the CRC-4 carried in bits 78, 79, 80 and 81 of the 81-bit frame. An APCRC alarm is declared when the CRC-4s do not match. Other than the alarm indication, no further action is taken. The ability to transmit the CRC-4 in error is provided for testing purposes. When control bit AIPCRE (bit 0 in register 400H) is written with a 1, the CRC-4 is transmitted inverted from its calculated value for one frame. To send another error, this control bit must be first written with a 0, followed by a 1.

The following is a summary of the various Alarm Indication Port (AIP) interface states and the actions taken in the transmit direction by the mate PHAST-3N.

- AIP interface Line RDI Indication (bit 1): A 1 causes an APLRDI alarm and Line RDI to be transmitted when control bits RING and TLRDIE are a 1. The interrupt mask bit is control bit AMLRDI.
- AIP interface New TOH APS Indication (bit 2): A 1 causes an APNAPS alarm when control bit RING is a 1. No other action is taken other than an interrupt when enabled. The interrupt mask bit is control bit AMNAPS.
- AIP interface New POH K3 APS Indication (bit 3): A 1 causes an APPAPS alarm when path ring mode (control bits G1nM(2-0) are equal to 111). No other action is taken other than an interrupt when enabled. The interrupt mask bit is control bit AMPAPS.
- The debounced K1 byte (bits 4-11) is provided in the memory map (register 072H) for microprocessor read cycle.
- The debounced K2 byte (bits 12-19) is provided in the memory map (register 073H) for a microprocessor read cycle.
- The debounced K3 byte (bits 20-27) for STM-1 VC-4, STS-3c SPE and for STS-3 STS-1 No. 1 is provided in the memory map (register 074H) for a microprocessor read cycle.
- AIP Interface B2 Errors Converted to a Line REI Value (bits 28-32): Detected B2 errors converted to a Line REI value from a mate device are transmitted as line REI errors in the ring mode (control bit RING is a 1). In addition, the value in this field at the transmit AIP interface is counted in the B2 Error performance counter when in ring mode and control bit RINGC is a 1. When control bit RINGC is a 0, receive line B2 errors are counted in the B2 Error performance counter.
- AIP Interface REI Errors (bits 33-37): REI errors in the Z23 byte of a mate device are counted in the Line REI Error performance counter via the transmit AIP interface when in ring mode (control bit RING is a 1) and control bit RINGC is a 1. No other action is taken by the PHAST-3N. When control bit RINGC is a 0, receive line REI errors in the Z23 byte are counted in the Line REI Error performance counter.
- AIP Interface B3 Errors (bits 38-41, 50-53, 62-65): Detected B3 errors from a mate device are transmitted as path REI errors in the G1 byte when in path ring mode (control bits G1nM(2-0) are equal to 111). In addition, the value in this field at the transmit AIP interface is counted in the B3 Error performance counter when in path ring mode and control bit CNTn is a 1. When control bit CNTn is a 0, receive line B3 errors are counted in the B3 Error performance counter.
- AIP Interface G1 byte Received REI Errors (bits 42-45, 54-57, 66-69): Path REI errors in the G1 byte of a mate device are counted in the path REI Error performance counter via the transmit AIP interface when in path ring mode (control bits G1nM(2-0) are equal to 111) and control bit CNTn is a 1. This field is also written into registers 075H - 077H. No other action is taken by the PHAST-3N. When control bit CNTn is a 0, G1 byte REI errors from the receive line are counted in the path REI Error performance counter.
- AIP Interface G1 Byte Path RDI Status (bits 46-48, 58-60, 70-72): The AIP RDI code (Server, Connectivity, or Payload) from a mate device is the source for the transmit path RDI when in path ring mode (control bits G1nM(2-0) are equal to 111). The codes at the transmit AIP interface are written into registers 075H-077H and the transmit POH RAM G1 byte location. RDI codes cause an APRDIn alarm. The APRDIn alarms are enabled when in path ring mode.
- AIP Loss of Signal Indication (receive loss-of-signal or signal fail - bit 74): A 1 causes an APLOS alarm when either in ring mode (control bit RING is a 1) and/or in path ring mode (control bits G1nM(2-0) are equal to 111. No other action is taken by the PHAST-3N other than an interrupt when enabled.
- AIP Loss of Frame Indication (bit 75): A 1 causes an APLOF alarm when either in ring mode (control bit RING is a 1) and/or in path ring mode (control bits G1nM(2-0) are equal to 111. No other action is taken by the PHAST-3N other than an interrupt when enabled.

POH BYTE INTERFACES

The nine received POH bytes in the VC-4 and the three sets of POH bytes associated with the three STS-1s are provided at a POH interface, in addition to being written into the memory map. The receive interface has the following output signal leads:

- Clock (RPCLK)
- Address latch enable (RPALE)
- Address (RPADD)
- Data latch enable (RPDLE)
- Data (RPDAT).

The transmit side has the following signal leads:

- Clock output (TPCLK)
- Address latch enable output (TPALE)
- Address output (TPADD)
- Data latch enable output (TPDLE)
- Data input (TPDAT).

The address latch enable signal is 12 clock cycles wide. This allows for an address capability of 12 bits in which the PHAST-3N will use 6 bits. The address field has the following format in both the receive and transmit directions:

A0 - A5	A6	A7	A8	A9	A10	A11	SONET/SDH Format and POH Byte
Not Used (Equal to 0s)	0	0	X	X	X	X	STS-3 STS-1 No. 1
	0	1	X	X	X	X	STS-3 STS-1 No. 2
	1	0	X	X	X	X	STS-3 STS-1 No. 3
	1	1	X	X	X	X	STM-1 VC-4
	X	X	0	0	0	0	J1 Byte
	X	X	0	0	0	1	B3 Byte
	X	X	0	0	1	0	C2 Byte
	X	X	0	0	1	1	G1 Byte
	X	X	0	1	0	0	F2 Byte
	X	X	0	1	0	1	H4 Byte
	X	X	0	1	1	0	F3 Byte
	X	X	0	1	1	1	K3 Byte
	X	X	1	0	0	0	N1 (Z5) Byte

POH Interface Address Field

Notes:
1. Address A0 is the MSB and the first bit sent.
2. Address bits A0 to A5 are not used and are sent as zeros.
3. The data bytes start with bit 1 in the POH byte (which is defined as the MSB and the first bit in the byte).
4. There is a one clock cycle-wide gap between the address latch enable and data latch enable signals. This allows for transfer time in an external FPGA.
5. The falling edge of the clock is used to clock out the POH interface signals in the receive direction. In the transmit direction, the rising edge of the clock is used to clock in the data.

The sequence of events for clocking out data from the receive POH interface is as follows:

- The Address Latch Enable signal (RPALE) goes high for 12 clock periods on a falling edge of the clock (RPCLK).
- During this time, the 12-bit serial address (RPADD) is clocked out.
- At the end of the address latch enable time, there will be an idle period of one clock cycle.
- The data latch enable signal (RPDLE) then goes high for 8 clock periods.
- During this time, the 8-bit POH byte corresponding to the address is clocked out. Bit 1 in the POH byte is the first bit clocked out.

The sequence of events for clocking in data from the transmit POH interface is as follows:

- The Address Latch Enable signal (TPALE) goes high for 12 clock periods on a falling edge of the clock (TPCLK).
- During this time, the 12-bit serial address (TPADD) is clocked out.
- At the end of the address latch enable time, there will be an idle period of one clock cycle.
- The data latch enable signal (TDLE) then goes high for 8 clock periods.
- During this time, the 8-bit POH byte corresponding to the address is clocked in. Bit 1 in the POH byte is the first bit clocked in.

B2 BER MEASUREMENT

The B2 BER threshold and time base detection and recovery registers are located in memory locations 44EH through 455H. In addition, control bit B2TBH (bit 5 in register 440H) is used to adjust the time base as either 500 microseconds (when set to 1) or 125 microseconds (when set to 0). This control bit is used to establish a time base for low B2 BER measurements. Control bit BURST (bit 6 in register 440H) is used to provide some measure of protection against sequential burst errors. The following table provides settings for various B2 BER measurements, with a 95% confidence level at BER 1.0E-4 and lower. The Alarm Notification Time is the maximum time that may elapse before an interrupt is generated or a software-polling bit is asserted. These Alarm Notification times give the host processor time to process the alarm and meet the GR-253-CORE Switch Initiation and Maximum Clearing times. The 1.0E-10 clearing threshold processing must be performed by the host processor since the PHAST-3N time base counters are not large enough to encompass the required integration period.

Table 11. B2 Bit Error Rate Measurement Settings

Detection Threshold	Detection Threshold Setting (44EH/44FH)	Detection Time Base Setting (450H/451H)	Alarm Notification Time - Detection (ms)	Clearing Threshold	Clearing Threshold Setting (452H/453H)	Clearing Time Base Setting (454H/455H)	Alarm Notification Time - Clearing (ms)
1.0E-3	004CH	0004H	1	1.0E-4	0010H	0008H	2
1.0E-4	0010H	0008H	2	1.0E-5	000CH	003EH	16
1.0E-5	000CH	003EH	16	1.0E-6	000AH	0208H	130
1.0E-6	000AH	0208H	130	1.0E-7	0010H	2082H	2,081
1.0E-7	0010H	2082H	2081	1.0E-8	000CH	F3D5H	15,605
1.0E-8	000CH	3CF5H*	15,605	1.0E-9	0005H	FDFEH*	65,022
1.0E-9**	0005H	FDFEH*	65,022	1.0E-10	------	------	------

* Control bit B2TBH = 1

** Recommend setting control bit BURST = 1

B3 BER MEASUREMENT

The B3 BER threshold and time base detection and recovery registers are located in memory locations X50H through X57H where X = 5, 6 or 7. In addition, control bits B3nTBH (bit 7 in registers n40, where n = 5, 6 or 7), are used to adjust the time base as either 500 microseconds (when set to 1) or 125 microseconds (when set to 0). These control bits are used to establish a time base for low B3 BER measurements. Control bit BURST (bit 6 in register 440H) is used to provide some measure of protection against sequential burst errors. The following table provides settings for various B3 BER measurements, with a 95% confidence level. The Alarm Notification Time is the maximum time that may elapse before an interrupt is generated or a software-polling bit is asserted. These Alarm Notification times give the host processor time to process the alarm and meet the GR-253-CORE Switch Initiation and Maximum Clearing times. The 1.0E-10 clearing threshold processing must be performed by the host processor since the PHAST-3N time base counters are not large enough to encompass the required integration period.

Table 12. B3 Bit Error Rate Measurement Settings

Detection Threshold	Detection Threshold Setting (X50H/X51H)	Detection Time Base Setting (X52H/X53H)	Alarm Notification Time - Detection (ms)	Clearing Threshold	Clearing Threshold Setting (X54H/X55H)	Clearing Time Base Setting (X56H/X57H)	Alarm Notification Time - Clearing (ms)
1.0E-3	0019H	0004H	1	1.0E-4	000CH	0014H	5
1.0E-4	000CH	0014H	5	1.0E-5	000CH	00C0H	48
1.0E-5	000CH	00C0H	48	1.0E-6	0009H	059CH	360
1.0E-6	0009H	059CH	360	1.0E-7	000FH	5D8AH	5,986
1.0E-7	000FH	1762H*	5,986	1.0E-8	000CH	BB14H*	47,892
1.0E-8	000CH	BB14H*	47,892	1.0E-9	0001H	9BE6H*	39,910
1.0E-9**	0001H	9BE6H*	39,910	1.0E-10	------	------	------

* Control bit B3nTBH = 1
** Recommend setting control bit BURST = 1

BIP ERROR MASK GENERATION

The PHAST-3N is equipped with both BIP-8 and BIP-24 error masks. The error mask capability for the B1 (BIP-8), B2 (BIP-24) and one or more B3 (BIP-8) bytes is enabled by writing a 1 to control bits B1EME (bit 7 in register 066H), B2EME (bit 6 in register 066H), or B3EME (bit 5 in register 066H), respectively. When an error mask is enabled, a 1 written into a TOH or POH RAM BIP location causes that bit to be transmitted inverted from its calculated value for the number of frames determined by the error repetition control register (register 070H). The B1 RAM location is register 0A3H. The B2 RAM locations are registers 0ACH, 0C7H and 0E2H. The B3 RAM locations are registers 171H, 271H and 371H. Also, control bit B3EME is common to the three AU-3s or STS-1s. B3 error mask capability is enabled only when path terminating mode is enabled (bit 7 in register X42H is a 1).

When a BIP byte from a TOH or POH interface is selected and enabled, a high in the external BIP byte bit position will cause an error to be transmitted. The value from the external interface is also written into the TOH or POH RAM BIP location. The number of frames in which bit errors are transmitted is controlled by an error repetition control register. For example, when control bit B1EME is written with a 1, and control bit TOHB1E is also written with a 1, the external error mask for the B1 byte is enabled. A 1 in any bit position of the B1 byte at the TOH interface will cause the corresponding calculated bit to be transmitted inverted from its calculated value.

The Error Repetition Control Register (location 070H) is provided which controls the number of frames for the generation of B1, B2 and B3 BIP errors via the error mask (whether sourced from the RAM location or external interface). The following table defines the number of frames for transmitting BIP errors based on the number of bits selected by the mask.

Error Repetition Control Register Value	B1EME or B2EME or B3EME	Action
XX	0	No BIP errors transmitted. Error mask can be set to any value.
00H	1	No BIP errors transmitted.
01H	1	BIP errors are transmitted for one frame. The bits in error in the BIP register are determined by the bits equal to 1 in the error mask. For example, if the error mask (RAM location) is equal to FF Hex, all bits in the BIP are transmitted in error.
02H	1	BIP errors are transmitted for two frames. The bits in error in the BIP register are determined by the bits equal to 1 in the error mask.
03-FDH		BIP errors are transmitted for 3-253 frames. The bits in error in the BIP register are determined by the bits equal to 1 in the error mask.
FEH	1	BIP errors are transmitted for 254 frames. The bits in error in the BIP register are determined by the bits equal to 1 in the error mask.
FFH	1	BIP errors are transmitted continuously. The bits in error in the BIP register are determined by the bits equal to 1 in the error mask. The error transmission is disabled by writing a 0 to control bit BnEME.

The error masks, the error repetition control register, and the error mask enable bits function in the following manner:

1.) The selected BIP error mask value (i.e., the microprocessor written RAM value or external interface value) defines the BIP bits that are to be transmitted in error. For example, writing a 01 Hex to the B3 error mask register for the B3 byte in the VC-4 indicates that only bit 1 in the B3 BIP-8 will be sent in error. The other BIP error masks (RAM locations) should be written with zeros, otherwise they will send their associated BIP errors when enabled.

2.) The Error Repetition Control Register is written with the number of frames to be transmitted in error (see table above).

3.) The last step is to write the corresponding Error Mask Enable (BnEME) with a value of 0 then 1 to initiate the error transmission. For all values of the Error Repetition Control register from 01H to FEH the specified number of frames will be sent with the selected bit locations inverted and then normal operation will be resumed. (Note: The only way to halt the continuous transmission of errors - when the Error Repetition value is FFH - is to write the Error Mask Enable bit with a value of 0).

LOOPBACKS

The PHAST-3N provides five loopback capabilities. See Figure 40:

- Device Line Loopback
- Serial Device Line Loopback
- Upstream Line Loopback
- Terminal Loopback
- STS-3 STS-1 terminal Loopback

Device Line Loopback: Enabled when a 1 is written to control bit DLBK (bit 7 in register 00FH). Transmit data and clock are looped back to the receive terminal output. The data is looped back as parallel data, independent of the line interface selected, parallel or serial. Receive data is disabled. In addition, transmit data will be sent to the SONET/SDH line. Note: always apply a RESETS (Register 00A, bit 7) after turning on this loopback to clear out any LOS alarms that may be present.

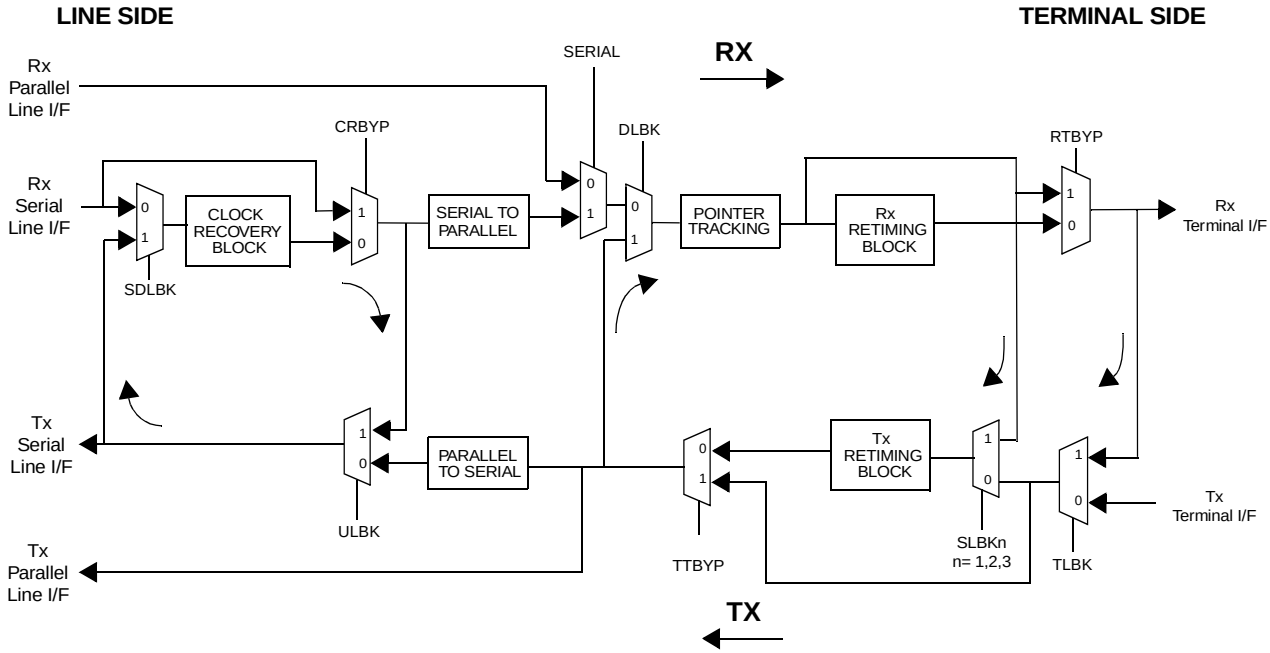
Serial Device Line Loopback: Enabled when a 1 is written to control bit SDLBK (bit1 in register 012H). This loopback is valid only for the serial line interface, and only when Clock Recovery is enabled (CRBYP, Lead No H3 is a 0). Transmit Data only is looped back to the input of the clock recovery block. Transmit data and clock outputs will continue to be provided.

Upstream line loopback: Enabled when a 1 is written to control bit ULBK (bit 0 in register 012H). This loopback is valid only for the serial line interface. Receive serial data and clock is looped back as transmit serial data and clock. Internal transmit data is inhibited.

Terminal Loopback: Enabled when a 1 is written to control bit TLBK (bit 6 in register 00FH). The terminal side receive data, clock, SPE and C1J1 are internally connected to the transmit input. The receive terminal output signals will continue to be provided. Control bit TTCIV (bit 3 in register 022H) must be set to 0 when this loopback is enabled. For Terminal loopback or STS-1 source timing mode, the transmit H4 mode must be either “terminal interface”, or “locked to terminal interface”. Memory map, or V1 pulse options cannot be used.

STS-3 STS-1 Terminal Loopback: The STS-3 mode must be selected. The STS-3 mode is selected when a 1 is written to control bit STS3 (bit 7 in register 00BH). The loopback is enabled when a 1 is written to control bit SLBKn (bits 3, 2 and 1 in 00FH). The loopback causes the receive output of the like-numbered STS-1 to be internally connected to the transmit input. The receive output signals will continue to be provided. Please note that this loopback is not be supported when the transmit retiming feature is bypassed (control bit TTBYP is a 1). For Terminal loopback or STS-1 source timing mode, the transmit H4 mode must be either “terminal interface”, or “locked to terminal interface”. Memory map, or V1 pulse options cannot be used.

Figure 40. Loopbacks



Tx to Rx Loopbacks
SDLBK, Serial Device Line Loopback: Reg 012, bit1
DLBK, Device Line Loopback: Reg 00F bit 7

Rx to Tx Loopbacks
ULBK, Upstream Line Loopback: Reg. 012, bit 0
TLBK, Terminal Loopback: Reg: 00F, bit 6
SLBK1, STS-3, STS-1 No. 1 Terminal Loopback: Reg. 00F, bit 3
SLBK2, STS-3, STS-1 No. 2 Terminal Loopback: Reg. 00F, bit 2
SLBK3, STS-3, STS-1 No. 3 Terminal Loopback: Reg. 00F, bit 1

Note:
CRBYP: Clock Recovery Block Bypass: Lead No. H3
SERIAL: Bit Serial Interface Enable: Lead No. K1
RTBYP: Receive Retiming Bypass Enable: Reg. 402, bit 4
TTBYP: Transmit Retiming Bypass Enable: Reg. 021, bit 3

HIGH IMPEDANCE TEST MODE

A lead designated as $\overline{\text{HIGHZ}}$ is provided for board testing. An active low placed on this lead causes all output leads (except TBDO, RTCO, TH4B7, TPOH and the PECL output leads) to be set to the high impedance state for board testing.

PSEUDO-RANDOM TEST GENERATOR AND ANALYZER

The PHAST-3N provides a Pseudo-Random Binary Sequence (PRBS) test generator and analyzer for both the STM-1 VC-4 and STS-3 STS-1 formats. The PRBS sequence is 2^{23}-1, which is defined in the ITU-T O.151 recommendation.

Transmit PRBS Test Generator

The transmit PRBS test generator is enabled according to the following table. Line and Path AIS generation, and unequipped generation overrides the PRBS test generator, if enabled. The transmit PRBS generator functions in either path terminating mode (control bit PTEn is a 1), or non-path terminating mode (control bit PTEn is a 0).

TPG1 (bit 1, 011H)	**TPG0** (bit 0, 011H)	**PRBS Test Generator Function for Transmit Direction**
0	0	PRBS Test Generator Disabled
0	1	PRBS pattern is inserted into the VC-4 columns when the STS3 control bit is a 0. When the STS3 control bit is a 1, the PRBS pattern is inserted into STS-3 STS-1 No. 1.
1	0	When control bit STS3 is a 1, the PRBS pattern is inserted into STS-3 STS-1 No. 2.
1	1	When control bit STS3 is a 1, the PRBS pattern is inserted into STS-3 STS-1 No. 3.

When the transmit PRBS generator is enabled, the following options are also available in both the path termination and non-path terminating modes.

PTEn (bit 7, X42H)	**TPPOH** (bit 1, 024H)	**PRBS Test Generator Overhead Options for Transmit Direction**
0	X	All POH bytes are forced to zero, except the B3 byte, which is recalculated. H1/H2 pointer generation operates the same as when the PRBS generator is disabled.
1	0	The POH bytes, and H1/H2 pointer generation, operate the same as when the PRBS generator is disabled.
1	1	All POH bytes are forced to zero, except the B3 byte, which is recalculated. H1/H2 pointer generation operates the same as when the PRBS generator is disabled, except when transmit retiming is disabled and the normal transmit terminal timing mode is selected. In this case, the H1/H2 pointer and SPE are forced to location 522 instead of being passed through unchanged from the terminal interface.

The ability to insert the PRBS pattern into the stuff columns will be activated according the following table when the PRBS generator is enabled (control bits TPG1, 0 are equal to 01, 10, or 11).

STS3 (bit 7, 00BH)	**PTEn** (bit 7, X42H)	**TFSV4** (bit 7, 020H)	**TFSn** (bit 6, 5, 4, 020H)	**TPSFC** (bit 2, 011H)	**PRBS Test Generator Stuff Column Pattern Insertion Options**
0	0	X	X	0	Columns 2 through 9 transmitted intact from the terminal side.
0	1	0	0	0	Columns 2 through 9 transmitted intact from the terminal side.
0	X	X	X	1	Columns 2 through 9 transmitted with PRBS pattern.
1	X	X	X	0	Columns 30 and 59 for STS-1 selected transmitted intact from the terminal side.
1	X	X	X	1	Columns 30 and 59 for STS-1 selected transmitted with PRBS pattern.

In STS-3 mode, the stuff column control bit TFSn (bits 6, 5, and 4 in 020H) are disabled for each corresponding STS-1 in which the PRBS generator is enabled.

In STM-1 AU-4 mode, the TFSV4 and TFSn control bits continue to operate when TPSFC=0. The table above shows how to pass stuff columns 2 - 9 intact from the terminal side when TPSFC = 0. Other possible stuff column options when TPSFC = 0 are shown in the table at register 020H, bit 7.

In addition, an error may be inserted into the PRBS pattern by writing a 1 to control bit TPRBSE (bit 0 in register 024H). To send another error, a 0 must be first written into this bit position followed by a 1.

Receive Test Analyzer

The test analyzer works independently of the test generator in the receive direction. The receive test analyzer is enabled when a 1 is written to control bit TPAON (bit 0 in register 405H). The test analyzer monitors the VC-4 or STS-3 STS-1 for the PRBS pattern according to the settings of the TPG1 and TPG0 bits (bits 1 and 0 in register 011H).

The selection of stuff columns to be monitored will be controlled by control bit TPSFC, as explained above. Note, however that when TPSFC = 0, the analyzer ignores the stuff columns. When another PHAST-3N device is used to generate the PRBS pattern, the TPSFC control bit should be set the same on both PHAST-3Ns. In applications in which the test pattern is not generated by a PHAST-3N, the possibility exists for an incompatibility with respect to the use of the stuff columns. For these situations, it is important to note that the analyzer will not go out-of-lock. Bit errors will be recorded in the PRBS error counter.

The test analyzer is in lock when 16 consecutive error-free sequences are received. An Out of Lock alarm (TPOOL) is declared when eight consecutive errored sequences are received. Errored sequence blocks are counted in a 16-bit counter (registers 45EH and 45FH). A sequence block is defined to be three consecutive bytes of the PRBS pattern. An errored sequence block is one in which at least one bit error occurs.

A control bit may be used to cause the PRBS analyzer to lose synchronization. That is, a 1 written to control bit TPLOS (bit 1 in register 405H) will cause the monitor to lose synchronization. A 0 must be written to the control bit, followed by another 1, to cause another loss of synchronization condition.

BOUNDARY SCAN

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint test Action Group (JTAG). Boundary scan is a specialized architecture that provides observability and controllability for the PHAST-3N device's interface leads. The Boundary Scan block consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan path bordering the input and output leads, as illustrated in Figure 41. The boundary scan test bus interface has four input signals: Test Clock (TBCK), Test Mode Select (TBMS), Test Data Input (TBDI), and a Test Reset ($\overline{\text{TBRS}}$). There is also a Test Data Output (TBDO).

The TAP controller receives external control information via a Test Clock (TBCK) signal and a Test Mode Select (TBMS) signal, and sends control signals to the internal scan paths. The scan path architecture consists of a 16 bit serial instruction register and multiple serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TBDI) and the Test Data Output (TBDO) signals. The Test Data Input (TBDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during scan operation. The Test Data Output (TBDO) is selected to send data from the selected register during scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output leads' signals to pass to and from the PHAST-3N device's internal logic, as illustrated in Figure 41. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 27 on page 67.

The maximum frequency that the PHAST-3N device will support for boundary scan is 10 MHz. The PHAST-3N supports the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS

EXTEST Test Instruction

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the PHAST-3N is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external PHAST-3N input and output leads.

SAMPLE/PRELOAD Test Instruction

When the SAMPLE/PRELOAD instruction is shifted in, the PHAST-3N device will remain fully operational. While in this test mode, PHAST-3N input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

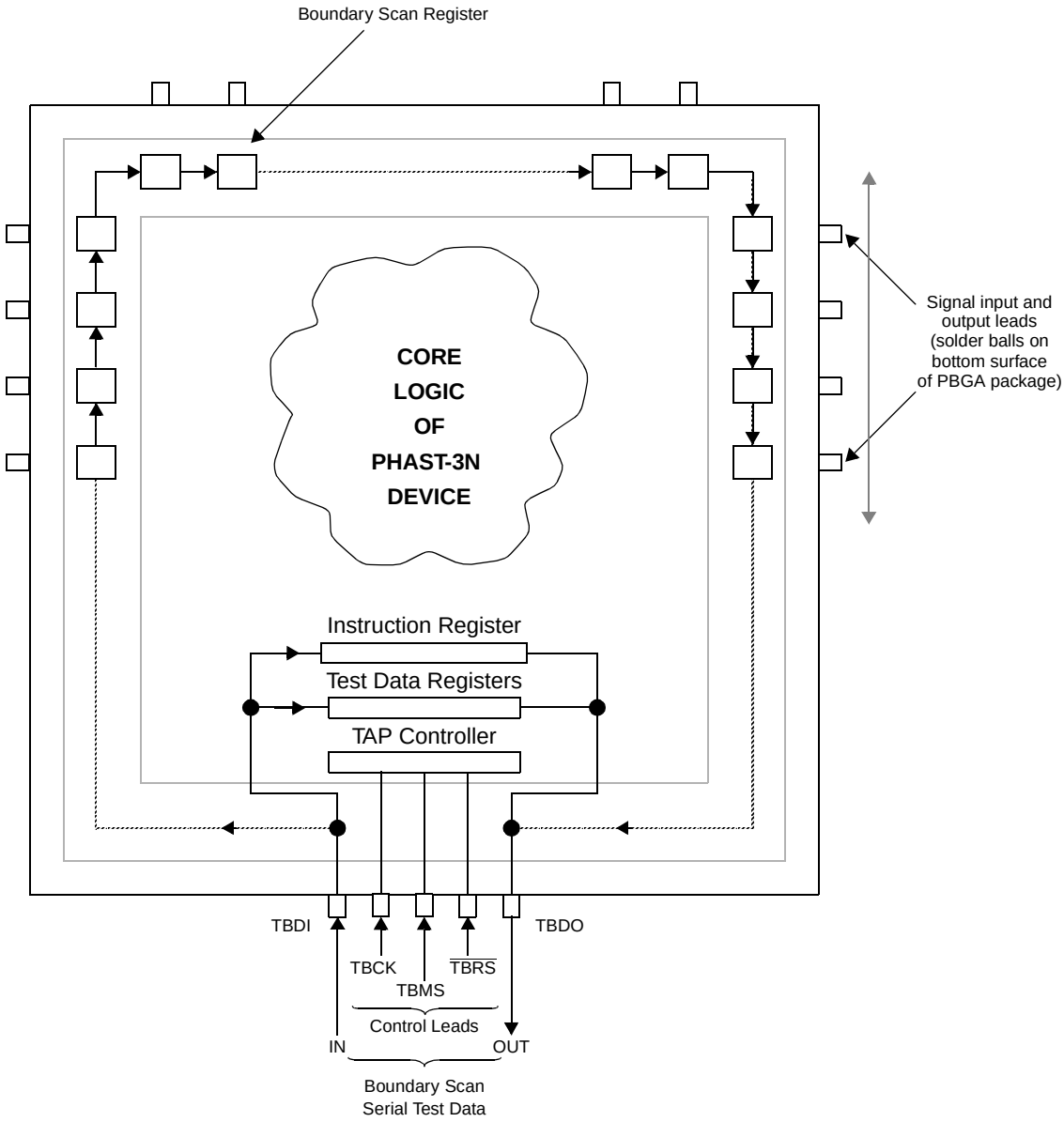
BYPASS Test Instruction

When the BYPASS instruction is shifted in, the PHAST-3N device will remain fully operational. While in this test mode, a scan operation will transfer serial data from the TBDI input, through the internal scan cell, to the TBDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

Boundary Scan Reset

Specific control of the $\overline{\text{TBRS}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead should be held low whenever boundary scan operations are not being performed. Placing a pull down resistor from $\overline{\text{TBRS}}$ lead to ground, which can allow a tester to drive the $\overline{\text{TBRS}}$ lead high, is suggested when the boundary scan testing feature is used.

Figure 41. Boundary Scan Schematic



Boundary Scan Chain

A Boundary Scan Description Language (BSDL) file for the PHAST-3N device is available via the Product Information / Product Software page of the TranSwitch Internet Web Site at www.transwitch.com.

INTERNAL PROCESSOR INITIALIZATION

Internal (ACE) Processor Boot-Up Strategy

The PHAST-3N is equipped with two internal (ACE) processors, one on the receive side and one on the transmit side. The purpose of the internal processors is to perform many of the TOH (RSOH and MSOH)/POH processes. Processing includes such routines as J1 trail trace message comparisons, and controlling the alarms that will generate Path RDI.

Each processor core has an instruction RAM (IRAM), Data RAM and Boot RAM memory. In the PHAST-3N, the microprocessor interface is used to load the boot RAM first followed by the instruction RAM of each processor. This is accomplished using a set of dedicated registers which are mapped to the host's memory. These registers can be found in the Memory Map and Bit Descriptions section as the “Transmit and Receive ACE Processor Access” registers.

Firmware Download Procedure

The device firmware (microcode) for the PHAST-3N device is available via the Product Information / Product Software page of the TranSwitch Internet Web site at www.transwitch.com.

The device firmware download consists of three phases, which are illustrated in Figures 44a, 44b, and 44c. The two internal ACE processors, on the receive and transmit sides, are booted up during the first phase (Boot RAM Load). The instructions for the receive side processor are downloaded during the second phase (Rx IRAM Load), and the instructions for the transmit side processor are downloaded during the third and final phase (Tx IRAM Load). Please note that a firmware download must always be preceded by resetting of the device by either an external active low $\overline{\text{RESET}}$ on lead W20 or through the Hardware Reset control bit, RESETH (bit 5 in register 00AH).

Figure 42a. Firmware Download Procedure Phase 1: Boot RAM Load

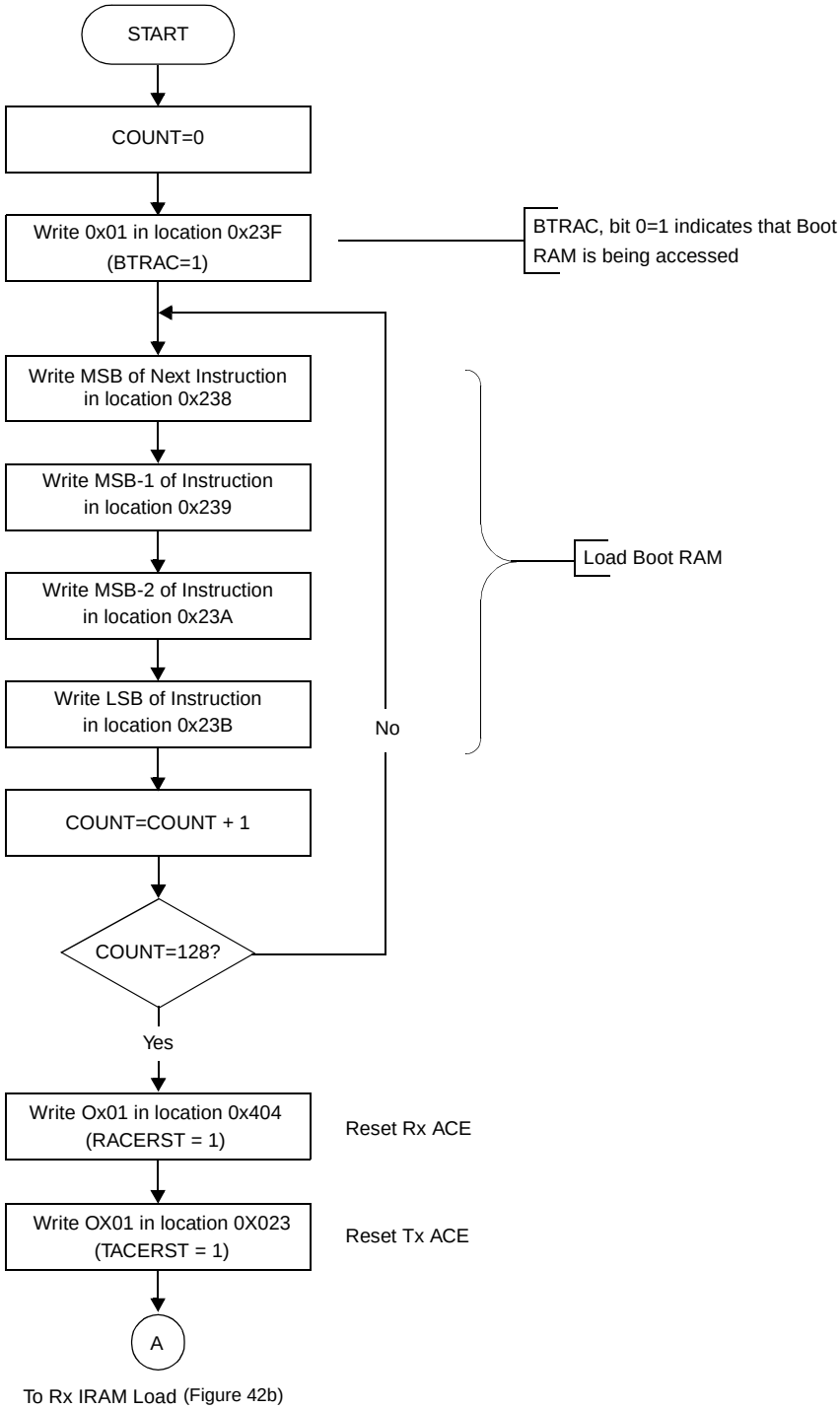


Figure 42b. Firmware Download Procedure Phase 2: Rx IRAM Load

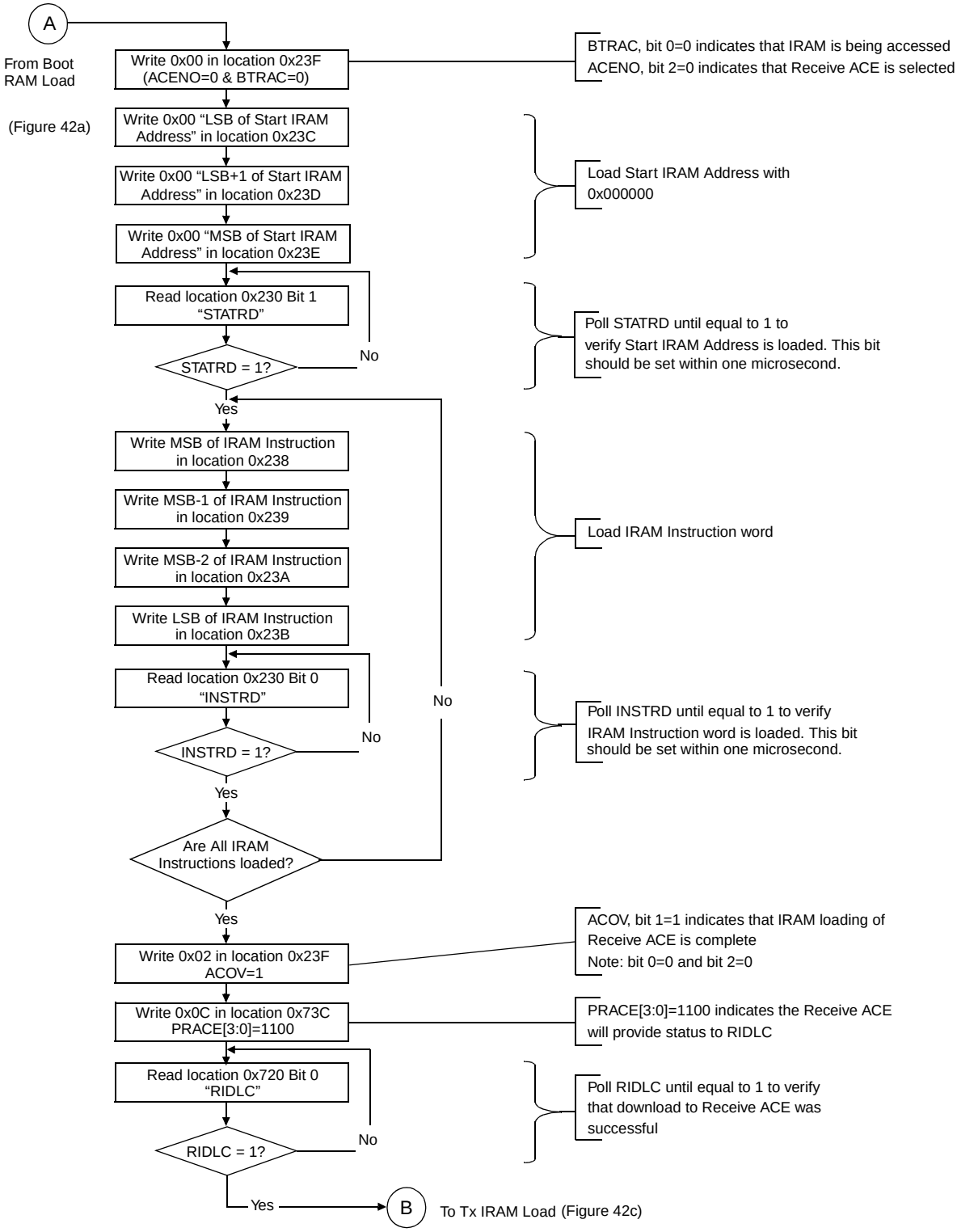
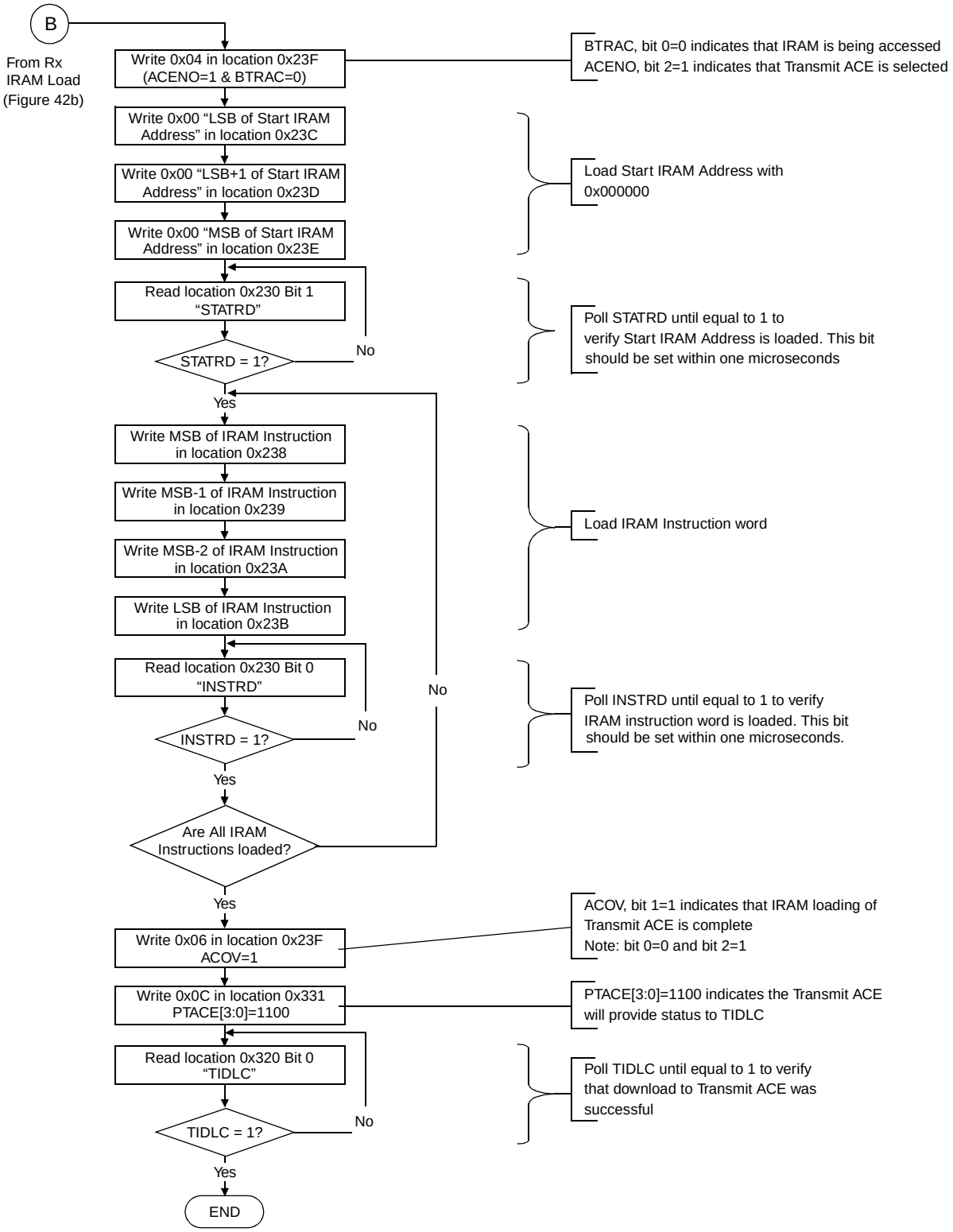


Figure 42c. Firmware Download Procedure Phase 3: Tx IRAM Load



POWER-UP AND INITIALIZATION

Recommended Power-up Sequence

The following procedure is recommended for powering up the PHAST-3N in a known good state from initial power-up (from step 1) or from a device reset (from step 2).

1.) **Power up device**

2.) **Reset the device** - using one of two methods shown below. Note that a firmware download MUST always be preceded with either of these reset methods, and only after VDD power is stable and clocks are stable.

- Apply an external hardware reset by applying a low to lead W20 ($\overline{\text{RESET}}$) for a minimum of 250 ns.
- OR write a 1 to Hardware Reset (RESETH) control bit located in register 00AH, bit 5.

3.) **Download Firmware**** - Load Boot RAM, Receive ACE IRAM, and finally Transmit ACE IRAM according to the firmware download procedures illustrated in the flow charts in Figures 42a, 42b and 42c. Table 13 is now valid.

4.) **Load control registers** - for user specific application, after waiting a minimum of 125 µs from the completion of the firmware download. This assures enough time for the internal processors to initialize control and mask registers to values as shown in Register Initialization.

5.) **Apply Software Reset** - (RESETS=1; bit 7 in register 00AH).

6.) **Apply Performance Counter Reset** - (RESETC=1; bit 6 in register 00AH), after waiting a minimum of 10 ms from applying RESETS.

** Note: Before firmware is downloaded the only registers that should be accessed by the external microprocessor interface are:

- Manufacturer and Device ID registers (000H - 009H)
- Common Control Registers (00AH - 017H)
- Transmit and Receive ACE Processor Access Registers (230H, 238H - 23FH, 320H, 331H, 720H and 73CH).

Register Initialization

The following table shows the initialization values of all configurable Control & Mask Registers upon completion of resetting the device (using lead $\overline{\text{RESET}}$ or control bit RESETH) (step 2 above), and downloading the firmware, (step 3 above). Please note that these registers are not affected by a Software Reset (RESETS; bit 7 in register 00AH) or a Performance Counter Reset (RESETC; bit 6 in register 00AH).

Table 13. Initialization State of Configurable Control & Mask Registers

Register Block	Register Name	Register Locations	Initialization value after firmware download
COMMON	Scratch-Pad	005-009	00H
	Common Control	00A-012, 017	00H
TX COMMON	Tx Common Control	020-024	00H
	Tx TU/VT Uneq	027-02D, 02F-035, 037-03D	00H
	Tx TOH Control	060-067, 070, 071	00H
	Tx TOH RAM	0A0-0F0	00H
	Tx J0 RAM	080-08F	00H
	Tx N1 RAM	090-09F	00H

Register Block	Register Name	Register Locations	Initialization value after firmware download
TX Per STS1 #1	Tx Control	100, 101	00H
	Tx Control	140-143	00H
	Tx POH RAM (except J1)	171-178	00H
	Tx J1 RAM	180-1BF	00H
TX Per STS1 #2	Tx Control	200, 201	00H
	Tx Control	240-243	00H
	Tx POH RAM (except J1)	271-278	00H
	Tx J1 RAM	280-2BF	00H
TX Per STS1 #3	Tx Control	300, 301	00H
	Tx Control	340-343	00H
	Tx POH RAM (except J1)	371-378	00H
	Tx J1 RAM	380-3BF	00H
RX COMMON	Rx Common Control	400-405	00H
	Rx AIS & RDI Enables	440-446	00H
	Rx Term A1/A2	447/448	F628H
	Rx B2 Error Threshold	44E/44F, 452/453	000AH
	Rx B2 Error Time Base	450/451, 454/455	0000H
	Rx uP J0 Compare RAM	470-47F	00H
	Rx uP N1 Compare RAM	490-49F	00H
RX Per STS1 #1	Rx Control	500, 501	00H
	Rx Control	540,541	00H
	Rx B3 Error Threshold	550/551, 554/555	000AH
	Rx B3 Error Time Base	552/553, 556/557	0000H
	Rx C2 Compare Value	558	01H
	Rx uP J1 Compare RAM	5B0-5BF	00H
RX Per STS1 #2	Rx Control	600, 601	00H
	Rx Control	640, 641	00H
	Rx B3 Error Threshold	650/651, 654/655	000AH
	Rx B3 Error Time Base	652/653, 656/657	0000H
	Rx C2 Compare Value	658	01H
	Rx uP J1 Compare RAM	6B0-6BF	00H

Register Block	Register Name	Register Locations	Initialization value after firmware download
RX Per STS1 #3	Rx Control	700, 701	00H
	Rx Control	740, 741	00H
	Rx B3 Error Threshold	750/751, 754/755	000AH
	Rx B3 Error Time Base	752/753, 756/757	0000H
	Rx C2 Compare Value	758	01H
	Rx uP J1 Compare RAM	7B0-7BF	00H
Mask Registers	Common	01A, 01B	00H
	Tx Common	0F4-0F6	00H
	Tx Per STS	1E0, 2E0, 3E0	00H
	Rx Common	4F4-4F7	00H
	Rx Per STS	5E0-5E2, 6E0-6E2, 7E0-7E2	00H

ACCESS OF REGISTERS LOCATED IN RAM

The PHAST-3N memory map is divided between registers located in Hardware (not shaded in Memory Map tables below) and registers located in RAM (shaded). The Registers located in RAM can further be divided into Transmit RAM (shaded with an "***Italic Bold type face***" in the Memory Map) and Receive RAM (shaded with a "Regular Type Face" in the Memory Map).

This is an example of how transmit RAM locations in italic bold type face appear in the Memory Map**:**

Add	Status	Bit 7
060	R/W	***TLA1A2E***

This is an example of how receive RAM locations in regular type face appear in the Memory Map:

Add	Status	Bit 7
440	R/W	J0AEN

The Transmit RAM and Receive RAM locations can be accessed by their respective Transmit or Receive ACE processor as well as by the external microprocessor. To prevent the external microprocessor from interrupting the ACE processor too often and corrupting ongoing internal processing, the RDY or $\overline{\text{DTACK}}$ pulse width will be extended to hold off the external microprocessor. This pulse may extend up to 324 ACE Clock (ACECI) cycles, or 6.75 µs worst case, and some external processors may time-out and generate a bus error within this specified period. To prevent this from happening, the PHAST-3N provides Busy bits in a hardware-mapped register. There are two Busy bits, one for the transmit ACE processor (TBUSY located in register 017H, bit 1) and one for the receive ACE processor (RBUSY located in register 017H, bit 0). When a Busy bit is 1 it indicates that the respective ACE processor is busy processing and should not be interrupted by the external microprocessor. If RAM accesses are preformed while the Busy bit is 1 then the RDY or $\overline{\text{DTACK}}$ pulse width may extend to 324 ACECI clock cycles.

The following protocol must be used for accessing registers located in Transmit or Receive RAM:

1) Poll the relevant Busy bit (TBUSY or RBUSY) until it is 0.

2) Access (Read/Write) the desired Transmit or Receive RAM location.

If the above protocol is followed then the RDY or $\overline{\text{DTACK}}$ pulse width shall be less than 50 ACECI clock cycles (1.042 µs) under all conditions.

A recommendation for spacing accesses to registers in RAM would be:

If the Busy bit is polled and it is high, (or a RAM access has recently been completed), then do not poll the Busy bit again for 200 ACECI clock cycles (4.167 µs). This would allow approximately 30 RAM accesses in a 125 µs SONET/SDH frame.

Some important notes:

1) Registers located in Hardware space do not need to poll the Busy bits. This includes the Software Polling bits, unlatched alarms, latched alarms, and interrupt mask registers.

2) The Busy bit becomes asserted as soon as an access to RAM is requested by the external microprocessor, therefore if the Busy bit is low when polled it will not go high until after the access to RAM is started.

3) Access to any one of the 16 bit Performance Counters located in RAM can be considered as a single access and there is no need to poll the Busy bit between the low byte and high byte.

MEMORY MAPS AND BIT DESCRIPTIONS

The memory map is organized in the following manner. The address range is 11 bits, from A10 to A0, where A10 is the most significant bit. The address range supported is 000 Hex to 7FF Hex, and address values are always stated in Hex (e.g., 01C Hex or 01CH). The specific functions assigned to the bits of the 8-bit register at each address location are described in tables below, first in a map that assigns symbols to the bits, then as descriptive text for each such symbol. Memory status is indicated for each register (R = Read-only; R(L) = Read-only, latched; R/W = Read/Write). Registers that are unassigned or marked as “Reserved” should not be accessed by the microprocessor that controls the PHAST-3N. Unassigned (“Not Used”) or “Reserved” bits within a used register should be ignored, except that they should be written as zero when the register is written.

Usually, when the state of A10 is equal to the value of 0, A10-A0 represents a register address used for the transmit direction, while the value of 1 in A10 indicates a register address used for the receive direction. Similarly, address bits A9 and A8 define functional memory segments, as described in the table below:

A9	A8	Definition
0	0	Common locations
0	1	STM-1 VC-4 or STS-3 STS-1 No. 1 locations
1	0	STS-3 STS-1 No. 2 locations
1	1	STS-3 STS-1 No. 3 locations

Address bits A7 through A0 are used to differentiate the various functions (e.g., performance counters) within the receive and transmit segments, as described in the table below:

Address in Hex	Definition
000 - 009	Manufacturer and device ID registers & user scratch pad
00A - 01F	Common control and alarm registers
020 - 025	Transmit common control registers
026 - 03F	Transmit TU/VT unequipped generation control registers
040 - 04F	Not used
050 - 05F	Not used
060 - 0FF	Transmit control and alarm registers
100 - 1FF	Transmit STM-1 VC-4 or STS-3 STS-1 No. 1 registers
200 - 2FF	Transmit STS-3 STS-1 No. 2 registers
300 - 3FF	Transmit STS-3 STS-1 No. 3 registers
400 - 40F	Receive common control registers
410 - 42F	Not used
430 - 43F	Not used
440 - 4FF	Receive control and alarm registers
500 - 5FF	Receive STM-1 VC-4 or STS-3 STS-1 No. 1 registers
600 - 6FF	Receive STS-3 STS-1 No. 2 registers
700 - 7FF	Receive STS-3 STS-1 No. 3 registers

The numbering convention used in this document for transmit and receive SDH/SONET bytes, and their relationship to bits in a memory map location, unless otherwise specified, is shown below.

SDH/SONET byte

Bit	1	2	3	4	5	6	7	8

Bit 1 is the Most Significant Bit (MSB), and is the first bit transmitted and received (e.g., SONET/SDH Serial Interface). This is also the convention used when making reference to SONET/SDH bytes.

Register byte

Bit	7	6	5	4	3	2	1	0

Bit 1 from SDH/SONET byte is mapped into bit 7 in a memory map register byte.

COMMON MEMORY MAP SEGMENTS

Manufacturer and Device ID & user scratch pad

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	0	1	1	1	0	0	0	0
002	R	0	1	1	1	1	1	0	1
003	R	Revision Level				0	0	0	1
004	R	0000				0000			
005 to 009	R/W	User-Defined (e.g., scratch pad - 5 bytes)							

Description

The manufacturer and device identification are based on the field format given in IEEE standard 1149.1 on Boundary Scan, and the ID assigned by the Solid State Products Engineering Council (JEDEC) to the TranSwitch Corporation. The serial format for this ID, which is located in registers 003H through 000H, is shown below with bit 7 of register 003H at the left and bit 0 of register 000H at the right:

MSB LSB

Revision	Part Number	Manufacturer Identifier	1
4 bits	16 bits	11 bits	

The manufacturer ID assigned for TranSwitch devices is defined as 107 Decimal, located in bits 7 through 1 (LSB) of register 000H, and bits 3 (MSB) through 0 of register 001H. The part number of the PHAST-3N is 06103, which is expressed as a binary number in bits 7 through 4 (LSB) in register 001H, bits 7 through 0 in 002H, and bits 3 (MSB) through 0 in 003H. The revision field occupies bits 7 through 4 (LSB) in register 003H. The registers at addresses from 005H to 009H are read/write locations that are allocated as a scratch pad for the user.

Common Control Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00A	R/W	RESETS	RESETC	RESETH					
00B	R/W	STS3	RING	RINGC	BLKS	BLKL	BLKP	AUGB3	CROV
00C	R/W	SCRMD	J0S16		TOHS2	TOHS1	TOHS0	INRT1	INRT0
00D	R/W			TCDL	TCBLK				
00E	R/W	J11S1	J11S0	J12S1	J12S0	J13S1	J13S0		
00F	R/W	DLBK	TLBK			SLBK1	SLBK2	SLBK3	
010	R/W				B1DIS	FRENB	TDRV2	TDRV1	HINT
011	R/W						TPSFC	TPG1	TPG0
012	R/W							SDLBK	ULBK
013 to 016		Reserved							
017	R/W							TBUSY	RBUSY
018		Reserved							

Description

Address	Bit	Symbol	Description
00A	7	RESETS	**Software Reset:** A 1 written to this control bit causes the internal FIFOs to be reset to preset values, internal logic and counters are preset to defined values. RESETS will automatically reset to 0 once the reset action is complete. Items to note: • Internal Processors ARE NOT affected and therefore firmware does not have to be re-loaded. • Configurable control and mask registers ARE NOT affected. • Performance Counters must be reset after a software reset. Apply the Performance Counter Reset (RESETC), at least 10 ms after the Software Reset (RESETS) is applied. • The following latched alarms will be set when the software reset function is complete: • Receive Out of Frame (ROOF; bit 5 in register 4F9H) • Receive Loss of Frame Alignment (RLOF; bit 4 in register 4F9H) • Receive Line AIS (RLAIS; bit 7 in register 4FBH) • Receive Line Loss of Clock (RLLOC; bit 6 in register 4F9H) • Receive Reference Loss of Clock (RRLOC; bit 1 in register 4FBH) if receive retiming is enabled (RTBYP=0). • Transmit Loss of Clock (TLOC; bit 7 in register 0F9H) • Transmit Reference Loss of Clock (TRLOC; bit 3 in register 0F9H) if transmit retiming is enabled (TTBYP=0).
	6	RESETC	**Performance Counter Reset:** A 1 written to this control bit causes all performance counters to be reset to zero when configured in saturating mode (CROV=0, bit 0 in register 00BH), or reset to FE/FEFF hex values (8/16 bit) when configured in rollover mode (CROV=1). RESETC will automatically reset to 0 once the reset action is complete.
	5	RESETH	**Hardware Reset:** A 1 written to this control bit causes the device to halt all processing and puts it in a state in which the firmware MUST be downloaded (see Firmware Download Procedure on page 132). Once the firmware download is complete the internal FIFOs will be reset to preset values, internal logic and counters are preset to defined values. All configurable control and mask registers are reset/preset to values defined in the Power-Up and Initialization section (see page 136). Performance Counters are all reset to zero. Counters will start in rollover mode since control bit CROV (bit 0 in register 00BH) defaults to zero after a hardware reset. RESETH will automatically reset to 0 once the reset action is complete.
	4-0		**Not Used:**

Address	Bit	Symbol	Description
00B	7	STS3	**STS-3 Mode Selection:** The SDH/SONET frame format selection is made according to the table shown below. STS3 Format Selected 1 STS-3 (STM-1 AU-3) format 0 STM-1 AU-4 (STS-3c) format
	6	RING	**Line Protected Ring Applications Enable:** A 0 configures the PHAST-3N for normal operation. A 1 enables the ring mode. In this mode of operation the transmit line REI (FEBE) value and line RDI value are controlled by the mate PHAST-3N using the Alarm Indication Port.
	5	RINGC	**Count B2 and Line REI Errors AIP Interface (Ring Mode):** A 1 enables the B2 and line REI (FEBE) performance counters to count the B2 error and line REI (FEBE) values present at the AIP interface when control bit RING (bit 6) is 1. A 0 enables the B2 error and line REI (FEBE) performance counters to count errors from the receive side independent of the state of the RING control bit.
	4	BLKS	**Block Count Section:** A 0 configures the B1 counter to count individual bit errors. A 1 configures the B1 counter to count one or more bit errors per frame as single block errors.
	3	BLKL	**Block Count Line:** A 0 configures the B2 and line REI (FEBE) counters to count individual bit errors. A 1 configures the B2 and line REI (FEBE) counters to count one or more bit errors per frame as a single block error.
	2	BLKP	**Block Count Path:** A 0 configures the B3 and path REI (FEBE) counters to count individual bit errors. A 1 configures the B3 and path REI (FEBE) counters to count one or more bit errors per frame as a single block error.
	1	AUGB3	**Disable B3 Calculation for Stuff Columns:** Enabled when control bit STS3 (bit 7) is a 1. A 1 disables the B3 parity detection and generation for the two stuff columns in the STS-1 format (i.e., columns 30 and 59).
	0	CROV	**Counters Roll-Over Enable:** A 0 configures all counters to be saturating unless otherwise noted. That is, all counters will stop at their specified maximum count value. A microprocessor read cycle will clear the respective saturating counter that is read. A 1 configures all counters to function in the roll-over mode. That is, when the maximum count is reached in a counter, the next count causes it to roll over and start at a count of 0. A microprocessor read cycle does not clear the counters when the counters are configured in the roll-over mode. For a detailed description please see the Performance Counters section on page 78.

Address	Bit	Symbol	Description
00C	7	SCRMD	**SDH/SONET Scrambler and Descrambler Disabled:** This bit is enabled when either the line side byte-parallel interface is selected or the bit-serial interface is selected. A 0 enables the SDH/SONET scrambler and descrambler. A 1 disables the scrambler and descrambler. Items to note when SCRMD=1 1) The receive loss of signal (RLOS) detection circuit is also disabled. 2) Always apply a RESETS (bit 7, register 00AH) after setting SCRMD to 1 to clear out any RLOS alarm that may have been present. 3) Clock Recovery cannot be used with an unscrambled input signal because there will not be enough transition density on the incoming signal and therefore CRBYP (lead No. H3) must be set to a high state. In addition the descrambler is disabled (for the serial or byte-parallel line side interface) when any of the following alarms occur: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm
	6	J0S16	**J0 (C1) message Size Bit Selection:** Common bit for selecting the message size of the J0 byte for both the receive and transmit directions. A 0 selects a single byte (ANSI), while a 1 configures the J0 byte to be 16-byte message (ETSI).
	5		**Not Used:**
	4 3 2	TOHS2 TOHS1 TOHS0	**TOH Byte Indication Selection:** A TOH marker pulse is provided for both the receive and transmit TOH byte interfaces. The marker pulse enables downstream circuitry to multiplex or demultiplex the selected TOH byte from the TOH byte serial bit interface stream. The following table selects the TOH byte marker indication that will be present on leads TTOHM and RTOHM. The indication is active for the TOH byte period indicated. TOHS2 TOHS1 TOHS0 Action 0 0 0 No byte marker selected 0 0 1 J0 (C1) byte 0 1 0 D1 - D3 bytes 0 1 1 D4 - D12 bytes 1 0 0 E1 byte 1 0 1 E2 byte 1 1 0 K1 and K2 bytes 1 1 1 F1 byte

Address	Bit	Symbol	Description
00C (cont.)	1 0	INRT1 INRT0	**Event Bit Transition:** An event bit (latched alarm) will latch on an alarm according to the states given in the table below: INRT1 INRT0 Action 0 0 All event bits latch on the positive level of an alarm 0 1 All event bits latch on the positive transition of an alarm 1 0 All event bits latch on the negative transition of an alarm 1 1 All event bits latch on the positive/negative transitions of an alarm
00D	7-6		**Not Used:**
	5	TCDL	**Tandem Connection Data Link Selection:** Common control bit for both the receive and transmit sides, which enables processing of bits 5 through 8 of the N1 byte. TCDL Action 0 In the receive direction, no ETSI message/OEI/REI processing. N1 byte bits 5 through 8 are mapped transparently from the line to terminal. In the transmit direction, no ETSI message/OEI/REI processing. N1 byte bits 5 through 8 operate according to PTE1 control bit (bit 7 in register 142H). 1 In the receive direction, ETSI message/OEI/REI is processed. N1 byte bits 5 through 8 are mapped transparently from the line to terminal. In the transmit direction, ETSI message/OEI/REI is processed independent of PTE1 control bit (bit 7 in register 142H). Please note that the control bit RTCEN (bit 0 in register 445H) enables receive side action and control bit TTCEN (bit 7 in register 064H) enables transmit side action.
	4	TCBLK	**Tandem Connection IEC Block Count Select:** A 1 configures the IEC bit and block counters to count one or more bit errors as a single block error. A 0 configures the IEC bit and block counters to count bit errors.
	3-0		**Not Used:**

Address	Bit	Symbol	Description
00E	7 6	J11S1 J11S0	**J11 Byte Message Selection Bits:** Common control bits for both the receive and transmit sides for the STM-1 VC-4 or STS-1 No. 1 format. The J1 byte is processed according to the following table. J11S1 / J11S0 / Action 0 0 — J1 byte RAM segment configured for a 64-byte message size. No comparison is performed. Received J1 bytes are written into the RAM locations on a rotating basis with an arbitrary starting address. 0 1 — J1 byte RAM segment configured for a 64-byte message size. No comparison is performed. Receiving an ASCII CR/LF, in sequence, will synchronize a counter such that the next J1 byte after the last LF is written into the starting address location of the RAM segment. The J1 alarms (J11LOL and J11TIM) are disabled. 1 0 — J1 RAM location segment is configured for a 16-byte message size. Received J1 bytes are written into the RAM segment on a rotating basis for a microprocessor read cycle. The J1 alarms (J11LOL and J11TIM) are disabled. 1 1 — J1 RAM location is configured for a 16-byte message size and a comparison. TIM comparison is performed against a microprocessor-written 16 byte message. The message must be written starting with the CRC-7 as the first byte in the segment. A CRC-7 calculation is not performed. The loss of lock (J11LOL) and mismatch (J11TIM) alarms are enabled.
	5 4	J12S1 J12S0	**J12 Byte Message Selection Bits:** Common control bits for both the receive and transmit sides for the STS-3 STS-1 No. 2 formats. These bits are disabled for the STM-1 AU-4 format. The J1 byte is processed according to the above table.
	3 2	J13S1 J13S0	**J13 Byte Message Selection Bits:** Common control bits for both the receive and transmit sides for the STS-3 STS-1 No. 3 formats. These bits are disabled for the STM-1 AU-4 format. The J1 byte is processed according to the above table.
	1-0		**Not Used:**

Address	Bit	Symbol	Description
00F	7	DLBK	**Device Line Loopback:** When the serial interface is selected, writing a 1 to this control bit loops back the transmit data (and clock) in a parallel format to the receive side, and continues to transmit the data. The receive pseudo-ECL serial data input is disabled. See Figure 40 on page 127. When the parallel interface is selected, writing a 1 to this control bit loops back the transmit parallel data (and clock) to the receive input, and continues to transmit the data. The receive parallel input is disabled. Note: always apply a RESETS (Register 00A, bit 7) after turning on this loopback to clear out any LOS alarms that may be present.
	6	TLBK	**Terminal Loopback:** A terminal side receive to transmit loopback is enabled when a 1 is written to this control bit. When enabled, terminal side data, clock, SPE, and C1J1 are internally connected to the transmit input. The receive terminal output signals are provided. Control bit TTCIV (bit 3 in register 022H) must be set to 0 when this loopback is enabled. Additionally, when the source timing mode is selected, the transmit retiming block must be enabled by setting control bit TTBYP (bit 3 in register 021H) to 0. See Figure 40 on page 127. For Terminal loopback or STS-1 source timing mode, the transmit H4 mode must be either “terminal interface”, or “locked to terminal interface”. Memory map, or V1 pulse options cannot be used.
	5-4		**Not Used:**
	3 2 1	SLBK1 SLBK2 SLBK3	**STS-3 STS-n Terminal Loopback:** A 1 written to control bit SLBKn will cause the n numbered STS-1 to be internally looped back, with the receive output connected to the transmit input. The receive terminal output signals will continue to be provided. These loopback control bits are enabled when control bit TTBYP (bit 3 in register 021H) is a 0 (transmit retiming feature is enabled). See Figure 40 on page 127. For Terminal loopback or STS-1 source timing mode, the transmit H4 mode must be either “terminal interface”, or “locked to terminal interface”. Memory map, or V1 pulse options cannot be used.
	0		**Not Used:**

Address	Bit	Symbol	Description
010	7-5		**Not Used:**
	4	B1DIS	**B1 Byte BIP Detection Disabled:** This control bit is enabled when either the SDH/SONET parallel or serial interfaces are selected. A 0 enables the B1 BIP parity calculation and generation. A 1 disables the B1 BIP parity calculation and generation. When disabled, the receive line side B1 byte can be used to carry an upstream B1 error count. Each bit in the B1 byte in each frame will be either counted as one error, or the combined errors will be counted as one block error, using the B1 performance counter, as configured by control bit BLKS (bit 4 in register 00BH). In the transmit direction the value written by the microprocessor to the transmit TOH B1 byte location is transmitted (when control bit TOHB1E equals 0) or the B1 byte from the TOH interface is transmitted (when control bit TOHB1E equals 1). Note that control bit B1EME and the Error Repetition control register are inoperative.
	3	FRENB	**Receive and Transmit FIFO Auto Reset Enable:** A 0 disables the receive and transmit FIFO (retiming circuits) from automatically resetting when an overflow/underflow alarm is detected. A 1 enables the FIFO to automatically reset upon an overflow/underflow alarm.
	2	TDRV2	**External Drive Bit No. 2 Control:** This bit controls the state of the EXCN2 output lead. A 1 causes the EXCN2 lead to be high.
	1	TDRV1	**External Drive Bit No. 1 Control:** This bit controls the state of the EXCN1 output lead. A 1 causes the EXCN1 lead to be high.
	0	HINT	**Hardware Interrupt Enable:** A 1 enables a hardware interrupt to occur on an active event (latched) bit provided the corresponding interrupt mask enable bit for the alarm is set to a 1. A 0 disables the hardware interrupt lead.

Address	Bit	Symbol	Description
011	7-3		**Not Used:**
	2	TPSFC	**Test Pattern Stuff Column Control:** In the STS-3 mode, corresponding to each STS-1 for which the PRBS generator is enabled, TFSn control bit (bits 6, 5 and 4 in register 020H) are disabled. In STM-1 AU4 mode, all these TFSn control bits are disabled when the PRBS generator is enabled. TPSFC — Action 0 — When control bit STS3 is a 0: Columns 2, 3, 4, 5, 6, 7, 8 and 9 are transmitted intact from the terminal side. When control bit STS3 is a 1: columns 30 and 59 for the STS-3 STS-1 selected are transmitted intact from the terminal side. The analyzer will ignore these columns. 1 — When control bit STS3 is a 0: Columns 2, 3, 4, 5, 6, 7, 8 and 9 are transmitted with the PRBS pattern when enabled. When control bit STS3 is a 1: columns 30 and 59 for the STS-3 STS-1 selected are transmitted with the PRBS pattern when enabled. The analyzer will include these columns when checking the incoming data.
	1 0	TPG1 TPG0	**PRBS Test Generator Selection:** The bits in the following table enable the PRBS (2^{23}-1) test generator and, in conjunction with the STS3 control bit (bit 7 in register 00BH), determine in which format the PRBS generator will insert the pattern, and which format the test analyzer will monitor. Please note that the test analyzer is enabled when control bit TPAON (bit 0 in register 405H) is a 1. Line AIS, path AIS, and unequipped generation override the PRBS generator. TPG1 — TPG0 — Action 0 — 0 — PRBS test generator is disabled. 0 — 1 — PRBS pattern inserted into the VC-4 when control bit STS3 is a 0; when control bit STS3 is a 1, selects STS-3 STS-1 No. 1 for PRBS insertion. 1 — 0 — PRBS pattern inserted into the STS-3 STS-1 No.2 when control bit STS3 is a 1. In the receive direction, the STS-3 STS-1 No. 2 format is selected for the analyzer when control bit STS-3 is a 1. 1 — 1 — PRBS pattern inserted into the STS-3 STS-1 No.3 when control bit STS3 is a 1. In the receive direction, the STS-3 STS-1 No. 3 format is selected for the analyzer when control bit STS-3 is a 1.

Address	Bit	Symbol	Description
012	7-2		**Not Used:**
	1	SDLBK	**Serial Device Line Loopback:** Writing a 1 to this bit enables the transmit serial data only to be looped back to the input of the Clock Recovery block. Transmit data and clock outputs will continue to be provided. This loopback is valid only for the serial line interface, and only when the Clock Recovery block is enabled (CRBYP, Lead No. H3 is a 0). See Figure 40 on page 127.
	0	ULBK	**Upstream Line Loopback:** Writing a 1 to this bit enables an upstream line loopback in the serial mode only. The received serial data and clock is looped back as transmit data and clock. The internal transmit path is disabled prior to the output. This loopback is valid for either clock recovery mode. See Figure 40 on page 127.
013-016	7-0		**Not Used:**
017	7-2		**Not used**
	1	TBUSY	**Transmit Processor Busy:** Used when the external microprocessor needs to access a register located in Transmit RAM (shaded "***Italic Bold type face***" in the Memory Map). A 1 in this bit indicates that the transmit ACE processor is busy processing and should not be interrupted by the external microprocessor to access a transmit RAM location. A 0 in this bit indicates that the external microprocessor should access the transmit RAM locations.
	0	RBUSY	**Receive Processor Busy:** Used when the external microprocessor needs to access a register located in Receive RAM (shaded "Regular Type Face" in the Memory Map). A 1 in this bit indicates that the receive ACE processor is busy processing and should not be interrupted by the external microprocessor to access a receive RAM location. A 0 in this bit indicates that the external microprocessor should access the receive RAM locations.

Software Polling Bits

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
019	R	SINTR	SINTT	SINTA	SINTG	SINTP1	SINTP2	SINTP3	SINTF

Description

Address	Bit	Symbol	Description
019	7	SINTR	**Software Polling bit - TOH level Alarms:** A SINTR indication is set when one of the following latched alarms occurs and the corresponding mask bit is set to 1: • External Scan Alarm 1 (SCAN1) • External Scan Alarm 2 (SCAN2) • Receive Loss Of Signal (RLOS) • Receive Line Loss Of Clock (RLLOC) • Receive Out Of Frame (ROOF) • Receive Loss Of Frame (RLOF) • External SDH/SONET Line Failure (SLFAIL) • Receive J0 Loss Of Lock (J0LOL) • Receive J0 Trace Mismatch (J0TIM) • B2 Bit Error Rate exceeded (B2BER) • Receive Line AIS (RLAIS) • Receive APS (RAPS) • Receive New APS (RNAPS) • Receive Line RDI (RLRDI) • Alarm Indication Port New APS (APNAPS) • Alarm Indication Port Loss of Frame Indication (APLOF) • Alarm Indication Port Loss of Signal Indication (APLOS) • Alarm Indication Port Line RDI (APLRDI) • Receive False Concatenation (RFHID) • Receive Line Parity Error (RLPERR) • Change in S1 byte value (SSMBC) • Test Pattern Out of Lock alarm (TPOOL) • Receive Clock Recovery Frequency Alarm (RROOL) • Receive Clock Recovery Loss Of Data Alarm (RDOOL)
	6	SINTT	**Software Polling Bit - Transmit Alarms:** A SINTT indication is set when one of the following latched alarms occurs and the corresponding mask bit is set to 1: • Transmit Loss Of Clock (TLOC) • Transmit Loss Of Signal (TLOS) • Transmit Parity Error (TPERR) • Transmit E1 Byte AIS Indication (TE1nAIS) • Transmit H4 Out Of Multiframe (TnOOM) • Transmit H4 Loss Of Multiframe (TnLOM) • Transmit H1/H2 AIS Indication (THnAIS)

Address	Bit	Symbol	Description
019 (cont.)	5	SINTA	**Software Polling Bit - Clocks, CRC-4 and Count Alarms:** A SINTA indication is set when one of the following latched alarms occurs and the corresponding mask bit is set to 1: • Receive Reference Loss Of Clock (RRLOC) • Transmit Reference Loss Of Clock (TRLOC) • Alarm Port Interface Loss Of Clock (APLOC) • Alarm Port Interface CRC-4 Error (APCRC) • Counter saturating at maximum count (COUNT)
	4	SINTG	**Software Polling Bit - Tandem Connection Alarms:** A SINTG indication is set when one of the following latched alarms occurs. Please note that the corresponding mask bit must be set to 1 and the tandem connection feature enabled for a polling indication to occur. • Tandem Connection Loss Of Frame (TCLOF) • Tandem Connection Loss Of Lock (TCLOL) • Tandem Connection Trace Mismatch (TCTIM) • Tandem Connection RDI (TCRDI) • Tandem Connection ODI (TCODI) • Tandem Connection Unequipped (TCUQ) • Receive Tandem Connection AIS indication (RTCAIS)

Address	Bit	Symbol	Description
019 (cont.)	3 2 1	SINTP1 SINTP2 SINTP3	**Software Polling Bit - Path Level Alarms:** A SINTPn indication is set when one of the following latched alarms occurs, and the corresponding mask bit is set to 1, where: n is 1 for an STM-1/STS-3c signal and STS-3 STS-1 No.1, n is 2 for STS-3 STS-1 No. 2, and n is 3 for STS-3 STS-1 No.3. Bit 3 is SINTP1. • Receive Path AIS (RnPAIS) • Receive Loss Of Pointer (RnLOP) • Receive New Pointer (RnNPTR) • Receive Single-Bit RDI (RnOLD) • Receive Remote Server Defect (RnSVD) • Receive Remote Payload Defect (RnPYD) • Receive Remote Connectivity Defect (RnCND) • Receive J1 Loss Of Lock (J1nLOL) • Receive J1 Trace Mismatch (J1nTIM) • B3 Error Rate Exceeded (B3nBER) • C2 Mismatch (C2nMM) • C2 PDI (C2nPDI) • VC AIS (VCnAIS) • Unequipped Status (UNEQn) • Receive Out Of Multiframe (RnOOM) • Receive Loss Of Multiframe (RnLOM) • Receive APS Byte (RPAPS) for SINTP1 only (K3 APS byte for STM-1 or STS-3 STS-1 No.1) • Alarm Indication Port (APPAPS) for SINTP1 only (K3 APS byte for STM-1 or STS-3 STS-1 No.1) • Alarm Indication Port RDI (APRDIn)
	0	SINTF	**Software Polling Bit - Receive and Transmit Retiming FIFOs:** A SINTF indication is set to 1 when one of the following latched alarms occurs, and the corresponding mask bit is set to 1: • Receive FIFO (RnFIFO) • Transmit FIFO (TnFIFO)

Common Interrupt Mask Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01A	R/W					SCAN2M	SCAN1M		CNTM
01B	R/W					RDOOLM	RROOLM		

Description

Address	Bit	Symbol	Description
01A	7-4		**Not Used:**
	3	SCAN2M	**Scan 2 Lead Mask Bit:** A 1 enables a SCAN2 alarm to cause a hardware interrupt, when enabled, and to set the software polling bit SINTR in bit 7 of register 019H. The software polling bit will be reset when the latched alarm is cleared.
	2	SCAN1M	**Scan 1 Lead Mask Bit:** A 1 enables a SCAN1 alarm to cause a hardware interrupt, when enabled, and to set the software polling bit SINTR in bit 7 of register 019H. The software polling bit will be reset when the latched alarm is cleared.
	1		**Not Used:**
	0	CNTM	**Counter Mask Bit:** A 1 enables a COUNT alarm to cause a hardware interrupt, when enabled, and to set the software polling bit SINTA in bit 5 of register 019H. The software polling bit will be reset when the latched alarm is cleared.
01B	7-4		**Not Used:**
	3	RDOOLM	**Clock Recovery Loss Of Data Alarm Mask Bit.** A 1 enables a Clock Recovery Loss Of Data alarm to cause a hardware interrupt, when enabled, and to set the software polling bit SINTR in bit 7 of register 019H. The software polling bit will be reset when the latched alarm is cleared.
	2	RROOLM	**Clock Recovery Loss Of Frequency Alarm Mask Bit.** A 1 enables a Clock Recovery Loss Of Frequency alarm to cause a hardware interrupt, when enabled, and to set the software polling bit SINTR in bit 7 of register 019H. The software polling bit will be reset when the latched alarm is cleared.
	1-0		**Not Used:**

Common Alarm Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01C	R					SCAN2	SCAN1		COUNT
01D	R(L)					SCAN2	SCAN1		COUNT
01E	R					RDOOL	RROOL		
01F	R(L)					RDOOL	RROOL		

Description

Address	Bit	Symbol	Description
01C	7-4		**Not Used:**
	3	SCAN2	**Scan 2 Alarm:** This alarm reflects the state present on the $\overline{\text{EXSN2}}$ lead. A low on the $\overline{\text{EXSN2}}$ lead will cause an alarm indication.
	2	SCAN1	**Scan 1 Alarm:** This alarm reflects the state present on the $\overline{\text{EXSN1}}$ lead. A low on the $\overline{\text{EXSN1}}$ lead will cause an alarm indication.
	1		**Not Used:**
	0	COUNT	**Count Alarm:** Enabled when control bit CROV (bit 0 in register 00BH) is either a 0 (saturating) or a 1 (roll-over). This alarm occurs when a counter is at its maximum count.
01D	7-0		The bits in this register are the same as the corresponding bit positions in register 01CH, except that each bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, as selected via control bits INRT1 and INRT0 (bits 1 and 0 in register 00CH). A latched bit position will remain set until it is cleared by a microprocessor read cycle.
01E	7-4		**Not Used:**
	3	RDOOL	**Receive Clock Recovery Loss Of Data Alarm.** Enabled when the clock recovery block is enabled. This alarm is a composite of two error conditions. This alarm occurs when there are no data transitions for 128 clock cycles or when the recovered clock is greater then 1000 ppm from the reference clock frequency. Recovery occurs when the data transition density is at least 13 transitions (10%) in a 128 clock cycle period or the recovered clock is within 250 ppm of the reference clock (CRREF).
	2	RROOL	**Receive Clock Recovery Frequency Alarm.** Enabled when the clock recovery block is enabled. This alarm occurs when the recovered clock is greater then 1000 ppm from the reference clock frequency. The alarm is cleared when the recovered clock is within 250 ppm of the reference clock (CRREF). Please note: this alarm is also or-gated with clock recovery loss of data error condition to for the RDOOL alarm.
	1-0		**Not Used:**
01F	7-0		The bits in this register are the same as the corresponding bit positions in register 01EH, except that each bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, as selected via control bits INRT1 and INRT0 (bits 1 and 0 in register 00CH). A latched bit position will remain set until it is cleared by a microprocessor read cycle.

TRANSMIT SIDE MEMORY MAP SEGMENTS

TRANSMIT COMMON REGISTERS

Transmit Common Control Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
020	R/W	TFSV4	TFS1	TFS2	TFS3	TOCI	TOB8	TFAISE	VTACT
021	R/W	TTSB1	TTSB0	TTCNT1	TTCNT0	TTBYP			
022	R/W	TPREV	TPRDO	TLREV	TLRDO	TTCIV	TTOS1	TTOS0	
023	R/W								TACERST
024	R/W							TPPOH	TPRBSE
025		Reserved							

Description

Address	Bit	Symbol	Description
020	7	TFSV4	**Transmit Fixed Stuff in VC-4 Enable:** Works in conjunction with control bits PTEn (bit 7 in register X42H) and TFSy (bits 6-4) according to the following table. Valid for the STM-1/STS-3c format (control bit STS3 is a 0) only. X can be in either state, 0 or 1. PTEn / TFSV4 / TFSy / Action 0 / X / X / POH, stuff columns, and payload bytes are mapped from terminal to line intact. 1 / 0 / 0 / No action taken on the incoming columns, mapped intact. 1 / 0 / 1 / A 1 causes zeros to be transmitted for the columns specified, otherwise the columns are transmitted intact from the terminal interface, where y=1 (TFS1) for columns 4 and 7, 2 (TFS2) for columns 5 and 8, and 3 (TFS3 for columns 6 and 9. Columns 2 and 3 are transmitted intact from the terminal. 1 / 1 / 0 / Columns 2 and 3 in the VC-4 are transmitted as zero. Other columns are transmitted intact from the terminal. 1 / 1 / 1 / Columns 2 and 3 in the VC-4 are transmitted as zero. This is followed by zeros transmitted for the columns specified. y=1 (TFS1) for columns 4 and 7, y=2 (TFS2) for columns 5 and 8, and y=3 (TFS3) for columns 6 and 9. PTE1 operates on columns 2, 3, 4 and 7. PTE2 operates on columns 5 and 8, while PTE3 operates on columns 6 and 9. PTE2 and PTE3 have no effect on columns 2 and 3.

Address	Bit	Symbol	Description
020 (cont.)	6 5 4	TFS1 TFS2 TFS3	**Transmit Stuff Control:** Works in conjunction with control bits TFSV4 (bit 7) and PTEn (bit 7 in register X42H) for STM-1 AU-4 operation as given in the table above. For STS-3 operation, the operation is given in the following table. X can be either state, 0 or 1. PTEn / TFSV4 / TFSy / Action 0 / 0 / X / POH, stuff column, and payload bytes for an STS-1 are mapped from terminal to the line intact. 1 / 0 / 0 / No action is taken on the incoming columns in the STS-1 SPEs. 1 / 0 / 1 / y = 1 (TFS1) for columns 30 and 59 for STS-1 No. 1; y = 2 (TFS2) for STS-1 No. 2; y = 3 (TFS3) for STS-1 No. 3. The specified columns (30 and 59) for the selected STS-1 will be transmitted as zeros.
	3	TOCI	**Transmit Order Wire Clock Inversion:** A 0 causes the transmit order wire data signals (TE1D and TE2D) to be clocked in on rising edge of the clock (TOWC), and the frame pulse (TOWF) to be clocked out on falling edge of the clock. A 1 causes the data (TE1D and TE2D) to be clocked in on falling edge of the clock, and the frame pulse (TOWF) to be clocked out on rising edge of the clock.
	2	TOB8	**Transmit Order Wire Frame Pulse on Bit 8 Enable:** A 0 causes the transmit order wire frame pulse (TOWF) to occur during bit 1 of the E1 and E2 bytes. A 1 causes the order wire frame pulse to occur during bit 8 of the E1 and E2 bytes.
	1	TFAISE	**Transmit Side FIFO Overflow/Underflow AIS Enable:** A 1 written to this bit enables path AIS to be generated when a transmit FIFO alarm (TnFIFO, bit 1 of register XF0H) occurs and control bits TnPAISE (bit 0 of register X01H) and FRENB (bit 3 of register 010H) are a 1. A 1 also enables a transmit FIFO re-center command (control bit TFnRST - bit 0 of register X00H) to transmit path AIS when control bit TnPAISE is a 1. Path AIS will be transmitted for a minimum of three frames. A 0 disables the alarm or re-center command from generating transmit path AIS.
	0	VTACT	**VT/TU AIS Enable:** A 1 enables a tributary AIS signal to be generated instead of an unequipped signal for the tributary VT/TU selected when an active low is placed on lead $\overline{\text{VTACT}}$ for the time slot periods that correspond to the VT/TU. A 0 enables an unequipped channel to be transmitted for the VT/TU selected.

Address	Bit	Symbol	Description
021	7 6	TTSB1 TTSB0	**Transmit Pointer SS-bit (Size bits) Value Selection:** The SS-bit states in the transmit terminal pointer (bits 5 and 6 in the H1 byte) will be generated according to the following table for either STM-1 AU-4 or STS-3 operation. TTSB1 TTSB0 Value Selected 0 0 SS-bits equal to 00 0 1 SS-bits equal to 01 1 0 SS-bits equal to 10 1 1 SS-bits equal to 11 When transmit retiming is bypassed, (control bit TTBYP, bit 3 in this register is a 1), these control bits are disabled and the SS-bits are transmitted equal to 00.
	5 4	TTCNT1 TTCNT0	**Transmit Pointer Y byte ss-bit Value Selection:** The ss-bits (bits 5 and 6) in the Y bytes for the STM-1 AU-4 transmit pointer will be generated according to the following table. These control bits are disabled when the STS-3 format is selected. TTCNT1 TTCNT0 Value Selected 0 0 ss-bits equal to 00 0 1 ss-bits equal to 01 1 0 ss-bits equal to 10 1 1 ss-bits equal to 11 When transmit retiming is bypassed, (control bit TTBYP, bit 3 in this register is a 1), these control bits are disabled and the ss-bits are transmitted equal to 00.
	3	TTBYP	**Transmit Retiming Bypass Enable:** A 0 enables transmit retiming for the VC-4 or the three STS-1s. A 1 bypasses transmit retiming. When retiming is enabled, a transmit reference clock (TRCI) and must be provided, as well as an optional frame pulse (TRFI).
	2-0		**Not Used:**
022	7	TPREV	**Transmit Terminal Odd/Even Parity Selection:** This control bit works in conjunction with the TPRDO control bit (bit 6) to provide the following parity modes for the transmit terminal interface signals for the transmit terminal timing mode. X can be either state, 0 or 1. TPREV TPRDO Action 0 0 Odd parity calculated over the TTDI(7-0), TSPE and TC1J1V1 signals. 0 1 Odd parity calculated over the TTDI(7-0) signals. 1 0 Even parity calculated over the TTDI(7-0), TSPE and TC1J1V1 signals. 1 1 Even parity calculated over the TTDI(7-0) signals. For the source timing mode, the parity calculation is the following. TPREV TPRDO Action 0 X Odd parity calculated over the TTDI(7-0) signals. 1 X Even parity calculated over the TTDI(7-0) signals.
	6	TPRDO	**Transmit Terminal Data Only Parity Enable:** A 1 selects data only for the parity calculation (see TPREV above).

Address	Bit	Symbol	Description
022 (cont.)	5	TLREV	**Transmit Line Odd/Even Parity Selection:** This control bit works in conjunction with the TLRDO control bit (bit 4) to provide the following parity modes for the transmit byte-parallel line interface signals. TLREV / TLRDO / Action 0 / 0 / Odd parity calculated over the TLDO(7-0) and TLFO signals. 0 / 1 / Odd parity calculated over the TLDO(7-0) signals. 1 / 0 / Even parity calculated over the TLDO(7-0) and TLFO signals. 1 / 1 / Even parity calculated over the TLDO(7-0) signals.
	4	TLRDO	**Transmit Line Data Only Parity Enable:** This control bit works in conjunction with the TLREV control bit (bit 5) according to the table given above.
	3	TTCIV	**Transmit Terminal Clock Inversion Control Bit:** A 1 causes the transmit terminal input signals to be clocked in on falling edges of the TTCI clock. A 0 causes the transmit terminal input signals to be clocked in on rising edges of the clock.
	2 1	TTOS1 TTOS0	**Transmit Data Byte Offset:** These two bits, in conjunction with TTCIV (bit 3), select the time delay, in clock periods, between the transmit terminal output timing signals and the input data byte TTDI(7-0), in the source timing mode, according to the following table. Please note: the TC1J1, TSPE, TPOH, and TH4B7/8 signals are always clocked out on positive transitions of TTCI. TTCIV / TTOS1 / TTOS0 / TTDI input delay after TTCI ↑ at start of J1 0 / 0 / 0 / 2 TTCI clock periods 0 / 0 / 1 / 3 TTCI clock periods 0 / 1 / 0 / 4 TTCI clock periods 0 / 1 / 1 / 5 TTCI clock periods 1 / 0 / 0 / 1.5 TTCI clock periods 1 / 0 / 1 / 2.5 TTCI clock periods 1 / 1 / 0 / 3.5 TTCI clock periods 1 / 1 / 1 / 4.5 TTCI clock periods
	0		**Not Used:**
023	7-1		**Not Used:**
	0	TACERST	**Transmit ACE Processor Reset:** A 1 resets the transmit ACE processor. This bit is self-clearing; it resets to 0 after the action is completed. Once this bit is set, the transmit ACE IRAM must be reloaded. See the software download procedure (Figure 42) for how it is used.

Address	Bit	Symbol	Description
024	7-2		**Not Used:**
	1	TPPOH	**Transmit PRBS Generator Pointer Value:** Enabled when control bits TPG1 and TPG0 (bits 1 and 0 in register 011H) are not equal to 0. Also works in conjunction with control bit PTEn (bit 7 in register X42H) according to the following table. X can be either state, 0 or 1. PTEn / TPPOH / Action 0 / X / Pointer value calculated. All POH bytes forced to 0, except the B3 byte which will be the calculated BIP-8 value. The POH bytes must be forced to zero for the B3 value to be correct. 1 / 0 / Valid POH bytes and pointer value. 1 / 1 / Pointer and SPE transmitted with the pointer value of 522 when retiming is bypassed or when the source timing mode is selected. Independent of retiming and source / normal timing, all POH bytes are forced to 0, except the B3 byte, which will be the calculated BIP-8 value.
	0	TPRBSE	**Transmit PRBS Error:** When the PRBS generator is enabled by control bits TPG1 and TPG0 (bits 1 and 0 in register 011H), a 1 inserts a single error into the transmitted PRBS pattern. To send another error, a 0 must first be written into this bit position, followed by a 1.

Transmit TU/VT Unequipped or AIS Generation Control Registers

Please refer to the TU-N/VTN Tributary Unequipped Status and AIS Generation subsection of the Operation section for more information about the use of these control registers.

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
026		Reserved							
027	R/W	TUG3A					T3AUE		
028	R/W	TGA211	TGA210	TGA221	TGA220	TGA231	TGA230	TGA241	TGA240
029	R/W	TGA251	TGA250	TGA261	TGA260	TGA271	TGA270		
02A	R/W	TU1A1	TU2A1	TU3A1	TU4A1	TU5A1	TU6A1	TU7A1	
02B	R/W	TU1A2	TU2A2	TU3A2	TU4A2	TU5A2	TU6A2	TU7A2	
02C	R/W	TU1A3	TU2A3	TU3A3	TU4A3	TU5A3	TU6A3	TU7A3	
02D	R/W	TU1A4	TU2A4	TU3A4	TU4A4	TU5A4	TU6A4	TU7A4	
02E		Reserved							
02F	R/W	TUG3B					T3BUE		
030	R/W	TGB211	TGB210	TGB221	TGB220	TGB231	TGB230	TGB241	TGB240
031	R/W	TGB251	TGB250	TGB261	TGB260	TGB271	TGB270		
032	R/W	TU1B1	TU2B1	TU3B1	TU4B1	TU5B1	TU6B1	TU7B1	
033	R/W	TU1B2	TU2B2	TU3B2	TU4B2	TU5B2	TU6B2	TU7B2	
034	R/W	TU1B3	TU2B3	TU3B3	TU4B3	TU5B3	TU6B3	TU7B3	
035	R/W	TU1B4	TU2B4	TU3B4	TU4B4	TU5B4	TU6B4	TU7B4	
036		Reserved							
037	R/W	TUG3C					T3CUE		
038	R/W	TGC211	TGC210	TGC221	TGC220	TGC231	TGC230	TGC241	TGC240
039	R/W	TGC251	TGC250	TGC261	TGC260	TGC271	TGC270		
03A	R/W	TU1C1	TU2C1	TU3C1	TU4C1	TU5C1	TU6C1	TU7C1	
03B	R/W	TU1C2	TU2C2	TU3C2	TU4C2	TU5C2	TU6C2	TU7C2	
03C	R/W	TU1C3	TU2C3	TU3C3	TU4C3	TU5C3	TU6C3	TU7C3	
03D	R/W	TU1C4	TU2C4	TU3C4	TU4C4	TU5C4	TU6C4	TU7C4	
03E to 05F		Reserved							

Description

Address	Bit	Symbol	Description
027	7	TUG3A	**TUG-3 A Select:** A 1 selects TUG-3 A. A 1 enables an unequipped status (or AIS) to be generated for TUG-3 A. This bit must be set, in addition to T3AUE (also in this register), in order to send unequipped or AIS.
	6-3		**Not Used:**
	2	T3AUE	**TUG-3 A Unequipped Generation:** A 1 enables an unequipped status (or AIS) to be generated for TUG-3 A. This bit must be set, in addition to control bit TUG3A (also in this register), in order to send unequipped or AIS.
	1-0		**Not Used:**
028 029	7-0 7-2	TGA2ny1, TGA2ny0 in pairs for (n = 1 - 7)	**TU-2/TU-12/TU-11 (VT6/VT2/VT1.5) Selection Enable for TUG-2s (VT Groups) in TUG-3 A (STS-1 No. 1):** The TUG-2 (VT Group) number is represented by n, with values from 1 to 7. For example, bits 7 (y1) and 6 (y0) in register 028H determine the tributary (VT) type carried in TUG-2/VT group 1 in TUG-3 A (STS-1 No. 1). The y1 and y0 values select the TU-2 (VT6), TU-12 (VT2) or TU-11 (VT1.5) used within the TUG-2 (VT Group), according to the following table: y1 y0 TU/VT Selected 0 0 TU-12 (VT2) 0 1 TU-2 (VT6) 1 0 Not Used 1 1 TU-11 (VT1.5)
	1-0		**Not Used:**
02A 02B 02C 02D	7-1 7-1 7-1 7-1 (bit 0 is not used)	TUnA1 TUnA2 TUnA3 TUnA4 (n = 1 - 7)	**Send Unequipped Status (or AIS) for the Tributaries (or VTs) Selected in TUG-3 A (STS-1 No. 1):** The tributary (VT) type for the TUG-2 (VT Group) number n in TUG-3 A (STS-1 No. 1) is selected by the control bits in registers 028H and 029H. These four registers determine which tributaries (or VTs) within the TUG-2s (VT Groups) will be enabled. There may be four TU-11s (VT1.5s), three TU-12s (VT2s) or one TU-2 (VT6) within each numbered TUG-2 (VT Group). For example, when a TU-11 (VT1.5) is selected in registers 028H/029H for a TUG-2 (VT Group), control bits TUnA1-TUnA4 select TU-11 (VT1.5) numbers 1 to 4. If a TU-12 (VT2) is selected by registers 028H/029H, control bits TUnA1-TUnA3 select TU-12 (VT2) numbers 1 to 3. Control bit TUnA4 is disabled. For a TU-2 (VT6) selection, only control bit TUnA1 is enabled.

Address	Bit	Symbol	Description
02F	7	TUG3B	**TUG-3 B Select:** A 1 selects TUG-3 B. A 1 enables an unequipped status (or AIS) to be generated for TUG-3 B. This bit must be set, in addition to T3BUE (also in this register), in order to send unequipped or AIS.
	6-3		**Not Used:**
	2	T3BUE	**TUG-3 B Equipped Generation:** A 1 enables an unequipped status (or AIS) to be generated for TUG-3 B. This bit must be set, in addition to control bit TUG3B (also in this register), in order to send unequipped or AIS.
	1-0		**Not Used:**
030 031	7-0 7-2	TGB2ny1, TGB2ny0 in pairs for (n = 1 - 7)	**TU-2/TU-12/TU-11 (VT6/VT2/VT1.5) Selection Enable for TUG-2s (VT Groups) in TUG-3 B (STS-1 No. 2):** The TUG-2 (VT Group) number is represented by n, with values from 1 to 7. For example, bits 7 (y1) and 6 (y0) in register 030H determine the tributary (VT) type carried in TUG-2/VT group 1 in TUG-3 B (STS-1 No. 2). The y1 and y0 values select the TU-2 (VT6), TU-12 (VT2) or TU-11 (VT1.5) used within the TUG-2 (VT), according to the following table: y1 y0 TU/VT Selected 0 0 TU-12 (VT2) 0 1 TU-2 (VT6) 1 0 Not Used 1 1 TU-11 (VT1.5)
	1-0		**Not Used:**
032 033 034 035	7-1 7-1 7-1 7-1 (bit 0 is not used)	TUnB1 TUnB2 TUnB3 TUnB4 (n = 1 - 7)	**Send Unequipped Status (or AIS) for the Tributaries (or VTs) Selected in TUG-3 B (STS-1 No. 2):** The tributary (VT) type for the TUG-2 (VT Group) number n in TUG-3 B (STS-1 No. 2) is selected by the control bits in registers 030H and 031H. These four registers determine which tributaries (or VTs) within the TUG-2s (VT Groups) will be enabled. There may be four TU-11s (VT1.5s), three TU-12s (VT2s), or one TU-2 (VT6) within each numbered TUG-2 (VT Group). For example, when a TU-11 (VT1.5) is selected in registers 030H/031H for a TUG-2 (VT Group), control bits TUnB1-TUnB4 select TU-11 (VT1.5) numbers 1 to 4. If a TU-12 (VT2) is selected by registers 030H/031H, control bits TUnB1-TUnB3 select TU-12 (VT2) numbers 1 to 3. Control bit TUnB4 is disabled. For a TU-2 (VT6) selection, only control bit TUnB1 is enabled.

Address	Bit	Symbol	Description
037	7	TUG3C	**TUG-3 C Select:** A 1 selects TUG-3 C. A 1 enables an unequipped status (or AIS) to be generated for TUG-3 C. This bit must be set, in addition to T3CUE (also in this register), in order to send unequipped or AIS.
	6-3		**Not Used:**
	2	T3CUE	**TUG-3 C Equipped Generation:** A 1 enables an unequipped status (or AIS) to be generated for TUG-3 C. This bit must be set, in addition to control bit TUG3C (also in this register), in order to send unequipped or AIS.
	1-0		**Not Used:**
038 039	7-0 7-2	TGC2ny1, TGC2ny0 in pairs for (n = 1 - 7)	**TU-2/TU-12/TU-11 (VT6/VT2/VT1.5) Selection Enable for TUG-2s (VT Groups) in TUG-3 C (STS-1 No. 3):** The TUG-2 (VT Group) number is represented by n, with values from 1 to 7. For example, bits 7 (y1) and 6 (y0) in register 038H determine the tributary (VT) type carried in TUG-2/VT group 1 in TUG-3 C (STS-1 No. 3) The y1 and y0 values select the TU-2 (VT6), TU-12 (VT2) or TU-11 (VT1.5) used within the TUG-2 (VT), according to the following table: y1 y0 TU/VT Selected 0 0 TU-12 (VT2) 0 1 TU-2 (VT6) 1 0 Not Used 1 1 TU-11 (VT1.5)
	1-0		**Not Used:**
03A 03B 03C 03D	7-1 7-1 7-1 7-1 (bit 0 is not used)	TUnC1 TUnC2 TUnC3 TUnC4 (n = 1 - 7)	**Send Unequipped Status (or AIS) for the Tributaries (or VTs) Selected in TUG-3 C (STS-1 No. 3):** The tributary (VT) type for the TUG-2 (VT Group) number n in TUG-3 C (STS-1 No. 3) is selected by the control bits in registers 038H and 039H. These four registers determine which tributaries (or VTs) within the TUG-2s (VT Groups) will be enabled. There may be four TU-11s (VT1.5s), three TU-12s (VT2s) or one TU-2 (VT6) within each numbered TUG-2 (VT Group). For example, when a TU-11 (VT1.5) is selected in registers 038H/039H for a TUG-2 (VT Group), control bits TUnC1-TUnC4 select TU-11 (VT1.5) numbers 1 to 4. If a TU-12 is selected by registers 038H/039H, control bits TUnC1-TUnC3 select TU-12 (VT2) numbers 1 to 3. Control bit TUnC4 is disabled. For a TU-2 (VT6) selection, only control bit TUnC1 is enabled.

Transmit TOH Control Registers

Note that if the TOH RAM is the selected source, the control bit(s) which select the TOH RAM as the source must be written first, followed by a write of the value(s) to be transmitted.

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
060	R/W	***TLA1A2E***	***TOHAAE***	***TOHJ0E***		***TOHB1E***		***TOHE1E***	***E1INE***
061	R/W	***TOHF1E***		***TRPTR***	***TOHHBE***	***TOHB2E***	***TOHKBE***	***TAPSE***	
062	R/W	***TOHDE***	***TSBE***	***TLBE***	***TOHE2E***	***E2INE***	***TOHS1E***		
063	R/W	***TOHM1E***				***TSAISE***	***E1AISE***	***TLRDIE***	***HAISE***
064	R/W	***TTCEN***	***TTAEN***	***TCRDIE***	***TCODIE***	***TTCNZ***			
065	R/W	***TTRDI***	***TTODI***			***TRLAIS***	***TRLRDI***		
066	R/W	***B1EME***	***B2EME***	***B3EME***					
067	R/W	***RDIO***						***TLAISE***	
068 to 06F		***Reserved***							
070	R/W	***Error Repetition Control Register, 00 (no errored frame sent) to FF Hex (continuous errors)***							
071	R/W	***Transmit Frame 73, 74, 75, 76 ETSI Message Spare Bits***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
060	7	TLA1A2E	**Transmit A1/A2 bytes:** Works in conjunction with control bit TOHAAE (bit 6) to provide the following transmitted generated A1/A2 bytes. X can be either state, 0 or 1. TLA1A2E / TOHAAE / Action 0 / 0 / Internally generated fixed F628H pattern 1 / 0 / Microprocessor-written value X / 1 / TOH interface byte value
	6	TOHAAE	**Transmit A1, A2 Bytes From TOH interface Enable:** Works in conjunction with control bit TLA1A2E according to the table given above.

Address	Bit	Symbol	Description
060 (cont.)	5	TOHJ0E	**Transmit J0 (C1) Byte From TOH Interface Enable:** Works in conjunction with control bit J0S16 (bit 6 in register 00CH) to provide the following actions. X can be either state, 0 or 1. TOHJ0E / J0S16 / Action 0 / 0 / Microprocessor writes the single byte to be transmitted for J0 into the Tx TOH RAM. 0 / 1 / Microprocessor writes the 16-byte message to be transmitted for J0 into the 16-byte RAM segment. 1 / X / The transmitted J0 byte is provided from the TOH interface each frame. The bytes are also written into the 16-byte RAM segment.
	4		**Not Used:**
	3	TOHB1E	**B1 Error Mask From TOH Interface Enable:** Works in conjunction with control bit B1EME (bit 7 in register 066H) to provide the following actions. X can be either state, 0 or 1. B1EME / TOHB1E / Action 0 / X / Error mask disabled. B1 BIP calculated and transmitted. 1 / 0 / Value written in the transmit TOH B1 byte location is used as an error mask to error the calculated B1 BIP for a number of frames determined by the value written to the error repetition register (070H). 1 / 1 / B1 byte from the TOH interface is used as an error mask to error the calculated BIBIP for a number of frames determined by the value written to the error repetition register (070H). The byte is also written into the memory map. See the BIP Error Mask Generation paragraph in the OPERATION section for more detail.
	2		**Not Used:**
	1	TOHE1E	**Transmit E1 Byte from the TOH Interface:** Works in conjunction with control bit E1INE (bit 0) according to the following table. X can be either state, 0 or 1. TOHE1E / E1INE / Action 0 / 0 / E1 byte memory map location transmitted X / 1 / E1 byte from the E1 Orderwire Interface transmitted. This byte is also written into the memory map. 1 / 0 / E1 byte from the TOH interface transmitted. This byte is also written into the memory map.
	0	E1INE	**Transmit E1 Byte from the E1 Byte Interface:** Works in conjunction with control bit TOHE1E bit according to the table given above.

Address	Bit	Symbol	Description
061	7	TOHF1E	**Transmit F1 Byte From TOH interface Enable:** A 1 enables the F1 byte to be transmitted from the TOH interface. The byte is also written into the memory map. A 0 enables the F1 byte to be transmitted from the memory map.
	6		**Not Used:**
	5	TRPTR	**Transmit Non-Calculated Pointer Bytes Enable:** Works in conjunction with control bit TOHHBE (bit 5) according to the following table. X can be either state, 0 or 1. TRPTR / TOHHBE / Action 0 / 0 / The transmitted H1/H2 bytes are recalculated or provided from the terminal interface (retiming circuit is bypassed) according to their POH bytes/payload location, and transmitted. Transmit TOH RAM is updated via the microprocessor interface. 1 / 0 / H1/H2 byte values from the memory map are transmitted. The H1/H2 bytes that are transmitted will have no effect on the location of the POH bytes/payload, whose position will be based on either a pointer recalculation or established by downstream circuitry. X / 1 / H1/H2 bytes from the TOH interface are transmitted. The H1/H2 bytes that are transmitted from the TOH interface will have no effect on the location of the POH bytes/payload, whose position will be based on either a pointer recalculation or established by downstream circuitry. The transmitted H3 bytes are always forced to zero, except in the case of a negative justification.
	4	TOHHBE	**Transmit H1/H2 Bytes from the TOH Interface:** Works in conjunction with control bit TRPTR according to the table given above.
	3	TOHB2E	**B2 Error Mask From TOH interface Enable:** Works in conjunction with control bit B2EME (bit 6 in register 066H) to provide the following actions. X can be either state, 0 or 1. B2EME / TOHB2E / Action 0 / X / Error mask disabled. B2 BIP calculated and transmitted. 1 / 0 / Values written in the transmit TOH B2 locations are used as an error mask to error the calculated B2 BIP for a number of frames determined by the value written to the error repetition register (070H). 1 / 1 / B2 bytes from the TOH interface are used as an error mask to error the calculated B2 BIP for a number of frames determined by the value written to the error repetition register (070H). The bytes are also written into the memory map. See the BIP Error Mask Generation paragraph in the OPERATION section for more detail.

Address	Bit	Symbol	Description
061 (cont.)	2	TOHKBE	**Transmit K1/K2 Bytes from the TOH Interface:** Works in conjunction with control bit TAPSE (bit 1) according to the following table. Please note that the transmitted K1 and K2 bytes may be modified for transmit line RDI and line AIS, as required. X can be either state, 0 or 1. TOHKBE / TAPSE / Action 0 / 0 / K1/K2 byte Tx TOH RAM locations transmitted. Line RDI and Line AIS do not modify the TOH RAM. X / 1 / K1/K2 bytes from the APS byte interface transmitted. The K1/K2 bytes are also written into the TOH RAM locations. Line RDI modifies TOH RAM but line AIS does not. 1 / 0 / K1/K2 bytes from the TOH interface transmitted. The K1/K2 bytes are also written into the TOH RAM locations. Line RDI modifies TOH RAM but Line AIS does not.
	1	TAPSE	**Transmit K1/K2 Bytes from the APS Interface:** Works in conjunction with control bit TOHKBE according to the table shown above.
	0		**Not Used:**
062	7	TOHDE	**Transmit Data Communication Bytes from the TOH Interface:** Works in conjunction with control bit TSBE (bit 6) and TLBE (bit 5) according to the following tables. X can be either state, 0 or 1. Section Data Communication Bytes: TOHDE / TSBE / Action 0 / 0 / D1-D3 data communication bytes in the memory map locations are transmitted X / 1 / D1-D3 data communication bytes from the section data communication interface are transmitted. These bytes are also written into the memory map. 1 / 0 / D1-D3 data communication bytes from the TOH interface are transmitted. The bytes are also written into the memory map. Line Data Communication Bytes: TOHDE / TLBE / Action 0 / 0 / D4-D12 data communication bytes in the memory map locations are transmitted X / 1 / D4-D12 data communication bytes from the line data communication interface are transmitted. These bytes are also written into the memory map. 1 / 0 / D4-D12 data communication bytes from the TOH interface are transmitted. The bytes are also written into the memory map.
	6	TSBE	**Transmit Section Data Communication (D1-D3) Bytes from the Section Data Communication Interface Enable:** Works in conjunction with control bit TOHDE according to the table shown above.
	5	TLBE	**Transmit Line Data Communication (D4-D12) Bytes from the Line Data Communication Interface Enable:** Works in conjunction with control bit TOHDE according to the table given above.

Address	Bit	Symbol	Description
062 (cont.)	4	TOHE2E	**Transmit E2 Byte from the TOH Interface:** Works in conjunction with control bit E2INE (bit 3) according to the following table. X can be in either state, 0 or 1. TOHE2E / E2INE / Action 0 / 0 / E2 byte memory map location transmitted X / 1 / E2 byte from the E2 byte interface transmitted. The byte is also written into the memory map. 1 / 0 / E2 byte from the TOH interface transmitted. The byte is also written into the memory map.
	3	E2INE	**Transmit E2 Byte from the E1 Byte Interface:** Works in conjunction with control bit TOHE2E according to the table shown above.
	2	TOHS1E	**Transmit S1 (Z11) Byte From TOH interface Enable:** A 1 enables the S1 byte to be transmitted from the TOH interface. A 0 enables the S1 byte to be transmitted from the memory map.
	1-0		**Not used:**
063	7	TOHM1E	**M1 Byte From TOH Interface Enable:** Works in conjunction with the RING (bit 6 in register 00BH) according to the following table. X can be either state, 0 or 1. TOHM1E / RING / Action 0 / 0 / M1 byte transmitted with received B2 error count converted to an REI (FEBE) value and also written into the memory map. 1 / 0 / M1 byte value (any value) from the TOH interface transmitted. The byte is also written into the memory map. X / 1 / M1 byte transmitted with AIP port B2 error count converted to an REI (FEBE) value. The byte is also written into the memory map.
	6-4		**Not Used:**
	3	TSAISE	**Transmit Terminal Side AIS Detection Enable:** A 1 enables the transmit terminal E1 byte and H1/H2 byte AIS detection circuits. A 0 disables these two detection circuits.
	2	E1AISE	**Transmit E1 Byte AIS Enable:** Common control bit for the three STS-1s in the STS-3 format. A 1 enables an AIS indication present in the E1n byte (in the TOH bytes) at the transmit terminal interface to generate a transmit path AIS when control bits TnPAISE (bit 0 in register X01H) and TSAISE (bit 3 in this register) are both 1, and Line AIS when TSAISE and TLAISE (address 067H, bit 1) are both 1.
	1	TLRDIE	**Transmit Line RDI Enable:** A 1 enables line RDI to be transmitted for specified alarms.
	0	HAISE	**H1/H2 Byte AIS Enable:** A 1 enables transmit path AIS transmission when an AIS condition is detected in the terminal side H1/H2 bytes and control bits TnPAISE (bit 0 in register X01H) and TSAISE (bit 3 in this register) are a 1.

Address	Bit	Symbol	Description
064	7	TTCEN	**Transmit Tandem Connection Enable:** A 1 enables the transmit tandem connection feature. Bits 5 through 8 of the N1 byte (ETSI message) are processed according to control bit TCDL (bit 5 in register 00DH). Bits 1 through 4 of the N1 byte (IEC field) are forced to zero when in path terminating mode (PTE = 1), while IEC insertion occurs when in non path terminating mode (PTE = 0). TC AIS generation overrides IEC processing when PTE = 0 or 1, but has no effect on ETSI message processing (bits 5 through 8). Path AIS, line AIS and unequipped status override all tandem connection processing.
	6	TTAEN	**Transmit Tandem Connection AIS Generation Enable:** A 1 enables a tandem connection AIS to be generated when defined alarms occur.
	5	TCRDIE	**Transmit Tandem Connection Remote Defect Indication Enable:** Enabled when control bits TTCEN (bit 7 above) and TCDL (bit 5 in register 00DH) are equal to 1. A 1 enables specified alarms to send a TC RDI.
	4	TCODIE	**Transmit Tandem Connection Outgoing Defect Indication Enable:** Enabled when control bits TTCEN and TCDL are equal to 1. A 1 enables specified alarms to send a TC ODI.
	3	TTCNZ	**Transmit Tandem Connection Zero Error Value:** A 1 causes the value 1001 to be transmitted in the IEC field when zero errors are detected. A 0 causes a 0000 to be transmitted in the IEC field when zero errors are detected.
	2-0		**Not Used:**
065	7	TTRDI	**Transmit Tandem Connection RDI:** When control bits TTCEN and TCDL are equal to 1, a 1 enables a TC RDI to be transmitted.
	6	TTODI	**Transmit Tandem Connection ODI:** When control bits TTCEN and TCDL are equal to 1, a 1 enables a TC ODI to be transmitted.
	5-4		**Not Used:**
	3	TRLAIS	**Transmit Line AIS:** A 1 causes transmit line AIS to be transmitted. Line AIS is defined as valid section overhead bytes with a scrambled all ones pattern in the remainder of the bytes.
	2	TRLRDI	**Transmit Line RDI:** Enabled when control bit RING is 0. A 1 causes a line RDI to be transmitted in the K2 byte (bits 6, 7 and 8 are equal to 110).
	1-0		**Not Used:**
066	7	B1EME	**B1 Byte Error Mask Enable Control Bit:** A 1 enables the error mask for the B1 BIP.
	6	B2EME	**B2 Byte Error Mask Enable Control Bit:** A 1 enables the error mask for the B2 BIP.
	5	B3EME	**B3 Byte Error Mask Enable Control Bit:** A 1 enables the error mask for the B3 BIP when control bit PTEn is a 1.
	4-0		**Not Used:**

Address	Bit	Symbol	Description
067	7	RDIO	**Single Bit Remote Defect Indication:** A 1 configures the transmit RDI generation block to send single-bit RDI (G1 byte, bits 5, 6 and 7 equal to 100) for alarms, ring configurations, or under microprocessor control. A 0 configures the transmit RDI block for three-bit RDI.
	6-2		**Not Used:**
	1	TLAISE	**Transmit Line AIS Enable:** A 1 enables specified transmit alarms to generate a transmit line AIS. A 0 disables the ability of line-defined alarms to generate a transmit line AIS. Please note that control bit TRLAIS (bit 3 in register 065H) overrides the state of this bit.
	0		**Not Used:**
070	7-0		**Error Repetition Control Register:** Works in conjunction with the control bits B1EME, B2EME, and B3EME (bits 7, 6 and 5 in register 066H) for sending BIP errors according to the following table. Control bits TOHB1E (bit 3, register 060H), TOHB2E (bit 3, register 061H), and EXnB3 (bit 3, registers X41H) determine the error mask source. BnEME Value Action 0 XXH No BIP errors transmitted. 1 00H No BIP errors transmitted. 1 01H BIP error transmitted for 1 frame. 1 02H BIP errors transmitted for 2 frames. . . . . 1 FEH BIP errors transmitted for 254 frames. 1 FFH Continuous BIP errors are transmitted. See the BIP Error Mark Generation paragraph in the Operation section for more detail.
071	7-0		**Transmit ETSI Tandem Connection Message Spare Bits:** The following table reflects the bit usage for this register. These bits control the state of the spare bits in the transmit tandem connection message when this feature is enabled. Frame 73 - Bit 7 represents bit 7 in the frame, Bit 6 is not used Frame 74 - Bit 5 is not used, Bit 4 represents bit 8 in the frame Frame 75 - Bits 3 and 2 represent bits 7 and 8 in the frame Frame 76 - Bits 1 and 0 represent bits 7 and 8 in the frame

Transmit AIP Registers

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
072	R	***Alarm Indication Port Debounced K1 Byte***							
073	R	***Alarm Indication Port Debounced K2 Byte***							
074	R	***Alarm Indication Port Debounced K3 Byte (STM-1 VC-4 Format and STS-3 STS-1 No. 1)***							
075	R	***STM-1/STS-3 STS-1 No. 1 - AIP REI Count***				***- AIP G1 Byte RDI***			***- AIP G1 Bit 8***
076	R	***STS-3 STS-1 No. 2 - AIP REI Count***				***- AIP G1 Byte RDI***			***- AIP G1 Bit 8***
077	R	***STS-3 STS-1 No. 3 - AIP REI Count***				***- AIP G1 Byte RDI***			***- AIP G1 Bit 8***
078 to 07F		***Reserved***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
072	7-0		**AIP Interface Debounced K1 Byte:** The bits in this register are the AIP interface debounced K1 byte.
073	7-0		**AIP Interface Debounced K2 Byte:** The bits in this register are the AIP interface debounced K2 byte.
074	7-0		**AIP Interface Debounced K3 Byte:** The bits in this register are the AIP interface debounced K3 byte. The K3 byte is provided for the STM-1/STS-3c and STS-3 STS-1 No. 1.
075	7-4		**AIP Interface Path REI (FEBE) Count for STM-1 AU4 VC-4 or STS-3 STS-1 No.1:** This register contains the value of the transmit AIP port POH G1 byte REI (FEBE) value for STM-1 or STS-3 STS-1 No.1 (bits 42-45 of the AIP frame)
	3-1		**AIP Interface RDI Value for STM-1 AU4 VC-4 or STS-3 STS-1 No.1:** This register contains the value of the transmit AIP port POH G1 byte RDI value for STM-1 or STS-3 STS-1 No.1 (bits 46-48 of the AIP frame)
	0		**AIP Interface G1 Bit 8 Value for STM-1 AU4 VC-4 or STS-3 STS-1 No.1:** This register contains the value of the transmit AIP port POH G1 byte Bit 8 value for STM-1 or STS-3 STS-1 No.1 (bit 49 of the AIP frame)
076	7-4		**AIP Interface Path REI (FEBE) Count for STS-3 STS-1 No.2:** This register contains the value of the transmit AIP port POH G1 byte REI (FEBE) value for STS-3 STS-1 No.2 (bits 54-57 of the AIP frame)
	3-1		**AIP Interface RDI Value for STS-3 STS-1 No.2:** This register contains the value of the transmit AIP port POH G1 byte RDI value for STS-3 STS-1 No.2 (bits 58-60 of the AIP frame)
	0		**AIP Interface G1 Bit 8 Value for STS-3 STS-1 No.2:** This register contains the value of the transmit AIP port POH G1 byte Bit 8 value for STS-3 STS-1 No.2 (bit 61 of the AIP frame)

Address	Bit	Symbol	Description
077	7-4		**AIP Interface Path REI (FEBE) Count for STS-3 STS-1 No.3:** This register contains the value of the transmit AIP port POH G1 byte REI (FEBE) value for STS-3 STS-1 No.3 (bits 66-69 of the AIP frame)
	3-1		**AIP Interface RDI Value for STS-3 STS-1 No.3:** This register contains the value of the transmit AIP port POH G1 byte RDI value for STS-3 STS-1 No.3 (bits 70-72 of the AIP frame)
	0		**AIP Interface G1 Bit 8 Value for STS-3 STS-1 No.3:** This register contains the value of the transmit AIP port POH G1 byte Bit 8 value for STS-3 STS-1 No.3 (bit 73 of the AIP frame)

Transmit TOH Byte Locations

Map

Transmit TOH Bytes								
A1 (0A0)	***A1 (0BB)***	***A1 (0D6)***	***A2 (0A1)***	***A2 (0BC)***	***A2 (0D7)***	***J0 (0A2)***	***N1 (0BD)***	***N2 (0D8)***
B1 (0A3)	***MDB1 (0BE)***	***MDB2 (0D9)***	***E1 (0A4)***	***MDB3 (0BF)***	***U1 (0DA)***	***F1 (0A5)***	***N3 (0C0)***	***N4 (0DB)***
D1 (0A6)	***MDB4 (0C1)***	***MDB5 (0DC)***	***D2 (0A7)***	***MDB6 (0C2)***	***U2 (0DD)***	***D3 (0A8)***	***U3 (0C3)***	***U4 (0DE)***
H1 (0A9)	***H1 (0C4)***	***H1 (0DF)***	***H2 (0AA)***	***H2 (0C5)***	***H2 (0E0)***	***H3 (0AB)***	***H3 (0C6)***	***H3 (0E1)***
B2 (0AC)	***B2 (0C7)***	***B2 (0E2)***	***K1 (0AD)***	***U5 (0C8)***	***U6 (0E3)***	***K2 (0AE)***	***U7 (0C9)***	***U8 (0E4)***
D4 (0AF)	***U9 (0CA)***	***U10 (0E5)***	***D5 (0B0)***	***U11 (0CB)***	***U12 (0E6)***	***D6 (0B1)***	***U13 (0CC)***	***U14 (0E7)***
D7 (0B2)	***U15 (0CD)***	***U16 (0E8)***	***D8 (0B3)***	***U17 (0CE)***	***U18 (0E9)***	***D9 (0B4)***	***U19 (0CF)***	***U20 (0EA)***
D10 (0B5)	***U21 (0D0)***	***U22 (0EB)***	***D11 (0B6)***	***U23 (0D1)***	***U24 (0EC)***	***D12 (0B7)***	***U25 (0D2)***	***U26 (0ED)***
S1(Z11) (0B8)	***Z12 (0D3)***	***Z13 (0EE)***	***Z21 (0B9)***	***Z22 (0D4)***	***M1 (0EF)***	***E2 (0BA)***	***N5 (0D5)***	***N6 (0F0)***

Note: For a description of the shading used above, please see page 139.

Description

The above memory map locations are all read/write locations. Please note that the J0 message size can be set for one byte or 16 bytes. When control bits TOHJ0E (bit 5 in register 060H) and J0S16 (bit 6 in register 00CH) are 0, the byte written into register 0A2H by the microprocessor is transmitted.

The bytes in these TOH (section and line) byte locations may be sent by the PHAST-3N depending upon the options programmed. For example, when control bit TLA1A2E (bit 7 in register 060H) is a 1 and control bit TOHAAE (bit 6 in register 060H) is a 0, the values written into 0A0H, 0BBH, 0D6H, 0A1H, 0BCH, and 0D7H by the microprocessor are transmitted. Please note that TOH byte location(s) must first be selected as the source, followed by write of the value(s) to be transmitted. Regardless of the programmed source for these TOH byte locations, these byte locations are not overwritten during line AIS.

Transmit TOH J0 Byte Locations - 16-Byte Message

Map

Transmit TOH Bytes							
J0(1) (080)	***J0(2) (081)***	***J0(3) (082)***	***J0(4) (083)***	***J0(5) (084)***	***J0(6) (085)***	***J0(7) (086)***	***J0(8) (087)***
J0(9) (088)	***J0(10) (089)***	***J0(11) (08A)***	***J0(12) (08B)***	***J0(13) (08C)***	***J0(14) (08D)***	***J0(15) (08E)***	***J0(16) (08F)***

Description

The above memory map locations are all read/write locations. Please note that the J0 message size can be set for one byte or 16 bytes. When control bit TOHJ0E is a 0 and J0S16 is a 1, the bytes written into 080H through 08F by the microprocessor are transmitted. Please note: the PHAST-3N does not perform a CRC-7 calculation, nor does it insert the multiframe sequence into bit 1 of the J0 bye.

Transmit N1 (TC) Byte Locations - 16-Byte Message

Map

Transmit ETSI 16 Byte Message Bytes							
N1(1) (090)	***N1(2) (091)***	***N1(3) (092)***	***N1(4) (093)***	***N1(5) (094)***	***N1(6) (095)***	***N1(7) (096)***	***N1(8) (097)***
N1(9) (098)	***N1(10) (099)***	***N1(11) (09A)***	***N1(12) (09B)***	***N1(13) (09C)***	***N1(14) (09D)***	***N1(15) (09E)***	***N1(16) (09F)***

Description

The above memory map locations are all read/write locations. The PHAST-3N does not perform a CRC-7 calculation, nor does it insert the multiframe sequence into bit 1 of the 16 byte message.

Transmit Interrupt Mask Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F1 to 0F3		***Reserved***							
0F4	R/W	TLOCM	TLOSM	TPERRM		TRLOCM			
0F5	R/W	AMCRC	AMLOC	AMLRDI	AMPAPS	AMNPAS	AMRDI1	AMRDI2	AMRDI3
0F6	R/W							APLOFM	APLOSM
0F7	R/W	***Reserved***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
0F4	7	TLOCM	**Transmit Loss Of Clock Mask Bit:** A 1 enables a TLOC latched alarm to cause a hardware interrupt when control bit HINT (bit 0 in register 010H) is a 1, and also to set the software polling SINTT (bit 6 in register 019H). The software polling bit will be reset when the TLOC latched alarm is cleared.
	6	TLOSM	**Transmit Loss Of Signal Mask Bit:** A 1 enables a TLOS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTT (bit 6 in register 019H). The software polling bit will be reset when the TLOS latched alarm is cleared.
	5	TPERRM	**Transmit Parity Error Mask Bit:** A 1 enables a TPERR latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTT (bit 6 in register) 019H. The software polling bit will be reset when the TPERR latched alarm is cleared.
	4		**Not Used:**
	3	TRLOCM	**Transmit Reference Loss Of Clock Mask Bit:** A 1 enables a TRLOC latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in SINTA (bit 5 in register 019H). The software polling bit will be reset when the TRLOC latched alarm is cleared.
	2-0		**Not Used:**
0F5	7	AMCRC	**AIP Interface CRC Error Mask Bit:** A 1 enables an APCRC latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in SINTA (bit 5 in register 019H). The software polling bit will be reset when the APCRC latched alarm is cleared.
	6	AMLOC	**AIP Interface Loss Of Clock Mask Bit:** A 1 enables an APLOC latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTA (bit 5 in register 019H). The software polling bit will be reset when the APLOC latched alarm is cleared.
	5	AMLRDI	**AIP Interface Line RDI Mask Bit:** A 1 enables an APLRDI latched alarm to cause a hardware interrupt when control bit HINT is a 1.
	4	AMPAPS	**AIP Interface New VC-4 POH K3 APS Indication Mask Bit:** A 1 enables an APPAPS latched alarm to cause a hardware interrupt when control bit HINT is a 1.
	3	AMNAPS	**AIP Interface New APS Indication Mask Bit:** A 1 enables an APNAPS latched alarm to cause a hardware interrupt when control bit HINT is a 1.
	2 1 0	AMRDI1 AMRDI2 AMRDI3	**AIP Interface Path RDI Mask Bit:** A 1 enables an APRDIn latched alarm to cause a hardware interrupt when control bit HINT is a 1. Control bit AMRDI1corresponds to the STM-1 AU-4 (STS-3c) format and STS-3 STS-1 No.1.
0F6	7-2		**Not Used:**
	1	APLOFM	**AIP Interface Mate Loss Of Frame Mask Bit:** A 1 enables an APLOF latched alarm to cause a hardware interrupt when control bit HINT is a 1.
	0	APLOSM	**AIP Interface Mate Loss Of Signal Mask Bit:** A 1 enables an APLOS latched alarm to cause a hardware interrupt when control bit HINT is a 1.

Transmit Alarm Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F8	R	TLOC	TLOS	TPERR		TRLOC			
0F9	R(L)	TLOC	TLOS	TPERR		TRLOC			
0FA	R	APCRC	APLOC	APLRDI	APPAPS	APNAPS	APRDI1	APRDI2	APRDI3
0FB	R(L)	APCRC	APLOC	APLRDI	APPAPS	APNAPS	APRDI1	APRDI2	APRDI3
0FC	R							APLOF	APLOS
0FD	R(L)							APLOF	APLOS
0FE 0FF		***Reserved***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
0F8	7	TLOC	**Transmit Loss Of Clock (and Source Reference Loss Of Clock) Alarm:** In the normal transmit timing mode, the transmit terminal clock is an input. A transmit loss of clock alarm is declared when no transitions are detected in the input clock signal (TTCI) for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition. When the source timing mode is selected, a transmit loss of clock alarm is declared when no transitions are detected in the source timing reference clock (STRCI) for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition.
	6	TLOS	**Transmit Loss Of Signal Alarm:** The transmit terminal side byte data signal is monitored for a loss of signal. A transmit loss of signal alarm (TLOS) occurs when no data transitions are detected in the TTDI(7-0) byte-wide data signals for 125 microseconds (one frame). Recovery occurs on the first data transition.
	5	TPERR	**Transmit Parity Error Alarm:** Parity (odd or even, and data only or data plus bus signals) is calculated for the transmit terminal side input signals and compared against the state of the TTPAR input lead. When a parity error is detected, a TPERR alarm will occur. No other actions are taken (other than the alarm indication and interrupt if enabled), and the device will continue to operate. This alarm will be active for a minimum of one frame (125 µs). This alarm is inhibited when the following alarm occurs: • Transmit Loss of Signal Alarm (TLOS)
	4		**Not Used:**
	3	TRLOC	**Transmit Reference Loss Of Clock Alarm:** The retiming reference clock (TRCI) is monitored for loss of clock when the transmit justification function is enabled by setting control bit TTBYP (bit 3 in register 021H) to a 0. A transmit loss of clock reference alarm (TRLOC) occurs when the reference clock is stuck high or low for 1000 ± 500 ns. Recovery occurs on the first clock transition.
	2-0		**Not Used:**

Address	Bit	Symbol	Description
0F9	7-0		The bits in this register are the same as the corresponding bit positions in register 0F8H, except that each bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.
0FA	7	APCRC	**AIP Interface CRC Error:** For ring applications, a CRC-4 is calculated for the incoming AIP data stream and it is compared against the CRC-4 carried in bits 78, 79, 80 and 81 of the 81-bit frame. An APCRC alarm occurs when the CRC-4s do not match. Other than the alarm indication and interrupt when enabled, no further action is taken by the PHAST-3N. The CRC-4 generating polynomial is $x^4 + x + 1$. This alarm is enabled when control bit RING is a 1 and/or control bits G1nM(2-0) are 111, and is inhibited by the APLOC alarm.
	6	APLOC	**AIP Interface Loss Of Clock Alarm:** The AIP interface clock (TAIPC) is monitored for operation. An APLOC alarm occurs when no transitions are detected in the input clock for a period of between 500 and 2000 nanoseconds. Recovery occurs on the first transition in the input clock signal. Besides causing an interrupt when enabled, an APLOC alarm in ring operation will cause the line REI (FEBE) value and path REI (FEBE) value to be transmitted with a value equal to 0. In addition, an alarm will cause a remote server defect alarm (or single-bit RDI) and line RDI to be transmitted. This alarm is enabled when control bit RING is a 1 and/or control bits G1nM(2-0) are 111.
	5	APLRDI	**AIP Interface Line RDI Alarm:** This bit reflects the state of the line RDI bit in the Alarm Indication Port interface frame when control bits RING (bit 6 in register 00BH) and TLRDIE (bit 1 in register 063H) are both 1. Also, when control bits RING and TLRDIE are a 1, the state of the line RDI bit from the AIP port determines the transmitted RDI state. This alarm is inhibited by the APLOC alarm.
	4	APPAPS	**AIP Interface New VC-4 POH K3 APS Indication:** This bit reflects the state of the New POH K3 APS byte alarm indication bit, carried in the Alarm Indication Port interface frame, and detected at the transmit AIP interface. Other than an alarm indication, no action is taken by the PHAST-3N. This alarm is enabled when control bits G1nM(2-0) are 111, and is inhibited by the APLOC alarm.
	3	APNAPS	**AIP Interface New APS Indication:** This bit reflects the state of the New TOH APS byte alarm indication bit, carried in the Alarm Indication Port interface frame, and detected at the transmit AIP interface. Other than an alarm indication, no action is taken by the PHAST-3N. This alarm is enabled when control bit RING is a 1, and is inhibited by the APLOC alarm.

Address	Bit	Symbol	Description
0FA (cont.)	2 1 0	APRDI1 APRDI2 APRDI3	**AIP Interface Path RDI Alarm:** These bits reflect the Alarm Indication Port Interface RDI Indications (for Server, Payload or Connectivity RDI). The AIP RDI states control the path RDI when control bits G1nM(2-0) are equal to 111. The G1 byte is also provided in the memory map. Please note that, since the RDI indication is over the three-bit RDI, the AIP interface G1 byte may be read to determine which RDI caused the indication. Alarm APRDI1 corresponds to the STM-1 AU-4 (STS-3c) format and STS-3 STS-1 No.1. These alarms are enabled when control bits G1nM(2-0) are 111, and are inhibited by the APLOC alarm.
0FB	7-0		The bits in this register are the same as the corresponding bit positions in register 0FAH, except that each bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.
0FC	7-2		**Not Used:**
	1	APLOF	**AIP Interface Mate Loss Of Frame Alarm:** This bit reflects the state of the Alarm Indication Port (AIP) loss-of-frame status indication at the transmit AIP interface. Other than an alarm indication, no action is taken by the PHAST-3N. This alarm is enabled when control bit RING is a 1 and/or control bits G1nM(2-0) are 111, and is inhibited by the APLOC alarm.
	0	APLOS	**AIP Interface Mate Loss Of Signal Alarm:** This bit reflects the state of the Alarm Indication Port (AIP) loss-of-signal status indication at the transmit AIP interface. Other than an alarm indication no action is taken by the PHAST-3N. This alarm is enabled when control bit RING is a 1 and/or control bits G1nM(2-0) are 111, and is inhibited by the APLOC alarm.
0FD	7-0		The bits in this register are the same as the corresponding bit positions in 0FCH, except that each bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.

TRANSMIT REGISTERS PER STM-1 VC-4 OR STS-3 STS-1 NO. n

The variable X for a register location and a control bit is defined as 1, 2 or 3. A value of X and n = 1 defines the registers and control bits for an STM-1 VC-4 or STS-3 STS-1 No. 1 format. The value X and n = 2 define the registers and control bits for STS-3 STS-1 No. 2. The value X and n = 3 define the registers and control bits for STS-3 STS-1 No. 3. For an STM-1 VC-4 format, the values for X and n equal to 2 or 3 are ignored by the PHAST-3N.

Transmit Control Registers - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X00	R/W								TFnRST
X01	R/W								TnPAISE
X02 to X3F	R/W	Reserved							
X40	R/W	***G1nM2***	***G1nM1***	***G1nM0***	***CNTn***	***TnRSDI***	***TnRCDI***	***TnRPDI***	***TG1nB8***
X41	R/W	***EXnJ1***	***EXnB3***	***EXnC2***	***EXnH4***	***EXnF2***	***EXnF3***	***EXnK3***	***EXnN1***
X42	R/W	***PTEn***	***TH4nM1***	***TH4nM0***					
X43	R/W	***UQnEN***	***POHnE***	***TRnPAIS***		***STCAIS***			
X44 to X6F	R/W	***Reserved***							

Note: For a description of the shading used above, please see page 139. STCAIS (bit 3 of X43H above) occurs at bit 3 of 143H only (X = 1).

Description

Address	Bit	Symbol	Description
100 200 300 (n = 1-3)	7-1		**Not Used:**
	0	TFnRST	**Transmit FIFO Reset:** This self clearing control bit works in conjunction with control bit FRENB (bit 3 in register 010H) according to the following table. Control bit FRENB has the same function on the receive side. FRENB / TFnRST / Action 0 / 0 / No re-centering action taken on a FIFO overflow/underflow alarm condition. 1 / 0 / FIFO will automatically be reset (re-centered) on an overflow/underflow alarm. X / 1 / Resets the FIFO to half-full
101 201 301 (n = 1-3)	7-1		**Not Used:**
	0	TnPAISE	**Transmit Path AIS Enable:** A 1 enables specified alarms to transmit a path AIS.

Address	Bit	Symbol	Description
140 240 340 (n = 1-3)	7 6 5	G1nM2 G1nM1 G1nM0	**G1 Byte Transmit Mode Selection:** Enabled when control bit PTEn (bit 7 in register X42H) is a 1. Otherwise the G1 byte that is transmitted is the terminal side byte. The bits in the G1 byte are transmitted according to the following table. G1nM2 G1nM1 G1nM0 Action 0 0 0 G1 byte sent equal to 00H. 0 0 1 REI (FEBE) transmitted is the number of B3 errors detected locally. The RDI state is under microprocessor control only. Bit 8 is controlled by control bit TG1nB8. 0 1 0 REI (FEBE) transmitted is the number of B3 errors detected locally. The RDI state is controlled by alarms and the microprocessor. Bit 8 is controlled by control bit TG1nB8. 0 1 1 REI (FEBE) transmitted is the number of B3 errors detected locally. The RDI state is sent as a single-bit RDI only. Bit 8 is controlled by control bit TG1nB8. 1 0 0 The G1 byte that is transmitted is the value written to the memory map by the microprocessor. 1 0 1 REI (FEBE) transmitted is the number of B3 errors detected locally. RDI state is controlled by the value present in the G1 byte at the POH interface. The microprocessor can also control the RDI state. Single-bit or three-bit RDI can be transmitted depending upon the state of control bit RDIO. Bit 8 is controlled by the value present in the G1 byte at the POH interface. 1 1 0 POH interface value (any value) for G1 byte is transmitted. 1 1 1 The G1 byte is controlled by the value present at the AIP interface.
	4	CNTn	**Count B3 and Path REI Errors from AIP Interface:** A 1 enables the B3 and path REI (FEBE) performance counters to count the B3 error and path REI (FEBE) values present at the AIP interface when control bits G1nM2, G1nM1, and G1nM0 are 111. A 0 enables the B3 error and path REI (FEBE) performance counters to count errors from the receive side independent of the state of the G1nM2, G1nM1 and G1nM0 control bits.

Address	Bit	Symbol	Description
140 240 340 (n = 1-3) (cont.)	3	TnRSDI	**Transmit Remote Server Defect Indication:** This bit works in conjunction with the control bits TnRPDI (bit 1) and TnRCDI (bit 2) for transmitting three-bit RDI when control bit RDIO (bit 7 in register 067H) is a 0, according to the following table. Control bits G1nM2, G1nM1 and G1nM0 must be set to an appropriate state (001, 010 or 101). TnRSDI / TnRPDI / TnRCDI / Action 0 / 0 / 1 — Remote Connectivity Defect Indication transmitted; G1 byte bits 5, 6, 7 = 110 0 / 1 / 0 — Remote Payload Defect Indication transmitted; G1 byte bits 5, 6, 7 = 010 1 / 0 / 0 — Remote Server Defect Indication transmitted; G1 byte bits 5, 6, 7 = 101 Other states — No RDI, G1 byte bits 5, 6, 7 = 001 When control bit RDIO is 1, single-bit RDI is transmitted according to the following table. TnRSDI / TnRPDI / TnRCDI / Action 1 / 0 / 0 — Remote Defect Indication transmitted; G1 byte bits 5, 6, 7 = 100 Other states — No RDI, G1 byte bits 5, 6, 7 = 000
	2	TnRCDI	**Transmit Remote Connectivity Defect Indication:** This bit works in conjunction with the TnRSDI and TnRPDI control bits according to the table given above.
	1	TnRPDI	**Transmit Remote Payload Defect Indication:** This bit works in conjunction with the TnRSDI and TnRCDI control bits according to the table given above.
	0	TG1nB8	**Transmit G1 Bit 8 State:** A 1 transmits bit 8 as a 1 when enabled. A 0 transmits bit 8 as a 0. Control bits G1nM2, G1nM1 and G1nM0 must be set to the appropriate state.

Address	Bit	Symbol	Description
141 241 341 (n = 1-3)	7	EXnJ1	**Transmit POH Interface Bytes for J1:** Enabled when control bit PTEn (bit 7 in register X42H) is a 1. A 1 enables the J1 byte present at the POH interface to be transmitted and also to be written into the memory map.
	6	EXnB3	**B3 Error Mask From POH interface Enable:** Enabled when control bit PTEn (bit 7 in resister X42H) is a 1. Works in conjunction with control bit B3EME (bit 5 in register 066H) to provide the following actions. X can be either state, 0 or 1. B3EME / EXnB3 / Action 0 / X / Error mask disabled. B3 BIP calculated and transmitted. 1 / 0 / Values written in the transmit POH B3 locations are used as an error mask to error the calculated B3 BIP for a number of frames determined by the value written to the error repetition register (070H). 1 / 1 / B3 bytes from the POH interface are used as an error mask to error the calculated B3 BIP for number of frames determined by the value written to the error repetition register (070H). The bytes are also written into the memory map. See the BIP Error Mask Generation paragraph in the OPERATION section for more detail.
	5	EXnC2	**Transmit POH Interface Bytes for C2:** Enabled when control bit PTEn is a 1. A 1 enables the C2 byte present at the POH interface to be transmitted and also to be written into the memory map.
	4	EXnH4	**Transmit POH Interface Byte for H4:** Enabled when control bit PTEn is a 1. A 1 enables the H4 byte present at the POH interface to be transmitted and also to be written into the memory map.
	3	EXnF2	**Transmit POH Interface Byte for F2:** Enabled when control bit PTEn is a 1. A 1 enables the F2 byte present at the POH interface to be transmitted and also to be written into the memory map.
	2	EXnF3	**Transmit POH Interface Byte for F3:** Enabled when control bit PTEn is a 1. A 1 enables the F3 byte present at the POH interface to be transmitted and also to be written into the memory map.
	1	EXnK3	**Transmit POH Interface Byte for K3:** Enabled when control bit PTEn is a 1. A 1 enables the K3 byte present at the POH interface to be transmitted and also to be written into the memory map.
	0	EXnN1	**Transmit POH Interface Byte for N1 (Z5):** Enabled when control bit PTEn is a 1. A 1 enables the N1 (Z5) byte present at the POH interface to be transmitted and also to be written into the memory map. access. Please note that the functions performed by this control bit when enabled override the tandem connection states that may be present in the N1 (Z5) byte when enabled.

Address	Bit	Symbol	Description
142 242 342 (n = 1-3)	7	PTEn	**Transmit Path Terminating Mode Selection:** When control bit PTEn is a 0, the POH bytes from the transmit terminal side are inserted into the VC-4 POH column or the three STS-1 POH columns intact. The POH bytes will also be written into the PHAST-3N POH memory map locations for microprocessor access. A 1 enables the path terminating mode for the STS-3 STS-1 selected or STM-1 AU-4. POH bytes (and bits) are inserted from memory map locations, the POH interface, the receive side (e.g., REI) or the AIP interface (path protected rings).
	6 5	TH4nM1 TH4nM0	**Transmit Side H4 Byte Selection Bits:** The H4 byte is transmitted according to the following table. It is enabled when control bits PTEn (bit 7) is a 1 and EXnH4 (bit 4 in register X41H) is a 0. Normal Timing: TH4nM1 TH4nM0 Action 0 0 H4 byte transmitted from memory map 0 1 H4 byte transmitted from terminal interface. 1 0 H4 byte derived from H4 detector/generator which is locked to terminal side H4 byte. 1 1 H4 byte is derived from H4 detector/generator which is locked to terminal side V1 pulse. Source Timing: TH4nM1 TH4nM0 Action 0 0 H4 byte transmitted from memory map 0 1 H4 byte transmitted from terminal interface. 1 0 H4 byte is derived from H4 detector/generator which is locked to terminal side H4 byte. 1 1 H4 byte derived from H4 detector/generator which provides terminal side V1 pulse as an output.
	4-0		**Not Used:**

Address	Bit	Symbol	Description
143 243 343 (n = 1-3)	7	UQnEN	**Transmit Unequipped Status Indication:** This bit works in conjunction with control bit POHnE (bit 6 in this register). An unequipped status or unequipped supervisory status is transmitted according to the states given in the following table. Please note that transmit path AIS over rides unequipped status and supervisory unequipped status when enabled. UQnEN / POHnE / Action 0 / X / Unequipped insertion disabled. 1 / 0 / Unequipped channel status transmitted. Control bit PTEn must be set to 1 for this mode. Overrides the state of the TC feature if enabled. The payload bytes are transmitted as zeros. Except for the B3 byte, all other POH bytes are transmitted as zeros. The B3 byte will be a valid BIP-8. Please note that a valid BIP-8 is equal to zero when the remaining bits in the SPE are equal to zero. The pointer and SPE are aligned to a pointer value of 522. 1 / 1 / Supervisory Unequipped channel status transmitted. Control bit PTEn must be set to 1 for this mode. The TC feature is overwritten if enabled. The payload bytes are transmitted equal to zero. The J1 and G1 bytes are valid, and the C2 byte is transmitted equal to zero. The B3 byte will be transmitted with a valid BIP-8 value. The bit 8 state in the G1 byte is controlled by control bit TG1nB8. The remaining POH bytes will be transmitted as zeros, including the TC byte N1 if enabled. The pointer and SPE are aligned to a 522 pointervalue.
	6	POHnE	**Transmit POH bytes for Unequipped Supervisory Status:** This bit works in conjunction with the UQnEN control bit as shown in the table above.
	5	TRnPAIS	**Transmit Path AIS:** A 1 causes a path AIS to be transmitted. Please note that a path AIS state will override an unequipped status, supervisory unequipped status or tandem connection AIS, if enabled.
	4		**Not Used:**
	3	STCAIS	**Transmit Tandem Connection AIS:** A 1 causes a TC AIS to be transmitted, when enabled by control bit TTAEN (bit 6 in register 064H). Note: This bit occurs at 143H only.
	2-0		**Not Used:**

Transmit POH Ram Locations - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Transmit POH Bytes								
J1n (X70)	***B3n (X71)***	***C2n (X72)***	***G1n (X73)***	***F2n (X74)***	***H4n (X75)***	***F3n (X76)***	***K3n (X77)***	***N1n (X78)***
Reserved (X79 - X7F)								

Description

The above memory map locations are all read/write locations. When n is equal to 1, locations 170H through 178H are used for path overhead byte terminations for the STM-1 VC-4 or STS-3 STS-1 No.1. When n is equal to 2, locations 270H through 278H are used for path overhead byte terminations for STS-3 STS-1 No. 2. When n is equal to 3, locations 370H through 378H are used for path overhead byte terminations for STS-3 STS-1 No. 3.

When control bit PTEn (bit 7 in register X42H) is a 0, the terminal side path overhead bytes are written into these locations and sent intact to the line side. The terminal side J1 byte is also written sequentially into the Transmit J1 16/64-byte RAM segment at an arbitrary starting address. The B3 byte can be accessed by the microprocessor, but error mask capability is disabled. The POH RAM is overwritten during Line AIS, path AIS, and unequipped.

When control bit PTEn is a 1, and the corresponding control bit EXn (POH byte) in register X41H is a 0, the bytes written into these locations by the microprocessor are transmitted, except for the J1 byte which is transmitted from the Transmit J1 16/64-byte RAM segment, and the B3 byte which is used as an error mask if enabled by control bit B3EME. With the exception of the J1 byte, the POH RAM is not overwritten during path AIS, line AIS, or unequipped. The J1 byte POH RAM location is overwritten, however the 16/64-byte J1 RAM segment (which is the transmit source for the J1 byte) is not. These source locations are not over written during AIS or unequipped so that the user won't have to re-write these locations upon exit of one of these states.

When control bit PTEn is a 1, and the corresponding control bit EXn (POH byte) is a 1, the corresponding byte from the POH interface is used for transmission, except for the B3 byte. The POH interface B3 byte is used as an error mask if enabled by control bit B3EME. In addition, the POH interface bytes are also written into the memory map. When path AIS, line AIS, or unequipped is transmitted, the POH RAM is overwritten by the AIS or unequipped, over riding the value from the POH interface.

Note also that for those bytes in which the POH RAM (or segment RAM for the J1 byte) is the selected source, the selection control bit (EXn) must first be set to zero, followed by a write of the value(s) to be transmitted.

Transmit J1 16/64-byte Ram Locations - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Transmit POH Bytes - J1
J1n(Numbered 1 - 64) (X80H - XBFH)

Note: For a description of the shading used above, please see page 139.

Description

The J1 RAM locations are all read/write locations. When n is equal to 1, locations 180H through 1BFH are used for J1 path overhead byte terminations for STM-1 VC-4 or STS-3 STS-1 No.1. When n is equal to 2, locations 280H through 2BFH are used for path overhead byte terminations for STS-3 STS-1 No.2. When n is equal to 3, locations 380H through 3BFH are used for path overhead byte terminations for STS-3 STS-1 No. 3.

When control bit PTEn (bit 7 in register X42H) is a 0, the terminal side path overhead bytes are written into the 16 or 64 byte segment, depending upon the size selected. The starting address is arbitrary.

When control bit PTEn is a 1 (POH termination mode), the segment is configured for either 16 bytes or 64 bytes. The segment is determined by the state written to control bit J1nS1 (bit 7, 6 or 5 in register 00EH). When J1nS1 is 1 the RAM is dimensioned for 16 bytes (x80H to X8FH), and when J1nS1 is 0 it is dimensioned for 64 bytes (X80H to XBFH). When control bit EXnJ1 is a 0, the bytes written into these locations by the microprocessor are used for transmitting the J1 bytes. When control bit PTEn is a 1, and the control bit EXnJ1 (bit 7 in register X41H) is a 1, the J1 byte from the POH interface is used for transmission. In addition, it is also written into this memory map segment (and the single byte location, register X70H).

Transmit Performance Counters - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XC0	R/W	***Transmit Pointer Justification Increment Count***							
XC1	R/W	***Transmit Pointer Justification Decrement Count***							
1C2	R/W	***Transmit TC IEC Error Count, lower 8 bits of 16 bits***							
2C2		***Reserved***							
3C2									
1C3	R/W	***Transmit TC IEC Error Count, higher 8 bits of 16 bits***							
2C3		***Reserved***							
3C3									
XC4 to XDF		***Reserved***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
1C0 2C0 3C0 (n = 1-3)	7-0		**Transmit Pointer Justification Increment Count:** This 8-bit counter counts the number of pointer increments. This counter is inhibited for the following alarms or control bit settings: • Control bit TTBYP (Transmit Retiming Bypassed) is a 1 • Transmit Loss Of Signal alarm (TLOS) • Transmit Loss of Clock alarm (TLOC)
1C1 2C1 3C1 (n = 1-3)	7-0		**Transmit Pointer Justification Decrement Count:** This 8-bit counter counts the number of pointer decrements. This counter is inhibited for the following alarms or control bit settings: • Control bit TTBYP (Transmit Retiming Bypassed) is a 1 • Transmit Loss Of Signal alarm (TLOS) • Transmit Loss of Clock alarm (TLOC)
1C2	7-0		**Transmit TC IEC Error Count - Low Byte:** The low byte of a 16-bit counter which counts terminal side N1 (Z5) byte IEC count (before IEC insertion by the PHAST-3N) as either bit or block errors. When control bit TCBLK is a 1, the IEC errors are counted as blocks. Enabled when control bit TTCEN (bit 7 in register 064H) is a 1.

Address	Bit	Symbol	Description
1C3	7-0		**Transmit TC IEC Error Count - High Byte:** The high byte of a 16-bit counter which counts terminal side N1 (Z5) byte IEC count (before IEC insertion by the PHAST-3N) as either bit or block errors. When control bit TCBLK is a 1, the IEC errors are counted as blocks. Enabled when control bit TTCEN (bit 7 in register 064H) is a 1.

Transmit Interrupt Mask Registers - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XE0	R/W	TnOOMM	TnLOMM	TE1nAM	THnAM			TnFIFM	
XE1 to XEF		***Reserved***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
1E0 2E0 3E0 (n = 1-3)	7	TnOOMM	**Transmit Out Of Multiframe Alignment Mask Bit:** A 1 enables a transmit H4 multiframe detector TnOOM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTT (bit 6 in register 019H). The software polling bit will be reset when the TnOOM latched alarm is cleared.
	6	TnLOMM	**Transmit Loss Of Multiframe Alignment Mask Bit:** A 1 enables a transmit H4 multiframe TnLOM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTT (bit 6 in register 019H). The software polling bit will be reset when the TnLOM latched alarm is cleared.
	5	TE1nAM	**Transmit E1 Byte AIS Indication Mask Bit:** A 1 enables a transmit E1 byte AIS indication (TEnAIS) latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTT (bit 6 in register 019H). The software polling bit will be reset when the TEnAIS latched alarm is cleared.
	4	THnAM	**Transmit H1/H2 AIS Indication Mask Bit:** A 1 enables a transmit H1/H2 byte AIS (THnAIS) indication latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTT (bit 6 in register 019H). The software polling bit will be reset when the THnAIS latched alarm is cleared.
	3-2		**Not Used:**
	1	TnFIFM	**Transmit FIFO Alarm Mask Bit:** A 1 enables a transmit FIFO (TnFIFO) latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTF (bit 8 in register 019H). The software polling bit will be reset when the TnFIFO latched alarm is cleared.
	0		**Not Used:**

Transmit Alarm Registers - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XF0	R	TnOOM	TnLOM	TE1nAIS	THnAIS			TnFIFO	
XF1	R(L)	TnOOM	TnLOM	TE1nAIS	THnAIS			TnFIFO	
XF2 to XFF		***Reserved***							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
1F0 2F0 3F0 (n = 1-3)	7	TnOOM	**Transmit Out Of Multiframe Alignment:** When the transmit H4 detector is enabled, an Out Of Multiframe (TnOOM) alarm is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive VC-4 frames.
	6	TnLOM	**Transmit Loss Of Multiframe Alignment:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multiframe (TnLOM) alarm is declared. Recovery will occur when the multiframe is recovered. Please note that no alarm actions are taken. When control bits TH4M1 and TH4M0 (bits 6 and 5 in register X42H) are 11, the V1 pulse is monitored for loss of V1. A loss of V1 (i.e., H4 multiframe alarm TnLOM) occurs when the V1 pulse is absent for two consecutive multiframe times. Recovery occurs when the V1 pulse is present once.
	5	TE1nAIS	**Transmit E1 Byte AIS Indication:** The E1 bytes (E11, E12 and E13) may be used to carry an AIS indication from downstream circuitry. For STM-1 AU-4/STS-3c operation, the detection circuit for one E1 byte (E11) is enabled. For AU-3/STS-3 operation, the three E1 bytes associated with each of the three AU-3/STS-1 signals will be checked independently for an AIS indication. This alarm is enabled by control bit TSAISE (address 063H, bit 3). When a majority of ones (5 or more bits in the E1 byte) is detected once, this alarm bit will set. Recovery occurs when fewer than 5 bits (any five bits) are equal to zero. This alarm condition generates transmit path AIS when control bits E1AISE (address 063H, bit 2) and TnPAISE (address X01H, bit 0) are both 1. The TE11AIS alarm generates Line AIS when control bits E1AISE and TLAISE (address 067H, bit 1) are both 1.
	4	THnAIS	**Transmit H1/H2 AIS Indication:** The transmit terminal side H1/H2 bytes, when enabled, by control bit TSAISE (address 063H, bit 3) are monitored for an AIS (all ones) state. For AU-4/STS-3c operation, only one set of H1/H2 bytes is monitored. For AU-3/STS-3 operation, each of the three H1/H2 bytes associated with the three SPEs is monitored. When all ones are detected in the H1/H2 bytes three or more consecutive times, this alarm will set. Recovery occurs when a normal NDF (bits 1 through 4 in the H1 byte) is detected three consecutive times. A normal NDF is defined as a 0110 (and also a 1110, 0010, 0100 or 0111). This alarm condition generates transmit path AIS when control bits HAISE (address 063H, bit 0) and TnPAISE (address X01H, bit 0) are both 1.
	3-2		**Not Used:**

Address	Bit	Symbol	Description
1F0 2F0 3F0 (n = 1-3) (cont.)	1	TnFIFO	**Transmit FIFO:** The transmit retiming block uses a 29-byte long FIFO upon which three length measurements are performed on each side of center. The FIFO is used as an elastic store between the transmit terminal bus and output. For AU-4/STS-3c operation, only one payload (261 columns) is justified to the reference frequency and its frame pulse. For AU-3/STS-3 operation the three AU-3/STS-1 payloads are independently justified. Payload bytes are written directly into the FIFOs on payload timing. FIFO read is on the reference timing. This bit is set on an overflow or underflow condition. The FIFO may be cleared and this bit reset automatically when control bit FRENB is a 1. The FIFO may also be reset manually by writing a 1 to control bit TFnRST. Please note: the reference clock (TRCI) and either STRCI (source timing mode) or TTCI (normal timing mode) must be present in order for this alarm to function.
	0		**Not Used:**
1F1 2F1 3F1 (n = 1-3)	7-0		The bits in this register are the same as the corresponding bit positions in register XF0H, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.

RECEIVE SIDE MEMORY MAP SEGMENTS

The receive side memory map segments are comprised of common registers, status registers and RAM locations which are used in the STM-1 AU-4, and STS-3 modes of operation. The designation n (n = 1, 2 or 3) is used to identify the three STS-1s, starting with STS-1 No. 1, and the STM-1 VC-4. For example, there are three RFnRST control bits, RF1RST, RF2RST and RF3RST. When n is equal to 1 it corresponds to the STM-1 VC-4, or STS-3 STS-1 No. 1 formats.

RECEIVE COMMON REGISTERS

Receive Common Control Registers

Map

The following registers are common to the STM-1 and STS-3 modes of operation.

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
400	R/W	RFRME				ROCI	ROB8	LOSUS	AIPCRE
401	R/W	PSBEN	SBIT1	SBIT0	PTALE	RTSB1	RTSB0	RTCNT1	RTCNT0
402	R/W	RPREV	RPRDO	RPPOH	RTBYP	RTCIV	RBHZE	RTUBZ	
403	R/W	RLPRE	RLPDO			RFAISE	EXTAIS		
404	R/W								RACERST
405	R/W							TPLOS	TPAON
406 to 43F		Reserved							

Description

Address	Bit	Symbol	Description
400	7	RFRME	**Receive Frame Pulse Enable:** This control bit is enabled when the parallel interface is selected (the SERIAL lead is low), and TOH/POH processing is enabled (the $\overline{\text{TOHENB}}$ lead is low). The input frame pulse (RLFI) lead is enabled when a 1 is written to this control bit. When enabled, the active high frame pulse identifies the third A2 byte in the SDH/SONET frame. When this bit is written with a 0, an internal circuit searches the data for the A1/A2 byte frame pattern to determine the start of the frame.
	6-4		**Not Used:**
	3	ROCI	**Receive Order Wire Interface Clock Inversion:** A 0 causes the receive order wire interface data for the E1 and E2 bytes (RE1D and RE2D) and frame pulse (ROWF) signals to be clocked out on falling edges of the order wire clock (ROWC). A 1 causes the data and frame pulse to be clocked out on rising edges of the clock.
	2	ROB8	**Receive Order Wire Frame Pulse on Bit 8 Enable:** A 0 causes the receive order wire frame pulse to occur during bit 1 for the E1 and E2 byte interfaces (RE1D and RE2D). A 1 causes the frame pulse to occur during bit 8.

Address	Bit	Symbol	Description
400 (cont.)	1	LOSUS	**Receive Loss Of Signal Parameter Selection:** The serial interface data signal, is monitored for a loss of signal There are two requirements regarding loss of signal detection: The ANSI LOS definition is enabled when this control bit is a 1. The loss of signal parameters are specified in T1M1.3/97. The ETSI LOS definition is enabled when this control bit is a 0. Loss of signal is defined in the document ETSI ETS 300 4-1-1, January 1997.
	0	AIPCRE	**Generate AIP Interface CRC Error:** Writing a 1 into this bit causes all four CRC-4 bits to be inverted at the receive AIP interface until this bit is written with a 0.
401	7	PSBEN	**Pointer SS-bits Enable:** A 0 disables the check of the SS-bits in the pointer tracking state machine. A 1 enables the pointer tracking state machine to include the SS-bits as part of the state machine check.
	6 5	SBIT1 SBIT0	**H1/H2 Byte SS-bit Value Selection:** Enabled when control bit PSBEN (bit 7) is a 1. The SS-bit value used in the check will be according to the following table. The selection is valid for both the STM-1 au-4 and STS-3 formats. SBIT1 SBIT0 Value Selected 0 0 SS-bits equal to 00 0 1 SS-bits equal to 01 1 0 SS-bits equal to 10 1 1 SS-bits equal to 11
	4	PTALE	**Pointer AIS to LOP Transition Enable:** A 1 enables the AIS to LOP transition in the pointer tracking state machine. A 0 disables the transition.
	3 2	RTSB1 RTSB0	**Receive Terminal Pointer Generation H1/H2 Byte SS-bit Value Selection:** Selects the terminal SS-bit value when the retiming circuit is enabled (control bit RTBYP (bit 4 in register 402H is a 0), according to the following table. The selection is valid for both the STM-1 au-4 and STS-3 formats. RTSB1 RTSB0 Value Selected 0 0 SS-bits equal to 00 0 1 SS-bits equal to 01 1 0 SS-bits equal to 10 1 1 SS-bits equal to 11
	1 0	RTCNT1 RTCNT0	**Receive Terminal Pointer Y byte ss-bit Value Selection:** The Selects the terminal side ss-bits (bits 5 and 6) in the Y bytes for the STM-1 AU-4 format according the following table. RTCNT1 RTCNT0 Value Selected 0 0 ss-bits equal to 00 0 1 ss-bits equal to 01 1 0 ss-bits equal to 10 1 1 ss-bits equal to 11

Address	Bit	Symbol	Description
402	7	RPREV	**Receive Terminal Odd/Even Parity Selection:** This control bit works in conjunction with control bits RPRDO (bit 6) and RPPOH (bit 5) to provide the following parity modes for the receive terminal interface signals. RPREV RPRDO RPPOH Action 0 0 0 Odd parity calculated over the RTDO(7-0), RSPE and RC1J1V1 signals. 0 0 1 Odd parity calculated over the RTDO(7-0), RSPE, RC1J1V1 and RPOH signals. 0 1 X Odd parity calculated over the RTDO(7-0) signals. 1 0 0 Even parity calculated over the RTDO(7-0), RSPE and RC1J1V1 signals. 1 0 1 Even parity calculated over the RTDO(7-0), RSPE, RC1J1V1 and RPOH signals. 1 1 X Even parity calculated over the RTDO(7-0) signals.
	6	RPRDO	**Receive Terminal Data Only Parity Selection:** Works in conjunction with control bits RPREV and RPPOH according to the table given above.
	5	RPPOH	**Receive Terminal POH Signal Parity Selection:** Works in conjunction with control bits RPREV and RPRDO according to the table given above.
	4	RTBYP	**Receive Retiming Bypass Enable:** A 0 enables the receive retiming circuit for the VC-4 and for each of the three STS-1s. A 1 bypasses the retiming circuit. When the retiming circuit is enabled, a receive reference clock (RRCI) and frame pulse (RRFI) must be provided.
	3	RTCIV	**Receive Terminal Clock Inversion Control Bit:** A 1 causes the receive terminal signals to be clocked out on rising edges of the clock (RTCO). A 0 causes the receive terminal signals to be clocked out on falling edges of the clock.
	2	RBHZE	**Receive Terminal Data Bus High-Z Enable:** A 0 enables the receive terminal output data bus leads. A 1 causes the data bus and parity bit to be forced to a high impedance state.
	1	RTUBZ	**Receive Terminal Unused Bytes Forced to Tri-state:** A 1 enables the receive terminal data bus (and parity) to be tristated for unused TOH bytes placed on the bus. Unused TOH bytes are those TOH bytes other than A1, A2, H1, H2, and optionally E1, E2, K1, and K2. See control bits RTK1BE, RTE1CH, and RTE1BE (register 445H, bits 6-4) regarding receive terminal interface options for K1, K2, E1 and E2. A 0 enables the data bus to be forced to 0 for the unused TOH bytes. Output lead $\overline{\text{RTBUSI}}$ is high for the unused TOH bytes, regardless of the state of this control bit.
	0		**Not Used:**

Address	Bit	Symbol	Description
403	7	RLPRE	**Receive Line Even/Odd Parity Selection:** This bit is enabled only when the line interface is configured for a parallel interface. This bit works in conjunction with control bit RLPDO (bit 6) to select the line parity option, as given in the table below: Please note: control bit RFRME (bit 7 in register 400H) must be set to 1 for all selections to be available. When control bit RFRME is set to 0, the parity calculation is over data only (control bit RLPDO=0 options are unavailable). RLPRE / RLPDO / Action 0 / 0 / Odd parity calculation. Odd parity is calculated over the data byte RLDI(7-0) and the frame pulse RLFI for each clock cycle. 1 / 0 / Even parity calculation. Even parity is calculated over the data byte RLDI(7-0) and the frame pulse (RLFI) for each clock cycle. 0 / 1 / Odd parity calculation. Odd parity is calculated over the data byte RLDI(7-0) only for each clock cycle. 1 / 1 / Even parity calculation. Even parity is calculated over the data byte RLDI(7-0) only for each clock cycle.
	6	RLPDO	**Receive Line Data Only Parity Selection:** Works in conjunction with control bit RLPRE according to the table given above.
	5-4		**Not Used:**
	3	RFAISE	**Receive FIFO AIS Enable:** A 1 enables a receive FIFO overflow/underflow alarm (RnFIFO bit 3 in register XF4H) to generate a receive terminal path AIS indication when control bits PnAISE (bit 2 in register X00H) and FRENB (bit 3 in register 010H) are a 1. A 1 also enables a receive FIFO re-center command (control bit RFnRST, bit 0 in register X00H) to generate a receive terminal path AIS when control bit PnAISE is a 1. Path AIS will be generated for a minimum of three frames. A 0 disables the alarm or the re-center command to generate a receive path AIS.
	2	EXTAIS	**External Alarm AIS Enable:** A 1 enables an active low on one or more $\overline{\text{FAISn}}$ leads to generate a path AIS provided control bit PnAISE (bit 2 in register X00H) is also a 1. Please note that the $\overline{\text{FAISn}}$ leads can also be used for sending RDI, when enabled.
	1-0		**Not Used:**
404	7-1		**Not Used:**
	0	RACERST	**Receive ACE Processor Reset:** A 1 resets the receive ACE processor. This bit is self-clearing and is set to 0 after the reset is complete. Once this bit is set, receive ACE IRAM must be reloaded. See Software Download Procedure (Figure 42) for how it is used.

Address	Bit	Symbol	Description
405	7-2		**Not Used:**
	1	TPLOS	**PRBS Loss Of Sync Enable:** Enabled when control bit TPAON (bit 0) is a 1. A 1 cause the test analyzer to lose synchronization. A 0 must be first written, followed by a 1, for an additional loss of synchronization condition.
	0	TPAON	**PRBS Test Analyzer On:** A 1 enables the PRBS analyzer. The Analyzer will monitor the receive side for a PRBS pattern in the VC-4 or STS-3 STS-1 according to the settings of control bits TPG1 and TPG0 (bits 1 and 0 in register 011H). The selection is common with the transmit side test generator.

AIS and RDI Enable Common Control Registers

Map

The following registers are common to the STM-1 and STS-3 formats.

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
440	R/W	J0AEN	BURST	B2TBH	RSTB2	C2CID	C2PID	PRDI5	
441	R/W		TCAISE				JOAISE	B2AISE	RLAISE
442	R/W	J1AISE	TCMSAE	B3AISE	VCAISE	C2AISE	UQAISE		H4AISE
443	R/W	J1CDIE	TCALME	B3CDIE	VCSDIE	C2PDIE	UQCDIE	TCUQE	H4PDIE
444	R/W			B3SDIE		RFRDIE	ERCDIE	ERSDIE	ERPDIE
445	R/W	RTABE	RTK1BE	RTE1CH	RTE1BE	SLAIS	ETCRDI	RTCTZ	RTCEN
446	R/W							B2RDIE	J0RDIE

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
440	7	J0AEN	**J0 (C1) Mismatch Alarm Bits Enable:** A 1 enables the mismatch detection circuit and alarms (J0TIM and J0LOL) for the J0 byte. A 0 disables the mismatch detection and alarms for the J0 byte.
	6	BURST	**Burst Protection Feature Enable:** A 1 enables the burst protection feature for the B2 BER and the B3 BER detection circuits.
	5	B2TBH	**B2 BER Time Base Selection:** When set to 1, the time base for the B2 BER detection circuit is defined as 500 microseconds. A 0 defines the time base as 125 microseconds.
	4	RSTB2	**B2 BER Measurement Circuit Reset:** A 1 clears the B2 BER detection circuit. This is a self-clearing reset. Subsequent writes to this register should not occur until after this bit has cleared. This bit must be set after a change to either the BURST (bit 6 of this register) or B2TBH (bit 5 of this register) control bits.

Address	Bit	Symbol	Description
440 (cont.)	3	C2CID	**C2 Code 1 Mismatch Detection Disabled:** This bit works in conjunction with the C2PID bit (bit 2) according to the states given in the following table, when the received C2 byte value is compared. C2CID / C2PID / Action 0 / 0 / Set Mismatch alarm (C2nMM) if match is not detected against the microprocessor-written value, the 01H value, or a PDI code value of EYH or FXH (where Y= 1 to F, X = 0 to C). Set PDI alarm (C2nPDI) if the incoming C2 value matches one of these PDI code values. 0 / 1 / Set Mismatch alarm (C2nMM) if match is not detected against the microprocessor-written value or the 01H value. The C2nPDI alarm is disabled. 1 / 0 / Set Mismatch alarm (C2nMM) if match is not detected against the microprocessor-written value or a PDI code value of EYH or FXH (where Y= 1 to F, X = 0 to C). Set PDI alarm (C2nPDI) if the incoming C2 value matches one of these PDI code values. 1 / 1 / Set Mismatch alarm (C2nMM) if match is not detected against the microprocessor-written value. The C2nPDI alarm is disabled.
	2	C2PID	**C2 PDI Mismatch Detection Disabled:** Works in conjunction with control bit C2CID according to the table given above.
	1	PRDI5	**Path RDI Detection 5 Consecutive Events:** A 0 configures the path RDI detection circuits (three-bit RDI or single-bit RDI) to declare a path RDI alarm when ten or more consecutive RDI states are detected. Recovery occurs when no defect states are detected for ten or more consecutive events. A 1 configures the path RDI detection circuits to declare an alarm when five or more consecutive RDI states are detected. Recovery occurs when no defect state is detected for five or more consecutive events.
	0		**Not Used:**

Address	Bit	Symbol	Description
441	7		**Not Used:**
	6	TCAISE	**Receive Tandem Connection AIS Alarm Terminal AIS Enable:** When the TC feature is enabled by control bit RTCEN (bit 0 in register 445H), a 1 enables a detected TC AIS (RTCAIS) alarm to generate path AIS downstream provided the global enable bit P1AISE (bit 2 in register 501H) is a 1.
	5-3		**Not Used:**
	2	J0AISE	**Receive J0 Mismatch Alarm Terminal AIS Enable:** A 1 enables a J0 mismatch (J0TIM) or loss of lock (J0LOL) alarm (when the detector is enabled) to generate line AIS or path AIS downstream provided the global enable bit (PnAISE or RLAISE) is a 1.
	1	B2AISE	**Receive B2 BER Terminal AIS Enable:** A 1 enables a B2 BER (B2BER) alarm to generate line AIS or Path AIS downstream provided the global enable bit PnAISE (bit 2 in register X01H) or RLAISE (bit 0 of this register) is a 1.
	0	RLAISE	**Receive Terminal Line AIS Enable:** A global control bit that enables specified alarms, when enabled, to generate a terminal side line AIS downstream. A 0 disables line AIS generation. Please note that the microprocessor may generate line AIS independent of the state of this control bit by writing a 1 to control bit SLAIS (bit 3 in register 445H).
442	7	J1AISE	**Receive J1 Mismatch Alarm Terminal AIS Enable:** A 1 enables a J1 mismatch (J1TIM) or loss of lock (J1LOL) alarm (when the detector is enabled) to generate Path AIS downstream when the global enable bit (PnAISE) is a 1
	6	TCMSAE	**Receive Tandem Connection ETSI Message Alarms Terminal AIS Enable:** A 1 enables the following ETSI TC alarms to generate path AIS downstream when the global enable bit (P1AISE) is a 1. • TC Loss Of Frame (TCLOF) alarm • TC Unequipped (TCUQ) alarm
	5	B3AISE	**Receive B3 BER Alarm Terminal AIS Enable:** A 1 enables a B3 BER (B3nBER) alarm to generate path AIS downstream when the global enable bit (PnAISE) is a 1.
	4	VCAISE	**Receive VC AIS Alarm Terminal AIS Enable:** A 1 enables a C2 byte detected all ones alarm (VCnAIS) to generate path AIS downstream when the global enable bit (PnAISE) is a 1.
	3	C2AISE	**Receive C2 Mismatch Alarm Terminal AIS Enable:** A 1 enables a C2 mismatch (C2nMM) alarm to generate path AIS downstream when the global enable bit (PnAISE) is a 1.
	2	UQAISE	**Receive Unequipped Alarm Terminal AIS Enable:** A 1 enables an unequipped (UNEQn) alarm to generate path AIS downstream when the global enable bit (PnAISE) is a 1.
	1		**Not Used:**

Address	Bit	Symbol	Description
442 (cont.)	0	H4AISE	**Receive H4 Multiframe Alarm Terminal AIS Enable:** A 1 enables an H4 multiframe (RnLOM) alarm (when the detector is enabled) to generate path AIS when the global enable bit (PnAISE) is a 1.
443	7	J1CDIE	**J1 Alarm Transmit Remote Connectivity Defect Indication Enable:** A 1 enables a remote connectivity defect indication or single-bit RDI to be generated when a J1 mismatch (J1nTIM) or loss of lock (J1nLOL) alarm is detected.
	6	TCALME	**Tandem Connection Alarms TCRDI and TCODI Enable:** A 1 enables the following alarms to generate TCRDI and TCODI in the transmit direction: • Receive TC Loss Of Frame alarm (TCLOF)
	5	B3CDIE	**B3 BER Alarm Transmit Remote Connectivity Defect Indication Enable:** A 1 enables a remote connectivity defect indication to be generated when a B3 BER (B3nBER) alarm is detected.
	4	VCSDIE	**VC AIS Alarm Transmit Remote Server Defect Indication Enable:** A 1 enables a remote server defect indication or single-bit RDI to be generated when a C2 all ones (VCnAIS) alarm is detected.
	3	C2PDIE	**C2 Mismatch Alarm Transmit Remote Payload Defect Indication Enable:** A 1 enables a remote payload defect indication or single-bit RDI to be generated when a C2 mismatch (C2nMM) alarm is detected.
	2	UQCDIE	**Unequipped Alarm Transmit Remote Connectivity Defect Indication Enable:** A 1 enables a remote connectivity defect indication or single-bit RDI to be generated when an unequipped (UNEQn) alarm is detected.
	1	TCUQE	**Tandem Connection Unequipped Alarm Transmit TCRDI/ODI Enable:** A 1 enables a TCRDI and TCODI to be generated when a TC unequipped alarm (TCUQ) is detected.
	0	H4PDIE	**H4 Multiframe Alarm Transmit Remote Payload Defect Indication Enable:** A 1 enables a remote payload defect indication or single-bit RDI to be generated when an H4 multiframe (RnLOM) alarm is detected.

Address	Bit	Symbol	Description
444	7-6		**Not Used:**
	5	B3SDIE	**B3 BER Alarm Transmit Remote Server Defect Indication Enable:** A 1 enables a remote server defect indication or single-bit RDI to be generated when a B3 BER (B3nBER) alarm is detected.
	4		**Not Used:**
	3	RFRDIE	**Receive FIFO Transmit Remote Server Defect Indication Enable:** A 1 enables a remote server defect indication or single-bit RDI to be generated on FIFO underflow and overflow when the retiming circuit is enabled (control bit RTBYP is a 0).
	2	ERCDIE	**External Transmit Remote Connectivity Defect Indication Enable:** A 1 enables an active low on a $\overline{\text{FAISn}}$ lead to generate a remote connectivity defect indication.
	1	ERSDIE	**External Transmit Remote Server Defect Indication Enable:** A 1 enables an active low on a $\overline{\text{FAISn}}$ lead to generate a remote server defect indication or a single-bit RDI.
	0	ERPDIE	**External Transmit Remote Payload Defect Indication Enable:** A 1 enables an active low on a $\overline{\text{FAISn}}$ lead to generate a remote payload defect indication.
445	7	RTABE	**Receive Terminal Interface A1/A2 Bytes Enable:** A 0 enables a fixed F628H frame pattern for the terminal side data. A 1 enables the insertion of a microprocessor-written A1/A2 value from the memory map (447/448H) to be transmitted.
	6	RTK1BE	**Receive Terminal K1/K2 Byte Enable:** A 1 enables the line side K1 and K2 bytes to be provided at the receive terminal. A 0 forces the K1 and K2 bytes to be either tristated or forced to 0, depending upon the state of control bit RTUBZ (address 402, bit 1).
	5	RTE1CH	**Receive Terminal E1/E2 Byte Selection:** This bit works in conjunction with control bit RTE1BE (bit 4) to provide the following E1/E2 byte modes of operation according to the following table. X can be either state, 0 or 1. RTE1CH / RTE1BE / Action 0 / X / Terminal side E1 and E2 bytes are either tristated or forced to 0, depending upon the state of control bit RTUBZ (address 402, bit 1). 1 / 0 / Terminal side E1 and E2 bytes are from the line side. 1 / 1 / In-band AIS indication inserted into the three E1n bytes, where E11 is for STM-1 AU-4 or STS-3 STS-1 no.1, etc. The E2 byte locations will be either tristated or forced to 0, depending upon the state of control bit RTUBZ (address 402, bit 1).
	4	RTE1BE	**Receive Terminal E1 Bytes for AIS Enable:** This bit works in conjunction with control bit RTE1CH according to the table given above.
	3	SLAIS	**Send Receive Terminal Side Line AIS:** A 1 causes a terminal side line AIS to be sent, independent of line AIS enable control bits and alarm states.

Address	Bit	Symbol	Description
445 (cont.)	2	ETCRDI	**Enable External Control of Tandem Connection RDI/ODI:** A 1 enables a transmit TC RDI (bit 8 of frame 73) and a TC ODI (bit 7 of frame 74) to be sent as a 1 when the external input lead $\overline{\text{FAIS1}}$ is low.
	1	RTCTZ	**Receive Terminal Tandem Connection N1 (Z5) Byte Action Selection:** This control works in conjunction with control bit RTCEN (bit 0) according to the states given in the following table. X can be either state, 0 or 1. RTCEN / RTCTZ / Action 0 / X / Receive tandem connection feature disabled. The terminal side N1 bytes are the line side N1 bytes. 1 / 0 / Receive tandem connection feature enabled. The N1 byte is provided at the terminal side transparently without B3 compensation. 1 / 1 / Receive tandem connection feature enabled. The N1 byte is forced to 0 at the terminal side, and the B3 byte is compensated.
	0	RTCEN	**Receive Tandem Connection Enable:** A 1 enables the receive tandem connection feature.
446	7- 5		**Not Used:**
	4	TCTLME	**Tandem Connection Trace Identifier Alarms TCRDI and TCODI Enable:** A 1 enables the following alarms to generate TCRDI and TCODI in the transmit direction: • Receive TC Loss of Lock Alarm (TCLOL) • Receive TC Trace ID Mismatch Alarm (TCTIM)
	3	TCTSAE	**Receive Tandem Connection Trace Identifier Alarms Terminal AIS Enable:** A 1 enables the following ETSI TC alarms to generate path AIS downstream, when the global enable bit (P1AISE) is a 1. • Receive TC Loss of Lock Alarm (TCLOL) • Receive TC Trace ID Mismatch Alarm (TCTIM)
	2	TCTIME	**Tandem Connection Trace Identifier Mismatch Alarm Enable:** If this bit is a 1, a mismatch in the incoming Trace ID will trigger the alarm bit TCTIM (address 4FC bit 5)
	1	B2RDIE	**B2 BER Alarm Transmit Line RDI Enable**: A 1 enables the B2 BER alarm to generate line RDI in the K2 byte.
	0	J0RDIE	**J0 Alarms Transmit RDI Enable:** A 1 enables the J0 Loss Of Lock alarm (J0LOL) or the J0 Trail trace Identifier Mismatch alarm (J0TIM) to generate line RDI in the K2 byte.

Note: TCMSAE (address 442 bit 6) and TCTSAE (address 446 bit 3) also generate E1 byte AIS and internal AIS for the alarms in which each operates when these types of AIS are enabled (P1AISE = 0 and R1AISE = 1 for internal AIS; RTE1CH and RTE1BE both = 1 for E1 AIS).

Receive Terminal Microprocessor-written A1/A2 Bytes

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
447	R/W	Microprocessor-Written A1 Byte - Receive Terminal							
448	R/W	Microprocessor-Written A2 Byte - Receive Terminal							

Note: For a description of the shading used above, please see page 139.

Description

The two bytes written into registers 447H and 448H are sent downstream for the A1 and A2 bytes when enabled (control bit RTABE bit 7 in register 445H is a 1). When control bit RTABE bit 7 in register 445H is a 0, a fixed F628H pattern is generated and sent downstream for the A1 and A2 bytes. Please note that a B1 and B2 BIP-8 are not recalculated. Bit 7 represents bit 1 in the sent byte. For example, an F6H for the A1 byte would be written as 1111 0110.

Receive Tandem Connection Spare Bits and APS Bytes (K1, K2, K3) Debounced Register

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
449	R	Received Frame 73, 74, 75, 76 ETSI Message Spare Bits							
44A	R	Received Debounced K1 Byte							
44B	R	Received Debounced K2 Byte							
44C	R	Received Debounced K3 Byte (STM-1/STS-3c or STS-3 STS-1 No.1)							
44D	R	Received Debounced S1 Byte							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
449	7-0		The bits is this register are the two bits received in bits 7 and 8 of the N1 (Z5) byte in frames 73, 74, 75 and 76 when the receive tandem connection and message processing features are enabled (control bits RTCEN (bit 0 in register 445H) and TCDL (bit 5 in register 00DH) are both a 1). This feature is disabled when the TCLOF alarm (bit 7 in register 4FCH) is active. Bits 7 and 6 are equal to bits 7 and 8 in frame 73, etc. Note that the TC RDI and ODI bits are not stored in this register.
44A	7-0		The bits in this register contain the debounced K1 byte value. The K1 byte is debounced on a three-frame basis. The debounced K1 byte is also provided at the AIP interface.
44B	7-0		The bits in this register contain the debounced K2 byte value. The K2 byte is debounced on a three-frame basis. The debounced K2 byte is also provided at the AIP interface.
44C	7-0		The bits in this register contain the debounced K3 byte value. The K3 byte is debounced on a three-frame basis. Please note that the debounced capability is provided for the STM-1 AU-4 formats and also for STS-3 STS-1 No.1.
44D	7-0		Bits 3 through 0 in this register contain the debounced S1 byte value (bits 5 through 8 of the S1 byte). The S1 byte is debounced on a three-frame basis. In addition, a change of synchronization indication SSMBC (bit 0 in register 4FCH) is provided if bits 5, 6, 7 and 8 have changed for three consecutive frames. Bits 1-4 when read will return a value equal to 0.

Receive B2 BER Segment Threshold Settings

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
44E	R/W	B2 BER Error Threshold Detection (upper 8 bits)							
44F	R/W	B2 BER Error Threshold Detection (lower 8 bits)							
450	R/W	B2 BER Error Time Base Detection (upper 8 bits)							
451	R/W	B2 BER Error Time Base Detection (lower 8 bits)							
452	R/W	B2 BER Error Threshold Recovery (upper 8 bits)							
453	R/W	B2 BER Error Threshold Recovery (lower 8 bits)							
454	R/W	B2 BER Error Time Base Recovery (upper 8 bits)							
455	R/W	B2 BER Error Time Base Recovery (lower 8 bits)							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
44E	7-0		**B2 BER Error Threshold Detection (upper 8 bits):** Upper byte of a 16-bit value that defines the number of detected errors in the B2 BER threshold.
44F	7-0		**B2 BER Error Threshold Detection (lower 8 bits):** Lower byte of a 16-bit value that defines the number of detected errors in the B2 BER threshold.
450	7-0		**B2 BER Error Timebase Detection (upper 8 bits):** Used in conjunction with control bit B2TBH (time base length). Upper byte of a 16-bit value that defines the time base for the B2 BER threshold.
451	7-0		**B2 BER Error Timebase Detection (lower 8 bits):** Used in conjunction with control bit B2TBH (time base length). Lower byte of a 16-bit value that defines the time base for the B2 BER threshold.
452	7-0		**B2 BER Error Threshold Recovery (upper 8 bits):** Upper byte of a 16-bit value that defines the number of errors in the B2 BER recovery threshold.
453	7-0		**B2 BER Error Threshold Recovery (lower 8 bits):** Lower byte of a 16-bit value that defines the number of errors in the B2 BER recovery threshold.
454	7-0		**B2 BER Error Timebase Recovery (upper 8 bits):** Used in conjunction with control bit B2TBH (time base length). Upper byte of a 16-bit value that defines the time base for the B2 BER recovery threshold.
455	7-0		**B2 BER Error Timebase Recovery (lower 8 bits):** Used in conjunction with control bit B2TBH (time base length). Lower byte of a 16-bit value that defines the time base for the B2 BER recovery threshold.

Receive Performance Counters

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
456	R/W	B1 Error Counter (Low order 8 bits)							
457	R/W	B1 Error Counter (High order 8 bits)							
458	R/W	B2 Error Counter (Low order 8 bits)							
459	R/W	B2 Error Counter (High order 8 bits)							
45A	R/W	Line REI (FEBE) Error Counter (Low order 8 bits)							
45B	R/W	Line REI (FEBE) Error Counter (High order 8 bits)							
45C	R/W	TC REI Block Error Counter (8 bits)							
45D	R/W	TC OEI Block Error Counter (8 bits)							
45E	R/W	PRBS Error Counter (Low order 8 bits)							
45F	R/W	PRBS Error Counter (High order 8 bits)							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
456	7-0		**B1 Error Counter - Low order 8 bits:** This is the lower byte of the 16-bit B1 error counter. B1 errors will be counted as either bit or block errors. When control bit BLKS (bit 4 in register 00BH) is a 1, one or more B1 bit errors is counted as a 1. The counter is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm
457	7-0		**B1 Error Counter - High order 8 bits:** This is the higher byte of a 16-bit counter, as described above.
458	7-0		**B2 Error Counter - Low order 8 bits:** This is the lower byte of the 16-bit B2 error counter. B2 errors will be counted as either bit or block errors. When control bit BLKL (bit 3 in register 00BH) is a 1, one or more B1 bit errors is counted as a 1. The counter is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • Receive Line AIS (RLAIS) alarm • External SDH/SONET Line Failure (SLFAIL) alarm
459	7-0		**B2 Error Counter - High order 8 bits:** This is the higher byte of a 16-bit counter, as described above.

Address	Bit	Symbol	Description
45A	7-0		**Line REI (FEBE) Error Counter - Low order 8 bits:** This is the lower byte of the Line REI 16-bit counter. Line REI (FEBE) errors are counted as either bits or blocks. When control bit BLKL (bit 3 in register 00BH) is a 1, one or more errors are counted as a 1. The counter is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • Receive Line AIS (RLAIS) alarm • External SDH/SONET Line Failure (SLFAIL) alarm
45B	7-0		**Line REI (FEBE) Error Counter - High order 8 bits:** This is the higher byte of a 16-bit counter, as described above.
45C	7-0		**TC REI Block Error Counter:** Enabled when control bit RTCEN (bit 0 in register 445H) is a 1 and control bit TCDL (bit 5 in register 00DH) is a 1. This 8-bit counter counts the number of REI bits received as a 1 in bit 5 (TC REI) in the N1 (Z5) byte. The counter is inhibited when any of the following alarms is declared: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss Of Pointer (R1LOP) alarm
45D	7-0		**TC OEI Block Error Counter:** Enabled when control bit RTCEN (bit 0 in register 445H) is a 1 and control bit TCDL (bit 5 in register 00DH) is a 1. This 8-bit counter counts the number of OEI bits received as a 1 in bit 6 (TC OEI) in the N1 (Z5) byte. The counter is inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss of Pointer (R1LOP) alarm
45E	7-0		**PRBS Error Counter - Low order 8 bits:** Enabled when control bit TPAON (bit 0 in register 405H) is a 1. This is the lower byte of a 16-bit counter. This counter counts the number of errored sequences when the PRBS analyzer is in lock. An In lock state requires 16 consecutive error-free sequences, while out of lock state occurs on 8 consecutive errored sequences.
45F	7-0		**PRBS Error Counter - High order 8 bits:** This is the higher byte of a 16-bit counter, as described above.

Receive TOH Byte Locations

Map

Receive TOH Bytes								
A1 (4A0)	A1 (4BB)	A1 (4D6)	A2 (4A1)	A2 (4BC)	A2 (4D7)	J0 (4A2)	N1 (4BD)	N2 (4D8)
B1 (4A3)	MDB1 (4BE)	MDB2 (4D9)	E1 (4A4)	MDB3 (4BF)	U1 (4DA)	F1 (4A5)	N3 (4C0)	N4 (4DB)
D1 (4A6)	MDB4 (4C1)	MDB5 (4DC)	D2 (4A7)	MDB6 (4C2)	U2 (4DD)	D3 (4A8)	U3 (4C3)	U4 (4DE)
H1 (4A9)	H1 (4C4)	H1 (4DF)	H2 (4AA)	H2 (4C5)	H2 (4E0)	H3 (4AB)	H3 (4C6)	H3 (4E1)
B2 (4AC)	B2 (4C7)	B2 (4E2)	K1 (4AD)	U5 (4C8)	U6 (4E3)	K2 (4AE)	U7 (4C9)	U8 (4E4)
D4 (4AF)	U9 (4CA)	U10 (4E5)	D5 (4B0)	U11 (4CB)	U12 (4E6)	D6 (4B1)	U13 (4CC)	U14 (4E7)
D7 (4B2)	U15 (4CD)	U16 (4E8)	D8 (4B3)	U17 (4CE)	U18 (4E9)	D9 (4B4)	U19 (4CF)	U20 (4EA)
D10 (4B5)	U21 (4D0)	U22 (4EB)	D11 (4B6)	U23 (4D1)	U24 (4EC)	D12 (4B7)	U25 (4D2)	U26 (4ED)
S1(Z11) (4B8)	Z12 (4D3)	Z13 (4EE)	Z21 (4B9)	Z22 (4D4)	M1 (4EF)	E2 (4BA)	N5 (4D5)	N6 (4F0)

Description

The above memory map locations are read-only locations. These locations are updated each frame when lead $\overline{\text{TOHENB}}$ is low.

Receive J0 Byte Locations

Map

Receive J0 Byte Location							
J0(1) (460)	J0(2) (461)	J0(3) (462)	J0(4) (463)	J0(5) (464)	J0(6) (465)	J0(7) (466)	J0(8) (467)
J0(9) (468)	J0(10) (469)	J0(11) (46A)	J0(12) (46B)	J0(13) (46C)	J0(14) (46D)	J0(15) (46E)	J0(16) (46F)

Note: For a description of the shading used above, please see page 139.

Description

The J0 RAM locations are read-only locations, except for J0(1) which is read/write and are enabled when lead $\overline{\text{TOHENB}}$ is low. The received J0 bytes are written into the RAM segment on a rotating basis with an arbitrary starting address when control bits J0AEN (bit 7 in register 440H) and J0S16 (bit 6 in register 00CH) are equal to 01. When control bits J0AEN and J0S16 are equal to 11 (16 byte message comparison), the bytes are aligned to the multiframe pattern carried in received message in J0 byte and written into the RAM segment starting with J0(1). When control bits J0AEN and J0S16 are equal to 10 (single-byte message with compare), the single-byte message is not written into the RAM segment. Instead, the message is written to the Rx TOH RAM. When J0AEN and J0S16 are equal to 00 (single-byte message - no compare), the single-byte message is written into both the Rx TOH RAM and J0(1).

Receive Microprocessor-written J0 Byte Locations - Compare Message

Map

Microprocessor-Written J0 Byte Locations							
J0(1) (470)	J0(2) (471)	J0(3) (472)	J0(4) (473)	J0(5) (474)	J0(6) (475)	J0(7) (476)	J0(8) (477)
J0(9) (478)	J0(10) (479)	J0(11) (47A)	J0(12) (47B)	J0(13) (47C)	J0(14) (47D)	J0(15) (47E)	J0(16) (47F)

Description

The above RAM locations are read/write. This segment is used for storing the microprocessor written ITU/ETSI 16 byte J0 Trace Identifier message used for comparison against the received J0 message. The 16-byte message must be written into the RAM segment starting with location 470H. The PHAST-3N does not perform a CRC-7 check.

For single byte comparisons, the single byte is written into location 470H.

Receive N1 (ETSI TC) Byte Locations

Map

Receive N1 Byte Location							
N1(1) (480)	N1(2) (481)	N1(3) (482)	N1(4) (483)	N1(5) (484)	N1(6) (485)	N1(7) (486)	N1(8) (487)
N1(9) (488)	N1(10) (489)	N1(11) (48A)	N1(12) (48B)	N1(13) (48C)	N1(14) (48D)	N1(15) (48E)	N1(16) (48F)

Description

The N1 byte RAM locations are read-only locations. The receive tandem connection feature and the message processing feature are enabled when control bits RTCEN (bit 0 in register 445H) and TCDL (bit 5 in register 00DH) are equal to 1. The 16-byte ETSI message, carried in bits 7 and 8 in frames 9 through 72 in the N1 byte, is written into the N1 RAM segment, starting with location 480H. The PHAST-3N does not perform a CRC-7 calculation on the incoming bytes.

Receive Microprocessor-written N1 Byte Locations - Compare Message

Map

Microprocessor-Written N1 Byte Locations							
N1(1) (490)	N1(2) (491)	N1(3) (492)	N1(4) (493)	N1(5) (494)	N1(6) (495)	N1(7) (496)	N1(8) (497)
N1(9) (498)	N1(10) (499)	N1(11) (49A)	N1(12) (49B)	N1(13) (49C)	N1(14) (49D)	N1(15) (49E)	N1(16) (49F)

Note: For a description of the shading used above, please see page 139.

Description

The receive microprocessor written N1 byte RAM locations are read/write locations. This segment is used for comparison against the received N1 byte message. The 16-byte message must be written into the RAM segment starting with location 490H. The PHAST-3N does not perform a CRC-7 check.

Receive Interrupt Mask Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4F1 to 4F3		Reserved							
4F4	R/W	RLOSM	RLOCM	ROOFM	RLOFM	J0LOLM	J0TIMM	B2BERM	SLFAILM
4F5	R/W	RLAISM	RAPSM	RNAPSM	RLRDIM	RFHIDM	RPAPSM	RRLCM	RLPERM
4F6	R/W	TCLOFM	TCLOLM	TCTIMM	TCRDIM	TCODIM		TCUQM	SSMBCM
4F7									MTPOOL

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
4F4	7	RLOSM	**Receive Loss Of Signal Mask Bit:** A 1 enables a RLOS latched alarm to cause a hardware interrupt when control bit HINT (bit 0 in register 010H) is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RLOS latched alarm is cleared.
	6	RLOCM	**Receive Line Loss Of Clock Mask Bit:** A 1 enables a RLLOC latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RLLOC latched alarm is cleared.
	5	ROOFM	**Receive Out Of Frame Mask Bit:** A 1 enables a ROOF latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the ROOF latched alarm is cleared.
	4	RLOFM	**Receive Loss Of Frame Mask Bit:** A 1 enables a RLOF latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RLOF latched alarm is cleared.
	3	J0LOLM	**Receive J0 Loss Of Lock Mask Bit:** A 1 enables a J0LOL latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the J0LOL latched alarm is cleared.
	2	J0TIMM	**Receive J0 Trace Identifier Mismatch Mask Bit:** A 1 enables a J0TIM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the J0TIM latched alarm is cleared.
	1	B2BERM	**Receive B2 BER Alarm Mask Bit:** A 1 enables a B2BER latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the B2BER latched alarm is cleared.
	0	SLFAILM	**External SDH/SONET Line Failure Indication Mask Bit:** A 1 enables an SLFAIL latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the SLFAIL latched alarm is cleared.

Address	Bit	Symbol	Description
4F5	7	RLAISM	**Receive Line AIS Indication Mask Bit:** A 1 enables a RLAIS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RLAIS latched alarm is cleared.
	6	RAPSM	**Receive APS Indication Mask Bit:** A 1 enables a RAPS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RAPS latched alarm is cleared.
	5	RNAPSM	**Receive New APS Indication Mask Bit:** A 1 enables a RNAPS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RNAPS latched alarm is cleared.
	4	RLRDIM	**Receive Line RDI Indication Mask Bit:** A 1 enables a RLRDI latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RLRDI latched alarm is cleared.
	3	RFHIDM	**Receive False Concatenation (Pointer) Indication Mask Bit:** A 1 enables a RFHID latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RFHID latched alarm is cleared.
	2	RPAPSM	**Receive Path APS Indication Mask Bit:** A 1 enables a RPAPS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTP1 (bit 3 in register 019H). The software polling bit will be reset when the RPAPS latched alarm is cleared.
	1	RRLCM	**Receive Reference Loss Of Clock Mask Bit:** A 1 enables a RRLOC latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTA (bit 5 in register 019H). The software polling bit will be reset when the RRLOC latched alarm is cleared.
	0	RLPERM	**Receive Line Parity Error Mask Bit:** A 1 enables a RLPERR latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the RLPERR latched alarm is cleared.

Address	Bit	Symbol	Description
4F6	7	TCLOFM	**Tandem Connection Loss Of Frame Mask Bit:** A 1 enables a TCLOF latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTG (bit 4 in register 019H). The software polling bit will be reset when the TCLOF latched alarm is cleared.
	6	TCLOLM	**Tandem Connection Loss Of Lock Mask Bit:** A 1 enables a TCLOL latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTG (bit 4 in register 019H). The software polling bit will be reset when the TCLOL latched alarm is cleared.
	5	TCTIMM	**Tandem Connection Trace Identifier Mismatch Mask Bit:** A 1 enables a TCTIM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTG (bit 4 in register 019H). The software polling bit will be reset when the TCTIM latched alarm is cleared.
	4	TCRDIM	**Tandem Connection Remote Defect Indication Mask Bit:** A 1 enables a TCRDI latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTG (bit 4 in register 019H). The software polling bit will be reset when the TCRDI latched alarm is cleared.
	3	TCODIM	**Tandem Connection Outgoing Defect Indication Mask Bit:** A 1 enables a TCODI latched alarm to cause a hardware interrupt, when control bit HINT is a 1, and also to set the software polling bit SINTG (bit 4 in register 019H). The software polling bit will be reset when the TCODI latched alarm is cleared.
	2		**Not Used:**
	1	TCUQM	**Tandem Connection Unequipped Status Mask Bit:** A 1 enables a TCUQ latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTG (bit 4 in register 019H). The software polling bit will be reset when the TCUQ latched alarm is cleared.
	0	SSMBCM	**Change In Synchronization Indication - S1 Byte Mask Bit:** A 1 enables a SSMBC latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit SINTR (bit 7 in register 019H). The software polling bit will be reset when the SSMBC latched alarm is cleared.
4F7	7-1		**Not Used:**
	0	MTPOOL	**Test Pattern Analyzer Out Of Lock Mask Bit:** A 1 enables a TPOOL latched alarm to cause a hardware interrupt when control bit HINT is a 1.

Receive Alarm Registers

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4F8	R	RLOS	RLLOC	ROOF	RLOF	J0LOL	J0TIM	B2BER	SLFAIL
4F9	R(L)	RLOS	RLLOC	ROOF	RLOF	J0LOL	J0TIM	B2BER	SLFAIL
4FA	R	RLAIS	RAPS	RNAPS	RLRDI	RFHID	RPAPS	RRLOC	RLPERR
4FB	R(L)	RLAIS	RAPS	RNAPS	RLRDI	RFHID	RPAPS	RRLOC	RLPERR
4FC	R	TCLOF	TCLOL	TCTIM	TCRDI	TCODI		TCUQ	SSMBC
4FD	R(L)	TCLOF	TCLOL	TCTIM	TCRDI	TCODI		TCUQ	SSMBC
4FE	R								TPOOL
4FF	R(L)								TPOOL

Description

Address	Bit	Symbol	Description
4F8	7	RLOS	**Receive Loss Of Signal:** When the SERIAL lead is high there are two requirements, one for ANSI applications, and the other for ITU-T/ETSI applications. The ANSI loss of signal alarm requirement is enabled when control bit LOSUS (bit 1 in register 400H) is a 1. The loss of signal parameters are specified in T1M1.3/97. An alarm is declared upon the detection of no transitions within the incoming signal (before descrambling) for the time T, where 2.3 µs ≤ T ≤ 100 µs. Recovery occurs when two consecutive frame alignment bytes (A1, A2) are detected, and no all zeros pattern has been detected during the intervening time to the next frame (i.e., one frame). The ITU-T/ETSI loss of signal alarm requirement is enabled when control bit LOSUS is a 0. A loss of signal alarm is specified to occur when there are no transitions for N consecutive pulse intervals, where 10 ≤ N ≤ 255. This implies 64 ns to 1.6 µs at the 155.52 MHz rate. Recovery occurs when the same boundary conditions exist for a signal having transitions. A detection and recovery parameter (N) of 128 (823 ns) is used. When the SERIAL lead is low (i.e. parallel interface), the incoming data signal is checked for a stuck high or low condition each frame when the scrambler/descrambler is enabled. If a stuck high/low condition is detected for one frame a LOS alarm occurs. Recovery occurs when a transition is detected in the next frame.
	6	RLLOC	**Receive Line Loss Of Clock:** A receive line loss of clock alarm is declared when the internal 19.44 MHz line clock is stuck high or low for the equivalent of 1000 ± 500 ns for either the parallel or serial line interface modes. Recovery occurs on the first transition. Please note that a receive line loss of clock alarm is provided as an alarm indication only, and no action will be taken on this alarm.

Address	Bit	Symbol	Description
4F8 (cont.)	5	ROOF	**Receive Out of Frame (Severely Errored Frame):** An Out Of Frame alarm is equivalent to the ANSI T1M1.3 Severely Errored Frame (SEF) parameter. An Out Of Frame alarm is declared when the incoming signal has a minimum of four consecutive errored frame patterns and a Receive Loss Of Signal (RLOS) alarm has not been declared. The maximum OOF detection time will be 625 µs for a random signal (or greater then 985 BIP violations in a 1000 frames). Please note that an OOF condition does not inhibit the data stream and performance counters. In addition, the frame algorithm used to check the alignment is designed so that a Bit Error Rate (BER) of 10^{-3}, assuming a Poisson distribution, will not cause an Out Of Frame alarm once every six minutes. Recovery occurs when two consecutive frames (250 µs) do not have a frame error (provided the signal has no emulated frame patterns) or a Receive Loss Of Signal (RLOS) alarm has been declared.
	4	RLOF	**Receive Loss Of Frame Alignment:** A Loss Of Frame alarm is declared when the Out Of Frame alarm persists for 3 ms and a Receive Loss Of Signal (RLOS) alarm has not been declared. Recovery will occur when there is 1 millisecond of a continuous in-frame condition or Receive Loss Of Signal (RLOS) alarm has been declared.
	3	J0LOL	**J0 Loss Of Lock Alarm:** This alarm is declared when the alignment of the 16-byte J0 trace identifier message has not been established. The detection circuit and alarm are enabled when control bits J0AEN (bit 7 in register 440H) and J0S16 (bit 6 in register 00CH) are both equal to 1. This alarm is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) • Receive Loss of Frame (RLOF) • External SDH/SONET Line Failure (SLFAIL) alarm
	2	J0TIM	**J0 Trace Identifier Mismatch Alarm:** When J0 lock is established, this alarm is declared when the 16-byte received message (460H-46FH) did not match the microprocessor-written message (470H-47FH) for one byte or message time. For the 16-byte message, recovery from this alarm occurs when the 16-byte received J0 message matches the microprocessor-written comparison message. Please note that the PHAST-3N does not perform a CRC-7 calculation. For a single-byte message, this alarm is declared when the single-byte message does not match the written single-byte value for three or more consecutive message times. This alarm is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) • Receive Loss of Frame (RLOF) • External SDH/SONET Line Failure (SLFAIL) alarm

Address	Bit	Symbol	Description
4F8 (cont.)	1	B2BER	**B2 Bit Error Alarm:** A B2 BER alarm occurs when the receive detect threshold setting has been exceeded. Recovery occurs when the recovery threshold setting has been exceeded. This alarm is inhibited when any of the following alarms or conditions occurs: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm
	0	SLFAIL	**External SDH/SONET Line Failure Indication:** This lead is enabled when the parallel interface is selected. This alarm is declared when the input lead (EXFAIL) is high. The alarm detection and recovery activation times are within 125 µs. The actions performed by this alarm are the same as those for a loss of frame alarm or a loss of signal alarm.
4F9	7-0		The bits in this register are the same as the corresponding bit positions in register 4F8H, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.
4FA	7	RLAIS	**Receive Line AIS:** A receive line AIS alarm is declared when five consecutive occurrences of 111 are detected in bits 6, 7 and 8 in the K2 byte. Recovery occurs when 5 consecutive occurrences of bits 6, 7 and 8 in the K2 byte are not equal to 111. The receive line AIS alarm is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm
	6	RAPS	**Receive APS Byte Failure:** The incoming K1 byte is monitored for an APS byte failure. An APS byte failure alarm is declared when no three consecutive K1 bytes of the last 12 successive frames are identical, starting with the last frame containing a previously consistent byte. Please note that there are no requirements placed on the K2 byte for this alarm. Recovery occurs when three consecutive, identical K1 bytes are received. The APS byte alarm is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm

Address	Bit	Symbol	Description
4FA (cont.)	5	RNAPS	**Receive Change in APS Byte Status Indication:** A change in APS byte status Indication is declared when three consecutive new values are detected in the K1 byte and in the first five bits of the K2 byte from the previous stable value or following an APS byte failure. Recovery occurs in the next K1 byte time. The alarm is inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm The RNAPS status indication is provided at the Alarm Indication Port for the mate PHAST-3N in ring configuration applications.
	4	RLRDI	**Receive Line RDI (FERF):** A receive line RDI alarm is declared when three consecutive occurrences of 110 are detected in bits 6,7 and 8 of the K2 byte. Recovery occurs when three consecutive occurrences of bits 6, 7 and 8 in the K2 byte are not equal to 110. The line RDI alarm is inhibited when any of the following alarms or conditions occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm

Address	Bit	Symbol	Description
4FA (cont.)	3	RFHID	**False Concatenation (Pointer) Indication:** When the PHAST-3N is configured for an STM-1 AU-4 format, the concatenation indications (Y bytes and 1s bytes), are monitored for a false concatenation indication. A Y and 1s value not equal to 1001ss11 11111111 and 1001ss11 11111111 for four or more consecutive frames will result in a false concatenation indication. Recovery occurs when a value equal to 1001ss11 11111111 and 1001ss11 11111111 is detected for four or more consecutive frames. The alarm indicates that the incoming format is an STS-3 format, and not an STM-1 AU-4/STS-3c format. The four consecutive detect and recovery frames provide protection against bit errors. Please note that the ss bits are undefined and are assumed to be equal to 00. Any ss bits value other than 00 will cause this alarm indication. When the STS-3 operating mode is selected, a value equal to 1001ss11 11111111 (H12, H22) or 1001ss11 11111111 (H13 and H23) will result in a receive LOP alarm for STM-1 AU-3 B and C, or STS-3 STS-1 No. 2 and STS-1 No. 3. When the two LOP alarms are detected, the H12, H22, H13 and H23 bytes will be checked. If the H12, H22, H13, and H23 bytes are also equal to 1001ss11 11111111 1001ss11 11111111, a false concatenation indication will be declared. Recovery occurs when either LOP has recovered. The alarm indicates that the incoming format is a STM-1/STS-3c format, and not a STM-1 AU-3 or STS-3 format. The false concatenation indication will be inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm
	2	RPAPS	**Path APS Processing (Protection Switching Byte Failure):** The incoming K3 byte in the STM-1 VC-4, STS-3c or STS-3 STS-1 No.1 SPE is monitored for a change in the path APS byte. A path APS byte alarm indication occurs when three consecutive new values of the K3 byte are detected, starting with the last frame containing a previously consistent byte. The alarm is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss Of Pointer (R1LOP)

Address	Bit	Symbol	Description
4FA (cont.)	1	RRLOC	**Receive Reference Loss Of Clock:** The reference clock (RRCI) for the receive justification circuit is monitored for loss of clock. A receive reference loss of clock alarm occurs when the clock is stuck high or low for the equivalent of 1000 ± 500 ns. Recovery occurs on the first clock transition. This alarm is disabled when the justification FIFO is bypassed, i.e., control bit RTBYP (bit 4 in register 402H) is a 1.
	0	RLPERR	**Receive Line Parity Error (odd or even):** Parity over the data byte, or data byte and frame pulse, as selected by control bits RLPRE and RLPDO (register 403H, bits 7 and 6), is calculated and compared against the state of the RLPR input lead. When a parity error is detected (by comparing the calculated parity of the input signals against the input parity lead), this alarm occurs. No other actions are taken, beyond the alarm indication, and the PHAST-3N will continue to operate normally. This alarm will be present for 1 frame minimum (125 µs). This alarm is inhibited when the following alarm occurs: • Receive Loss of Signal Alarm (RLOS)

Address	Bit	Symbol	Description
4FB	7-0		The bits in this register are the same as those in the corresponding bit positions in register 4FAH, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.
4FC	7	TCLOF	**Tandem Connection Loss Of Frame:** The receive tandem connection feature is enabled when control bit RTCEN (bit 0 in register 445H) is a 1 and the message processing feature is enabled when control bit TCDL (bit 5 in register 00DH) is a 1. The frame alignment signal is carried in bits 7 and 8 of frames 1 through 8. Frame alignment is declared lost when two consecutive frame alignment sequences (1111 1111 1111 1110) are detected in error (i.e., there is more than one error in each of the frame alignment patterns). Recovery occurs when two consecutive error-free frame alignment patterns are detected. A TC loss of frame alignment alarm inhibits the following alarms: • TC Loss of Lock detection and alarm (TCLOL) • TC Mismatch detection and alarm (TCTIM) • TC ODI detection and alarm (TCODI) • TC RDI detection and alarm (TCRDI) All tandem connection alarms are inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss Of Pointer (R1LOP) alarm Note: This alarm is not inhibited by an incoming TCAIS.
	6	TCLOL	**Tandem Connection Loss Of Lock Alarm:** This alarm is declared when the alignment of the 16-byte TC trace identifier message has not been established. If the incoming 16-byte message repeats three times in a row after the multiframe pattern is detected, without an error, the memory map segment (480H - 48FH) is updated. This is an in-lock condition. If the receive message changes for five consecutive 16-byte messages, the TCLOL alarm is asserted and the TCTIM mismatch alarm (bit 5 in register 4FCH) is reset. The detection circuit and alarm are enabled when control bit RTCEN is set to 1, and control bit TCDL (bit 5 in register 00DH) is set to 1.

Address	Bit	Symbol	Description
4FC (cont.)	5	TCTIM	**Tandem Connection Trace Identifier Mismatch Alarm:** When lock is established, a comparison is performed between the microprocessor written 16 byte N1 compare message (490H - 49FH) and the receive N1 byte RAM segment (480H - 48FH). An alarm is declared when any byte in the message does not match. Recovery occurs when there is a match between the microprocessor written message and the accepted message. The PHAST-3N does not perform a CRC-7 calculation. This alarm is enabled when control bits RTCEN (bit 0 in register 445H) and TCDL (bit 5 in register 00DH) and TCTIME (bit 2 in register 446) are set to 1. Note: This alarm is not inhibited by an incoming TCAIS.
	4	TCRDI	**Receive Tandem Connection RDI Alarm:** Bit 8 in frame 73 in the ETSI TC message is defined as a Tandem Connection Remote Detect Indication (TC RDI). When control bit RTCEN (bit 0 in register 445H) is a 1 and TCDL (bit 5 in register 00DH) is a 1, and TC frame alignment is established, the TC RDI alarm is declared when a 1 has been detected in bit 8 in frame 73 for 5 consecutive multiframes (each multiframe is defined as 9.5 ms, or 125 µs times 76 frames). The TC RDI state is exited when bit 8 is equal to 0 for 5 consecutive multiframes. **Note:** This alarm in not inhibited by an incoming TC AIS.
	3	TCODI	**Receive Tandem Connection ODI Alarm:** Bit 7 in frame 74 in the ETSI TC message is defined as a Tandem Connection Outgoing Detect Indication (TC ODI). When control bit RTCEN (bit 0 in register 445H) is a 1 and TCDL (bit 5 in register 00DH) is a 1, and TC frame alignment is established, the TC ODI alarm is declared when a 1 has been detected in bit 7 in frame 74 for 5 consecutive multiframes (each multiframe is defined as 9.5 ms, or 125 µs times 76 frames). The TC ODI state is exited when bit 8 is equal to 0 for 5 consecutive multiframes. **Note:** This alarm in not inhibited by an incoming TC AIS.
	2		**Not Used:**
	1	TCUQ	**Receive Tandem Connection Unequipped Status Alarm:** The tandem connection unequipped feature is enabled when control bit RTCEN (bit 0 in register 445H) is a 1. A tandem connection unequipped status alarm is declared when the received N1 (Z5) byte has all 8 bits equal to 0 for 5 or more consecutive frames. The TC unequipped status alarm is exited when five or more consecutive received N1 (Z5) bytes do not have all 8 bits equal to 0. The TCUQ alarm inhibits all other tandem connection alarms, and the receive IEC, REI and OEI error counters.

Address	Bit	Symbol	Description
4FC (cont.)	0	SSMBC	**Change In Synchronization Indication - S1 Byte:** Bits 5, 6, 7 and 8 in the S1 byte (synchronization status message byte) are designated to carry a synchronization status message. A change in status indication will occur when three consecutive new messages are detected in bits 5, 6, 7 and 8. Bits 1 through 4 are unassigned and are not used in the detection circuitry. The SSMBC indicator is inhibited when any of the following alarms or conditions occurs: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm
4FD	7-0		The bits in this register are the same as the corresponding bit positions in register 4FCH, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.
4FE	7-1		**Not Used:**
	0	TPOOL	**Test Pattern Out Of Lock Alarm:** This alarm is enabled when control bit TPAON (bit 0 in register 405H) is 1. Control bits TPG1 and TPG0 (bits 1 and 0 in register 011H) determine which format the analyzer monitors. An out of lock is declared when eight or more consecutive errored PRBS sequences are detected where a sequence is defined to be 24 consecutive bits of the PRBS pattern. Recovery, or in lock, occurs when 16 consecutive error-free sequences are detected. The TPOOL indicator is inhibited when any of the following alarms or conditions occurs: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm. Note that this alarm is asserted after initialization (after the internal processor code is downloaded).
4FF	7-0		The bits in this register are the same as the corresponding bit positions in register 4FEH, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.

RECEIVE REGISTERS PER STM-1 VC-4 OR STS-3 STS-1 NO. n

The leading Hex digit X of a register location address is defined as 5, 6 or 7. A value of X = 5 defines the registers for the STM-1 VC-4 or STS-3 STS-1 No. 1 format. The value X = 6 define the registers for STS-3 STS-1 No. 2. The value X = 7 define the registers for STS-3 STS-1 No. 3. For an STM-1 VC-4 format the values for X equal to 6 or 7 are either ignored or disabled by the PHAST-3N.

The designation n in a control bit symbol is defined as 1, 2 or 3. A value of n = 1 defines the control bits for the STM-1 VC-4 or STS-3 STS-1 No. 1 format. The value n = 2 defines the control bits for STS-3 STS-1 No. 2. The value n = 3 defines the control bits for STS-3 STS-1 No. 3. For an STM-1 VC-4 format the values for n equal to 2 or 3 are ignored by the PHAST-3N.

Receive Control Registers - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X00	R/W								RFnRST
X01	R/W						PnAISE	RnAISE	
X02 to X3F		Reserved							
X40	R/W	B3nTBH	RSTB3n			SnPAIS	SnIAIS		
X41	R/W	RH4nM1	RH4nM0						
X42 to X4F		Reserved							
X50	R/W	B3 BER Error Threshold Detection (Upper 8 bits) VC-4 or STS-3 STS-1 No. n							
X51	R/W	B3 BER Error Threshold Detection (Lower 8 bits) VC-4 or STS-3 STS-1 No. n							
X52	R/W	B3 BER Error Time Base Detection (Upper 8 bits) VC-4 or STS-3 STS-1 No. n							
X53	R/W	B3 BER Error Time Base Detection (Lower 8 bits) VC-4 or STS-3 STS-1 No. n							
X54	R/W	B3 BER Error Threshold Recovery (Upper 8 bits) VC-4 or STS-3 STS-1 No. n							
X55	R/W	B3 BER Error Threshold Recovery (Lower 8 bits) VC-4 or STS-3 STS-1 No. n							
X56	R/W	B3 BER Error Time Base Recovery (Upper 8 bits) VC-4 or STS-3 STS-1 No. n							
X57	R/W	B3 BER Error Time Base Recovery (Lower 8 bits) VC-4 or STS-3 STS-1 No. n							
X58	R/W	Receive C2 Mismatch Comparison Value STM-1 or STS-3 STS-1 No. n							
X59 to X5F		Reserved							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
500 600 700 (n = 1-3)	7-1		**Not Used:**
	0	RFnRST	**Receive FIFO Reset:** This self-clearing control bit works in conjunction with control bit FRENB (bit 3 in register 010H) according to the following table. Control bit FRENB is also used on the transmit side. FRENB RFnRST Action 0 0 No re-centering action taken on a FIFO overflow/underflow alarm condition. 1 0 FIFO will automatically be reset (re-centered) on an overflow/underflow alarm. X 1 Resets the FIFO to half-full
501 601 701 (n = 1-3)	7-3		**Not Used:**
	2	PnAISE	**Path AIS Enable:** This is a global control bit which, when set to 1, enables specified alarms to generate path AIS at the receive terminal interface. When set to 0, the generation of path AIS is disabled. Please note that path AIS can be generated by the microprocessor regardless of the state of this bit and the alarms by writing a 1 to control bit SnPAIS (bit 3 in register X40H).
	1	RnAISE	**TranSwitch-Defined Path AIS Enable:** Enabled when PnAISE (bit 2) is a 0. This is a global control bit which, when set to 1, enables specified alarms to generate a TranSwitch-defined path AIS at the receive terminal interface. When set to 0, the generation of the TranSwitch-defined path AIS is disabled. Please note that the TranSwitch-defined path AIS can be generated by the microprocessor regardless of the state of this bit and the alarms by writing a 1 to control bit SnPAIS and a 0 to control bit SnIAIS (bits 3 and 2 in register X40H). A TranSwitch-defined path AIS consists of a pointer value equal to 620A Hex in the H1 and H2 bytes, zeros in the H3 byte, and ones in the entire payload, including the POH bytes, except for the H4 byte. The contents of the H4 byte will contain a two-bit H4 count from the internal H4 tracking machine, and the RSPE and RC1J1 signals will be sourced from an internal generator. The RPOH signal will be low, because it is not sourced from an internal generator. The intent is to generate the “skeleton” of a payload with sufficient timing signals to allow for VT/TU signals to be added to it, to continue an add/drop link after an input failure. Coming out of AIS, NDF is sent once, followed by a normal pointer (same as if no pointer movement took place). The J1 pulse jumps when TranSwitch-defined AIS is selected, and jumps back to the normal pointer location after the release of AIS.
	0		**Not Used:**

Address	Bit	Symbol	Description
540 640 740 (n = 1-3)	7	B3nTBH	**B3 BER Time Base Selection:** When set to 1, the time base is defined as 500 µs. A 0 defines the time base as 125 µs.
	6	RSTB3n	**B3 BER Measurement Circuit Reset:** A 1 clears the B3 BER measurement circuit. This is a self-clearing reset. Subsequent writes to this register should not occur until after this bit has cleared. This bit must be set after a change to either the BURST (address 440, bit 6) or B3nTBH (bit 7 of this register group) control bits.
	5-4		**Not Used:**
	3	SnPAIS	**Send Path AIS:** When set to 1, path AIS is generated and sent at the receive terminal interface independent of global control bits and the alarms detected. Path AIS will continue to be sent until this bit is written with a 0.
	2	SnIAIS	**Send TranSwitch-Defined Path AIS:** Enabled when SnPAIS (bit 3) is a 0. When set to 1, a TranSwitch-defined path AIS is generated and sent at the receive terminal interface independent of global control bits and the alarms detected. The TranSwitch-defined path AIS will continue to be sent until this bit is written with a 0.
	1-0		**Not Used:**
541 641 741 (n = 1-3)	7 6	RH4nM1 RH4nM0	**Receive H4 Mode Control Bits:** These bits control the various operating modes of the receive H4 detector/generator according to the following table. RH4nM1 / RH4nM0 / Action 0 / 0 / H4 detector/generator (and alarm) and V1 pulse insertion into C1J1 signal are disabled. 0 / 1 / H4 detector/generator (and alarm) is enabled. H4 generator synchronized to the H4 detector. The H4 generator generates a terminal side H4 pattern (for bits 6 and 7). When the detector loses the H4 multiframe pattern, the H4 generator continues to run, providing a terminal side H4 multiframe pattern. A V1 pulse is not inserted into the C1J1 signal. Bits 1 through 6 from the line side are mapped transparently to the terminal side. Please note: the B3 byte is not recalculated. 1 / 0 / H4 detector/generator (and alarm) are enabled. H4 generator synchronized to the H4 detector. The H4 generator generates a terminal side H4 pattern (for bits 6 and 7). When the detector loses the H4 multiframe pattern, the H4 generator continues to run, providing a terminal side H4 multiframe pattern. A V1 pulse is inserted into the C1J1 signal to form C1J1V1. Bits 1 through 6 from the line side are mapped transparently through the PHAST-3N to the terminal side. Please note: the B3 byte is not recalculated. 1 / 1 / Not used
	5-0		**Not Used:**

Address	Bit	Symbol	Description
550 650 750 (n = 1-3)	7-0		**B3 BER Error Threshold Detection (upper 8 bits):** Upper byte of a 16-bit value that defines the number of detected errors in the B3 BER threshold.
551 651 751 (n = 1-3)	7-0		**B3 BER Error Threshold Detection (lower 8 bits):** Lower byte of a 16-bit value that defines the number of detected errors in the B3 BER threshold.
552 652 752 (n = 1-3)	7-0		**B3 BER Error Timebase Detection (upper 8 bits):** Used in conjunction with control bit B3nTBH (time base length). Upper byte of a 16-bit value that defines the B3 BER detection time base (measurement period).
553 653 753 (n = 1-3)	7-0		**B3 BER Error Timebase Detection (lower 8 bits):** Used in conjunction with control bit B3nTBH (time base length). Lower byte of a 16-bit value that defines the B3 BER detection time base (measurement period).
554 654 754 (n = 1-3)	7-0		**B3 BER Error Threshold Recovery (upper 8 bits):** Upper byte of a 16-bit value that defines the number of errors in the B3 BER recovery threshold.
555 655 755 (n = 1-3)	7-0		**B3 BER Error Threshold Recovery (lower 8 bits):** Lower byte of a 16-bit value that defines the number of errors in the B3 BER recovery threshold.
556 656 756 (n = 1-3)	7-0		**B3 BER Error Timebase Recovery (upper 8 bits):** Used in conjunction with control bit B3nTBH (time base length). Upper byte of a 16-bit value that defines the B3 BER recovery time base (measurement period).
557 657 757 (n = 1-3)	7-0		**B3 BER Error Timebase Recovery (lower 8 bits):** Used in conjunction with control bit B3nTBH (time base length). Lower byte of a 16-bit value that defines the B3 BER recovery time base (measurement period).
558 658 758 (n = 1-3)	7-0		**Receive C2 Mismatch Comparison Value:** The value written into this register is compared against the received C2 for mismatch detection. Several options are available, including internal comparison against an 01H value and PDI comparison.

Receive POH Ram Locations - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Receive POH Bytes - STM-1 VC-4 and STS-3 STS-1 No. n								
J1n (X60)	B3n (X61)	C2n (X62)	G1n (X63)	F2n (X64)	H4n (X65)	F3n (X66)	K3n (X67)	N1n (X68)
Reserved (X69H - X6FH)								

Description

The above memory map locations are read-only locations. These locations are updated each frame. When n is equal to 1, locations 560H through 568H are used for path overhead byte terminations for the STM-1 VC-4 or STS-3 STS-1 No. 1. When n is equal to 2, locations 660H through 668H are used for path overhead byte terminations for STS-3 STS-1 No. 2. When n is equal to 3, locations 760H through 768H are used for path overhead byte terminations for STS-3 STS-1 No. 3.

Receive J1 16/64-Byte RAM Locations - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Receive POH Bytes - STM-1 VC-4 and STS-3 STS-1 No. n
J1n(Numbered 1 - 64) (X70H - XAFH)

Description

This segment is used for storing the 16-byte or 64-byte J1 segment. When control bits J1nS1 and J1nS0 (bits 7-2 in register 00EH) are equal to 00, the received J1 bytes will be written into this 64-byte segment on a rotating basis, starting with an arbitrary address. When these control bits are equal to 01, the 64 bytes written into this 64-byte segment will be aligned based on the ASCII CR/LF characters. That is, the message will start with X70H. When the control bits are equal to 10, only the X70H to X7FH segment is used (16-byte ITU-T/ETSI message). The bytes will be written into the 16-byte segment on a rotating basis starting with an arbitrary address. When the control bits are equal to 11, the 16-byte message in this segment will be aligned to the multiframe pattern (1000… starting in bit 7 in location X70H).

Receive J1 Byte 16-byte Processor-written Message - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Microprocessor-Written J1 Byte Locations							
J1n(1) (XB0)	J1n(2) (XB1)	J1n(3) (XB2)	J1n(4) (XB3)	J1n(5) (XB4)	J1n(6) (XB5)	J1n(7) (XB6)	J1n(8) (XB7)
J1n(9) (XB8)	J1n(10) (XB9)	J1n(11) (XBA)	J1n(12) (XBB)	J1n(13) (XBC)	J1n(14) (XBD)	J1n(15) (XBE)	J1n(16) (XBF)

Note: For a description of the shading used above, please see page 139.

Description

The above memory map RAM locations are read/write locations. This segment is used for storing the microprocessor-written ITU-T/ETSI 16-byte J1 trace identifier message that is used for comparison against the received J1 message. The 16-byte message must be loaded starting with bit 1 in the J1n byte written to bit 7 in location XB0H. The PHAST-3N does not perform the CRC-7 calculation.

Receive Performance Counters - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XC0	R/W	Receive Pointer Tracking State Machine Increment Counter for STM-1 or STS-3 STS-1 No. n							
XC1	R/W	Receive Pointer Tracking State Machine Decrement Counter for STM-1 or STS-3 STS-1 No. n							
XC2	R/W	Receive Pointer Justification Increment Counter for STM-1 or STS-3 STS-1 No. n							
XC3	R/W	Receive Pointer Justification Decrement Counter for STM-1 or STS-3 STS-1 No. n							
XC4	R/W	B3 Error Counter (Bit/Block) Low Order 8 bits of 16 bits for STM-1 or STS-3 STS-1 No. n							
XC5	R/W	B3 Error Counter (Bit/Block) High Order 8 bits of 16 bits for STM-1 or STS-3 STS-1 No. n							
XC6	R/W	Path REI Counter (Bit/Block) Low Order 8 bits of 16 bits for STM-1 or STS-3 STS-1 No. n							
XC7	R/W	Path REI Counter (Bit/Block) High Order 8 bits of 16 bits for STM-1 or STS-3 STS-1 No. n							
5C8	R/W	Receive TC IEC Error Counter, low 8 bits of 16 bits							
6C8		Reserved							
7C8									
5C9	R/W	Receive TC IEC Error Counter, high 8 bits of 16 bits							
6C9		Reserved							
7C9									
XCA to XDF		Reserved							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Description
5C0 6C0 7C0 (n = 1-3)	7-0		**Receive Pointer Tracking State Machine Increment Counter:** An 8-bit counter which counts the number of pointer increments detected by the pointer tracking state machine. This counter is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm

Address	Bit	Symbol	Description
5C1 6C1 7C1 (n = 1-3)	7-0		**Receive Pointer Tracking State Machine Decrement Counter:** An 8-bit counter which counts the number of pointer decrements detected by the pointer tracking state machine. This counter is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
5C2 6C2 7C2 (n = 1-3)	7-0		**Receive Pointer Justification Increment Counter:** An 8-bit counter which counts the number of pointer increments detected by the pointer justification circuit relative to the reference clock and frame. This counter is inhibited when any of the following control bits are set or alarms are active: • Control bit RTBYP is a 1 • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive generated path AIS • Receive generated TranSwitch-Defined path AIS • Receive generated line AIS
5C3 6C3 7C3 (n = 1-3)	7-0		**Receive Pointer Justification Decrement Counter:** An 8-bit counter which counts the number of pointer decrements detected by the pointer justification circuit relative to the reference clock and frame. This counter is inhibited when any of the following control bits are set or alarms are active: • Control bit RTBYP is a 1 • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive generated path AIS • Receive generated TranSwitch-Defined path AIS • Receive generated line AIS

Address	Bit	Symbol	Description
5C4 6C4 7C4 (n = 1-3)	7-0		**B3 Error Counter (Bit/Block) Low Order 8 bits of 16-bit Counter:** These are the lower 8 bits of a 16-bit counter that counts the number of received B3 errors as either block errors (control bit BLKP is a 1) or bit errors (control bit BLKP is a 0). This counter will count the number of B3 errors via the AIP interface when control bit CNTn is a 1 and the G1nM(2-0) control bits are equal to 111. This counter is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss of Pointer (RnLOP) alarm
5C5 6C5 7C5 (n = 1-3)	7-0		**B3 Error Counter (Bit/Block) High Order 8 bits of 16-bit Counter:** These are the upper 8 bits of a 16-bit counter that counts the number of received B3 errors as either block errors (control bit BLKP is a 1) or bit errors (control bit BLKP is a 0). This counter will count the number of B3 errors via the AIP interface when control bit CNTn is a 1 and the G1nM(2-0) control bits are equal to 111. This counter is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss of Pointer (RnLOP) alarm
5C6 6C6 7C6 (n = 1-3)	7-0		**Path REI (FEBE) Error Counter (Bit/Block) Low Order 8 bits of 16-bit Counter:** These are the lower 8 bits of a 16-bit counter that counts the number of received REI errors as either block errors (control bit BLKP is a 1) or bit errors (control bit BLKP is a 0). This counter will count the number of REI errors via the AIP interface when control bit CNTn is a 1 and the G1nM(2-0) control bits are equal to 111. This counter is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss of Pointer (RnLOP) alarm

Address	Bit	Symbol	Description
5C7 6C7 7C7 (n = 1-3)	7-0		**Path REI (FEBE) Error Counter (Bit/Block) High Order 8 bits of 16-bit Counter:** These are the upper 8 bits of a 16-bit counter that counts the number of received REI errors as either block errors (control bit BLKP is a 1), or bit errors (control bit BLKP is a 0). This counter will count the number of REI errors via the AIP interface when control bit CNTn is a 1 and the G1nM(2-0) control bits are equal to 111. This counter is inhibited when any of the following alarms occur: • Receive Loss of Signal (RLOS) alarm • Receive Loss of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss of Pointer (RnLOP) alarm
5C8	7-0		**Receive Tandem Connection IEC Error Counter (Bit/Block) Low Order 8 bits of 16-bit Counter:** These are the lower 8 bits of a 16-bit counter that counts the magnitude of the difference between the calculated number of B3 BIP-8 errors and the number of errors in the IEC field of the N1 (Z5) byte. The errors are counted as either block errors (control bit TCBLK is a 1), or bit errors (control bit TCBLK is a 0). Enabled when control bit RTCEN (bit 0 in register 445H) is a 1. This counter is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss Of Pointer (R1LOP) alarm
5C9	7-0		**Receive Tandem Connection IEC Error Counter (Bit/Block) High Order 8 bits of 16-bit Counter:** These are the upper 8 bits of a 16-bit counter that counts the magnitude of the difference between the calculated number of B3 BIP-8 errors and the number of errors in the IEC field of the N1 (Z5) byte. The errors are counted as either block errors (control bit TCBLK is a 1), or bit errors (control bit TCBLK is a 0). Enabled when control bit RTCEN (bit 0 in register 445H) is a 1. This counter is inhibited when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss Of Pointer (R1LOP) alarm

Receive Interrupt Mask Register - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XE0	R/W	RnPASM	RnLOPM	RnNPTM	VCASnM	RnSVDM	RnPYDM	RnCNDM	RnOLDM
XE1	R/W	J1nLLM	J1nTIMM	B3nBRM	C2nPDM	C2nMK	UNEQnM	RnOOMM	RnLOMM
XE2	R/W	RTCAM				RnFIFM			
XE3 to XEF		Reserved							

Note: For a description of the shading used above, please see page 139. RTCAM (bit 7 of XE2H above) occurs at bit 7 of 5E2H only (X = 5).

Description

Address	Bit	Symbol	Description
5E0 6E0 7E0 (n = 1-3)	7	RnPASM	**Receive Path AIS Alarm Mask Bit:** A 1 enables an RnPAIS latched alarm to cause a hardware interrupt when control bit HINT (bit 0 in register 010H) is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnPAIS latched alarm is cleared.
	6	RnLOPM	**Receive Loss Of Pointer Alarm Mask Bit:** A 1 enables an RnLOP latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnLOP latched alarm is cleared.
	5	RnNPTM	**Receive New Pointer Alarm Mask Bit:** A 1 enables an RnNPTR latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnNPTR latched alarm is cleared.
	4	VCASnM	**C2 Byte AIS Indication Mask Bit:** A 1 enables a VCnAIS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the VCnAIS latched alarm is cleared.

Address	Bit	Symbol	Description
5E0 6E0 7E0 (n = 1-3) (cont.)	3	RnSVDM	**Receive Remote Server Defect Alarm (Three-Bit RDI) Mask Bit:** A 1 enables an RnSVD latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnSVD latched alarm is cleared.
	2	RnPYDM	**Receive Remote Payload Defect Alarm (Three-Bit RDI) Mask Bit:** A 1 enables an RnPYD latched alarm to cause a hardware interrupt, when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnPYD latched alarm is cleared.
	1	RnCNDM	**Receive Remote Connectivity Defect Alarm (Three-Bit RDI) Mask Bit:** A 1 enables an RnCND latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnCND latched alarm is cleared.
	0	RnOLDM	**Receive Remote Defect Indication Alarm (Single-Bit RDI) Mask Bit:** A 1 enables an RnOLD latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnOLD latched alarm is cleared.

Address	Bit	Symbol	Description
5E1 6E1 7E1 (n = 1-3)	7	J1nLLM	**J1 Loss Of Lock Alarm Mask Bit:** A 1 enables a J1nLOL latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the J1nLOL latched alarm is cleared.
	6	J1nTIMM	**J1 Trace Identifier Mismatch Alarm Mask Bit:** A 1 enables a J1nTIM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the J1nTIM latched alarm is cleared.
	5	B3nBRM	**B3 BER Alarm Mask Bit:** A 1 enables a B3nBER latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the B3nBER latched alarm is cleared.
	4	C2nPDM	**C2 PDI Detection Mask Bit:** A 1 enables a C2nPDI latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the C2nPDI latched alarm is cleared.
	3	C2nMK	**C2 Mismatch Alarm Mask Bit:** A 1 enables a C2nMM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the C2nMM latched alarm is cleared.
	2	UNEQnM	**Unequipped Alarm Mask Bit:** A 1 enables a UNEQn latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the UNEQn latched alarm is cleared.

Address	Bit	Symbol	Description
5E1 6E1 7E1 (n = 1-3) (cont.)	1	RnOOMM	**H4 Out Of Lock Alarm Mask Bit:** A 1 enables a RnOOM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnOOM latched alarm is cleared.
	0	RnLOMM	**H4 Loss Of Multiframe Alarm Mask Bit:** A 1 enables a RnLOM latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 3, 2 or 1 (SINTP1, SINTP2 or SINTP3) in 019H, where: SINTP1 is for the STM-1 AU-4 (STS-3c) and STS-3 STS-1 No. 1 (STM-1 AU-3 VC-3 A) formats; SINTP2 is for STS-3 STS-1 No. 2 (STM-1 AU-3 VC-3 B); and SINTP3 is for STS-3 STS-1 No. 3 (STM-1 AU-3 VC-3 C). The software polling bit will be reset when the RnLOM latched alarm is cleared.
5E2 6E2 7E2 (n = 1-3)	7	RTCAM	**Receive Tandem Connection AIS Alarm Mask Bit:** A 1 enables a RTCAIS latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 4 (SINTG) in 019H. The software polling bit will be reset when the RTCAIS latched alarm is cleared. Note: This bit occurs at 5E2H only.
	6-4		**Not Used:**
	3	RnFIFM	**Receive FIFO Alarm Mask Bit:** A 1 enables a RnFIFO latched alarm to cause a hardware interrupt when control bit HINT is a 1, and also to set the software polling bit in bit 0 (SINTF) in 019H. The software polling bit will be reset when the RnFIFO latched alarm is cleared.
	2-0		**Not Used:**

Receive Alarm Registers - STM-1 VC-4 and STS-3 STS-1 No. n

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XF0	R	RnPAIS	RnLOP	RnNPTR	VCnAIS	RnSVD	RnPYD	RnCND	RnOLD
XF1	R(L)	RnPAIS	RnLOP	RnNPTR	VCASIn	RnSVD	RnPYD	RnCND	RnOLD
XF2	R	J1nLOL	J1nTIM	B3nBER	C2nPDI	C2nMM	UNEQn	RnOOM	RnLOM
XF3	R(L)	J1nLOL	J1nTIM	B3nBER	C2nPDI	C2nMM	UNEQn	RnOOM	RnLOM
XF4	R	RTCAIS				RnFIFO			
XF5	R(L)	RTCAIS				RnFIFO			
XF6 to XFF		Reserved							

Note: For a description of the shading used above, please see page 139. RTCAIS (bit 7 of XF4H and XF5H above) occurs at bit 7 of 5F4H and 5F5H only.

Description

Address	Bit	Symbol	Description
5F0 6F0 7F0 (n = 1-3)	7	RnPAIS	**Receive Path AIS:** A receive path AIS alarm is declared when an all ones condition is detected in three consecutive H1 and H2 bytes by the pointer tracking state machine. Path AIS is disabled when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm
	6	RnLOP	**Receive Loss Of Pointer:** A receive loss of pointer alarm is declared when an invalid pointer is detected and the pointer tracking state machine enters the LOP state. Loss of pointer is disabled when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm
	5	RnNPTR	**Receive New Pointer:** A receive new pointer alarm is declared when three new pointers are detected or one NDF is detected. A receive new pointer is not declared as a result of pointer increments or decrements. The receive new pointer alarm is disabled when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm • Receive Path AIS (RnPAIS) alarm
	4	VCnAIS	**C2 Byte AIS Indication:** A VC AIS indication is declared when the received C2 byte is equal to all ones for 5 consecutive frames. The VC AIS alarm is exited when five consecutive C2 values not equal to all ones are received. The VC AIS detection circuit is inhibited for: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm

Address	Bit	Symbol	Description
5F0 6F0 7F0 (n = 1-3) (cont.)	3	RnSVD	**Receive Remote Server Defect Alarm (Three-Bit RDI):** When control bit PRDI5 is a 0, a remote server defect alarm is declared when bits 5, 6 and 7 in the G1 byte are equal to 101 for 10 consecutive frames. The alarm is cleared when there are no defect states for 10 consecutive frames. When control bit PRDI5 (bit 1 in register 440H) is a 1, five consecutive events are used for detection and recovery. A remote server defect alarm is generated at the remote end when a path AIS or loss of pointer is detected. The RDI detection circuit for three-bit RDI is inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
	2	RnPYD	**Receive Remote Payload Defect Alarm (Three-Bit RDI):** When control bit PRDI5 is a 0, a remote payload defect alarm is declared when bits 5, 6 and 7 in the G1 byte are equal to 010 for 10 consecutive frames. The alarm is cleared when there are no defect states for 10 consecutive frames. When control bit PRDI5 is a 1, five consecutive events are used for detection and recovery. A remote payload defect alarm is generated at the remote end when a loss of cell delineation or C2 path label mismatch alarm is detected. The RDI detection circuit for three-bit RDI is inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
	1	RnCND	**Receive Remote Connectivity Defect Alarm (Three-Bit RDI):** When control bit PRDI5 is a 0, a remote connectivity defect alarm is declared when bits 5, 6 and 7 in the G1 byte are equal to 110 for 10 consecutive frames. The alarm is cleared when there are no defect states for 10 consecutive frames. When control bit PRDI5 is a 1, five consecutive events are used for detection and recovery. A remote connectivity defect alarm is generated at the remote end when a unequipped or J1 trace mismatch alarm is detected. The RDI detection circuit for three-bit RDI is inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm

Address	Bit	Symbol	Description
5F0 6F0 7F0 (n = 1-3) (cont.)	0	RnOLD	**Receive Remote Defect Indication Alarm (Single-Bit RDI):** When control bit PRDI5 is a 0, a remote defect indication defect alarm is declared when bits 5, 6 and 7 in the G1 byte are equal to 100 or 111 for 10 consecutive frames. The alarm is cleared when there are no defect states for 10 consecutive frames. When control bit PRDI5 is a 1, five consecutive events are used for detection and recovery. A remote defect indication is generated at the remote end when a path level alarm is detected. The RDI detection circuit for single-bit RDI is inhibited when any of the following alarms is declared: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
5F1 6F1 7F1 (n = 1-3)	7-0		The bits in this register are the same as the corresponding bit positions in register YF0H, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 (bits 1 and 0 in register 00CH) control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.
5F2 6F2 7F2 (n = 1-3)	7	J1nLOL	**J1 Loss Of Lock Alarm:** A J1 Loss of Lock alarm is declared when the alignment of the 16-byte J1 trace identifier message has not been established. The detection circuit and alarm are enabled when control bits J1nS1 and J1nS0 are equal to 1. The J1 comparison circuit is inhibited for any of the following alarms: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
	6	J1nTIM	**J1 Trace Identifier Mismatch:** When J1 lock is established, a comparison is performed between the microprocessor-written 16-byte J1 message (XB0H-XBFH) and the received J1 message (X70H-X7FH). An alarm is declared when any byte in the message does not match. Recovery occurs when there is a match between the microprocessor-written message and the received J1 message. Please note that the PHAST-3N does not perform a CRC-7 calculation. The J1 comparison circuit is inhibited for any of the following alarms: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm

Address	Bit	Symbol	Description
5F2 6F2 7F2 (n = 1-3)	5	B3nBER	**B3 Bit Error Alarm:** For a B3 BER measurement, two programmable BER measurement circuits are provided, one for detection and one for recovery. Each circuit consists of two 16-bit down counters, one of which is preset by the error threshold (i.e., number of errors) while the other counter is preset by a frame or time threshold selection. The time counter decrements to a selected time threshold value of 125 or 500 microseconds. When control bit B3nTBH is a 1, the time base is 500 microseconds. For a 10^{-7} BER, a 16-bit setting and 500 microseconds provides a time base of 32 seconds. For a 10^{-3} BER, and using a decrement time threshold of 125 microseconds, a value of 64 (which is 64 frames) is required to meet the 8 ms time. The threshold counter decrements to B3 (BIP-8) errors. Writing a 1 to control bit BURST enables the burst protection feature. A reset control bit (RSTB3n) clears all of the counters and internal circuits, thus allowing both measurement circuits to start in sync. The alarm is inhibited and the internal circuits are reset when any of the following alarms occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
	4	C2nPDI	**C2 PDI Detection:** The C2 PDI alarm detection circuit is enabled when control bit C2PID (bit 2 in register 440H) is equal to 0. The alarm is set when the incoming C2 value matches PDI code of EYH and FXH (Y=1 to F, X=0 to C, in hex) five or more consecutive times. Recovery occurs on five or more consecutive non-PDI events. The C2 PDI detection circuit is inhibited on the following alarms or conditions: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm Please note that it is the responsibility of the microprocessor to read the value of the received C2 byte when this alarm occurs.
	3	C2nMM	**C2 Mismatch Alarm:** The received C2 byte is compared against the microprocessor-written value, PDI values and 01H, depending upon the setting of control bits C2CID (bit 3 in register 440H) and C2PID (bit 2 in register 440H). The alarm is set if a match is not detected five or more consecutive times. Recovery occurs on five or more consecutive matches. The C2 mismatch detection circuit is inhibited on the following alarms or conditions. • All ones are received (used for VC AIS detection) • Unequipped status (UNEQn) alarm for n • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm

Address	Bit	Symbol	Description
5F2 6F2 7F2 (n = 1-3) (cont.)	2	UNEQn	**Unequipped Alarm:** The received C2 byte is checked for the all zeros state. An alarm is declared when the received C2 byte is equal to all zeros for 5 consecutive frames. The alarm is exited when five consecutive C2 values not equal to all zero are received. The unequipped status detection circuit is inhibited for any of the following alarms: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
	1	RnOOM	**H4 Out Of Lock Alarm:** The multiframe detector/generator is enabled when control bits RH4nM1 and RH4nM0 are equal to 01 and 10. An alarm is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte, Recovery occurs when, in four consecutive VC-4 frames, an error-free H4 sequence (00, 01, 10, 11) is found. This alarm will be inhibited for the following alarms: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
	0	RnLOM	**H4 Loss Of Multiframe Alarm:** The multiframe detector/generator is enabled when control bits RH41M1 and RH41M0 are equal to 01 or 10. Once in the OOM state, if recovery does not take place within 1 ms, a Loss Of Multiframe alarm will occur. Recovery occurs when the multiframe is recovered. The H4 generator will continue to run (also in the OOM state). The reason is that, for the generation of a TranSwitch-defined path AIS, an active H4 byte is provided at the terminal interface. Upon recovery, the H4 generator re-locks to the detector. This alarm will be inhibited for the following alarms. • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (RnPAIS) alarm • Receive Loss Of Pointer (RnLOP) alarm
5F3 6F3 7F3 (n = 1-3)	7-0		The bits in this register are the same as the corresponding bit positions in register XF2H, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.

Address	Bit	Symbol	Description
5F4 6F4 7F4 (n = 1-3)	7	RTCAIS	**Receive Tandem Connection AIS Alarm:** The receive TC feature is enabled by control bit RTCEN. The received bits in the IEC field in the N1 (Z5) byte are monitored for an AIS condition. When the IEC field is equal to 1110 for five or more consecutive frames an alarm is declared. Recovery occurs when the IEC field is equal to a value other than 1110 for five or more consecutive frames. The codes 0000, 1101 and 1111 represent a false AIS condition, and are not included in the detection scheme. This alarm will be inhibited when any of the following alarm conditions occurs: • Receive Loss Of Signal (RLOS) alarm • Receive Loss Of Frame (RLOF) alarm • External SDH/SONET Line Failure (SLFAIL) alarm • Receive Line AIS (RLAIS) alarm • Receive Path AIS (R1PAIS) alarm • Receive Loss Of Pointer (R1LOP) alarm The RTCAIS alarm inhibits all other tandem connection alarms, and the receive IEC, REI and OEI error counters. Note: This bit occurs at 5F4H only.
	6-4		**Not Used:**
	3	RnFIFO	**Receive FIFO alarm:** The receive retiming block uses a 29-byte long FIFO upon which three length measurements are performed on each side of center. The FIFO is used as an elastic store between the receive line and terminal bus output. Payload bytes are written directly into the FIFOs on payload timing. The FIFO read is performed on the reference timing. This bit is set on an overflow or underflow condition. The FIFO may be cleared and this bit reset automatically when control bit FRENB is a 1. The FIFO may also be reset manually by writing a 1 to control bit RFnRST. Please note: reference clock (RRCI) and the internal FIFO write clock must be present in order for this alarm to function.
	2-0		**Not Used:**
5F5 6F5 7F5 (n = 1-3)	7-0		The bits in this register are the same as the corresponding bit positions in register XF4H, except that a bit will latch on the positive transition, negative transition, positive/negative transition, or positive alarm level of its corresponding alarm in that register, according to the settings of the INRT1 and INRT0 (bit 1 and 0 in register 00CH) control bits. A latched bit position will remain set until it is cleared by a microprocessor read cycle.

TRANSMIT AND RECEIVE ACE PROCESSOR ACCESS

Map

Add	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
230	R	Reserved						STATRD	INSTRD
238	R/W	IRAM Instruction (31-24)							
239	R/W	IRAM Instruction (23-16)							
23A	R/W	IRAM Instruction (15-8)							
23B	R/W	IRAM Instruction (7-0)							
23C	R/W	IRAM Start Address (7-0)							
23D	R/W	IRAM Start Address (15-8)							
23E	R/W	IRAM Start Address (23-16)							
23F	R/W						ACENO	ACOV	BTRAC
320	R								TIDLC
331	R/W					PTACE3	PTACE2	PTACE1	PTACE0
3FC	R/W	***Transmit ACE Processor Watchdog TXPWD(7-0)***							
720	R								RIDLC
73C	R/W					PRACE3	PRACE2	PRACE1	PRACE0
7FC	R/W	Receive ACE Processor Watchdog RXPWD(7-0)							

Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Function
230	7-2		**Not used**
	1	STATRD	**Ready for First Instruction Download:** This bit is polled by the host microprocessor after it has written the three bytes of the IRAM start address to the device. When a 1, this bit indicates that the ACE has read the starting address and the microprocessor can proceed with the instruction download.
	0	INSTRD	**Ready for Next Instruction Download:** This bit is polled by the host microprocessor during IRAM loading after the microprocessor has written. When a 1, this bit indicates to the microprocessor that the instruction has been transferred to IRAM and the next instruction can be written to the device.
238, 239, 23A, 23B	7-0		**IRAM Instruction:** These are the individual bytes of the 32-bit long word instruction provided by the host microprocessor to be written to the boot memory during boot loading and the IRAM during IRAM loading. Address 238 hex contains the MS byte of the instruction and address 23B hex contains the LS byte.
23C 23D 23E	7-0		**IRAM Start:** These three registers contain the 24-bit starting address of IRAM from which the loading of IRAM Instruction will start. Location 23C hex is the LS byte and 23E hex is the MS byte of the IRAM address.

Address	Bit	Symbol	Function
23F	7-3		**Not Used:**
	2	ACENO	**ACE Processor Number:** This bit identifies the ACE processor whose IRAM is to be downloaded from the host microprocessor. A 0 selects the receive side ACE processor. A 1 selects the transmit side ACE processor.
	1	ACOV	**Microprocessor ACE Download completed:** This bit is used during IRAM downloading. When this bit is a 1, it indicates that the IRAM downloading by the microprocessor is complete. It is checked by the ACE processor boot routine after each instruction is downloaded.
	0	BTRAC	**Boot RAM Accessed:** A 1 indicates that the host microprocessor is accessing a Boot RAM location of the internal processor. A 0 indicates that the host microprocessor is accessing an Instruction RAM location of the internal processor.
320	7-1		**Not Used:**
	0	TIDLC	**Transmit Side Instruction Download Complete:** This bit is polled by the host microprocessor after it has written RTACE3-0 with a value of 1100. A 1 indicates that instruction downloading for the transmit side internal processor was successful.
331	7-4		**Not Used:**
	3-0	PTACE3 to PTACE0	**Poll - Transmit Side ACE Internal Processor (3-0):** A value of 1100 selects the transmit side internal processor for providing the status of instruction download through TIDLC in address 320. Other values are invalid and may cause abnormal device behavior.
3FC	7-0	TXPWD	**Transmit ACE Processor Watchdog:** This location provides two functions: 1. The value AAH will be written into this location ONLY after the correct number of instructions has been downloaded into the Transmit (Tx) ACE Processor's Instruction RAM (IRAM). If AAH is not seen in this location upon completion of the firmware download then it signifies that the download failed for the Tx IRAM. 2. Once the Transmit ACE Processor is operational and executing firmware from its IRAM, then this location will be continually written with the value AAH by the Tx Processor every 125 μs. This can be used as a method of verifying that the Tx Processor is operational by writing a value (other than AAH) into this location, waiting a minimum of 250 μs, and then reading the location to verify that the Tx Processor came back and overwrote the location with AAH.
720	7-1		**Not Used:**
	0	RIDLC	**Receive Side Instruction Download Complete:** This bit is polled by the host microprocessor after it has written PRACE3-0 with a value of 1100. A 1 indicates that instruction downloading for the receive side internal processor was successful.
73C	7-4		**Not Used:**
	3-0	PRACE3 to PRACE0	**Poll - Receive Side ACE Internal Processor (3-0):** A value of 1100 selects the receive side internal processor for providing the status of instruction download through RIDLC in address 720. Other values are invalid and may cause abnormal device behavior.

Address	Bit	Symbol	Function
7FC	7-0	RXPWD	**Receive ACE Processor Watchdog:** This location provides two functions: 1. The value AAH will be written into this location ONLY after the correct number of instructions has been downloaded into the Receive (Rx) ACE Processor's Instruction RAM (IRAM). If AAH is not seen in this location upon completion of the firmware download then it signifies that the download failed for the Rx IRAM. 2. Once the Receive ACE Processor is operational and executing firmware from its IRAM, then this location will be continually written with the value AAH by the Rx Processor every 125 µs. This can be used as a method of verifying that the Rx Processor is operational by writing a value (other than AAH) into this location, waiting a minimum of 250 µs, and then reading the location to verify that the Rx Processor came back and over-wrote the location with AAH.

Firmware Version

Map

Add	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7FD	R/W	Part 1 of three part Firmware Release Version (Major) number - (FWMAJ)							
7FE	R/W	Part 2 of three part Firmware Release Version (Minor) number - (FWMIN)							
7FF	R/W	Part 3 of three part Firmware Release Version (Patch) number - (FWPAT)							

* Note that these register locations are R/W and if overwritten by the external host processor the firmware version can be restored to these locations by applying a Software Reset, RESETS (bit 7 in register 00AH).

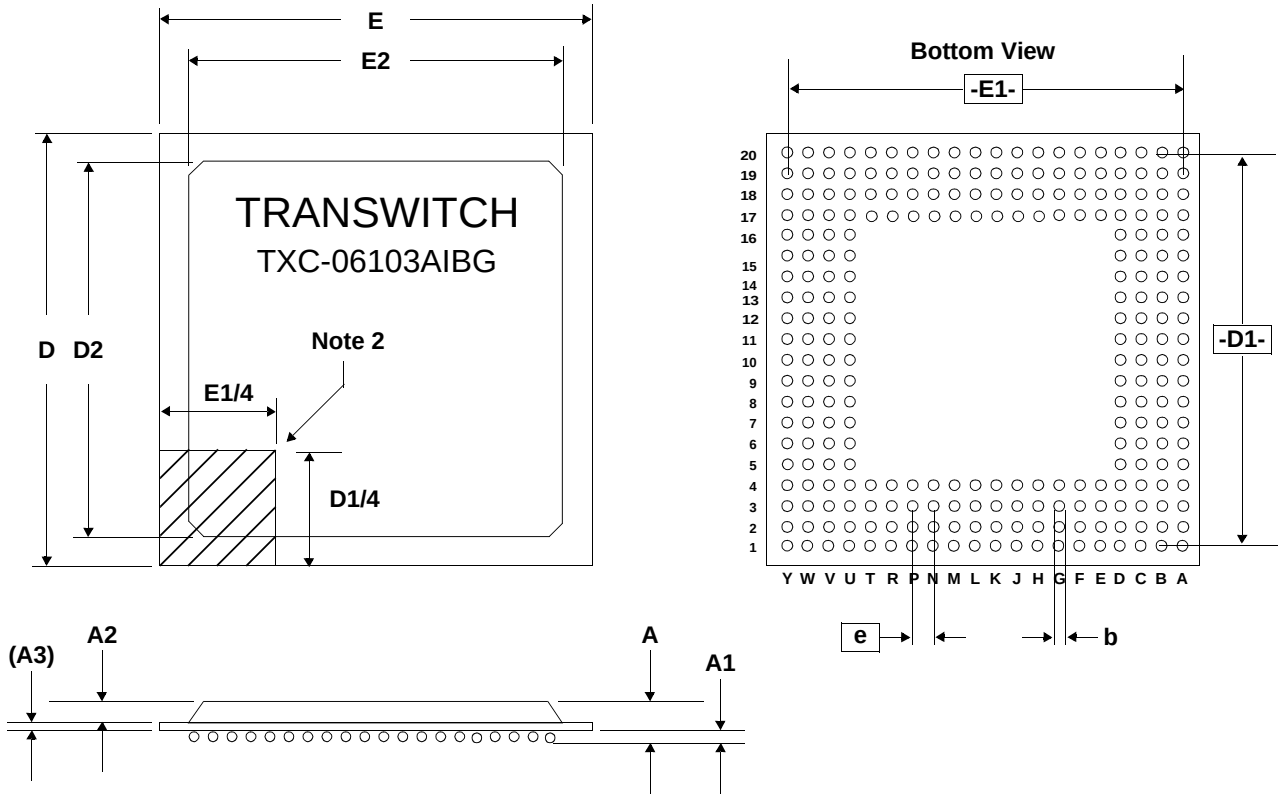
Note: For a description of the shading used above, please see page 139.

Description

Address	Bit	Symbol	Function
7FD	7-0	FWMAJ	Part 1 of three part Firmware Release Version (Major) number
7FE	7-0	FWMIN	Part 2 of three part Firmware Release Version (Minor) number
7FF	7-0	FWPAT	Part 3 of three part Firmware Release Version (Patch) number

PACKAGE INFORMATION

The PHAST-3N device is packaged in a 256-lead, 27 mm x 27 mm, plastic ball grid array package suitable for surface mounting, as illustrated in Figure 43.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 20 x 20, JEDEC code MO-151-BAL-2.

Dimension (Note 1)	Min	Max
A	1.92	2.32
A1	0.50	0.70
A2	1.12	1.22
A3 (Ref.)	0.30	0.40
b	0.60	0.90
D	27.00	
D1 (BSC)	24.13	
D2	23.95	24.70
E	27.00	
E1 (BSC)	24.13	
E2	23.95	24.70
e (BSC)	1.27	

Figure 43. PHAST-3N TXC-06103 256-Lead Plastic Ball Grid Array Package

APPLICATION DIAGRAM

This is a three STS-1 to/from one STS-3 mux example using the PHAST-3N.

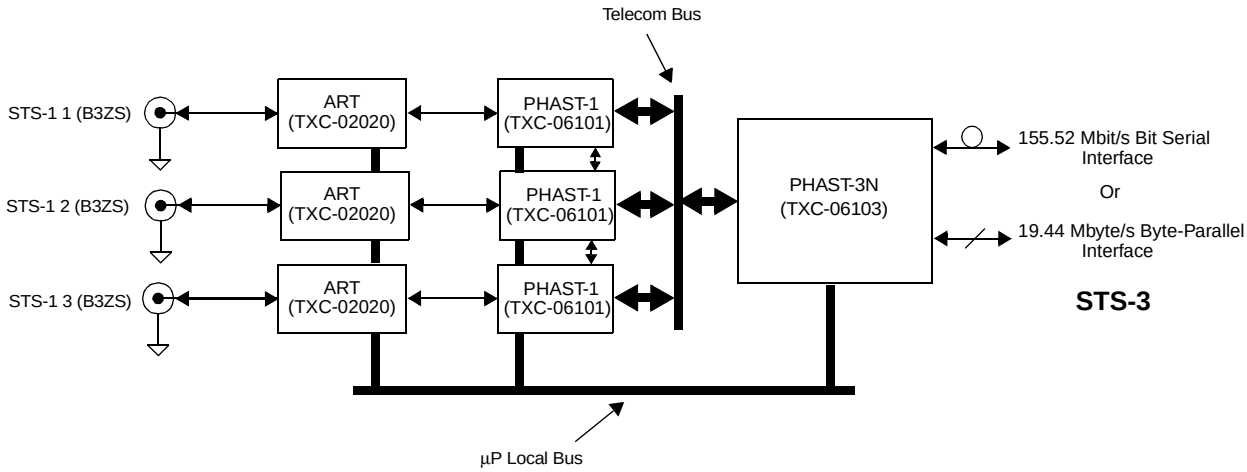


Figure 44. Mux of three STS 1 to/from one STS-3

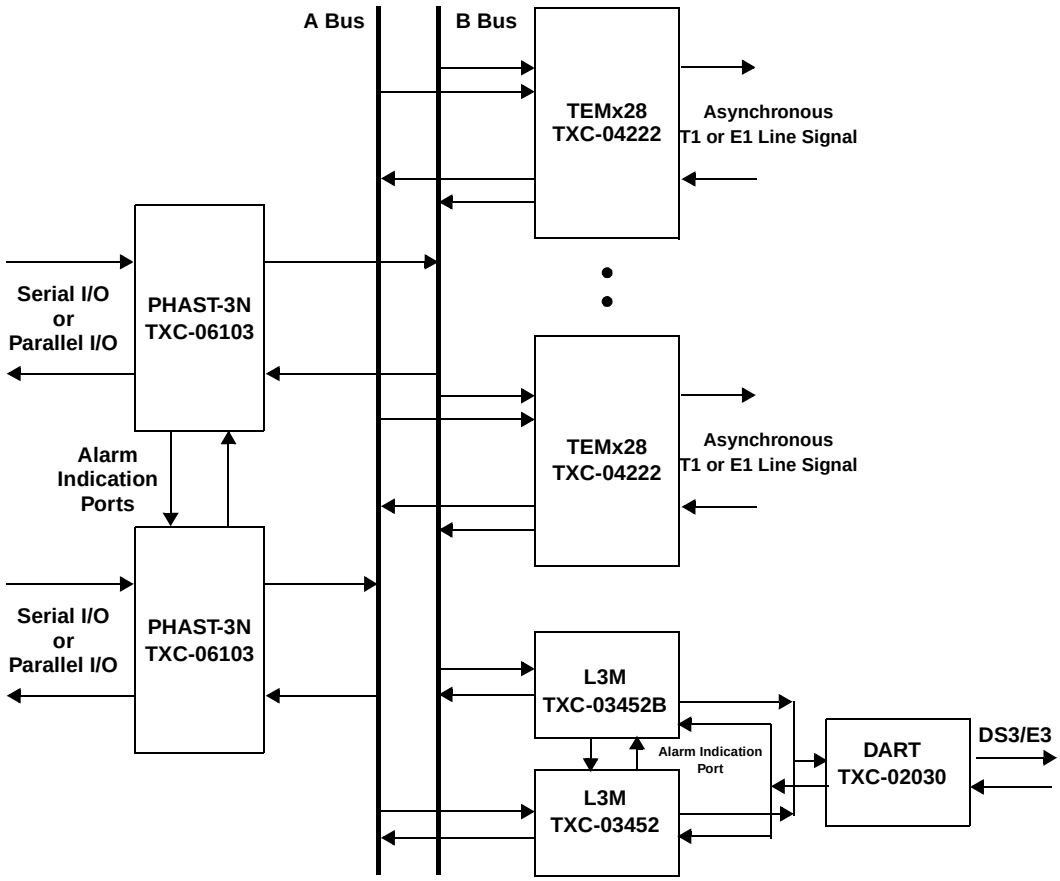


Figure 45. Bidirectional add/drop Fiber Multiplexer

ORDERING INFORMATION

Part Number: TXC-06103AIBG 256-Lead Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). The ART performs the transmit and receive line Body-indent interface functions for interfacing STS-1 (51.84 Mbit/s) and DS3 (44.736 Mbit/s) signals at a coaxial interface.

TXC-02030, DART VLSI Device (Advanced E3/DS3/STS-1 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s), STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). Maps a 44.736 Mbit/s DS3 or 34.368 Mbit/s E3 asynchronous line signal into an STM-1/STS-3/STS-1 formatted synchronous signal. Separate add/drop bus timing is available for loop multiplexers. The L3M provides the overhead processing for the mapped signal.

TXC-03453, TL3M VLSI Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3, or STS-3 STS-1 SPE SDH/SONET signal. An 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is COMBUS, byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

TXC-03456, L4M VLSI Device (Level 4 Mapper). Maps a 139.264 Mbit/s asynchronous line signal into an AU-4 VC-4/STS-3c SPE signal. The SONET/SDH signal is transmitted via the add bus with timing derived from the drop bus, add bus or an external source. The L4M provides test features such as line loopback, SONET/SDH loopback and on-chip test pattern generator and analyzer. The L4M meets strict jitter requirements to transport broadcast grade video signals.

TXC-04201 and TXC-04201B, DS1MX7 VLSI Device (DS1 Mapper 7-Channel). The DS1MX7 maps seven DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope.

TXC-04216, E1Mx16 Device (Sixteen channel E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects sixteen E1 signals with any sixteen asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface. This device is an MCM containing four TXC-04252 QE1M device dice.

TXC-04222, TEMx28 Device (21/28 Channel Dual Bus High Density Mapper). The TEMx28 device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-04228, T1Mx28 Device (DS1 Mapper 28-Channel). The T1Mx28 maps 28 DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope. This device is an MCM containing four TXC-004201B DS1Mx7 device dice.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. It has programmable STS-1 or STS-N modes. It operates from a 3.3 volt supply.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated PHAST-3N Data Sheet that have significant differences relative to the previous and now superseded PHAST-3N Data Sheet.

Updated PHAST-3N Data Sheet: *PRELIMINARY* Ed. 5, May 2001

Previous PHAST-3N Data Sheet: *PRELIMINARY* Ed. 4, October 2001

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of Changes
All	Changed edition number and date.
1	Updated Patent number on bottom of page.
93	In section Receive Path AIS Generation, changed in fourth and fifth bullet from the bottom of page “TCMSAE” to “TCTSAE”.
94	In section TranSwitch Defined Path AIS Generation, changed in fourth and fifth bullet from the bottom of page “TCMSAE” to “TCTSAE”.
97	In section Receive Terminal Interface Bus, changed in fourth and fifth bullet from the bottom of page “TCMSAE” to “TCTSAE”.
101	Added Note to second from last bullet on page.
103/104	Changed in bullet sections all references of “TCALME” to TCTLME”.
105	Added “and TSAISE are both a 1” to fourth bullet in section on top of page.
111	In description for H4 Byte, mode 110, changed in first sentence “input” to “output”.
126/148	Added the following sentences to Terminal Loopback and STS-3 STS-1 Terminal Loopback sections on page 125: For Terminal loopback or STS-1 source timing mode, the transmit H4 mode must be either “terminal interface”, or “locked to terminal interface”. Memory map, or V1 pulse options cannot be used. Added same sentences on page 147, address 00F bits 6, 3, 2, and 1.
197	In description for address 442 bit 6 , removed second and third bullets from description.
198	In description for address 443 bit 6 , removed last two bullets from description.
200	In address 446, added bits 2, 3, and 4 and included descriptions. Added Note to bottom of page referring to address 442.
217	In address 4FC bit 7, added the following Note: This alarm is not inhibited by an incoming TCAIS.
218	Added in address 4FC bit 5 “and TCTIME (bit 2 in register 446)” to last sentence in bit description, and added the following note: This alarm is not inhibited by an incoming TCAIS. Added in second sentence in descriptions for bits 3 and 4 “and TC frame alignment is established” and added Note to description.
243	In Figure 44, removed from drawing references to QE1M and QT1M, and replaced with TEMx28.
244	Replaced in Related Products section references to QE1M and QT1M, and replaced with TEMx28.
247	Updated List of Changes section.

- NOTES -

DOCUMENTATION UPDATE REGISTRATION FORM

If you would like to receive updated documentation for selected devices as it becomes available, please provide the information requested below (print clearly or type) then tear out this page, fold and mail it to the Marketing Communications Department at TranSwitch. Marketing Communications will ensure that the relevant Product Information Sheets, Data Sheets, Application Notes, Technical Bulletins and other publications are sent to you. You may also choose to provide the same information by fax **(203.926.9453)**, or by e-mail **(info@txc.com)**, or by telephone **(203.929.8810)**. Most of these documents will also be made immediately available for direct download as Adobe PDF files from the TranSwitch World Wide Web Site (**www.transwitch.com**).

Name: _____

Company: _____ Title: _____

Dept./Mailstop: _____

Street: _____

City/State/Zip: _____

If located outside U.S.A., please add - Country: _____ Postal Code: _____

Telephone: _____ Ext.: _____ Fax: _____

E-mail: _____

Please provide the following details for the managers in charge of the following departments at your company location.

Department	Title	Name
Company/Division	_____	_____
Engineering	_____	_____
Marketing	_____	_____

Please describe briefly your intended application(s) and indicate whether you would like to have a TranSwitch applications engineer contact you to provide further assistance:

_____

_____

_____

_____

If you are also interested in receiving updated documentation for other TranSwitch device types, please list them below rather than submitting separate registration forms:

_____ _____ _____ _____ _____ _____ _____

_____ _____ _____ _____ _____ _____ _____

Please fold, tape and mail this page (see other side) or fax it to Marketing Communications at 203.926.9453.

TRANSWITCH®

Engines for Global Connectivity

(Fold back on this line second, then tape closed, stamp and mail.)

TRANSWITCH

3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

First Class Postage Required

TranSwitch Corporation

Attention: Marketing Communications Dept.
3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

(Fold back on this line first.)

Please complete the registration form on this back cover sheet, and mail or fax it, if you wish to receive updated documentation on selected TranSwitch products as it becomes available.