EtherMap™-48 Device
OC-48 SONET/SDH Ethernet Mapper
TXC-06710

TECHNICAL OVERVIEW

PRODUCT PREVIEW

FEATURES

- Single STS-48/STM-16 or 4xSTS-12/STM-4 line-side interfaces
- On-chip 622 MHz clock synthesis
- 4xSTS-12/STM-4 and STS-48/STM-16 Framing
- Transport Overhead Termination and Processing
- Supports contiguous Concatenation at STS-1 granularity
- Pointer tracking at AU-4-16c/AU-4-4c/AU4/AU3/TU3 levels
- Full Duplex cross connect at both STS-1-VC-3 and TU-3-VC-3 granularity, with facility for Line and Terminal side STS-1 Path level loopbacks
- Full Path Overhead Processing and Termination, at the HO/LO Path Level.
- Retiming at HO Path Level (STS-1 through STS-48/48c level)
- Ring ports, K1/K2 ports, TOH and POH ports for TOH/POH Bytes
- Full support for HO Virtual Concatenation to ANSI T1.105/ITU-T G.707/G.783 with or without LCAS (ITU-T G.7042)
- Terminal-side interfaces for 4x GMII interfaces (Gigabit Ethernet with MAC) and up to 24x SMII Interfaces (100 Mbit/s Ethernet)
- Terminal-side Serial Data and Reference clock interfaces for the 4x1.25 GHz SerDes for 8B/10B block encoded clients
- Provides Ethernet 100/1000 Mbit/s Framed PDU mapping over GFP (ITU-T G.7041) or LAPS (ITU-T X.86)
- Provides transparent GFP mapping for standard 8B/10B block coded clients, such as Gigabit Ethernet, Fibre Channel (ANSI X3.230), ESCON (ANSI X3.296), and FICON.
- Provides configuration and Flow Control support for over-subscribed operation of Gigabit Ethernet (4xGigE into a single OC-48) or Fast Ethernet clients
- Mailbox interface with API for device configuration with higher level messages
- 2.5 V/3.3 V I/O, 1.3 V core
- 676-lead SFC Ball Grid Array package

DESCRIPTION

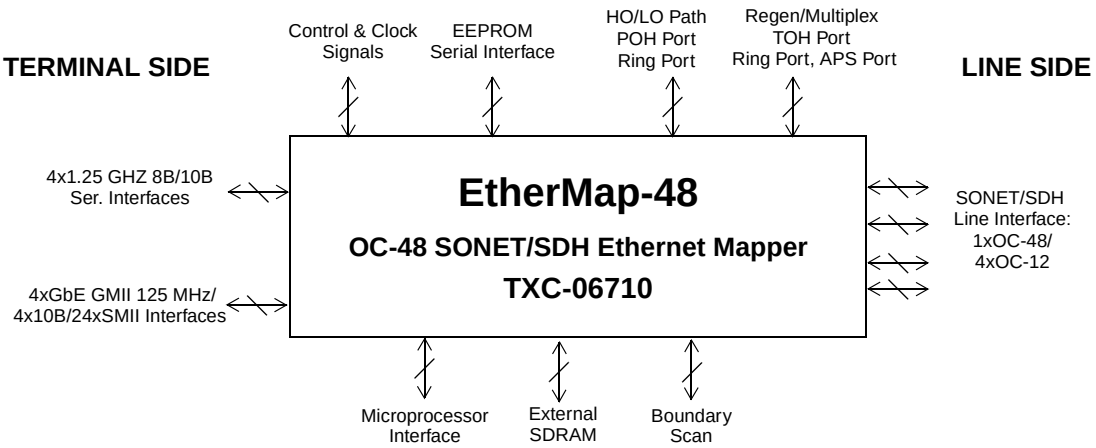
The EtherMap™-48 Device is a highly integrated, STS-48/STM-16 rate SONET/SDH VLSI device, for mapping of Gigabit/100BaseT Ethernet and 8B/10B block encoded traffic like Gigabit Ethernet, Fibre Channel, FICON, ESCON into SONET/SDH Transport. The EtherMap-48 addresses Metro applications such as the transport of switched Ethernet for point-to-point connections of aggregated Ethernet and Packet traffic, and Storage Area Networks (SAN).

The EtherMap-48 SONET/SDH interface consists of one full duplex STS-48/STM-16 channels, which can also operate at a 4xSTS-12/STM-4 rate. The EtherMap-48 provides single OC-48 or Quad OC-12 framing. There is full TOH/POH processing and monitoring, along with full Virtual Concatenation and LCAS support.

The EtherMap-48 Ethernet interface consists of four 1.25GHz SerDes for the 8B/10B clients, including Gigabit Ethernet, and 4xGMII interfaces for Gigabit Ethernet, lead-multiplexed with 24xSMII Fast Ethernet interface. Over-subscription for mapping four Gigabit Ethernet streams into a single STS-48/STM-16 by statistical multiplexing are supported via configuration and built-in flow control mechanisms.

APPLICATIONS

- SONET/SDH add/drop and terminal multiplexers
- Multi-service access platforms
- Next generation Ethernet switches
- Storage Area Network Equipment
- Transparent LAN services
- Ethernet Private Line Services



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LIST OF FIGURES

APPLICATION EXAMPLES

The EtherMap-48 can be used in a wide range of telecommunications applications, such as:

- SONET/SDH add/drop and terminal multiplexers
- Storage Area Network Applications
- Multi-service access platforms and LAN services
- Next generation Ethernet switches

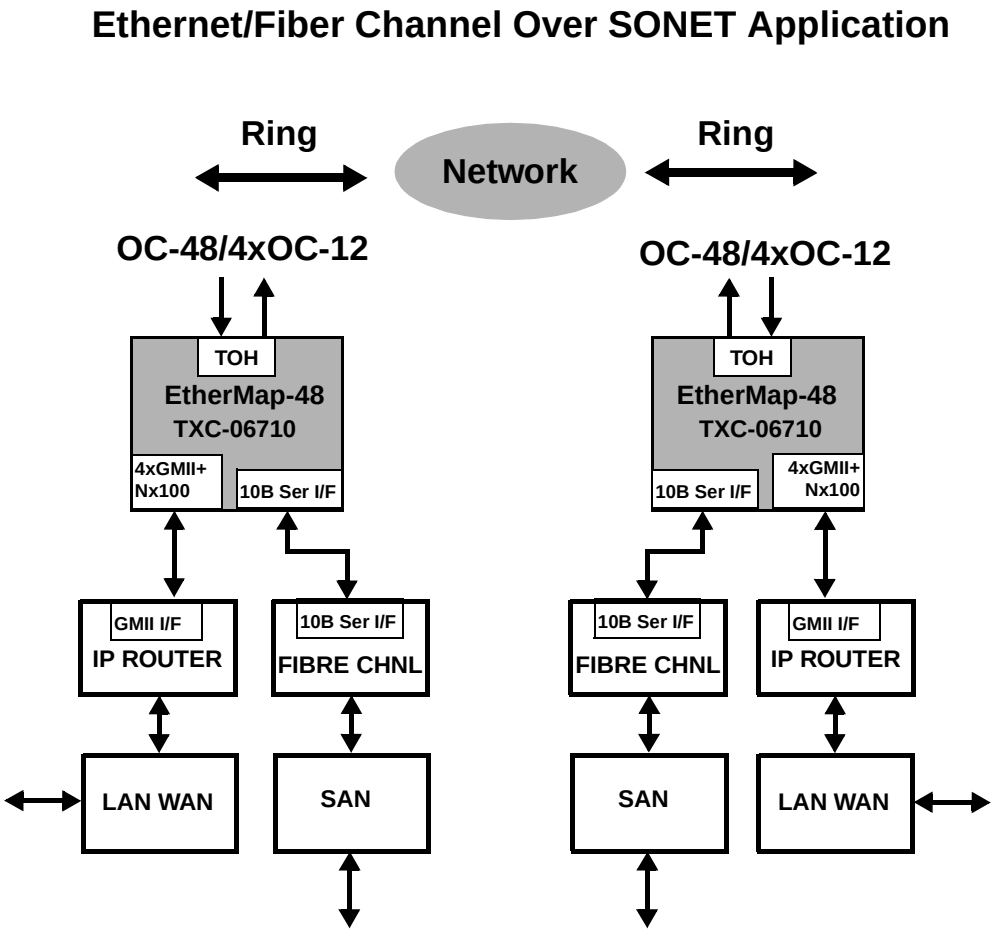

Figure 1. Typical Application using the EtherMap-48 Devices

Figure 1 shows two EtherMap-48 devices being used in a IP Router Application (with IEEE 802.3z Gigabit Ethernet over SONET/SDH as the Transport), and in a Storage Area Network Application, based on ANSI X3.230 Fibre Channel.

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In Figure 2 below, it is possible to map four Gigabit Ethernet interfaces into a single OC-48 line, in an over-subscribed mode. The full-duplex PAUSE frame flow control mechanism provided by the on-chip MACs supports this application. A scaled version of this application, i.e., a single GbE port into a single OC-12 application is also possible. The application is shown below with multiple GbE ports being used.

Multiple Gigabit Ethernet Mapping with Over-Subscription Application

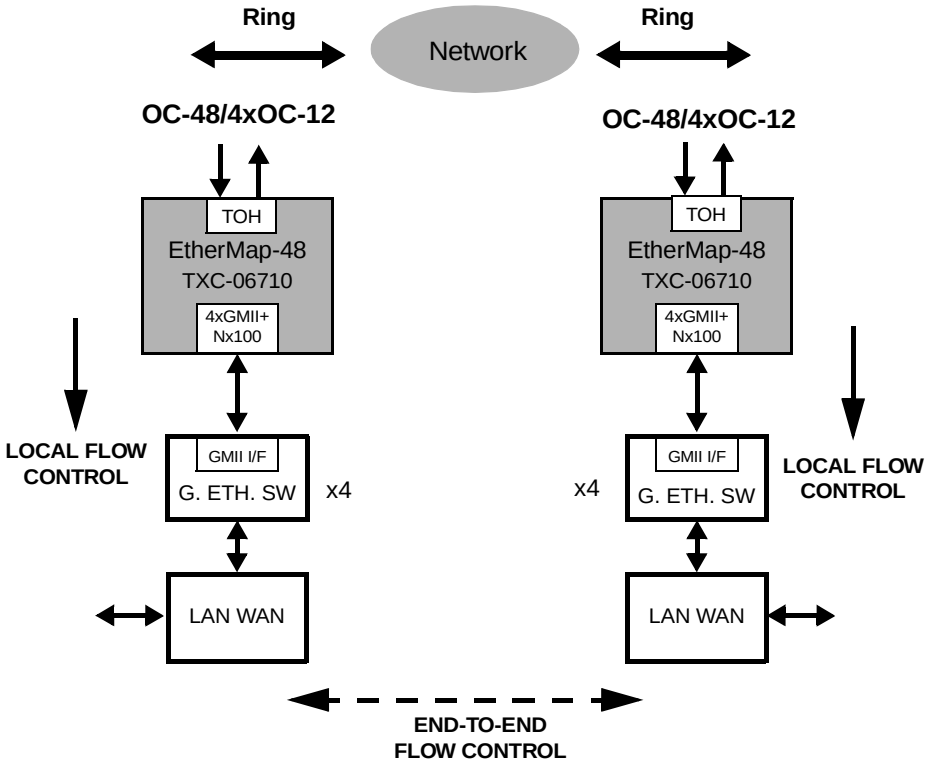

Figure 2. Typical Application for Over-Subscription

The 4xOC-12 Front end provides flexibility in Add/Drop Multiplexer Applications, and inter device operability. In the following diagram, most of the devices that are shown working together in a daisy chained manner, are with dual line interfaces, either OC-48 or OC-12. Note that it is not necessary for the devices pictured below, to be working at full capacity; it is the flexibility that is emphasized.

Flexible Add/Drop Multiplex Application

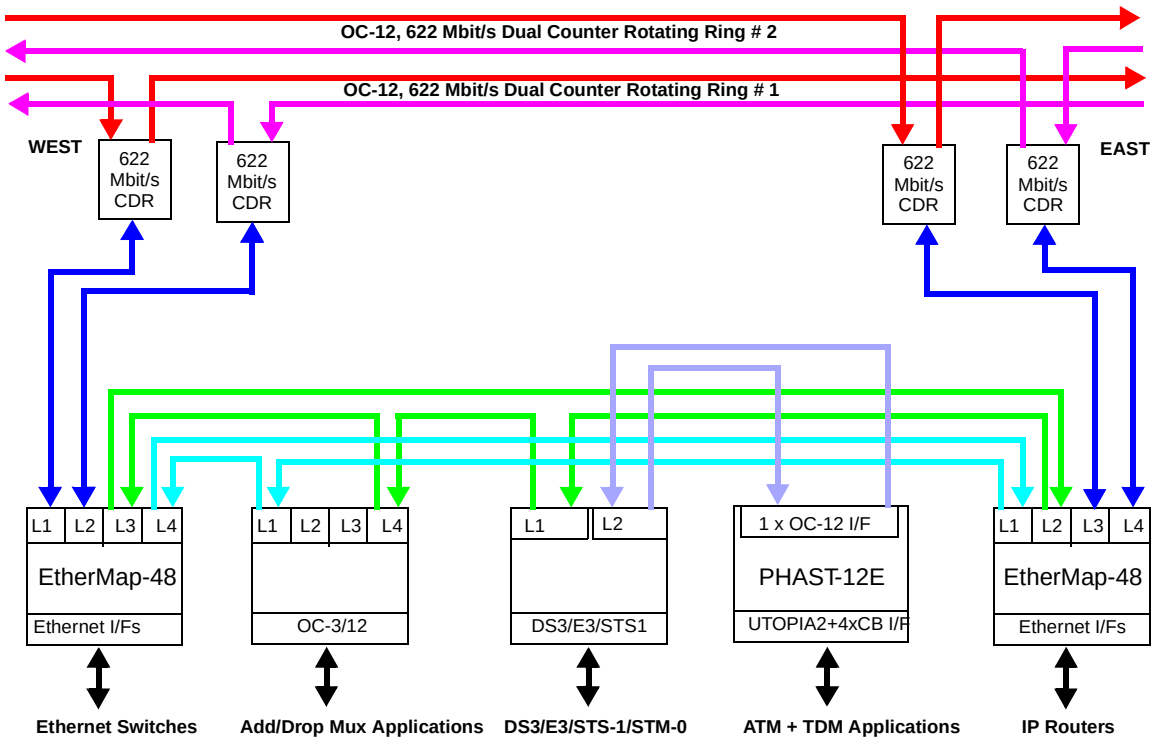

Figure 3. Flexible Add/Drop Multiplex Application

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FUNCTIONAL DESCRIPTION

The block diagram of the EtherMap-48 is shown in Figure 4 below:

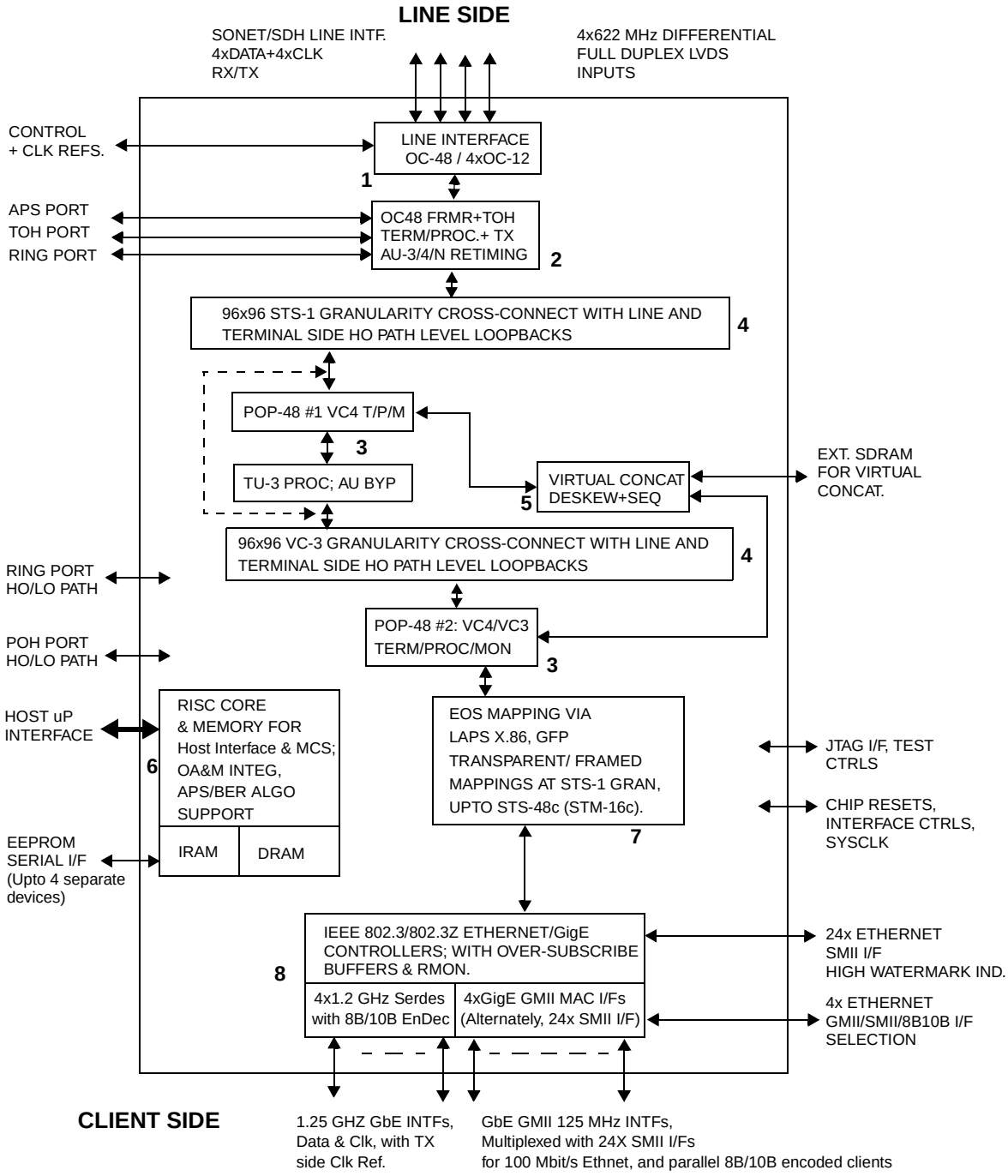


Figure 4. EtherMap-48 TXC-06710 Block Diagram

The TranSwitch EtherMap-48 provides the following features (Refer to the Block Diagram of Figure 4 above for the functional blocks, which are referenced by number in the following sections):

Line Interface (refer to functional block number 1):

- The Line Interface is configurable for Full Duplex 1xOC-48, or quad independent 4xOC-12 operation.
- The OC-48/4xOC-12 Line has 4x622 MHz Differential LVDS data/clock interface for each of the Receive and Transmit sides, with 4 independent differential clock input for the 4xOC-12 mode. The interface is to the OIF SFI-4 standard. Each OC-12 line is single 622 Mbit/s LVDS Data.
- On-chip Clock Synthesis for the Transmit side is provided. Reference input clock of 19.44 MHz is required.
- For the Receive Side Data and Clock input is assumed.
- Scrambled and Unscrambled Data input.
- LOS monitoring; Automatic Laser Shutdown, on a per OC-12 basis. (Per ITU-T G.775, ITU-T G.958)

Framing and TOH Processing (refer to functional block number 2):

Framing and TOH Processing provides OC-48/4xOC-12 SONET/SDH framing functionality and corresponding section and line overhead processing and termination. The general features of the framing block are as follows. The Framer block can be configured to operate in either OC-48 or OC-12 modes.

Receive side serial input interface and internal data flow comprising:

- A1x/A2x Frame detection is configurable for OC-12/48, optional De-scrambling.
- B1 Byte BIP-8 Calculation/Comparison, option for fixed error interpretation, configurable for OC-12/48.
- ANSI/ETSI options for LOS / OOF detection.
- H1x/H2x/H3x Pointer Byte processing for AU's/VC's, ANSI/ETSI options for SS bits and AIS to LOP transitions. The Pointer Tracking FSM handles contiguous concatenations of any order; STS-Mc, where $M \leq 48$.
- B2x, M1 Byte, BIP-384 Calculation/Comparison, option for bit/block error interpretation, configurable for OC-12/48.
- E1, E2, F1, S1, MDB1-6, D1-D12 Bytes to be extracted from the appropriate byte time slots, and forwarded to a RX TOH external interface comprising byte wide data, clock and frame reference, with a programmable marker pulse that can be programmed for identifying selected TOH bytes. The other bytes, A1/A2, C1/J0, H1/H2/H3, K1/K2 can also be forwarded, but unmarked.
- Dedicated K1/K2 APS RX Port in addition to the TOH Buffer and TOH Port.
- Internal Buffer provided for microprocessor access.
- ANSI J0 byte processing/ ITU-T J0 Trail Message Comparison for OC-12/48.
- Path AIS Detection.
- Received Positive and Negative Pointer justification and NDF Performance Counters

Transmit side serial output interface and internal data flow comprising:

- Test Line AIS insertion on input side faults - Transmit input Loss of Clock.
- Path AIS Insertion.
- E1, E2, F1, S1, MDB1-6, D1-D12 Bytes inserted into the appropriate byte time slots, read in from an internal TX TOH buffer, writable via Message Interface, that can be programmed for marking particular TOH bytes. The other bytes, A1/A2, C1/J0, H1/H2/H3 K1/K2 can also be read in from the byte wide TOH buffer, but unmarked.
- Dedicated K1/K2 APS TX Port in addition to the TOH Buffer and TOH Port.
- K2 RDI bits transmission on Receive side LOS, LOF, LOC or RX Line AIS detect.
- B2x, M1 Byte, BIP-384 Calculation and insertion.

- H1x/H2x/H3x Pointer Recalculation (for VC's) or Insertion (Pass through for AU's) with Concatenation Bytes to support arbitrary contiguous concatenations.
- Higher Order Path Retiming and Pointer Generation.
- B1 Byte BIP-8 Calculation (with option for fixed error interpretation) and Insertion.
- Optional Scrambling of the data stream - excepting the A1x/A2x/C1(J0) bytes.
- A1x/A2x Frame insertion.

Also provided are:

- Performance Counters for B1 BIP-8 errors, Positive and Negative Justification Counters for the Pointer Tracking and Pointer Generation state machines.
- Control options to disable TOH/DCC byte extraction and insertion in the RX and TX sides respectively.
- One external Section and Line Level Ring Port, with Serial Clock, Data and Frame Reference, that serve both the Framer and TOH Processing blocks.
- Two types of Line Side Loopbacks involving full payload: i) With the Serial Transmit output looped back towards the Serial Receive input, along with the Transmit side active clock; and ii) With the Received Line Side data and clock looped back towards the Transmit Line. It is not possible to engage both (i) and (ii) simultaneously, that is a bidirectional loopback.
- Independent Retiming FIFO's for 48 independent STS-1s.
- Pointer Generating State Machines 48 STS-1s.
- Retiming of concatenated AUGs, arbitrary concatenated SPEs, with concatenation indicator generation.
- Optional Path AIS insertion on FIFO Error.
- B2x byte BIP detectors, Bit and Block error counting, and BER measurement with programmable error thresholds and detection times.
- S1, Synchronization status byte, debounced and made available for readout.

STS-1_VC-3/4 and TU-3_VC-3 Cross Connects (refer to functional block number 4):

- There are two separate 96x96 Cross Connects provided, for HO/LO Receive and the Transmit paths, basically organized as a Time-Space-Time Switches. Serves to switch Frame aligned AU-3/AU-4 terminated STS-1 SPE columns, and Frame and SPE aligned TU-3 terminated VC3_SPE columns.
- The Input end supports HO/LO path level loopbacks, in the respective Cross-Connect blocks, in a completely general manner. There are no restrictions to the number STS-1/VC-3 path level loopbacks that may be engaged at any given time.
- Cross-Connect at minimum VC-3 (STS-1) granularity (in the case of the HO path switching, preserves any generalized contiguous concatenated group through the switching operation).
- Supports Broadcasting and Multicasting.
- Output End: Automatic HO/LO VC-3 level Unequipped Insertion if any output VC-3 (or corresponding block of bandwidth) is unassigned, as per the requirements of ITU-T G.783 and GR-253, TelCordia, September 2000.
- Output End: Per Path AIS insertion control (Squelching Functionality).

POH Processing Features (refer to functional block numbers 3 and 5):

- The block actually comprises two parts, 48 POH processing channels each, to handle the maximum possible 48 HO Path processing, and the max of 48 channels of LO Path (TU-3) path processing.
- Handles POH processing on a per STS-1/VC-3 basis, for the OC-48/4xOC-12 modes. Each channel of the HO POH processing block can be programmed to be on any of the total 48 STS-1 timeslots that are available; same is true for the LO POH and the low order VC-3 timeslots. All the concatenation types generated and recognized by the Framing and TOH block, are understood by the HO POH processing block.

- Microprocessor access to all nine POH bytes with read and write override capability on G1, N1, K3, F3 and H4.
- J1 16 byte storage with ITU/ETSI message comparison, CRC-7 check and optional Path AIS generation on Trace Identification Mismatch.
- 64 Byte ANSI J1 message comparison, with (a) CRC-7 option and (b) LF/CR option.
- 16 byte J1 insertion from microprocessor written Reference.
- B3 error checking and bit/ block error counting.
- B3 calculation and insertion with optional error insertion.
- C2 Path Signal Label mismatch, VC AIS and unequipped detection with optional Path AIS generation on mismatch.
- C2 insertion under microprocessor control.
- H4 byte processing for Virtual Concatenation, based on [G.707], [G.783], [G.803] and [G.805] along with Link Capacity Adjustment Scheme (LCAS), based on the [G.7042] document. The H4 processing on chip includes the Virtual Concatenation Multi Frame processing, along with the LCAS state machine to achieve hitless capacity adjustment. The LCAS packets uses Bits 7-4 of the H4 Byte, in a separate embedded Multi-frame structure. LCAS operation compatible with non LCAS systems. There is adequate memory on-chip to achieve 125us Differential Delay Compensation (for a total of single OC-48 worth of payload). All higher needs are met with an external SDRAM. It is important to note that when the POH processing channel applies to a TU-3_VC-3, the H4 byte processing Virtual Concatenation still applies, and may do so across different TUG-3 structures.
    - An external buffer memory is required by the EtherMap-48 device for Virtual Concatenation Processing. The on-chip memory controller provides a 'glueless' interface to high speed synchronous 64-bit wide SDR SDRAM, for the incoming OC-48 line. No external timing or control logic is required. The SDRAM memory controller directly addresses up to 16 Mbytes of external buffer memory offering significant buffering capacity. Thus the capacity of the external SDRAM interface is enough to compensate for up to 50 milliseconds of differential delay.
- G1 processing for single bit RDI, three bit RDI and REI with counter.
- G1 inserted either calculated from received B3 errors and selectable single or three bit RDI.
- Supervisory unequipped generation.
- Path Overhead Byte Insertion - From RAM, interfaces, terminal, ring (mate device) or Receive side (eg., RDI).
- K3 byte processing on chip, and K3 byte access.
- Single Alarm Indication Port (AIP) (or Ring Port) for combined High Order and Low Order Path Ring operation and USHR/P support. The external Port supports both the AU-3/4 and TU-3 Ring port information. There is a Top Level AIP/POH Port combiner block.
- The F2, F3 Data Links from all of the OC-48/4xOC-12 lines, are made available via an external port, for external processing as needed. The external Port supports both the AU-3/4 and TU-3 POH bytes.
- TU-3 Pointer tracking for all the constituent TU-3_VC-3s. TU-3 Pointer Tracking and Pointer Regeneration features are similar to what is provided for the HO pointer tracking and regeneration. The LO POH processing features are similar to the HO POH processing
- If there is no TU-3 Pointer Tracking applicable, then the same is bypassed.

Main Mapper Features (refer to functional block number 7):

The main Ethernet over SONET Mapper Block supports the following Mapping modes:

- Generic Framing Procedure per ITU-T G.7041 (January 2002)
    - Transparent Mode GFP, that assumes the following types of 8B/10B encoded clients: ESCON (Enterprise System Connectivity), FICON (Fibre Channel - 1GHz), Gigabit Ethernet (Transparently Mapped), DVB-ASI.

- Framed Mode GFP, that assumes the following types of clients: 100 Mbit/s Ethernet, Gigabit Ethernet.
- Link Access Procedure for SONET/SDH, ITU-T X.86 (Draft Documents):
  - LAPS (Link Access Procedure for SONET/SDH), ITU-T X.86: For 100 Mbit/s and Gigabit Ethernet mapping. Granularity - STS-1.
- Each of the Mapping modes is independently configurable, in variable proportions, in terms of STS-1 granularity. All variety of data paths can exist simultaneously. The blocks are configurable to allow a mixed mode operation for different channels.

GFP Framed Mapping Features (ITU-T G.7041) (refer to functional block number 7):

- GFP Core Header Framing, with Core Header scrambling. GFP Frame Delineation Algorithm is used to achieve GFP Frame Sync.
- GFP User (client data and management) frames to support PLI $\geq$ 4 with separate Payload Header and optional Payload FCS. Payload FCS uses the ITU-T CRC-32 polynomial. Message Length is programmable.
- In GFP User Frame Payload Header, in addition to the mandatory Type and tHEC fields, variable extension header also supported, together with an extension HEC (eHEC). The Extension Header is configurable up to 60 bytes. Also, the mandatory Type fields are configurable options (PTI, PFI, EXI and the UPI).
- Null, and Linear type Extension Headers are fully supported.
- Payload Area scrambler x^{43} +1. Receive Side DeScrambler activated only in the SYNC state.
- Loss of Synchronization Alarm and Loss of Signal Alarm for generation of GFP CSF frames.

GFP Transparent Mapping Features (ITU-T G.7041) (refer to functional block number 7):

As per Section 8 of [G.7041].

- On chip 1.25 GHz Serial /DeSerializer (Serdes) with 8B/10B Encoder/Decoder
- Multiplexing of clients possible, on a frame basis, via the port addresses in the User Payload Header in the Common Section.
- Adaptation of 8B/10B Client signals to the GFP Frame via 64B/65B Block codes, per section 8.1 of the [G.7041] document, with support for
  - 10B_ERR code.
  - 65B_PAD code.
- Adaptation of the GFP payload within the SONET/SDH container/Virtually Concatenated container is based on the 8x 64B/65B code block multiframe, with the leading bits of each 64B/65B code, along with a CRC-16 computation in two trailing octets.
- Special rules for running disparity initialization on boundaries of ordered sets for various 8B/10B clients, is supported.
- Rate Adaptation is as follows:
  - Minimum IPG rules for the 8B/10B clients are followed so that, when rate adapting to a local reference clock at the demapping end, even on worst case input-output clock differentials (clock offset requirements are significantly relaxed, +/- 100 - 200 ppm, for the supported frequency range for the 8B/10B clients), after deleting IPG idles, sufficient (> min) remains to ensure frame delineation. Jitter and Wander characteristics depends on the quality of the Local end clock.
  - After 8B/10B encoding, Fibre Channel and FICON full rate is 1062.5 MHz +/- 100 ppm; ESCON is 200 MHz +/- 0.04 MHz; and Gigabit Ethernet is 1250 MHz +/- 100 ppm.

- Alarms and failure Indications:
  - CSF alarms for Fibre Channel, per ANSI X3.230-1994: Loss of Light (LOL) or LOS; 8B/10B Loss of Synchronization. On a Transport ingress failure, the Fibre channel output does not report a CSF, but continuously outputs 10B_ERR.
  - CSF alarms for ESCON, per ANSI X3.296 -1997: LOS, Loss of 8B/10B sync, output failure on Transport Ingress fault.
  - CSF alarms for Gigabit Ethernet, per IEEE 802.3z-1998: LOS, Loss of 8B/10B Sync, output Failure on Transport Ingress fault.

Gigabit Ethernet MAC Features (refer to functional block number 8):

- The Ethernet Block comprises four Ethernet Sub-Blocks, p = 1-4, and comprises of the following components (note that the first three bullets below, form the common parallel multiplexed interface):
  - 4xGMII Gigabit Ethernet Interface.
  - 24xSMII Fast Ethernet interfaces.
  - 4x8B/10B Parallel Ten-bit Interface
  - 4xMACs for the Gigabit Ethernet Interfaces
  - 4xFrame/Flow Control Buffers, with Buffer Management Logic and Client Signal Rate Adaptation (This block is common for both Gigabit Ethernet and 8B/10B block encoded clients (with EOF/SOF and Idle seq. recognition); each buffer block is configurable for 6xFast Ethernet signals. Buffer Overflow/Underflow alarms apply uniformly to both PDU based and Block encoded clients. Flow control watermarks apply only to PDU based clients.
  - 24xSMII interface to MII processing block.
  - 4x8B/10B Block Encoder/Decoder
  - 4x8B/10B decoded character stream to GMII Mac Frame conversion block
  - 4x8B/10B Client and SerDes Alarm Processing Block that includes Disparity Error Checking.
  - Loss of Clock Monitoring for the Parallel multiplexed interface.
- There are four 8B/10B Encoders/Decoders that does the following:
  - Compliant with IEEE 802.3z 1998 Gigabit Ethernet standard, Fibre Channel to ANSI X3.230-1994, ESCON per ANSI X3.296-1997. This implies the 8B/10B Decoder/Encoder interprets the control characters based on a superset of the three standards, and fully supports all Ordered Sets for the Fibre-Channel, Gigabit Ethernet and ESCON.
  - The 8B/10B Block Encoder/Decoder are independently usable by 8B/10B clients not requiring the use of the on-chip SerDes.
  - 8B/10B Decoder/Encoder with Lookup tables. The complete data and control codes based on IEEE 802.3z, 1998 standard, Clause 36, Table 36-1b. Gigabit Ethernet specific ordered sets of control characters are fully supported.
- Client side loopbacks for diagnostic capability.
- Verifies frame integrity (FCS and Length checks).
- Errored frames are either filtered, or passed up to the higher layer.
- Egress Ethernet frame encapsulation, such as padding to achieve minimum length, add preamble, Inter packet Gap (IPG), and CRC generation.
- Programmable IPG.
- Minimum frame size - 64 bytes, maximum frame size: 9.6 k bytes.
- Transparent to IEEE 802.3-1998 VLAN (Virtual LAN) byte.
- Automatic Base page Autonegotiation - for optimal operating conditions, mechanism per IEEE 802.3. Optional Extended Page negotiation is supported.
- Supports IEEE 802.3 mandatory Control and Management Registers.
- Over Subscription support by Device Configuration and Flow Control.

- Option to support IEEE 802.3-1998 Flow Control at each Ethernet Port.
  - Programmable watermarks for FIFO full/empty conditions.
  - Automatic generation of Pause frames based on FIFO fill levels. Note that Full Duplex mode alone is supported.
  - Loss-less flow control on all valid frames of up to 9.6 k bytes. Adequate buffering to achieve this is included on -device in the RX/TX directions.
  - Provides per port side-band Pause state indication for upstream devices.
  - Control option to disable receiving Ethernet Pause frames, that enables transparent transmission of the Ethernet Pause frame.
- Control and Statistics (to IEEE 802.3z-1998) that includes:
  - Detection of device, initialization, Device ID
  - Standard Control and Status Registers grouped by function: MAC Receive and Transmit Control Registers, MAC Receive and Transmit Status Registers, Address Recognition Control Registers, RMON registers (for Network Management), Flow Control Registers
  - Performance counters to ensure roll-over compliance with standards
  - Provides statistic counters to support RMON implementations. For the DTE MIB group, counters is provided for i) TX/RX frames, ii) FCS errors, v) alignment errors, iii) Multicast frames transmitted or received, iv) Broadcast frames transmitted or received, v) Frame length Errors, vi) count valid frames, among others.

8B/10B 1.25 GHz SerDes Features (refer to functional block number 8):

There are four 1.0/1.25 GHz SerDes blocks having the following features:

- Compliant with IEEE 802.3z 1998/ ANSI X3.230 1994.
- For each of the four SerDes blocks, the Receive side Clock Recovery and the Transmit side PLLs are either software programmable (or hardware selectable, for example by a change in reference frequency supplied) to serve the range of clients Fibre Channel (1 GHz Encoded) and Gigabit Ethernet (1.250 GHz).
- Serial loopback.
- Current Mode Logic (CML) I/O pads.
- External differential reference clock input for the Clock Recovery and Synthesis Blocks.
- Loss of Signal Detection.
- Internal Termination resistors.

GigE GMII Interface Features (refer to functional block number 8):

- Each of the four Gigabit Ethernet ports have a GMII interface, to IEEE 802.3z 1998. The signal definitions are as follows:
  - Receive Side: GMII interface comprises byte data, clock, data valid and error indication.
  - Transmit Side: GMII interface comprises byte data, clock (for both Gigabit and fast Ethernet options), transmit enable and transmit error indication.
- The GMII Management Interface comprises Management Clock MDC and Management Serial data I/O.

Host Interface Processor Features (refer to functional block number 6):

- Provides message based communication with the external Host for device configuration/status-retrieval.
- No external dependency for boot up and can exchange simple read/write/goto messages immediately after reset is complete.
- Support for complete firmware download from an external SEEPROM. Requires a simple message from the Host to initiate the download. Optionally, firmware download from SEEPROM can be through a user downloaded program. Alternatively the complete firmware download can be from the Host, not requiring the external SEEPROM.
- Instructions/Data memories available on-chip.
- Writing to the external SEEPROM supported for firmware updates.
- 16-bit Host interface, lead selectable between Motorola/Intel modes.

Serial Boot/Application PROM Memory Feature:

- The EtherMap-48 uses an on-chip Primary and Secondary boot ROM with external SEEPROM Application memory, which initializes the device and performs a bootstrap startup and application load autonomously from this interface requiring minimal intervention from the host processor. After the EtherMap-48 has loaded itself, it will be ready for host communication for initialization and configuration. Firmware upgrades in the field can be downloaded to the external SEEPROM through EtherMap-48 via the host mailbox interface. It shall not be possible to over-write the Boot section of the PROM.

Test Features:

- Standard 5-lead, IEEE 1149.1 compliant TAP for boundary scan.
- Separate 5-lead JTAG port for debug access to the embedded processor.
- Scan and memBist for testability
- High-Z all output leads option
- Test Enable features

General Device Level Features:

- Control and Management via an Unified Messaging Interface
- 16 bit wide external host interface
- Standardized Interrupt, Alarm Handling and Reset schemes
- Internal Performance Counters (One second/ 15 minutes)
- One second Performance and Fault Monitoring registers, with Alarm and Performance Statistics Generation to TelCordia GR-253.
- On chip Ethernet RMON capability IEEE 802.1q
- Test Access Port for IEEE 1149.1 boundary scan
- 2.5 V/3.3 V I/O, 1.3 core
- 676-lead SFC ball grid array package

PRODUCT PREVIEW

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.3V nominal	V_{DD13}			V	Notes 1, 4
I/O Supply Voltage, +2.5V nominal	V_{DD25}			V	Notes 1, 4
DC input voltage	VIN			V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, Method 3015.7.
4. Device core is 1.3V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient			TBD	^{o}C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD25}		2.5		V	
I_{DD25}			TBD	mA	See Notes 1 and 2
P_{DD25}			TBD	W	See Notes 1 and 2
V_{DD13}		1.3		V	
I_{DD13}			TBD	mA	See Notes 1 and 2
P_{DD13}			TBD	W	See Notes 1 and 2

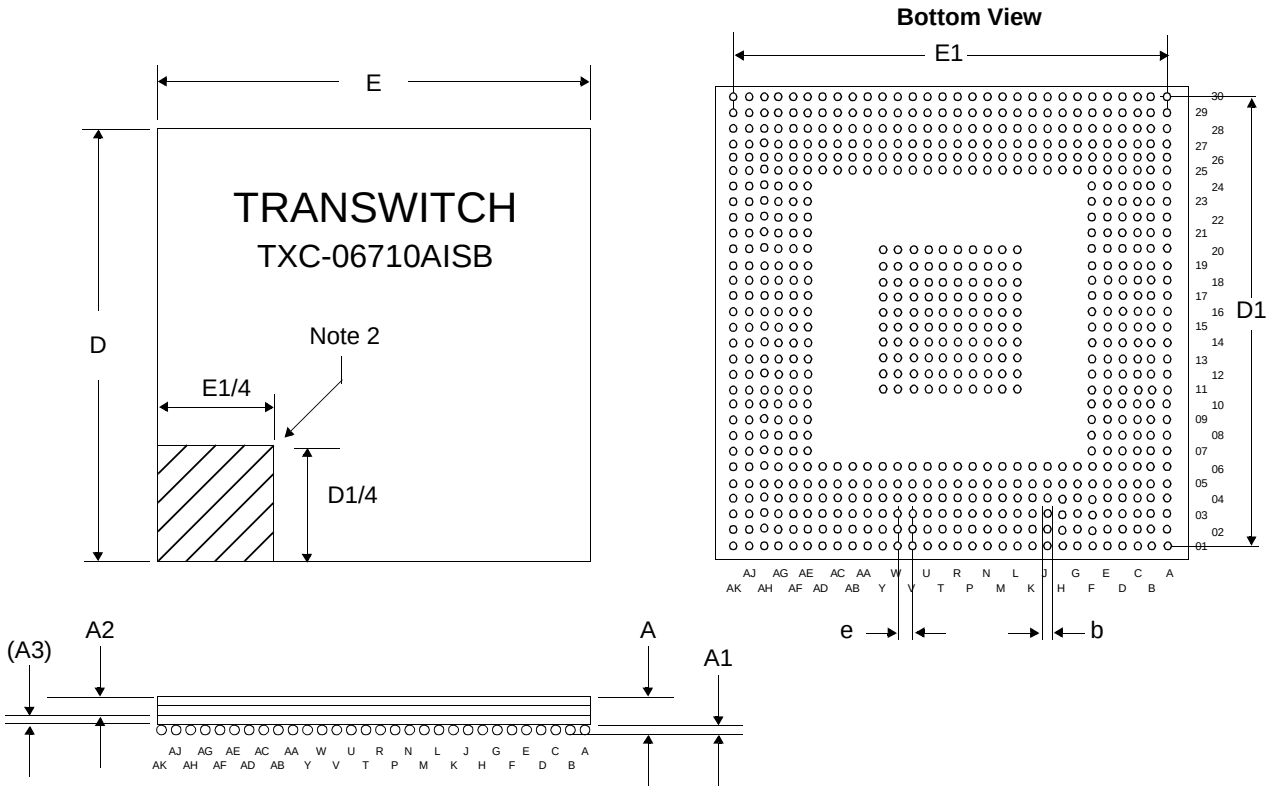
Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.

PRODUCT PREVIEW

PACKAGE INFORMATION

The EtherMap-48 device is packaged in a 676-lead SFC (Super Flip Chip) Ball Grid Array package suitable for surface mounting, as illustrated in Figure 5.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: TBD x TBD, JEDEC code TBD.

Dimension (Note 1)	Nominal
A A1 A2	3.20 0.50 2.54
A3 (Ref.)	1.20
b (Ref.)	0.64
D	31.0
D1 (BSC)	29.0
E	31.0
E1 (BSC)	29.0
e (BSC)	1.00

Figure 5. EtherMap-48 TXC-06710 Package Diagram

ORDERING INFORMATION

Part Number:	TXC-06710AISB	676-lead SFC ball grid array package

RELATED PRODUCTS

TXC-04226, EtherMap-3 Device (Ethernet into STS-3/STM-1 SONET/SDH Mapper). The EtherMap-3 is a highly integrated device that provides for mapping of 10/100/1000 Mbit/s Ethernet into SONET/SDH STS-3/STM-1 Transport payloads. The device supports connection for up to eight 10/100 Mbit/s Ethernet ports, using SMII interfaces, or a single 1000 Mbit/s Ethernet port, using a GMII interface. In the transmit direction, for each port, received Ethernet frames are encapsulated using either GFP, LAPS or LAPF protocol.

TXC-06212, PHAST-12E VLSI Device (Programmable, High Performance ATM/PPP/TDM SONET/SDH Terminator for Level 12 with Enhanced Features). The PHAST-12E is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines or a single STS-12/12c or STM-4/4c line.

PRODUCT PREVIEW

- NOTES -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