QE1F-*Plus* Device
Quad E1 Framer-*Plus*
TXC-03114

PRODUCT INFORMATION

FEATURES

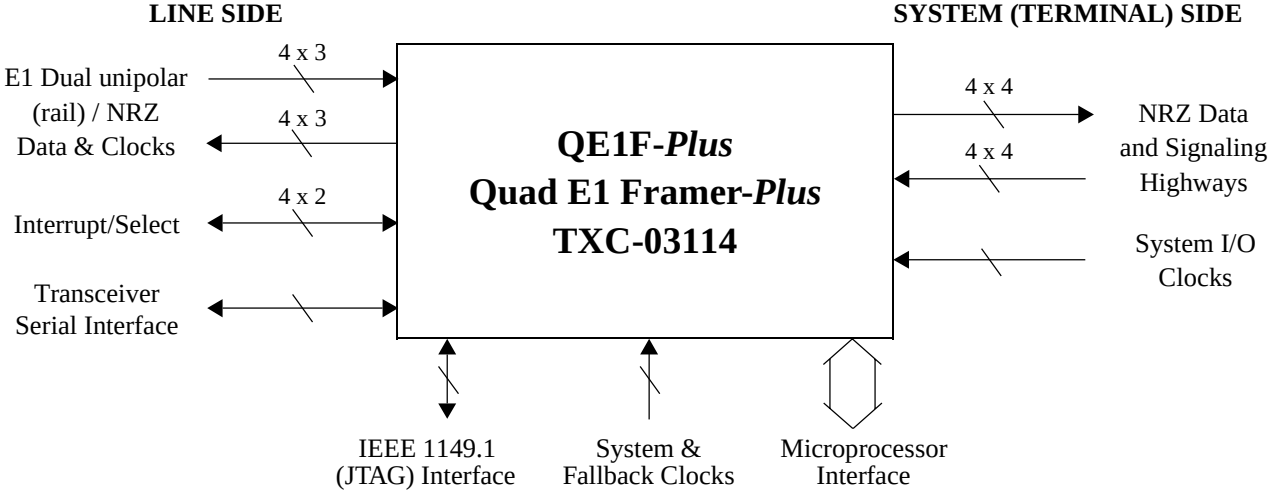
- Offline framer supports Standard and Frame Hold-Off frame alignment with CRC-4 multiframe check and selectable out of frame criteria, and transparent non-framing mode
- Frame alignment detection and loss of frame alignment declaration comply with ITU-T G.706
- Dual unipolar (HDB3/AMI) or NRZ line interface
- Two-frame slip buffers in both receive and transmit directions
- Supports channel-associated signaling in Time Slot 16
- Detects and forces RAI and AIS alarms; detects OOF and CFA framing conditions
- HDLC processing using national bits in Time Slot 0 (up to 20 kbit/s)
- Detects, counts and forces line code errors (BPVs), CRC-4 errors, and frame bit errors
- System Interfaces
  - 2 Mbit/s, 8 Mbit/s and 16 Mbit/s Transmission Modes with gapped clock option for 2Mbit/s
  - 2 Mbit/s MVIP® Mode, 8 Mbit/s H-MVIP® /H.100 Mode and 16 Mbit/s PCM Highway Mode
- Motorola/Intel-compatible microprocessor interface
- One-second interrupt input latches counter values and line events into shadow registers
- Local and remote line loopbacks
- Boundary scan capability (IEEE 1149.1)
- Single +3.3 or +5 V, ±5% power supply
- 128-pin thin plastic quad flat package

DESCRIPTION

The QE1F-*Plus* is a four-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703. The transmit and receive sections of each of the four framers are independent, with individual two-frame slip buffers, which allows operation with a wide range of switching and transmission products. Framing algorithm support for ITU-T G.704, G.706 and ETS 300-011. Access and control for signaling and data are provided via a Motorola/Intel-compatible microprocessor interface. For HDLC link applications, each framer supplies a full duplex HDLC controller in addition to on-board latching of all required performance parameters; minimal software overhead is required. Diagnostic, test, and maintenance functions are provided, including E1 local and remote loopbacks, time slot loopbacks and boundary scan (IEEE 1149.1).

APPLICATIONS

- SDH terminal or add/drop multiplexers supporting E1 byte synchronous operation
- DCS, digital central office or remote digital terminals
- E1 multiplexers
- E1 and fractional E1 CSUs
- ATM products with integrated E1 interfaces
- LAN routers with integrated E1 interfaces
- Multichannel E1 test equipment



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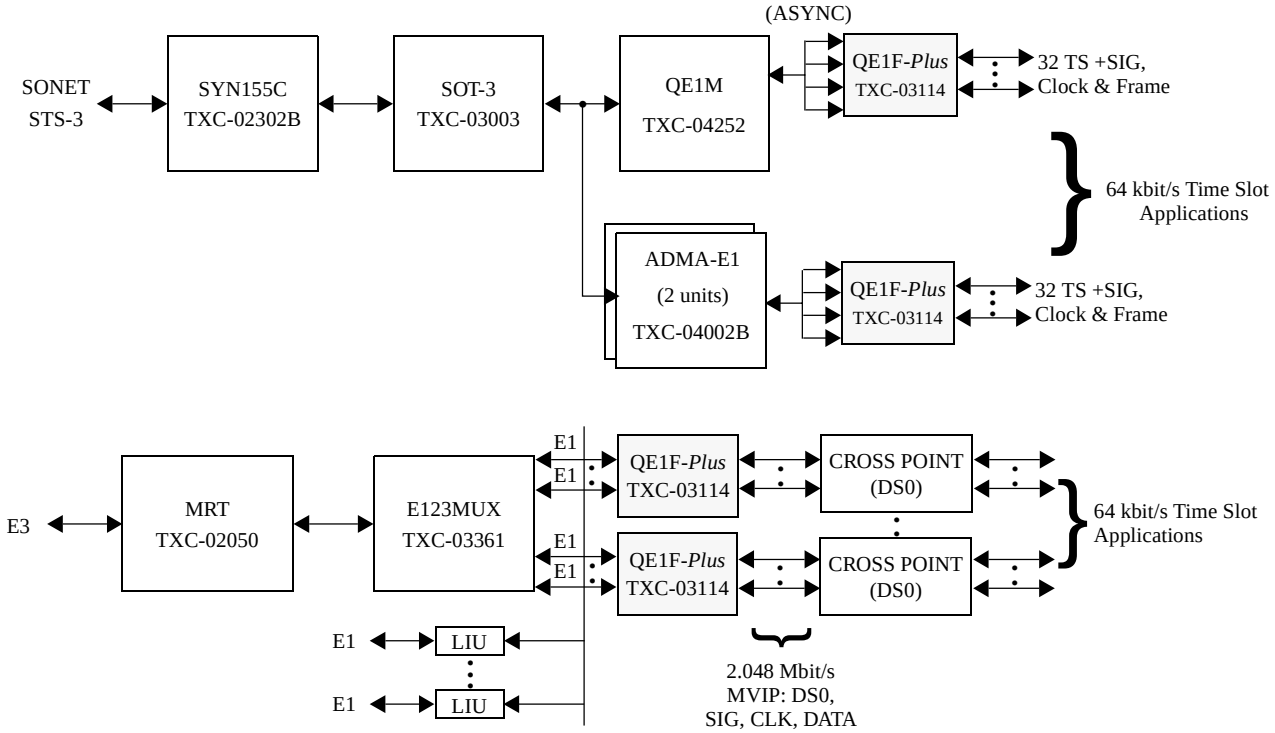
TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

APPLICATION DIAGRAM

The diagram below illustrates the use of the QE1F-*Plus* device to provide framing and Time Slot access for a variety of E1 sources. Direct control of most commercial line interface unit devices (LIUs) is provided. Note that these applications require operating the QE1F-*Plus* at V_{DD} = +5.0 volts to comply with the +5.0 volt parts connected to the QE1F-*Plus*.



RELATED PRODUCTS

• TXC-02020	Advanced STS-1/DS3 Receiver/Transmitter VLSI Device (ART)
• TXC-02021	Advanced STS-1/DS3 Receiver/Transmitter VLSI Device (ARTE)
• TXC-02302B	155-Mbit/s Synchronizer, Clock and Data Output VLSI Device (SYN155C)
• TXC-03001	SONET STS-1 Overhead Terminator VLSI Device (SOT-1)
• TXC-03001B	SONET STS-1 Overhead Terminator VLSI Device (SOT-1)
• TXC-03003	STM-1/STS-3/STS-3c Overhead Terminator VLSI Device (SOT-3)
• TXC-03003B	STM-1/STS-3/STS-3c Overhead Terminator VLSI Device (SOT-3)
• TXC-03011	SONET STS-1 Overhead Terminator VLSI Device (SOT-1E)
• TXC-03104	Quad E1 Framer VLSI Device (QE1F)
• TXC-04002B	Dual E1 to VT1.5 or TU-12 Async Mapper-Desync VLSI Device (ADMA-E1)
• TXC-04252	Quad E1 to AU-4/VT2 or TU-12 Async Mapper-Desync VLSI Device (QE1M)
• TXC-05101C	HDLC Controller, 36-Bit Terminal I/O VLSI Device (HDLC)
• TXC-05150	Cell Delineation Block VLSI Device (CDB)
• TXC-06125	Bit Error Rate Generator/Receiver VLSI Device (XBERT)

FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products.

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