PHAST-1 Device
SONET STS-1 Overhead Terminator
TXC-06101

PRODUCT INFORMATION

FEATURES

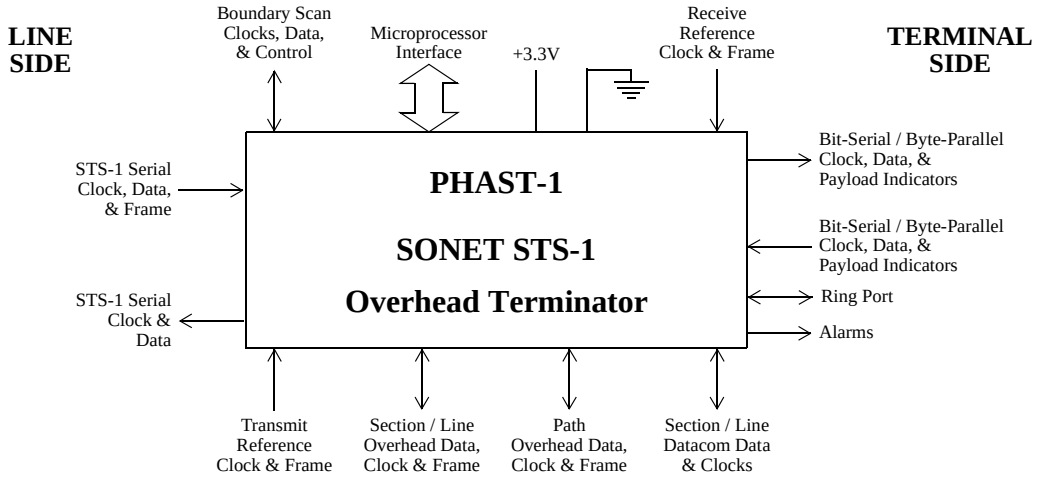
- Provides SONET interface to any type of payload
- Programmable STS-1 or STS-N modes
- Receive bit-serial STS-1 signal input to the Line Side using external reference frame pulse for STS-N applications
- Transmit bit-serial STS-1 signal output from the Line Side using external reference frame pulse for outgoing phase synchronization
- Programmable: full STS-1 or SPE-only I/O on the Terminal Side
- 51.84 Mbit/s bit-serial, or 6.48/19.44 Mbyte/s byte-parallel I/O on the Terminal Side
- Optional AIS communication with peer PHAST-1, SOT-1, SOT-1E, or SOT-3 devices
- Interfaces to microprocessors with hierarchical scan and optional hardware interrupt on alarms
- SONET alarm processing and performance monitoring
- Meets ANSI and Bellcore standards:
  - T1.105-1995
  - GR-1400-CORE
  - GR-253-CORE
  - GR-499
  - TR-NWT-000496
  - GR-1230
- Ring port for USHR/P support
- Boundary Scan Capability (IEEE 1149.1)
- Single + 3.3 volt ± 5% power supply
- 144-pin low profile plastic quad flat package

DESCRIPTION

The PHAST-1 SONET STS-1 Overhead Terminator performs Section, Line and Path Overhead processing for STS-1 SONET signals. This versatile device can be used anywhere in a SONET network where STS-1 signals are in use, e.g., repeaters, and Line or Path termination points. Interfaces are provided for both Section and Line Orderwire and Datacom channels. Further, control bits in the Memory Map enable the PHAST-1 to perform loopback and serial or parallel input/output. Line Side and Terminal Side clock rates can differ. The Receive and Transmit Pointers are recalculated as necessary to compensate for clock differences. All overhead bytes are stored in on-chip RAM. New overhead bytes can be substituted from RAM to either the Terminal or Line Side, depending on the application. The PHAST-1 also provides alarm detection and AIS generation, as well as software and hardware interrupts in the event of errors.

APPLICATIONS

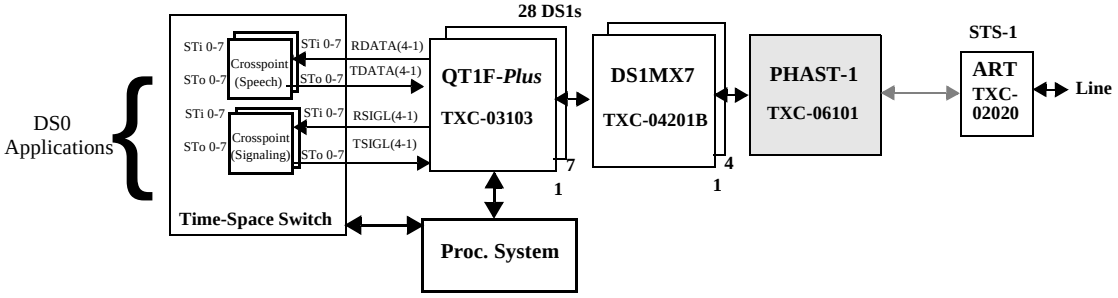
- SONET W-DCS/B-DCS
- SONET terminal or add/drop multiplexers
- High-speed data communication
- Payload extraction, introduction into STS-1
- STS-N multiplexer
- SONET test sets



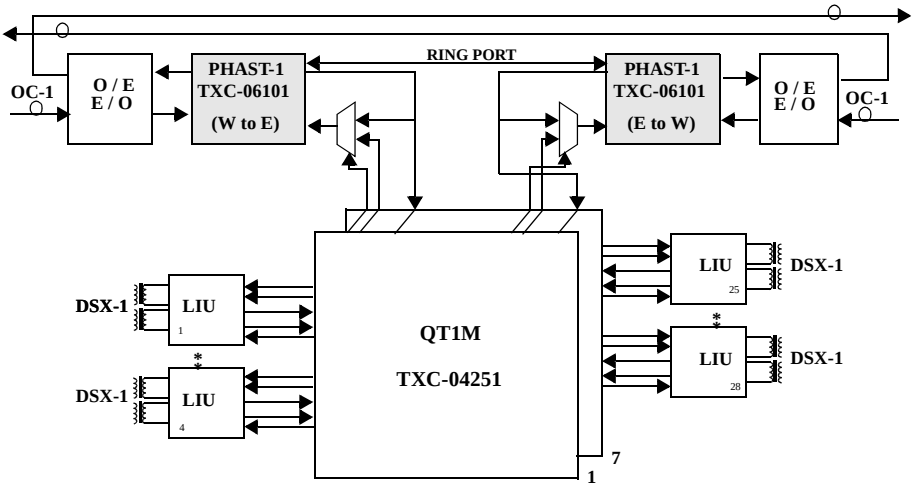
Document Number:
TXC-06101-MC
Ed. 1, July 1998

TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

APPLICATION DIAGRAMS



Asynchronous DS0 to/from Synchronous STS-1 Application



Asynchronous DSX-1 Mapped to OC-1 Ring-Protected Application

RELATED PRODUCTS

- TXC-02020 Advanced STS-1/DS3 Receiver/Transmitter VLSI Device (ART)
- TXC-02021 ART with Extended features (ARTE)
- TXC-03001B SONET STS-1 Overhead Terminator VLSI Device (SOT-1)
- TXC-03011 SOT-1 with Extended features (SOT-1E)
- TXC-03003B SONET STM-1/STS-3/STS-3c Overhead Terminator VLSI Device (SOT-3)
- TXC-03103 Quad T1 Framer-*Plus* VLSI Device (QT1F-*Plus*)
- TXC-03452B Level 3 Mapper/Desynchronizer VLSI Device (L3M)
- TXC-04001B Dual DS1 to VT1.5 Async, Mapper/Desynchronizer VLSI Device (ADMA-T1)
- TXC-04011 Dual DS1 to VT1.5 Async, Mapper/Desynchronizer VLSI Device (ADMA-T1P)
- TXC-04201B DS1 Mapper 7-Channel VLSI Device (DS1MX7)
- TXC-04251 Quad DS1 to TU-11/VT1.5 Async, Mapper/Desynchronizer VLSI Device (QT1M)
- TXC-04252 Quad E1 to TU-12/VT2 Async, Mapper/Desynchronizer VLSI Device (QE1M)
- TXC-05150 ATM Cell Delineation Block VLSI Device (CDB)
- TXC-06125 Bit Error Rate Generator/Receiver VLSI Device (XBERT)

FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products.

Document Number:
TXC-06101-MC
Ed. 1, July 1998