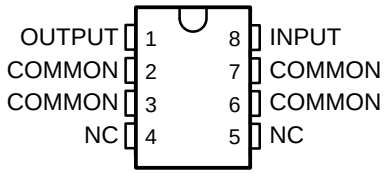
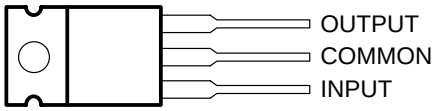
SLVS017M – SEPTEMBER 1987 – REVISED MAY 2002

- **Very Low Dropout Voltage, Less Than 0.6 V at 150 mA**
- **Very Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751L Series**
- **60-V Load-Dump Protection**
- **Reverse Transient Protection Down to –50 V**
- **Internal Thermal-Overload Protection**
- **Overvoltage Protection**
- **Internal Overcurrent-Limiting Circuitry**
- **Less Than 500-μA Disable (TL751L Series)**

TL750L . . . D PACKAGE
(TOP VIEW)



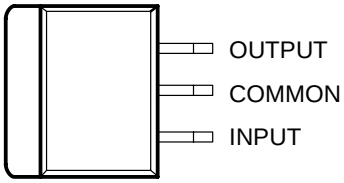
TL750L . . . KC PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

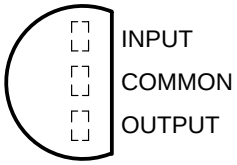
TO-220AB

TL750L . . . KTE PACKAGE
(TOP VIEW)



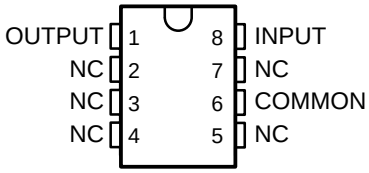
The common terminal is in electrical contact with the mounting base.

TL750L . . . LP PACKAGE
(TOP VIEW)

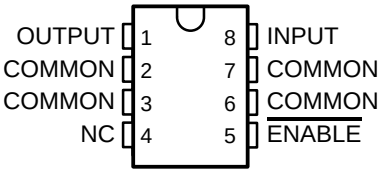


TO-226AA

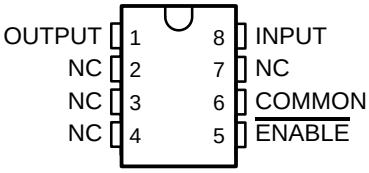
TL750L . . . P PACKAGE
(TOP VIEW)



TL751L . . . D PACKAGE
(TOP VIEW)



TL751L . . . P PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL750L and TL751L series of fixed-output voltage regulators offers 5-V, 8-V, 10-V, and 12-V options. The TL751L series has the addition of an enable ($\overline{\text{ENABLE}}$) input. When $\overline{\text{ENABLE}}$ is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

description (continued)

The TL750LxxC and the TL751LxxC series are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The TL750L05Q and TL751L05Q are characterized for operation over the virtual junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_J	V_O TYP AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	HEAT-SINK MOUNTED (KC)	POWER FLEX (KTE)	PLASTIC CYLINDRICAL (LP)	PLASTIC DIP (P)
0°C to 125°C	5 V	TL750L05CD TL751L05CD	TL750L05CKC	TL750L05CKTER	TL750L05CLP	–
	8 V	TL750L08CD	–	–	TL750L08CLP	–
	10 V	TL750L10CD TL751L10CD	–	–	TL750L10CLP	TL751L10CP
	12 V	TL750L12CD TL751L12CD	–	–	TL750L12CLP	TL751L12CP
–40°C to 125°C	5 V	TL750L05QD TL751L05QD	–	–	–	–

The D and LP packages are available taped and reeled. Add the suffix R to device type (e.g., TL750L05CDR). The KTE package is only available taped and reeled.

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Continuous input voltage . . . . . 26 V
Transient input voltage, T_A = 25°C (see Note 1) . . . . . 60 V
Continuous reverse input voltage . . . . . –15 V
Transient reverse input voltage, t ≤ 100 ms . . . . . –50 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 97°C/W
(see Notes 2 and 4): KC package . . . . . 25°C/W
(see Notes 2 and 4): KTE package . . . . . 23°C/W
(see Notes 2 and 3): LP package . . . . . 156°C/W
(see Notes 2 and 3): P package . . . . . 85°C/W
Virtual junction temperature range, T_J . . . . . –40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds . . . . . 260 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The transient input voltage rating applies to the waveform shown in Figure 1.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

				MIN	MAX	UNITS
V_I	Input voltage		TL75xL05	6	26	V
			TL75xL08	9	26	
			TL75xL10	11	26	
			TL75xL12	13	26	
V_{IH}	High-level $\overline{\text{ENABLE}}$ input voltage		TL751Lxx	2	15	V
V_{IL}†	Low-level ENABLE input voltage	T_A = 25°C	TL751Lxx	–0.3	0.8	V
		T_A = full range‡	TL751Lxx	–0.15	0.8	
I_O	Output current range		TL75xLxx	0	150	mA
T_J	Operating virtual junction temperature		TL75xLxxC	0	125	°C
			TL75xL05Q	–40	125	

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.
‡ Full range is 0°C to 125°C for the TL75xLxxC devices and –40°C to 125°C for the TL75L05Q devices.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted) (see Note 5)

PARAMETER	TEST CONDITIONS§			TL750L05 TL751L05			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V,	I_O = 0 to 150 mA	T_J = 25°C	4.80	5	5.2	V
			T_J = 0°C to 125°C	4.75		5.25	
Input regulation voltage	V_I = 9 V to 16 V				5	10	mV
	V_I = 6 V to 26 V				6	30	
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				20	50	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 6 V to 26 V,	I_O = 10 mA,	T_J = T_J(min) to 125°C¶		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

§ Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.
¶ T_J(min) is 0°C for the TL75xLxxC devices and –40°C for the TL75xLxxQ devices.
NOTE 5: For TL750L05Q/TL751L05Q, all characteristics are measured with a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 4.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL750L08 TL751L08			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V,	I_O = 0 to 150 mA	T_J = 25°C	7.68	8	8.32	V
			T_J = 0°C to 125°C	7.6		8.4	
Input regulation voltage	V_I = 10 V to 17 V				10	20	mV
	V_I = 9 V to 26 V				25	50	
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				40	80	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 9 V to 26 V,	I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL750L10 TL751L10			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V,	I_O = 0 to 150 mA	T_J = 25°C	9.6	10	10.4	V
			T_J = 0°C to 125°C	9.5		10.5	
Input regulation voltage	V_I = 12 V to 19 V				10	25	mV
	V_I = 11 V to 26 V				30	60	
Ripple rejection	V_I = 12 V to 22 V,	f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA				50	100	mV
Dropout voltage	I_O = 10 mA					0.2	V
	I_O = 150 mA					0.6	
Output noise voltage	f = 10 Hz to 100 kHz				700		μV
Input bias current	I_O = 150 mA				10	12	mA
	V_I = 11 V to 26 V,	I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V					0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

electrical characteristics, V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL750L12 TL751L12			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.52	12	12.48	V
		T_J = 0°C to 125°C	11.4		12.6	
Input regulation voltage	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Input bias current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V, I_O = 10 mA,	T_J = 0°C to 125°C		1	2	
	$\overline{\text{ENABLE}}$ > 2 V				0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TYPICAL CHARACTERISTICS

TRANSIENT INPUT VOLTAGE vs TIME

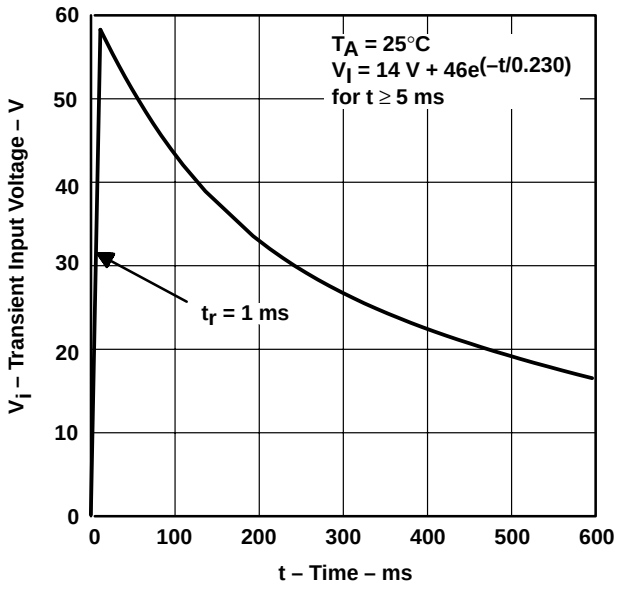


Figure 1

TL750L05 INPUT CURRENT vs INPUT VOLTAGE

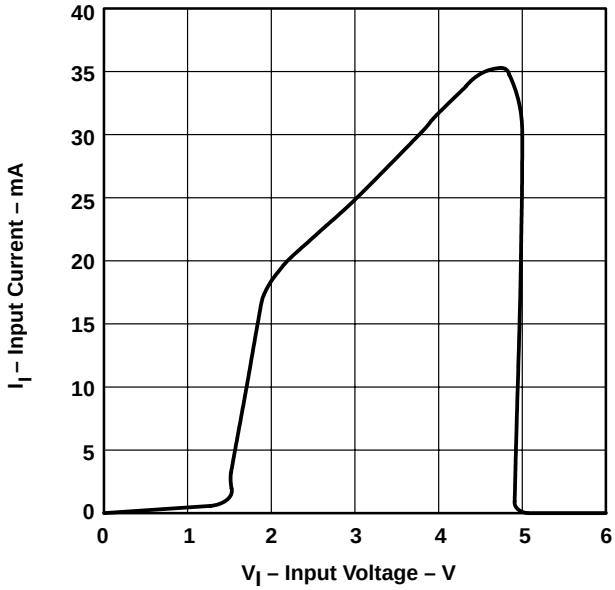


Figure 2

TL750L12 INPUT CURRENT vs INPUT VOLTAGE

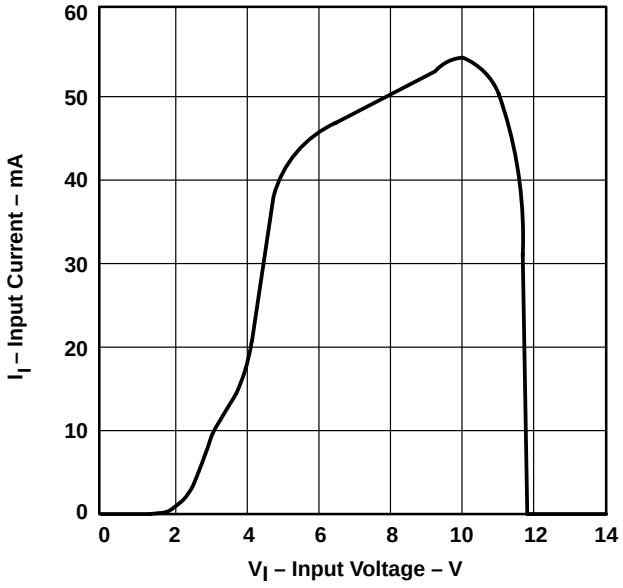


Figure 3

TYPICAL CHARACTERISTICS

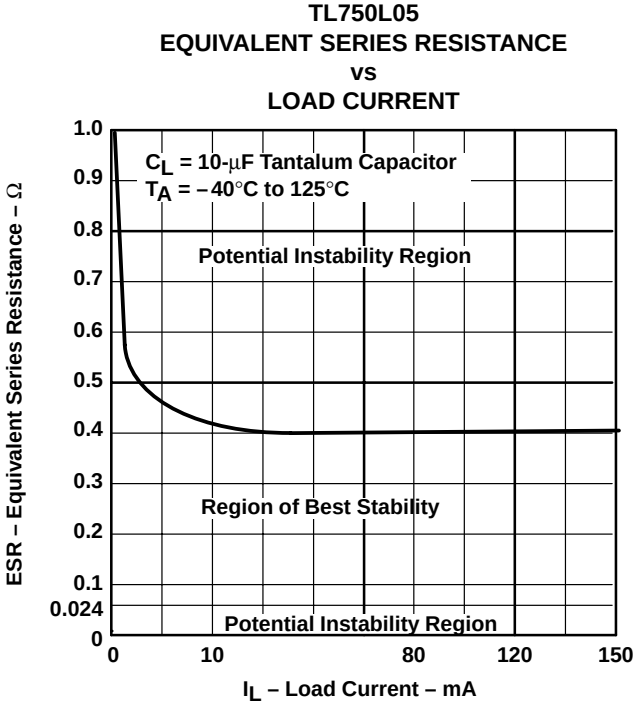


Figure 4

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265