Application Report
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TRF6901 Design Guide

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Mixed-Signal RF

ABSTRACT

This document briefly describes the TRF6901 single-chip RF transceiver and the major RF design techniques and system considerations involved in using the TRF6901 to establish a wireless data link. Many of the topics covered also apply to designing a wireless system using other products in the TRF6900 family.

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1 Introduction

The Texas Instruments TRF6901 is a low-cost RF transceiver that is intended for use to establish a frequency-programmable, half-duplex, bidirectional RF link in the European or North American industrial, scientific, and medical (ISM) bands. It supports binary frequency-shift keying (2-FSK) or on-off keying (OOK) modulation. A terminal location diagram of the TRF6901 is shown in Figure 1. Refer to the data sheet (TI Publication SLWS110, *TRF6901 Single-Chip RF Transceiver*) for additional information.

This document covers some of the basic design considerations and techniques in using the TRF6901 for a wireless transceiver system. Figure 2 is a block diagram of the TRF6901 device. DEM_VCC (terminal 40) supplies power to the band-gap reference as well as to the receive demodulator. If the TRF6901 is used for transmit-only operation, DEM_VCC still must be connected to V_{CC} even though the receive demodulator is not used.

Although every effort is made to provide accurate information, actual performance may vary from application to application. The designer is encouraged to review the latest documentation, available on the Texas Instruments Web site, and to do the necessary development testing to obtain the best results from the TRF6901.

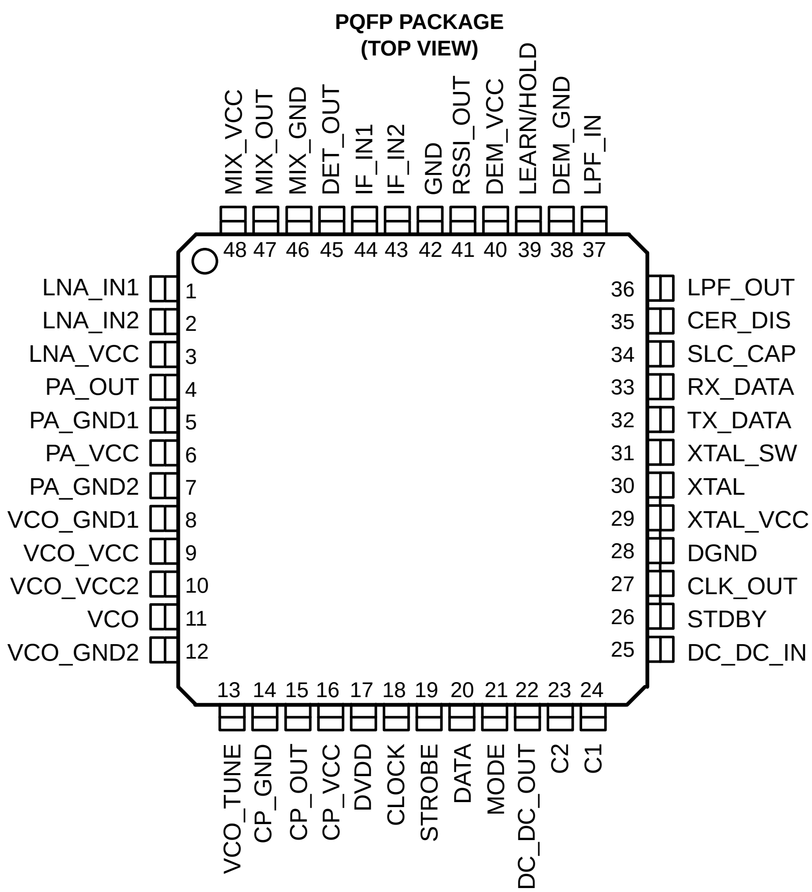


Figure 1. TRF6901 PQFP Package

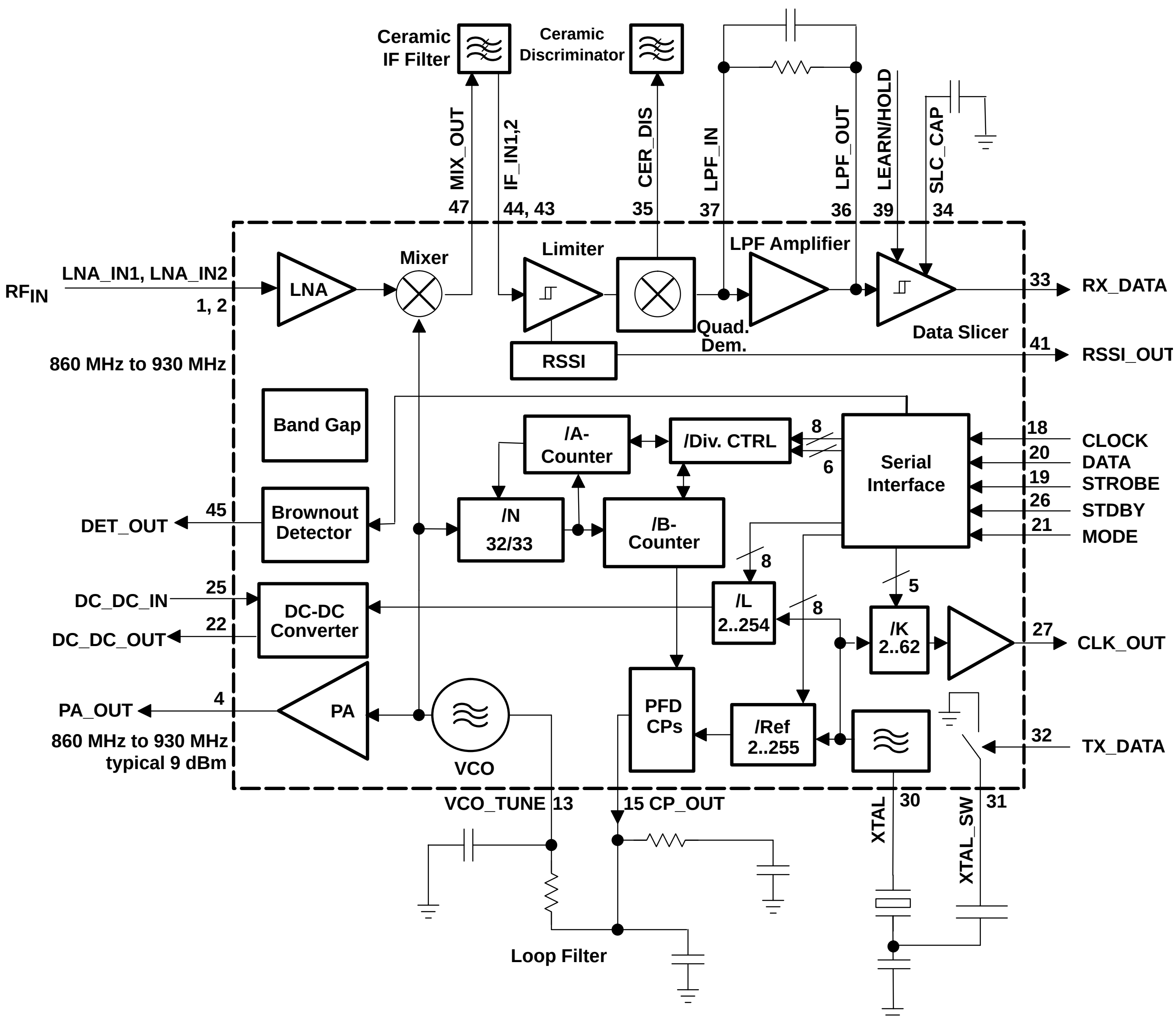


Figure 2. Functional Block Diagram

2 Initial Design

2.1 Design Flow

- Select the data rate, coding scheme, and modulation. Consider design complexity, performance, and cost tradeoffs. Determine components for RF matching networks, loop filter, post-detect low-pass filter, sample-and-hold capacitor. Do board layout for the engineering phase.
- Set up transmit section. Set up receive section. Test transmit and receive sections separately. Set up and test data link with cabled connection. Test wireless link with antennas and associated matching networks.

- Make modifications to production layout based on engineering test, characterization data, and production yield, centering and process requirements.

2.2 Design Complexity

The designer first determines the design complexity necessary to implement the system, chooses a data rate and coding scheme, and determines the number of required frequency channels.

Wireless transceiver designs can be loosely classified into three groups according to performance and design complexity. Simple designs are often characterized by low data rates (10 kbps), very low cost targets, and short transmission ranges (under 100 m). Cost is the primary driver in making design choices.

Complex designs have higher performance goals that may include higher data rates or longer transmission ranges (over 100 m). Performance largely determines design choices.

Intermediate designs fall between the two extremes, where additional system costs are carefully traded against the benefits of increased performance.

2.3 Data Coding

The choice of coding scheme has important implications for several parts of the transceiver design, including loop filter bandwidth, frequency deviation, and operating the TRF6901 in learn and hold modes.

Systems with low data rates (2.4 kbps to around 30 kbps) are often implemented with Manchester coding, in which a 1 is signified by a voltage transition from high to low, and a 0 is signified by a transition from low to high. There is a voltage change every bit (or symbol) period, hence the dc content of the data is zero or constant. In FSK systems, this means that the bit rate is the same as the rate at which the transmitter toggles between frequencies (symbol rate, data rate, or frequency modulation rate). If Manchester coding is used, the TRF6901 can be operated in the learn or hold modes when receiving data. The training sequence, used during the learn mode, is still required to establish a reference voltage at the sample-and-hold capacitor.

Systems with data rates higher than 30 kbps are often implemented with unipolar nonreturn-to-zero (NRZ) coding, in which a 1 is represented by a voltage high and 0 by a voltage low or zero volts. There is a voltage change only when the data changes from one to zero or vice versa, hence the voltage content of the bit stream and the frequency modulation rate depends on the data content. In FSK systems, this means that the bit rate is about twice the maximum frequency modulation rate. If NRZ coding is used, the TRF6901 must be operated in the learn mode while receiving the training sequence, and then the TRF6901 must be switched to the hold mode while receiving data.

There are other coding schemes in use, but many designers choose either Manchester or NRZ. Manchester- and NRZ-coding waveforms are shown in Figure 3.

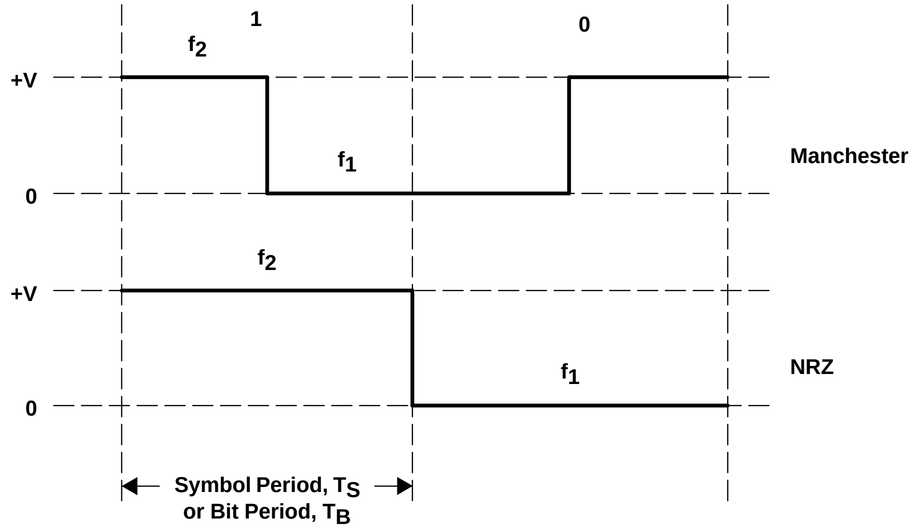


Figure 3. Manchester and Nonreturn-to-Zero Coding

2.4 FSK Coding Equations

For 2-FSK, we define

$B_L \equiv$ bandwidth of loop filter

$f_B \equiv$ bit rate, or rate of data transfer (bps)

$f_M \equiv$ frequency modulation rate, symbol rate, or maximum rate at which FSK frequencies are toggled, also sometimes called the data rate (Hz)

$T_S \equiv$ symbol period or bit period = T_B

then, for Manchester coding,

$B_L \approx f_M$

$f_M = f_B$

$T_B = T_S = 1/\ f_M$

and for NRZ coding,

$B_L \approx 1/2 \times f_B$

$f_M = 1/2 \times f_B$

$T_B = T_S = 1/2 \times 1/f_M$

2.5 Frequency Channels

Many system designs are single-channel and do not require multiple transmit-receive frequencies. Many designers plan for multiple channels, if for no other reason than to be able to avoid potential RF interference. There are several aspects to determining the spacing of frequency channels: the TRF6901 frequency-tuning ability, the external IF filter roll-off characteristic, and the requirement for out-of-band or adjacent-channel signal rejection.

The TRF6901 RF VCO is controlled by an integer-N phase-locked loop (PLL). This means that the TRF6901 can generate RF frequencies only at integer multiples of the PLL reference frequency, which is user-selectable and in typical use ranges from 100 kHz to 800 kHz. Therefore, the RF channel spacing must be an integer multiple of the PLL reference frequency.

The IF filter bandwidth and rolloff also influence the minimum channel spacing. The TRF6901 evaluation module (EVM) employs an external ceramic IF filter which has a nominal 3-dB bandwidth of 330 kHz. Outside of the pass band, the filter attenuation rapidly increases (rolloff characteristic). Channels must be spaced far enough apart so the IF filter adequately attenuates RF signals in an adjacent active channel.

3 Setting Up the PLL and Transmit Section

The voltage controlled oscillator (VCO) is both the RF frequency source for the transmit amplifier and the local oscillator (LO) for the receive mixer. Setting up the PLL and transmit section is a key first step in configuring the TRF6901 for use. Figure 4 is a PLL block diagram.

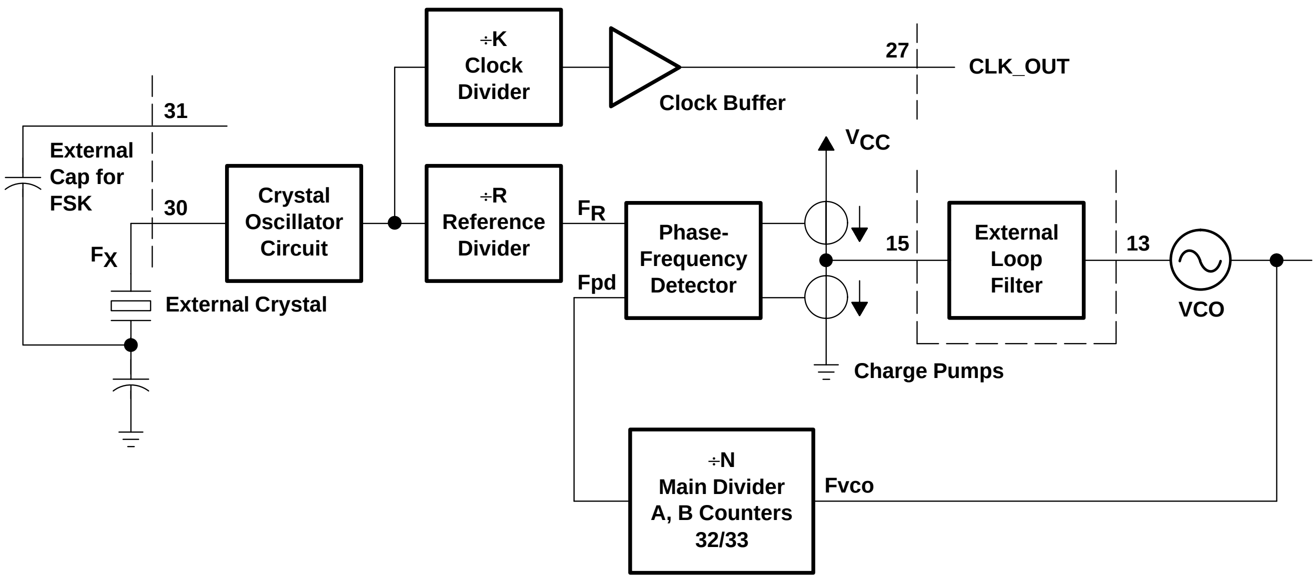


Figure 4. Integer-N Phase-Locked-Loop Block Diagram

3.1 Loop Filter

As a general rule, the loop filter bandwidth should be at least 1.2 times the data rate (frequency modulation rate), and 20% or less of the reference frequency. The normal setting for the charge pump current is 0.5 mA, which should suffice for most applications. Increasing the charge pump current reduces lock time and extends the bandwidth of a given loop filter.

An integer-N PLL has spurs in the RF output at integer multiples of the reference frequency; these are attenuated by the rolloff characteristics of the loop filter. The wider the loop filter bandwidth, the higher the spur levels for a given reference frequency. Normally, the reference spurs should be attenuated about 50 dB below the peak RF signal level to meet regulations. A wide loop filter also allows more noise into the RF signal.

A wide-bandwidth loop filter and/or high reference frequency allows faster lock time. This is important not only for quickly changing from one channel frequency to the next, but also for relocking the PLL as the FSK frequency is toggled when sending data. Lock time is longer for a frequency step of 1 to 10 MHz (changing channels) than for a step of 60 kHz to 100 kHz (FSK modulation). During modulation, the PLL should relock within 10% to 50% of the time spent at one frequency.

3.2 Loop Filter and VCO Equations

B_L ≡ bandwidth of loop filter

f_R ≡ PLL reference frequency

f_M ≡ modulation rate, symbol rate, or maximum rate at which FSK frequencies are toggled, also sometimes called the data rate

K_P ≡ phase-frequency detector gain

I_{CP} ≡ charge pump current (user selectable at 0.25, 0.50, 1.00 mA)

K_{VCO} ≡ VCO gain, design value is approximately 110 MHz/V

then,

$B_L \approx 1.2 \times f_M$ (wider bandwidth for design margin)

$B_L \approx f_R / 5$

$f_R \approx 6 \times f_M$

$K_P = I_{CP} / 2\pi$

3.3 Example Loop Filters

Loop filters are listed in Table 1 by 3-dB bandwidth, which roughly corresponds to the maximum FSK frequency modulation rate. As a general rule, the 3-dB bandwidth should be at least 1.2 times the modulation rate to allow for component variation. The TRF6901 was designed to support up to 64 kbps. Higher data rates may be possible by widening the loop filter, increasing the charge pump current, and using the highest practical reference frequency. Performance is a trade-off between spur rejection (narrow loop filter) and fast lock time (wide loop filter, high charge pump current). A high reference frequency contributes both to spur rejection and fast lock time at the expense of the number of available frequency channels.

Data rates at or above 30 kbps should probably be implemented with NRZ coding. The loop filters for data rates implemented with NRZ have design bandwidths that are approximately half of the data rate.

The low-pass post-detect filter and sample-and-hold capacitor values also must be adjusted according to the frequency modulation rate. These topics are covered in Section 4.3 and Section 4.4. The loop filter schematic in Figure 5 shows the component designators for which the values in Table 1 are listed.

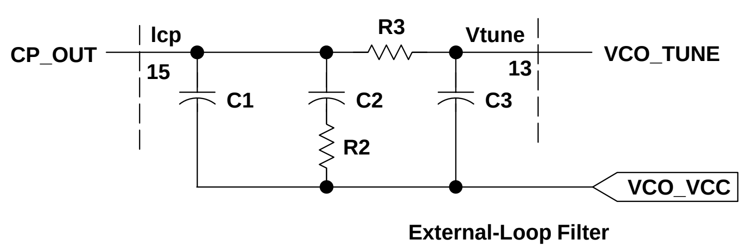


Figure 5. Loop Filter Configuration

Table 1. Loop Filter Components and Typical Performance for Various Design Bandwidths†

LOOP FILTER DESIGN BW, kHz	5	10	20	30	40	50
Data rate, kbps, Manchester	5	10	20	30	40	50
Data rate, kbps, NRZ	10	20	40	60	80	100
Reference frequency, kHz	222	190	444	444	667	667
Charge pump current, mA	0.25	0.5	0.5	0.5	0.5	0.5
R2, kΩ	5.6	10	8.2	12	16	20
C2, pF	15000	5600	3300	1500	820	510
C1, pF	1000	390	200	100	56	36
R3, kΩ	12	20	18	27	36	47
C3, pF	390	160	91	47	24	15
Reference spurs, dBc	–55	–52	–50	–51	–49	–49
Phase noise, dBc/Hz	–57	–63	–68	–71	–73	–73
Lock time, µs	60	60	12	10	8	6
Turnaround time, µs	650	350	175	100	80	60
Standby to Tx/Rx, µs	900	900	800	800	800	800

† The reference designators C1, R2, C2, R3, and C3 refer to Fig. 5 above; they correspond respectively to the following reference designators in the TRF6901 data sheet: C44, R19, C49, R14, and C36.

NOTE: The reference frequencies for most of the loop filters are higher than the design reference frequency, in order to maximize spur suppression and reduce lock time. The 3-dB bandwidth is increased by a higher operating reference frequency. Phase noise was measured at an offset equal to the design loop bandwidth. Lock times are for a typical 80-kHz step as the TX_DATA terminal is toggled. Turnaround time is the longest time observed for mode switching, from transmit to receive or vice-versa. Actual performance may differ due to component variance or other factors.

3.4 Reference Frequency

There are two restrictions on the reference frequency. At the transmitter, the desired RF output signal (CW, with the TX_DATA terminal low) must be an integer multiple of the transmitter reference frequency. At the receiver, the VCO must be set 10.7 MHz above or below the transmitted RF signal, and this also must be an integer multiple of the receiver reference frequency. The transmitter and receiver do not have to use the same reference frequency as long as the 10.7 MHz IF signal can be produced at the receive mixer, but virtually all systems do use the same reference frequency.

The default external crystal frequency for the TRF6901 EVM is 20 MHz. When both transmitter and receiver use the same crystal frequency and reference divider, not all reference frequencies provide down-converted IF signals that are close enough to 10.7 MHz to fit into the IF filter bandwidth. A reference divider of 200 gives an IF frequency of exactly 10.7 MHz. Some of the reference dividers that generate an IF frequency very close to 10.7 MHz are 43, 58, 71, 86, 99, 101, 114, 129, and 157.

In FSK operation, the average of both transmit frequencies should be centered in the IF bandwidth at 10.7 MHz and offset from 10.7 MHz by about half of the total frequency deviation. Example reference dividers that place a transmit signal 30 to 50 kHz below 10.7 MHz are 30, 45, 60, 77, 90, 107, 137, 165, and 195. Other reference dividers can be chosen to place the IF frequency above 10.7 MHz for systems using high-side LO injection; frequency alignment should be done with the TX_DATA terminal set high. Example reference dividers that place a transmit signal 30 to 70 kHz above 10.7 MHz are 26, 41, 54, 67, 80, 95, 108, 121, 136, 160, and 188. The designer should check all possible integer reference dividers to find the reference frequency that best suits the design goals. Table 2 is a partial list of reference dividers; Table 3 is a longer listing with fewer details about each divider.

The designer can change the crystal frequency in order to minimize the IF centering error for a desired reference frequency. If the crystal frequency is changed significantly, the operation of the TRF6901 must be checked, because many subcircuits are clocked at the crystal frequency.

Table 2. Partial List of Reference Dividers†

REFERENCE DIVIDER	REFERENCE FREQUENCY, kHz	IF CENTER/REF. FREQUENCY	FRACTIONAL REMAINDER, IF/REF. FREQUENCY	LOWEST FRACTIONAL ERROR	IF OFFSET FROM 10.7 MHz, kHz
60	333.333	32.100	0.100	–0.100	–33.3
61	327.869	32.635	0.635	0.365	119.7
62	322.581	33.170	0.170	–0.170	–54.8
63	317.460	33.705	0.705	0.295	93.7
64	312.500	34.240	0.240	–0.240	–75.0
65	307.692	34.775	0.775	0.225	69.2
66	303.030	35.310	0.310	–0.310	–93.9
67	298.507	35.845	0.845	0.155	46.3
68	294.118	36.380	0.380	–0.380	–111.8
69	289.855	36.915	0.915	0.085	24.6
70	285.714	37.450	0.450	–0.450	–128.6
71	281.690	37.985	0.985	0.015	4.2
72	277.778	38.520	0.520	0.480	133.3
73	273.973	39.055	0.055	–0.055	–15.1
74	270.270	39.590	0.590	0.410	110.8
75	266.667	40.125	0.125	–0.125	–33.3
76	263.158	40.660	0.660	0.340	89.5
77	259.740	41.195	0.195	–0.195	–50.6

† Dividers with resulting IF offsets from 10.7 MHz center frequency, assuming 20-MHz external crystal frequency and no other sources of frequency error.

Table 3. Reference Frequencies and IF Offsets for Various Reference Dividers (20-MHz Crystal Frequency)

REF DIV	REF FREQ kHz	IF OFFSET kHz	REF DIV	REF FREQ kHz	IF OFFSET kHz
20	1000.000	300.0	60	333.333	–33.3
21	952.381	–223.8	61	327.869	119.7
22	909.091	209.1	62	322.581	–54.8
23	869.565	–265.2	63	317.460	93.7
24	833.333	133.3	64	312.500	–75.0
25	800.000	–300.0	65	307.692	69.2
26	769.231	69.2	66	303.030	–93.9
27	740.741	–329.6	67	298.507	46.3
28	714.286	14.3	68	294.118	–111.8
29	689.655	334.5	69	289.855	24.6
30	666.667	–33.3	70	285.714	–128.6
31	645.161	267.7	71	281.690	4.2
32	625.000	–75.0	72	277.778	133.3
33	606.061	209.1	73	273.973	–15.1
34	588.235	–111.8	74	270.270	110.8
35	571.429	157.1	75	266.667	–33.3
36	555.556	–144.4	76	263.158	89.5
37	540.541	110.8	77	259.740	–50.6
38	526.316	–173.7	78	256.410	69.2
39	512.821	69.2	79	253.165	–67.1
40	500.000	–200.0	80	250.000	50.0
41	487.805	31.7	81	246.914	–82.7
42	476.190	–223.8	82	243.902	31.7
43	465.116	–2.3	83	240.964	–97.6
44	454.545	209.1	84	238.095	14.3
45	444.444	–33.3	85	235.294	–111.8
46	434.783	169.6	86	232.558	–2.3
47	425.532	–61.7	87	229.885	104.6
48	416.667	133.3	88	227.273	–18.2
49	408.163	–87.8	89	224.719	86.5
50	400.000	100.0	90	222.222	–33.3
51	392.157	–111.8	91	219.780	69.2
52	384.615	69.2	92	217.391	–47.8
53	377.358	–134.0	93	215.054	52.7
54	370.370	40.7	94	212.766	–61.7
55	363.636	–154.5	95	210.526	36.8
56	357.143	14.3	96	208.333	–75.0
57	350.877	–173.7	97	206.186	21.6
58	344.828	–10.3	98	204.082	–87.8
59	338.983	147.5	99	202.020	7.1

Table 3. Reference Frequencies and IF Offsets for Various Reference Dividers (20-MHz Crystal Frequency) (Continued)

REF DIV	REF FREQ kHz	IF OFFSET kHz	REF DIV	REF FREQ kHz	IF OFFSET kHz
100	200.000	–100.0	143	139.860	69.2
101	198.020	–6.9	144	138.889	–5.6
102	196.078	84.3	145	137.931	58.6
103	194.175	–20.4	146	136.986	–15.1
104	192.308	69.2	147	136.054	48.3
105	190.476	–33.3	148	135.135	–24.3
106	188.679	54.7	149	134.228	38.3
107	186.916	–45.8	150	133.333	–33.3
108	185.185	40.7	151	132.450	28.5
109	183.486	–57.8	152	131.579	–42.1
110	181.818	27.3	153	130.719	19.0
111	180.180	–69.4	154	129.870	–50.6
112	178.571	14.3	155	129.032	9.7
113	176.991	–80.5	156	128.205	–59.0
114	175.439	1.8	157	127.389	0.6
115	173.913	82.6	158	126.582	59.5
116	172.414	–10.3	159	125.786	–8.2
117	170.940	69.2	160	125.000	50.0
118	169.492	–22.0	161	124.224	–16.8
119	168.067	56.3	162	123.457	40.7
120	166.667	–33.3	163	122.699	–25.2
121	165.289	43.8	164	121.951	31.7
122	163.934	–44.3	165	121.212	–33.3
123	162.602	31.7	166	120.482	22.9
124	161.290	–54.8	167	119.760	–41.3
125	160.000	20.0	168	119.048	14.3
126	158.730	–65.1	169	118.343	–49.1
127	157.480	8.7	170	117.647	5.9
128	156.250	–75.0	171	116.959	–56.7
129	155.039	–2.3	172	116.279	–2.3
130	153.846	69.2	173	115.607	51.4
131	152.672	–13.0	174	114.943	–10.3
132	151.515	57.6	175	114.286	42.9
133	150.376	–23.3	176	113.636	–18.2
134	149.254	46.3	177	112.994	34.5
135	148.148	–33.3	178	112.360	–25.8
136	147.059	35.3	179	111.732	26.3
137	145.985	–43.1	180	111.111	–33.3
138	144.928	24.6	181	110.497	18.2
139	143.885	–52.5	182	109.890	–40.7
140	142.857	14.3	183	109.290	10.4
141	141.844	–61.7	184	108.696	–47.8
142	140.845	4.2	185	108.108	2.7

Table 3. Reference Frequencies and IF Offsets for Various Reference Dividers (20-MHz Crystal Frequency) (Continued)

REF DIV	REF FREQ kHz	IF OFFSET kHz	REF DIV	REF FREQ kHz	IF OFFSET kHz
186	107.527	52.7	194	103.093	21.6
187	106.952	–4.8	195	102.564	–33.3
188	106.383	44.7	196	102.041	14.3
189	105.820	–12.2	197	101.523	–40.1
190	105.263	36.8	198	101.010	7.1
191	104.712	–19.4	199	100.503	–46.7
192	104.167	29.2	200	100.000	0.0
193	103.627	–26.4			

3.5 Frequency Deviation

The amount of frequency shift during binary FSK, termed the frequency deviation, can be expressed either as a total deviation (difference between the two frequencies) or as a plus/minus deviation (amount of deviation from the arithmetic mean of the two frequencies). The amount of deviation required for a given application depends on the data (modulation) rate, and, to a lesser degree, on the frequency jitter of the transmit/receive VCOs, and on the linearity/sensitivity of the receiver data slicer. The mean of the two down-converted FSK transmitter frequencies must be centered in the 10.7-MHz IF bandwidth.

The modulation index is a measure of the total deviation as a fraction of the FSK center frequency, and is calculated by dividing the frequency deviation by the modulating data rate. As a general rule, and according to communications theory, the modulation index should be about one. If the deviation is too small, the signal to noise ratio deteriorates and the data slicer may have trouble delivering accurate decisions, driving up bit error rate. If the deviation is too large, the FSK frequencies may not fit into the IF filter bandwidth. Excessive IF bandwidth allows more noise into the demodulated signal. Large deviations incur longer lock times, which may not be fast enough for very high data rates. In practice, the total static frequency deviation that the designer chooses should be between approximately 60 kHz and 120 kHz. For modulation rates up to 30 kHz, 80 kHz of static deviation is sufficient. For higher data rates, more frequency deviation is required to satisfy communication theory.

3.6 IF Bandwidth Equations

For 2-FSK, we define

$h \equiv$ digital modulation index

$f_1 \equiv$ first FSK frequency, lower value

$f_2 \equiv$ second FSK frequency, higher value

$f_D \equiv$ total frequency deviation

$\Delta_F \equiv$ half of the total frequency deviation

$f_C \equiv$ FSK center frequency

$f_M \equiv$ modulation rate, symbol rate, or maximum rate at which FSK frequencies are toggled, sometimes called the data rate

$B_{IF} \equiv$ bandwidth of IF filter

then,

$h = f_D / f_M$

$f_D = 2 \times \Delta_F$

$f_C = 1/2 \cdot (f_1 + f_2)$

Use Carson's rule for determining the IF filter width of a sinusoidal FM signal for FSK operation; it states

$B_{IF} = 2\,(1 + f_D)\,f_M$ (upper bound)

Another form of Carson's rule approximated for FSK operation is

$B_{IF} = 2\,(f_D + f_M)$

Although Carson's rule can be used to choose an IF bandwidth, the bandwidth is also determined by the IF filters available, the frequency deviation achievable by the TRF6901 switch capacitor, PLL lock time, and the error stack-up in placing the two FSK frequencies in the center of the IF band.

Another method for determining IF bandwidth is to add the frequency deviation to the modulation rate, and then add a discretionary amount of bandwdth for tolerance. An example of this method would be to add 100 kHz deviation to 32 kHz frequency modulation, and add 70 kHz for parts variance to yield an IF bandwidth of about 200 kHz.

3.7 Switch Capacitor

Frequency deviation during FSK operation is influenced by the switch capacitor (C22), Csw, connected to terminal 31 (see Figure 6), and also by the series capacitor (C24) connected to one terminal of the crystal and to ground. The frequency deviation decreases as the series capacitor value is increased, for a given switch capacitor value. Total frequency deviation is shown in Figure 7 as a function of series capacitance for different values of switch capacitor Csw.

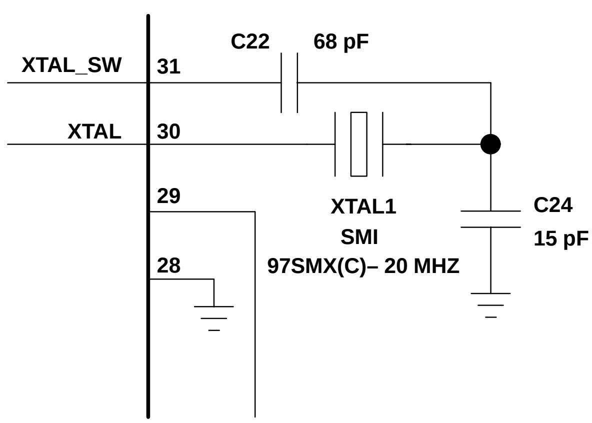


Figure 6. External Crystal, Switch Capacitor (C22), and Series Capacitor (C24)

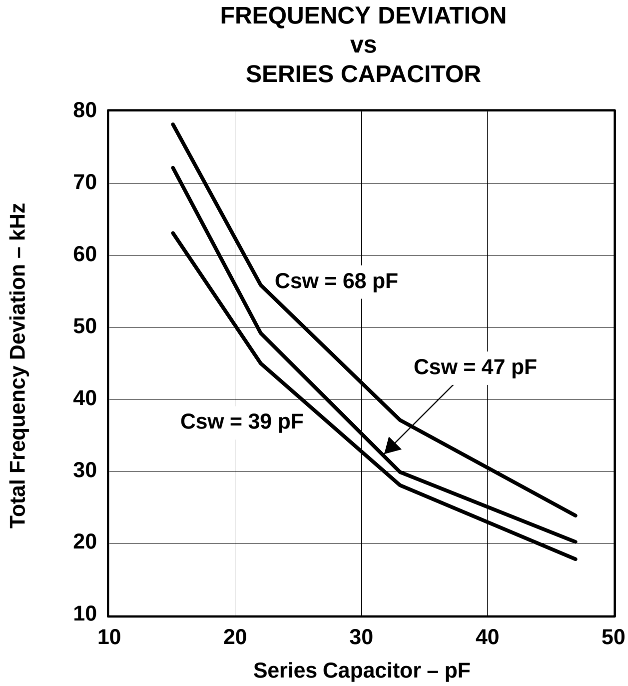


Figure 7. Frequency Deviation for Three Switch-Capacitor Values

3.8 Frequency Correction

Correcting the RF output frequency is done with the TRF6901 crystal tune feature. An internal user-selectable capacitor can be placed in shunt with the external reference crystal under the control of three bits in the serial word. This is normally done at assembly or production test and the correct value stored as part of the programming information for the unit. Frequency correction can also be done in hardware by adjusting a variable capacitor installed on the circuit board in shunt with the crystal.

3.9 Amplifier Harmonics

The RF output of the power amp may contain reference spurs at levels determined by the loop filter bandwidth. The RF signal also contains harmonics, at multiples of the fundamental RF frequency, that are produced by the nonlinear nature of semiconductor devices and amplifier circuit design. The second and third harmonics are usually attenuated to meet regulations through the use of a SAW filter, discrete LC filter, or harmonic traps. The filter must have low insertion loss in the RF pass band to avoid excess loss of signal.

4 Setting Up the Receive Section

During receive, the TRF6901 VCO provides the local oscillator (LO) frequency for the down-conversion mixer in the receive chain. The output of the mixer is a signal at the intermediate frequency (IF) of 10.7 MHz. The IF amplifier increases signal strength before the data are detected at the discriminator and data slicer.

4.1 Low- vs High-Side LO Injection

Setting the receive VCO for a frequency 10.7 MHz below the transmitted signal (nonmodulated CW frequency) results in noninverted data at the RX_DATA terminal. The receive VCO can also be set 10.7 MHz above the transmit signal, so that the receiver correctly down-converts and detects the data; however, the data is inverted at the output of the data slicer due to a phase shift through the mixer and IF amplifier stages.

4.2 Demodulation Discriminator

The discriminator, or resonator, is an external ceramic part that is tuned to the IF frequency and helps to detect the low-frequency data signal that is part of the IF amplifier output. This part is often custom-designed for various manufacturers' receivers, and is matched to the impedance of the IF amplifier. The discriminator can also be implemented with discrete components in a resonant parallel-RLC tank circuit (see Figure 8).

The discriminator center frequency is adjusted using three bits of the D word. The tuning bits are used to adjust the discriminator response for the parasitic effects of the circuit board. The tune bits control the size of a resistor in a bridge network. Increasing the tuning bits from D<14:12> = 000 toward D<14:12> = 111 decreases the resistor value and thus increases the center frequency of the discriminator response by a small amount. The suggested default setting of the demodulator tuning bits is D<14:12> = 110.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

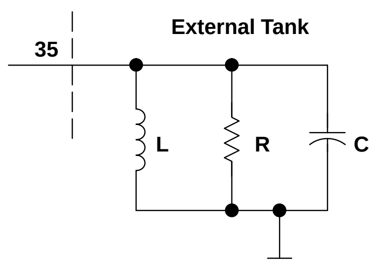


Figure 8. Discrete Element Implementation of Discriminator Circuit

4.3 Low-Pass Post-Detect Filter

The low-pass filter in the IF amplifier chain (see Figure 9) should have a bandwidth that is at least twice the data rate (frequency modulation rate). Table 4 lists component values for various data rates.

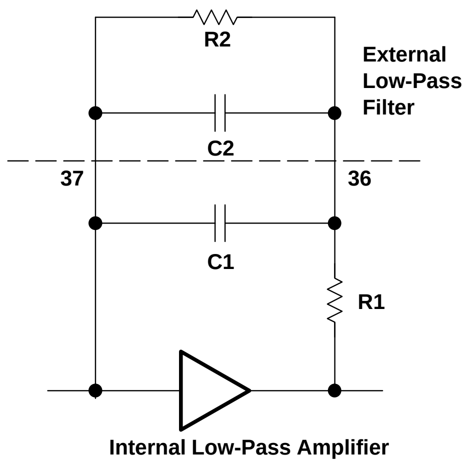


Figure 9. Post-Detect Low-Pass Filter

Table 4. Low-Pass Filter Components for Various Modulation (Symbol) Rates, or Loop Filter Bandwidths†

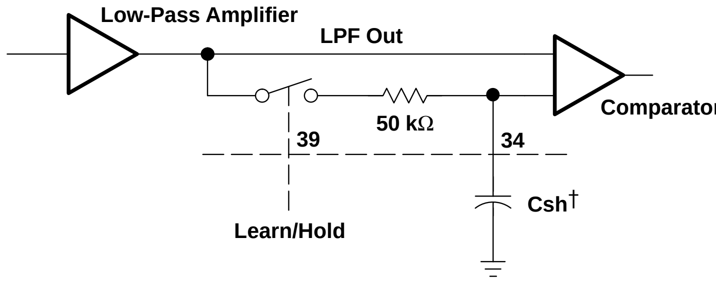
f_{3dB} (kHz)	5	10	20	30	40	50	60
R2 (kΩ)	220	220	220	220	220	220	220
C2 (pF)	150	68	33	22	15	12	10

† Reference designators R2 and C2 refer to Figure 9; the corresponding reference designators in the TRF6901 data sheet are R5 and C14, respectively.

4.4 Learn and Hold Modes

It is necessary to send a training sequence of alternating ones and zeros, with the TRF6901 in the learn mode, in order to establish a voltage reference at the sample-and-hold capacitor before the actual data are sent to the receiving unit.

When using Manchester (or other zero or constant dc) coding, the TRF6901 can remain in the learn mode or switch to the hold mode to receive the data that follow the training sequence. When using NRZ (or other nonconstant dc) coding, the TRF6901 must be switched to the hold mode before receiving data. During long data transmissions or after a long idle period, the sample-and-hold reference voltage may need to be re-established with another training sequence received in the learn mode. The sample-and-hold capacitor value should be chosen so that its RC time constant (with R = 50 kΩ) is approximately five times the bit period. The bit period is the inverse of the symbol rate, or frequency modulation rate. See Figure 10.



†External Sample-and-Hold Capacitor
$Csh \cong 5 \times T_B/50000$,
Where T_B Is the Bit Period

Figure 10. Data Comparator, Sample-and-Hold Capacitor

4.5 Intermediate Frequency Error

The IF filter bandwidth must be wide enough to accommodate the two FSK frequencies plus the total IF centering error. IF error can come from error in the crystal frequency (transmit or receive), LO frequency, or variances in the IF filter center frequency or bandwidth.

Crystals often have accuracy tolerances of around ±50 ppm; their frequency also drifts as a result of operating temperature or aging. More accurate crystals are available but they are more expensive. The TRF6901 has the capability to adjust the crystal frequency by about 50 kHz through the use of the internal tuning capacitors. The amount of correction is quasi-linear; a step up in capacitance lowers the crystal frequency by about 10 kHz to 15 kHz. It should be possible to trim the crystal frequency to within 10 kHz of the target value. The parasitic capacitance of the circuit board also has an effect on the crystal and VCO frequencies.

The tolerance of the IF filter depends on its design bandwidth; wider filters have greater variation.

An example check of the IF filter bandwidth might proceed by adding up the expected frequency variation from FSK operation and assorted errors for each half of the IF bandwidth. Many parts tolerances are stated (in the manufacturer's data sheet) as a plus/minus error for a given number of standard deviations from the population mean (manufactured lot). In a worst-case scenario, the plus/minus variations may go in opposite directions in transmit and receive units, adding together rather than canceling.

Half of the total frequency deviation (80 kHz):	40 kHz
Crystal trim error (tx + rx):	20 kHz
Crystal error from temperature, aging (tx+rx):	10 kHz
IF frequency error due to reference divider:	20 kHz
IF filter band-center tolerance:	50 kHz
Total, half of IF bandwidth:	140 kHz
Total, expected IF bandwidth:	280 kHz

In this example, a 330-kHz IF filter has 50 kHz of extra bandwidth.

4.6 Design Example

In this example, we review the TRF6901 setup for a 32-kbps FSK application using NRZ coding. Designers typically regard data rate as the amount of information to be transmitted, so here we use the term *modulation rate* rather than the term *data rate*.

NRZ coding at 32 kbps means the maximum FSK modulation rate through the loop filter will be 16 kHz. Choose a somewhat wider loop filter bandwidth. Table 1 shows the components for a third-order 20-kHz filter, at 0.5-mA charge pump current. The component values are 8.2 kΩ, 3300 pF, 200 pF, 18 kΩ, and 82 pF.

The switch capacitor sets the static frequency deviation; a 68-pF capacitor gives about 70 kHz of static frequency deviation, which is adequate for the symbol rate of 16 kHz.

The suggested reference frequency for the loop filter is 333 kHz for a 20-MHz crystal and reference divider 60. So far, we assume that the reference frequency is low enough to provide enough frequency channels, and that the IF filter rolloff is adequate to suppress signals in adjacent frequency channels.

For low-side LO injection, a transmit/receive frequency pair in the North American ISM band might be 915.000 MHz transmit (main divider 2745) and 904.333 MHz receive (main divider 2713). With the TX_DATA terminal set low (0), the IF frequency is 915.000 – 904.333 = 10.667 MHz. This is 33 kHz lower than the center of the IF band at 10.7 MHz, or about half of the deviation. When the TX_DATA terminal is set high, the RF transmit frequency is 915.000 MHz + 70 kHz = 915.070 MHz. The second IF frequency is 915.070 – 904.333 = 10.737 MHz, about 37 kHz above the IF center frequency. So the two FSK frequencies are approximately centered in the IF band.

Stacking up frequency tolerances for half of the IF bandwidth, we add 40 kHz (deviation), 40 kHz (reference error, centering error, temperature drift, aging), 50 kHz (filter tolerance), for a total of 260 kHz. A 280 kHz IF filter may be wide enough to allow for production and performance tolerances and will give better signal suppression for adjacent channels than the next-higher bandwidth filter (330 kHz). If the adjacent channel suppression is inadequate, frequency channels may have to be spaced at every other increment of the reference frequency.

The table of post-detect low pass filter values (Table 4) for 20-kHz modulation lists 220 kΩ and 33 pF.

The calculation for the sample-and-hold capacitor gives 6250 pF; check a few values between 0.01 µF and 1000 pF to see if there is an appreciable effect on BER. The waveform at the LPF_OUT terminal can also be examined to see if the sample-and-hold capacitor is charging efficiently for the training sequence of alternating ones and zeroes.

Benchtop testing includes tests for which crystal tune and demodulation tune bits to set; every tune bit should be exercised and the appropriate effect noted. The output spectrum must be checked to see that the loop filter bandwidth and reference frequency adequately suppress reference spurs.

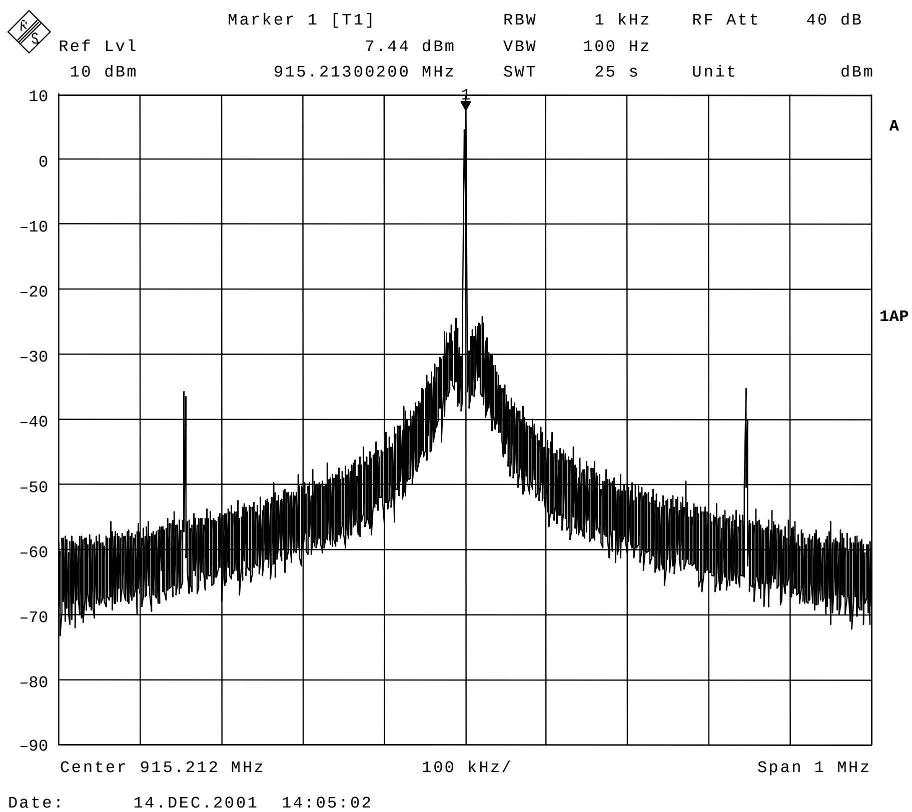
5 Operation and Troubleshooting

5.1 What to Look for in the Transmit Section

The RF output signal of the transmit amplifier should have only a single peak. There may be small spurs present, spaced at a frequency interval equal to the PLL reference frequency. The principal harmonics from the power amp are at two and three times the fundamental frequency.

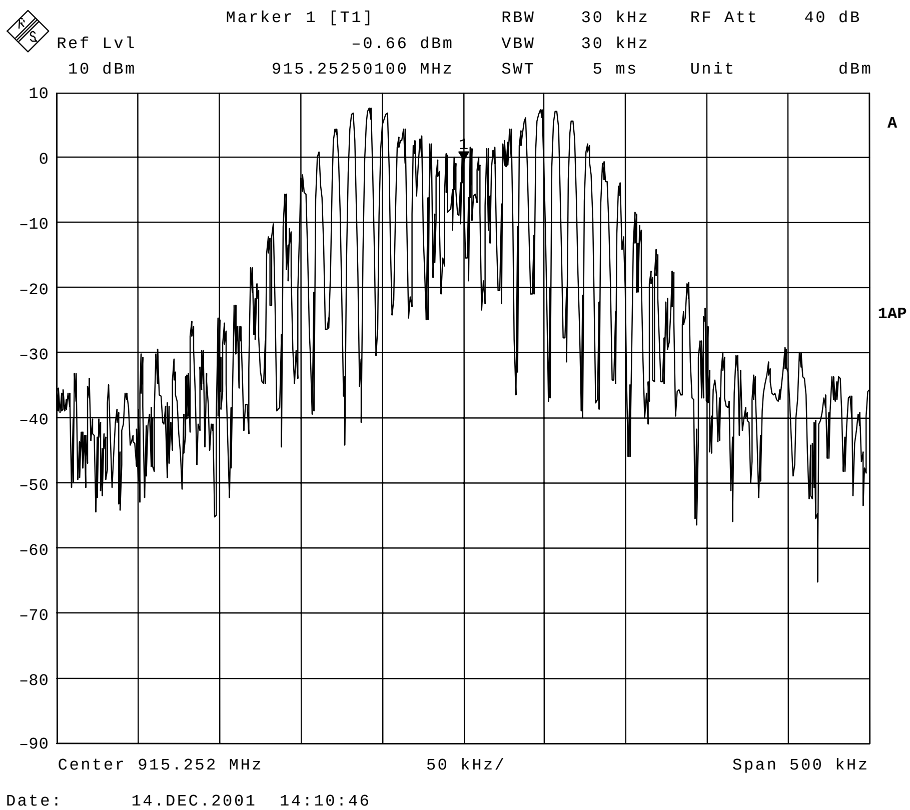
The FSK signal is examined on a spectrum analyzer by putting a 0-to-1.5-V square wave into the TX_DATA terminal of the TRF6901 at the expected RF modulation frequency. The analyzer video bandwidth should be greater than the RF modulation rate in order to see the modulation envelope; there are two visible frequency peaks. The separation depends on the modulation index, the spectrum analyzer settings, the PLL lock time, and the loop filter damping.

The frequency shift observed when setting the TX_DATA terminal high or low differs depending on the rate at which TX_DATA changes. The static deviation (TX_DATA changing very slowly) may be lower or higher than the dynamic deviation (TX_DATA changing rapidly). There are several reasons for this: the spectrum analyzer display is affected by the resolution settings and sweep/sampling rate, the spectral content of the signal changes with the frequency modulation rate, and PLL overshoot/undershoot. The two FSK frequencies may shift (or skew) together up or down slightly in comparison with their static values.



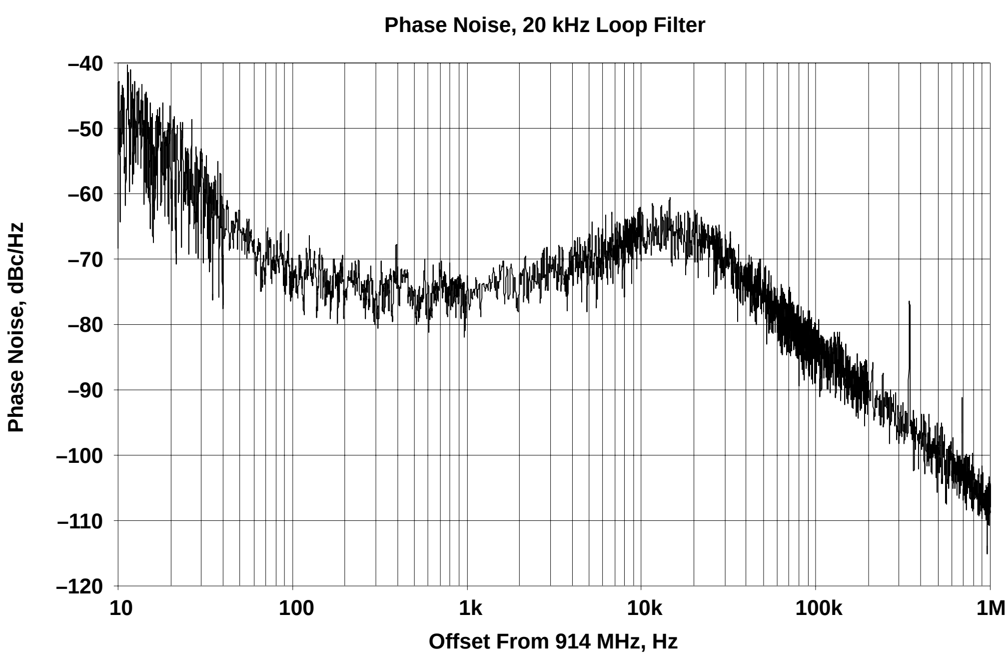
NOTE: Fundamental RF signal with reference frequency spurs offset 345 kHz to each side.

Figure 11. RF Spectrum, No Modulation



NOTE: Dynamic frequency deviation is about 100 kHz. Static frequency deviation is 70 kHz. Spectrum analyzer resolution bandwidth and video bandwidth have been set wider than the frequency modulation rate.

Figure 12. FSK Spectrum



NOTE: 20-kHz Loop Filter With 914-MHz Carrier, 0.5 mA Icp, 345-kHz Reference

Figure 13. Phase Noise Plot

5.2 What to Look for in the Receive Section

The receive section is tested first with the TRF6901 in learn mode and a CW (continuous wave, not modulated) RF signal. The RF signal at the mixer output should be 10.7 MHz. The IF filter performance can be checked by looking at the IF filter output while the LNA input signal is slowly adjusted in frequency. As the input signal is adjusted down in frequency, the mixer output signal increases slowly in frequency and diminishes in amplitude as the edge of the filter bandwidth is reached. The mean of the two expected FSK frequencies should be in the approximate center of the IF bandwidth.

The receive section is tested next with the TRF6901 in learn mode and the RF test signal modulated at the expected FSK data rate. The modulating waveform should be a square wave rather than a sinusoid. A sinusoid causes data jitter. The output of the low-pass post-detect filter should be a zero-centered square wave with amplitude between approximately 200 mV and 2 V peak-to-peak, depending on the input signal. The sample-and-hold capacitor should have a voltage that rises and falls with the FSK frequency. There should be a square wave present at the RX_DATA terminal that toggles between 0 V and V_{CC}.

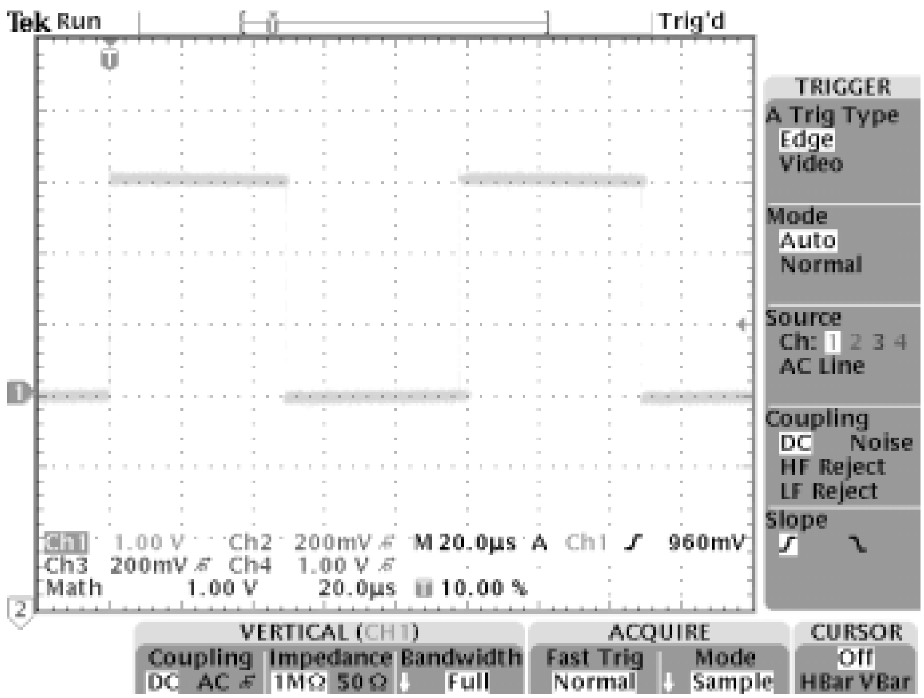


Figure 14. Oscilloscope Plot of RX_DATA Showing Demodulated Square Wave

5.3 Mode Switching and Lock Times

Standby to transmit/receive has been measured at 800 µs, typical, triggering on the standby line and determining the time to a stable power amplifier or IF signal.

Transmit/receive turnaround time has been measured at 300 µs, typical (20-kHz loop filter, 370-kHz reference, 0.5-mA Icp), triggering on the mode line and determining the time to a stable power amplifier or IF signal.

Frequency step time is influenced by the size of the frequency step and the PLL setup, including the reference frequency, loop filter bandwidth, and the charge pump current.

Determining lock time for transmit frequency modulation is somewhat subjective and there is some variance in the data. The effective lock time for the transceiver is the time to achieve a frequency shift that causes a reliable change of state in the receive data slicer. Frequency overshoot and ringing are not necessarily detrimental if the tuned frequency does not go near or back across the data slicer decision threshold. At high FSK data rates, the PLL may not have a chance to fully settle before the next symbol change, so the effective frequency deviation may be higher than a static measurement (measuring just one state change) would indicate. The minimum lock time for data transmission is often stated to be half of the symbol period, but there is some latitude in this requirement.

Some example lock time measurements are shown in Table 5, Table 6, and Figure 15.

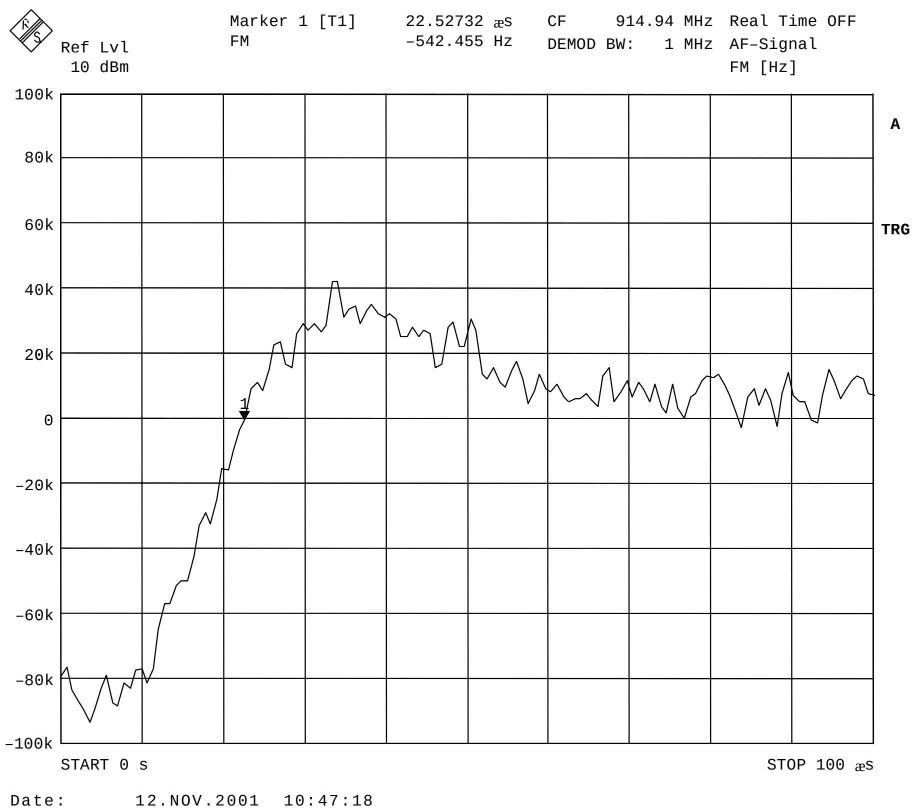
Table 5. Example Lock Times for Frequency Step, 10-kHz Loop Filter, Icp = 0.5 mA

REF. FREQ.	TYPICAL LOCK TIME, µs	
	~1 MHz STEP	~10 MHz STEP
100 kHz	600	800
200 kHz	300	400
400 kHz	200	300

Table 6. Example Lock Times for Frequency Step

FREQ. STEP	TYPICAL LOCK TIME, µs
10 MHz	100
800 kHz	50
60 kHz	20

NOTE: 20 kHz loop filter, Icp = 0.5 mA, 400-kHz reference frequency. Trigger on mode or tx_data



NOTE: Measurement for a 70–80-kHz step with 10-kHz loop filter, Icp = 0.5 mA, 370-kHz reference frequency. Lock time to zero error crossing is about 23 µs.

Figure 15. Example Lock Time Measurement

5.4 Using the DC-DC Converter

The dc-dc converter provides extra voltage to the VCO and PLL charge pumps as battery supply voltage drops below 2 V, extending the length of time the TRF6901 can operate. The converter supplies a low amount of current and is intended to power only the VCO and PLL portions of the TRF6901. When using the dc-dc converter, switching noise may need to be removed from the voltage output with an LC filter network. The VCO, PLL components, and RF amplifier bias networks are particularly sensitive to noise. Unwanted signals in these circuits usually cause degraded performance. The output of the dc-dc converter filter should have no ac component, or a weak component with less than 10 mV peak swing. The dc-dc converter is designed to work with a switching frequency of around 1 MHz or lower. Setting the converter divider ratio to a high value results in more power consumption, better regulation, and easier filtering of switching transients. Setting the divider to a low value results in less power consumption and more difficulty filtering noise from the output voltage.

If the dc-dc converter is not used, the dc-dc clock buffer divider register C[6:0] should be set to zero. Terminals 22 through 25 can be left open.

5.5 Low-Power Operation With Batteries

At low battery voltage, the power output of the transmitter amplifiers diminishes even though the dc-dc converter is operating. On-off (amplitude-shift) keying is often chosen for low data rate, low-power applications. Use the power amp attenuator to lower current consumption for short-range applications.

5.6 Using the Brown-Out Detector

The brown-out detector has four user-selectable voltage thresholds. A brown-out signal is used at the system level to issue warning messages or to make performance degradation or shutdown more graceful. A multinode network might reroute data or instructions to units that have more robust connections.

5.7 Using the External Clock Buffer

It is recommended that the buffer frequency be an even-integer divisor of the RF output frequency.

If the external clock buffer is not used, the clock buffer divider register C[12:8] should be set to zero and terminal 27 should be left open or terminated with a 50 Ω to 1 kΩ resistor to ground.

5.8 Common Issues

VCO does not lock. Some causes are incorrect loop filter component values, improper loop filter design, or charge pump current too low. One troubleshooting technique is to run the VCO open-loop, where the loop filter is removed and a stable dc voltage source is connected to terminal 13. The VCO operates from around 500 MHz almost to 1 GHz. With the loop closed (loop filter reinstalled), the tuning voltage into terminal 13 should be steady.

High reference spurs. Causes are wide loop filter bandwidth, low reference frequency, or high charge pump current.

Noise in RF output. Many causes; they include switching transients from switching regulator or TRF6901 dc-dc converter, inadequate power supply bypassing, RF leakage from other RF components or assemblies, coupling from digital signals into sensitive RF circuits, large unshielded inductors. Harmonics are not common noise; they are products of the nonlinear nature of the power amplifier, and often have to be attenuated with a SAW or discrete filter.

Low output power. Causes are inadequate power supply to the output stage of the transmit amplifier (in-line resistance or current limiting), or poor impedance matching with a SAW filter, RF switch, or antenna. Using a common RF port with no switch degrades output power by perhaps 3 dB to 6 dB.

Poor receive sensitivity. There are many possible causes, including improper impedance match to the filter, RF switch, or antenna, improper balun between LNA ports, poor match from mixer to IF filter, poor match from IF filter to IF amp, improper balun across IF amp terminals, FSK signals not centered in IF bandwidth, wrong low-pass filter bandwidth, detuned discriminator, inadequate frequency deviation, too-short training sequence, or wrong sample-and-hold capacitor value. Receive sensitivity problems are most often traced to poor impedance matching from the antenna to the LNA inputs, or IF centering problems.

Oscillation during OOK operation. Cause may be improper power amp impedance matching, current starvation in bias supply, inadequate supply bypassing, operation at very low temperatures.

5.9 Subtle Problems

Down-converted signals not centered at IF. Loss of receive sensitivity is the primary result of centering problems. Examine the frequency, coding, and modulation schemes.

Slow PLL lock time. Symptoms include low effective frequency deviation and high FSK bit error rate.

Timing issues in baseband software also can cause high bit error rates.

5.10 Enhancing Circuit Board Performance

Separate the traces for V_{CC}, logic, RF, and the VCO (loop filter). Reduce the potential crosstalk between major subcircuits. The loop filter and receive circuits are especially vulnerable to signal contamination.

Use adequate grounding, both for dc return, and to separate signal networks through the use of low-inductance ground planes and ground vias.

Use adequate bypassing on power supplies. Designers often use capacitors of varying values to bypass noise signals at varying frequencies. Capacitors have a resonant frequency above which they appear as an inductor and do not provide an adequate RF short to ground.

Use a board with 3 or 4 metalization layers. A four-layer board often has a layer for topside components and RF traces, a layer for RF ground, a power plane layer, and the fourth layer for analog components and some digital signals. Getting a two-layer board to work well is difficult, but it can be done. It is less expensive, and sometimes it is the only option for very low-cost systems.

Use 50-Ω traces for RF signals. Low-loss propagation of RF signals over distance depends on transmission line structures such as microstrip, stripline, or coplanar waveguide. When using FR4 as a board material, a 50-Ω microstrip line can be achieved with approximately 12 mils of substrate thickness and 14 mils of conductor width. Dimensions for a 50-Ω line vary by PCB manufacturer. Ground shields on the RF conductor layer should be kept away from RF lines by at least 3 substrate heights unless ground vias are used to prevent voltage discontinuities.

Use separable subcircuits to facilitate characterization and troubleshooting. There should be board access to circuits for data in, data out, RF transmit out, RF receive in, mixer out, IF filter out, VCO tuning voltage. Separate power supply networks for the TRF6901 from supply networks for other components such as LEDs, input buffers, etc. This layout approach is at odds with the compact, no-frills designs preferred for production. One approach is to have separate board layouts for engineering development and for production.

Use composite footprints wherever possible for components that are vendor dependent or may become hard to get, such as clock crystals, bandpass filters, ceramic capacitors, etc.

Minimize solder defects, particularly in circuits susceptible to small changes in dc values, such as the loop filter.

Use high-Q inductors in RF matching circuits for the LNA, PA, and in any discrete demodulation tank circuit. Consider putting shunt caps (100 pF to 1000 pF) on digital lines that change slowly, like mode and standby, in order to snub stray RF signals.

Use close-tolerance capacitors in RF matching circuits.

5.11 External Parts, Crystal, IF Filter, Discriminator

The default clock crystal for the TRF6901 EVM is 20 MHz. This should be a fundamental crystal rather than an overtone type and in a surface mount or through-hole package. The TRF6901 works with other clock frequencies that are close to 20 MHz, perhaps 16 to 24 MHz. Example crystals include SMI 97SMX, Citizen HCM49 and HC49US, and ICM HC45U.

Table 7. Example Crystal Information

CHARACTERISTIC	VALUE
Frequency tolerance	± 50 ppm
Operating temperature	–10 to 60°C
Load capacitance	18 pF
Shunt capacitance	7 pF
Drive level	100 μW
Aging (first year)	± 5 ppm max.

The IF filter commonly used is a Murata 10.7-MHz ceramic filter with a bandwidth of 330 kHz; the global part number is SFECV10.7MA2S-A-TC. The bandwidth is wide to accommodate extra IF centering error that may be encountered with integer-N PLLs. The narrower 280 kHz IF filter can also be used (SFECV10M7FA00-R0). Very wide IF filters allow more noise into the demodulation and detection circuits.

Murata discriminator (resonator) CDACV10M7GA001 was not specifically designed for the TRF6901 but works well. Discriminator CDSCA10M7GA119-R0 has reduced temperature drift and is optimized for the TRF6901.

5.12 Commonly Used Test Equipment

Following is a list of test equipment used for ISM wireless applications, although one could get by with equivalent instruments, or fewer instruments. Producing a successful design without using an oscilloscope, a spectrum analyzer, and function generator would be difficult.

Spectrum analyzer, HP 8560E, 30 Hz–2.9 GHz, with phase noise option. Used to examine RF transmit and IF signals, spurs, harmonics, loop filter bandwidth and phase noise, etc.

High-frequency probe, HP 85024A, 300 kHz–3 GHz. Use to examine RF signals on circuits not equipped with SMA connectors, such as MIX_OUT, the IF filter output, etc. The HF probe cannot be used to make very accurate or repeatable RF power measurements, but it can be used to trace large amounts of gain or loss in RF circuits, or to look for spurious signals within its measurement bandwidth.

Oscilloscope, Tektronix 2465B, 400 MHz, or Tektronix digital storage oscilloscope TDS 3054, 500 MHz, 5 GS/s. Use to examine the TX_DATA and RX_DATA terminals, post-detect signal, sample-and-hold capacitor, noise on power supplies, etc.

Oscilloscope probes, Tektronix P6137 or P6139A. Two probes are useful for measuring input and output waveforms.

Frequency counter, HP 5347A, 10 Hz–20 GHz, or Agilent 53131A, 200 MHz–5 GHz. Use to measure output frequency precisely, determine frequency corrections and check for large harmonic signal components.

Function generator, HP 8116A, 50 MHz, or Agilent 33250A, 80 MHz. Use to generate square-wave TX_DATA signal.

Signal generator, Rohde & Schwarz SMT03, 5 kHz–3 GHz. Use to generate FSK test signals at RF frequencies with known modulation and deviation to test receiver function.

Vector network analyzer, HP 8753D, 30 kHz–6 GHz. Used to measure complex input, output impedances, harmonics. Calibration standards should be included.

Power supplies, HP E3610A, 15 V, 2 A, or Agilent E3610A, 15 V, 2 A.

Multimeter for current and voltage measurements.

5.13 Transmit-Only or Receive-Only Operation

If the TRF6901 is used for transmit-only operation, the power supply connections to the receive circuits (terminals 3 and 48) should be left open. Terminal 40, DEM_VCC, should be left connected to V_{CC} to power the band-gap reference. Terminals 38, 42, and 46 should be connected to ground. Terminals 1, 2, 33–37, 39, 41, 43, 44, and 47 can be left open or terminated with 50 Ω to 1 kΩ resistors to ground.

If the TRF6901 is used for receive-only operation, terminal 6 (PA_VCC) can be left open. Terminals 4 and 32 can be left open or terminated in 50 Ω to 1 kΩ resistors to ground. However, to provide an RF test point for adjusting the VCO, it is useful to leave the power amplifier connections in their normal configuration.

6 Advanced Topics

6.1 Antenna Interface

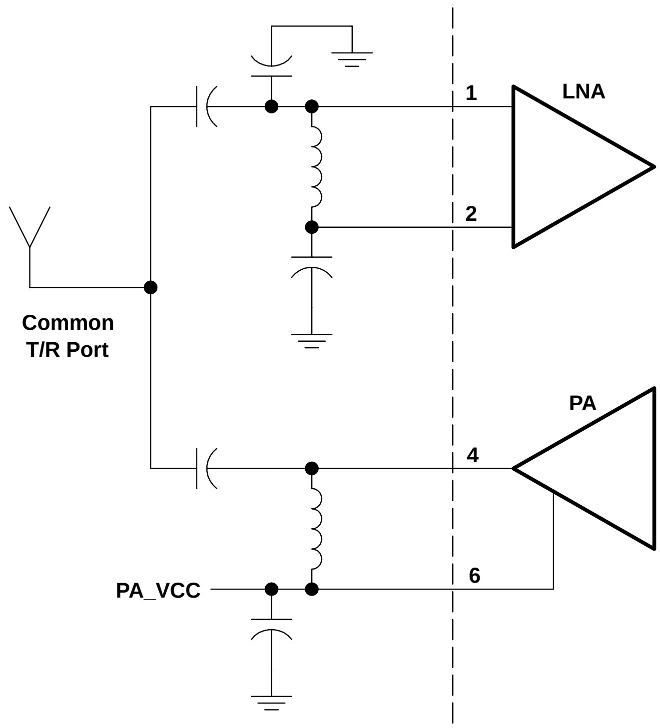
Many wireless systems have one antenna without a transmit-receive (TR) switch or circulator due to cost constraints. This is an acceptable design approach, but there is usually a reduction in transmit output power and receive sensitivity due to the difficulty of achieving a simultaneous impedance match to the antenna for both transmit and receive paths in the on and off states. Transmit power and receive sensitivity are degraded by as much as 3 dB to 5 dB.

One expedient method to implement the common port is simply to tie the individual transmit and receive circuits together, making sure each path has a series capacitor to dc-block the receive low-noise amplifier input and transmit power amplifier output (see Figure 16). The impedance match can be improved somewhat by taking s-parameter measurements of each path in the on and off states and adjusting the matching circuit component values to achieve the best compromise match. Even with a good compromise match, some power is always lost in the off path instead of being transferred to/from the antenna. Using a single-pole, double-throw switch allows a good impedance match between the antenna and the transmit path or receive path (see Figure 17).

With one transmit/receive antenna, a SAW filter can be next to the antenna where it is common to both transmit and receive paths. In this position it attenuates amplifier harmonics and out-of-band noise in the received signal, but receive sensitivity and noise figures are degraded by the insertion loss of the filter. An alternative approach is to use a SAW filter in the transmit path and a separate low-loss low-pass or band-pass filter in the receive path (see Figure 18). If out-of-band interference is expected to be low, a SAW or discrete filter can be used alone in the transmit path. Some common-antenna systems use diplexers, but these are suited to systems with widely separated transmit and receive frequencies.

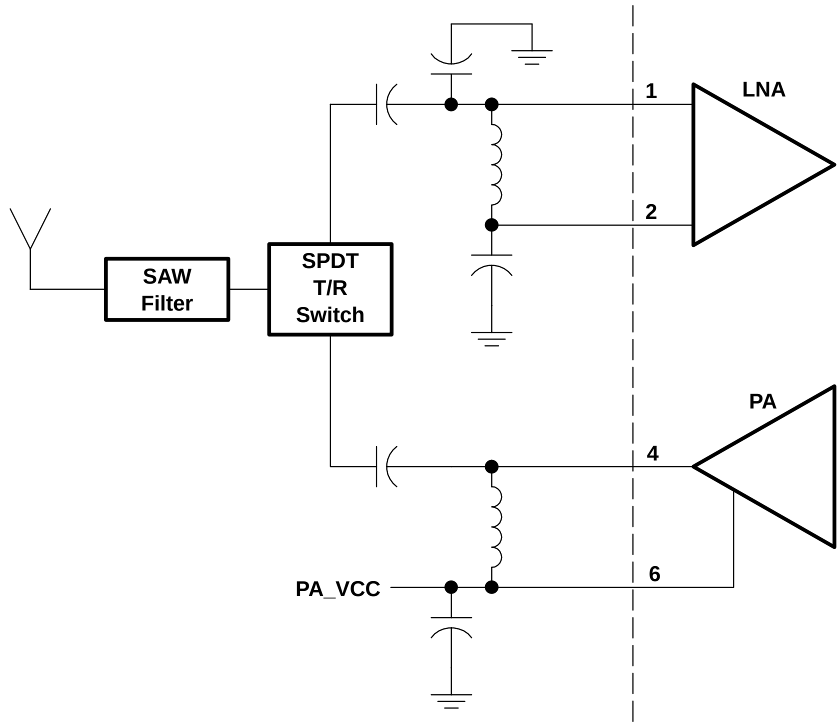
It is possible to use separate transmit and receive antennas with the TRF6901. In this arrangement, the transmit and receive ports of the TRF6901 are individually matched to their antennas. The near field of each antenna will overlap, so care must be taken in testing to determine if significant power absorption or re-radiation effects are present. Spacing and orientation of each antenna may be more critical than if one antenna is used.

Figure 16, Figure 17, and Figure 18 illustrate three methods for connecting the TRF6901 transmit and receive ports to a common antenna.



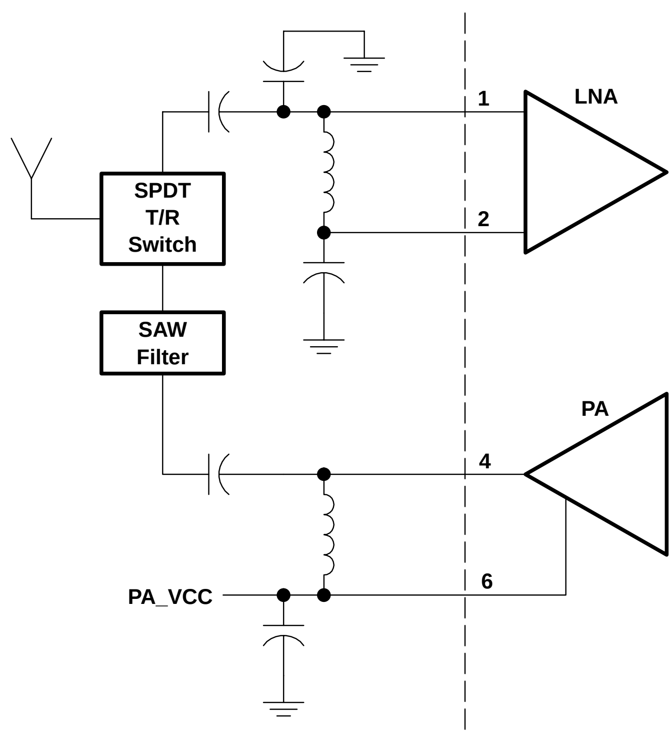
NOTE: The matching circuits are those found in the TRF6901 data sheet.

Figure 16. Common Antenna Port With No SPDT Switch



NOTE: The SAW filter attenuates amplifier harmonics and out-of-band receive noise. Receive sensitivity is degraded by the insertion loss of the filter and switch.

Figure 17. Single-Pole, Double-Throw TR Switch Inserted Between LNA, PA, and Antenna



NOTE: The SAW filter in this position attenuates transmit amplifier harmonics, but does not filter out-of-band receive interference.

Figure 18. SPDT Switch Used at Antenna Port

6.2 SAW and Discrete Filters

A surface acoustic wave (SAW) filter is often used to attenuate out-of-band noise, and to reduce transmit amplifier harmonics to levels that meet regulations. It is a highly tuned device that has a sharp rolloff characteristic out of the pass band. Its drawbacks are insertion loss and cost. The insertion loss in the pass band reduces transmit power and receive sensitivity. An example SAW filter for the 902–928 MHz ISM band is Murata SAFCH915MAA0N00.

A discrete-element LC filter can also be used to attenuate harmonics, but it is difficult to achieve a good match to more than one set of input-output impedances for transmit and receive frequencies that are close to each other. The pass band of a discrete filter with a few elements is usually broader than the pass band of a SAW filter.

6.3 TR Switches

A system with a larger transmission distance requirement may benefit from individual RF ports for transmit and receive. This affords an optimal impedance match for each port to individual antennas or to a SPDT transmit/receive switch. Switches can be diode or FET types, reflective or terminating. Diode switches usually have lower insertion loss, but require more bias current to turn on the active leg and isolate the off leg. FET switches consume little power, but have higher insertion loss.

6.4 External LNAs and PAs

Using an external receive low-noise amplifier or transmit power amplifier boosts sensitivity and transmission range. The disadvantages are added cost and bias requirements. Generally, systems that have external LNAs and PAs also have individual RF ports and dual antennas or use a TR switch to a common antenna. An external amplifier can compensate for the transmit power lost through a switch, SAW filter, or an inefficient antenna.

6.5 Gain and Loss Budgets

It is useful to add up the gain or loss of RF components and circuits between the antenna and the input to the LNA or PA, and to compare the results against the apparent output power and input sensitivity of the wireless system.

6.6 Commonly Used Antennas

A dipole is a simple antenna to implement. Polarization is linear. The dipole can be folded to give orthogonal polarizations, although the gain in each orientation is reduced. A balun is normally used to present the two arms of the dipole with opposing currents.

The monopole is another simple antenna. It can be analyzed as half of a dipole installed over a ground plane, hence the presence of a ground plane is necessary to get all of the available performance.

The loop antenna is often used with amplifiers that have differential inputs. One drawback is that the impedance or loading of the antenna can change according to near-field conditions or changes in amplifier input/output impedance.

The patch antenna can be fed to produce linear or circular polarization. Gain is low. A cavity is usually required behind the antenna to produce directivity.

Other types of antennas are linear arrays, Yagi-Uda arrays, spiral antennas, and horns. All have their specialized applications. Sometimes an antenna can be selective enough to reduce the harmonic content of a transmitted signal.

Many of the antennas used in wireless applications are physically small, perhaps smaller than their nominal electrical design parameters. In such cases the size of the antenna may influence performance more than the antenna type.

6.7 Transmission Range, Link Analysis

One form of the Friis transmission equation is

$$P_r = P_t\, G_t\, G_r\, (\lambda/(4\pi R))^2$$

Where:

P_t = power transmitted

P_r = power received

G_t = cascaded gain (loss) of antenna, SAW filter, and impedance mismatch—transmitter

G_r = cascaded gain (loss) of antenna, SAW filter, and impedance mismatch—receiver

R = transmission range, meters

λ = wavelength, meters

This equation can be used to make a rough estimate of the transmission range of a wireless system operating in free space. In practice, there are more complicated effects from signal multipath, fading, and polarization mismatches.

An example calculation using

0.5 mW (–3 dBm) delivered to the transmit antenna

0.5 (–3 dB) mismatch loss from common transmit RF port

0.5 (–3 dB) mismatch loss from common receive RF port

1.25 (+1 dB) transmit antenna gain

1.25 (+1 dB) receive antenna gain

0.5 (–3 dB) polarization mismatch from antenna misalignment

0.5 (–3 dB) receive front end loss, SAW filter, connector loss, etc.

100 m transmission range at 915 MHz

gives

$$P_r = (0.5)\,(0.5)^4\,(1.25)^2\,(6.807E{-}8)$$

or

P_r = 3.324E–9 mW, or –84.8 dBm received at the input to the LNA matching network.

Many TRF6901 implementations use a common RF port, SAW filter, and no external amplifiers, and have receive power sensitivities around –80 to –105 dBm.

6.8 Direct Modulation

It is possible to increase transmitted data rates greatly by directly modulating the VCO tuning voltage with a separate high-frequency voltage source. The VCO must be modulated outside the PLL loop filter bandwidth. This technique is for experienced designers and is not generally used for ISM applications. The TRF6901 was not specifically designed to support this technique.

6.9 Narrow IF Filter Bandwidth

The IF filter rolloff characteristics can be increased by cascading two IF filters in series. The resulting insertion loss reduces the normal signal gain through the IF strip and can affect receive sensitivity, but for those applications that require narrow or closely-spaced channels this technique may be worth considering. A narrow IF bandwidth requires more stringent control of the errors that contribute to off-center IF signals.

6.10 Dynamic Frequency Correction With RSSI

Under some circumstances it is possible to use the RSSI signal to more closely correct frequency errors at the receiving unit. Frequency alignment is more commonly done once, at production test or at installation.

6.11 Using a Microcontroller

One method of operation for the learn and hold modes is to sample the receive data stream and count training pulses. After 8 training pulses are detected, the microcontroller looks for the start bit and then switches the TRF6901 to the hold mode (if using NRZ coding) for data reception.

The training sequence can be implemented with a pulse train more rapid or slower than the actual data. This can shorten the length of time required for the training sequence.

For systems which must go into standby for long periods of time in order to conserve battery power, a programmable and variable sleep period may be useful. A unit may wake up, check for activity or transmit data, and then go back into standby.

A controller with flash memory can store a list of transmit/receive frequency pairs, correction values to trim the crystal frequency, etc. Under some circumstances, the RSSI signal can be used to determine a correction for the crystal frequency while a unit is in operation. If done carefully, a microcontroller can be dynamically reprogrammed by receiving new instructions transmitted by another unit.

The Texas Instruments MSP430 line of mixed-signal microcontrollers works well with the TRF6901. For more information on using the MSP430, see the references in Section 7.

6.12 North American Regulations

Regulatory compliance is as important as any of the other system performance criteria and should be considered from the beginning of the design process.

Some general notes follow regarding FCC regulations from Parts 15.209, 15.247, 15.249, and 15.35, regarding FSK and OOK systems operating in the North American 902–928 MHz unlicensed ISM band. The designer should refer to the latest revisions of the governing regulations.

Wireless ISM systems can be separated into two categories for regulatory purposes: stationary and channel hopping.

Stationary transmitters broadcast on one frequency for relatively long periods of time, changing channels only when interference is encountered or not at all. Transmitted power from the antenna is limited to –1.2 dBm effective isotropic radiated power (EIRP). Spurs must be –49.2 dBc (49.2 dB below the carrier) or lower. Harmonics are considered out-of-band spurious signals and must be –41.2 dBc or lower.

Channel-changing wireless systems offer the advantage of avoiding other interfering signals, and there are regulatory advantages given to systems that do not transmit continuously at one frequency.

Channel-hopping transmitters change frequencies after a period of continuous transmission, or when interference is encountered. These systems may have higher transmit power and relaxed limitations on in-band spurs. Transmission time on one channel is limited to 400 milliseconds (averaged over 10–20 seconds depending on channel bandwidth) before the transmitter must change frequency. There is a minimum frequency step when changing channels to resume transmission. If there are 25 to 49 frequency channels, EIRP may be 24 dBm, and spurs must be –20 dBc. Harmonics must be –41.2 dBc. With 50 or more channels, EIRP may be up to 30 dBm.

If the antenna directional gain exceeds +6 dBi (single-frequency or channel hopping transmitter), the peak transmit power must be reduced.

There are other emissions limits for out-of-band signals. In general, any wireless system should be designed to emit RF energy only in its intended frequency band of operation.

Systems using on-off keying (OOK) modulation may, under some circumstances, have higher allowable peak transmission power levels than FSK systems.

Fast-frequency-hopping transmitters and receivers, as used in wireless cellular telephony, change frequencies rapidly and employ spread spectrum or direct sequence techniques to increase message traffic over a set of frequencies. These wireless systems fall under a different class of regulations and are generally not used in ISM applications. The TRF6901 is not intended for use in these types of systems.

NOTE: The designer assumes all responsibility for compliance with applicable European, North American, or other governmental regulations in the use of the TRF6901 and other products made by Texas Instruments. Texas Instruments assumes no responsibility or liability for summarizing or interpreting regulations governing the use of wireless transmitters or receivers.

6.13 Printed-Circuit Board Construction

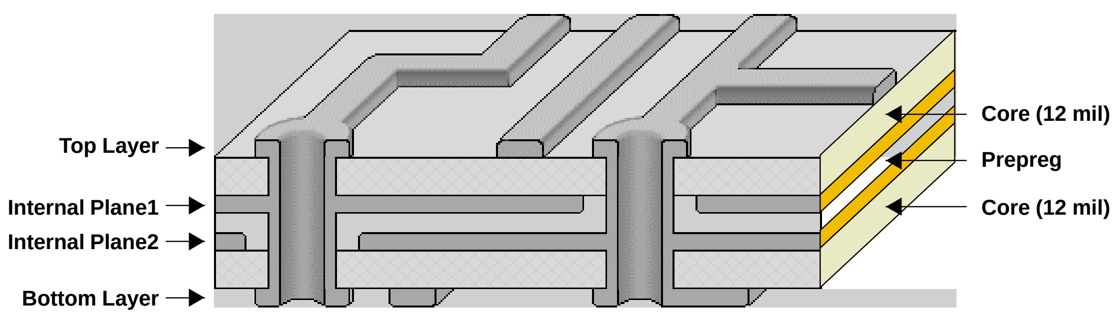


Figure 19. Printed-Circuit Board Layers and Via Construction

Four-layer board stack-up notes:

1. Four-layer PCB (top layer, internal planes 1 and 2, bottom layer). For FR4 material, $\epsilon_r = 4.3$
2. Top layer has 50-Ω controlled impedance

3. 50-Ω line on top layer is 22 mils wide, conductor thickness is 0.012”
4. 2-oz. Cu plating on external (top, bottom) layers, 1-oz. Cu on internal layers
5. The thickness between the top layer and internal plane 1, internal plane 2 and bottom layer is 0.012” core material. The remaining material thickness (prepreg) is determined by the manufacturer to yield a finished board thickness of 0.065” measured copper-to-copper.

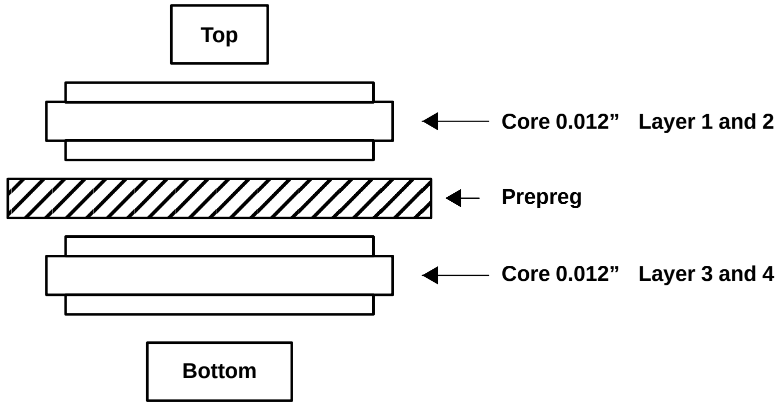


Figure 20. PCB Layers

6.14 Suggested PCB Signal Routing

Top (layer 1): RF, analog, dc (via up from bottom layer), other signals (analog or digital, via up from internal plane 2). Ground planes are poured on this layer. The distance between the top layer and internal layer 1, and the dielectric constant, determine the line width for any given impedance.

The RF/analog ground planes and digital ground planes on each layer are often separated by a moat, which is bridged on the top layer at one point. The ground planes are connected through each layer with vias spaced at 0.1 to 0.25 inches.

Internal layer 1: RF ground plane. Signals from internal layer 2 and the bottom layer via up to the top layer. Plated vias carrying signals must be cleared on the internal layers to prevent shorts.

Internal layer 2: Signal layer (digital, analog) with poured ground planes. Signals routed on this layer via up or down to top/bottom layer. Plated vias carrying signals must be cleared on the internal layers.

Bottom layer: DC and digital signals with poured ground planes. Power is supplied to ICs on the top layer by means of plated vias, which must be cleared on the internal layers.

In some cases, RF signals may be routed on the bottom layer, with appropriate clearance or ground shields around the microstrip line. The internal layers may carry RF signals using coplanar stripline transmission line.

7 Further Reading

For information on data coding, refer to TI publication SWRA033, *Designing With the TRF6900 Single-Chip RF Transceiver*

For information on baseband code and designing a data link, refer to TI publication SLAA121, *Implementing a Bidirectional, Half-Duplex FSK RF Link With TRF6900 and MSP430*

For information on receiver sensitivity, refer to TI publication SWRA030, *Understanding and Enhancing Sensitivity in Receivers for Wireless Applications*

For information on phase-locked loops, refer to TI publication SWRA029, *Fractional/Integer-N PLL Basics*

Wireless Communications, Theodore S. Rappaport, Prentice Hall, 1996

RF/Microwave Circuit Design for Wireless Applications, Ulrich L. Rohde, David P. Newkirk, John Wiley & Sons, 2000

Phase-Lock Basics, William F. Egan, John Wiley & Sons, 1998

TRF6901 Single-Chip RF Transceiver Data Manual, TI publication SLWS110

TRF6901 902 MHz to 928 MHz RF Tool Kit, TI publication SWRU005

TRF6901 868 MHz to 970 MHz RF Tool Kit, TI publication SWRU006

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