THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

TSPC932

OBJECTIVE SPECIFICATION

LOW VOLTAGE PLL CLOCK DRIVER

DESCRIPTION

The TSPC932 is a 3.3V compatible TTL based clock driver device targetted for zero delay applications. The device provides 6 outputs for driving clock loads plus a single feedback clock output. The dedicated feedback output gives the user six choices of input multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3.

TQFP 32
TD suffix

Thin Quad Flat Plastic package
Gullwing leads

MAIN FEATURES

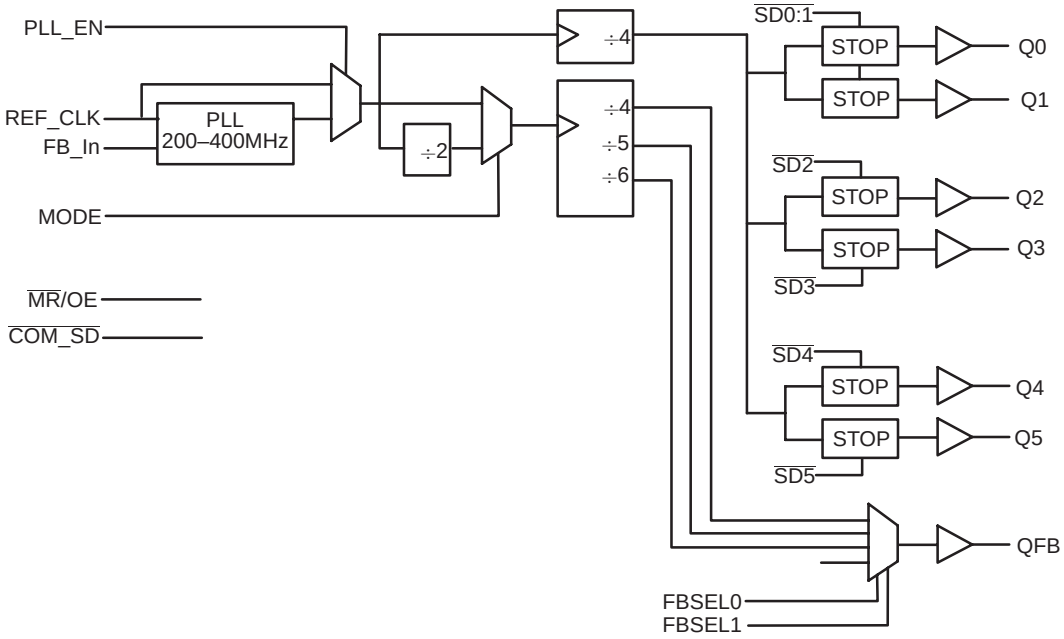
- **Vcc = 3.3V ± 5 %**
- **MILITARY TEMPERATURE RANGE**
- **PC603e™, TSPC740/750 and TSPC2605 COMPANION**
- **SIX LOW SKEW OUTPUTS**
- **ONE DEDICATED FEEDBACK OUTPUT**
- **INDIVIDUAL OUTPUT ENABLE CONTROL**
  - – All outputs can go into high impedance (3-state) for board test purpose.
  - – Test Mode pin provided for low frequency testing.
- **FULLY INTEGRATED PLL**
- **OUTPUT FREQUENCY UP TO 100MHz**
- **SIX INPUT/OUTPUT RATIOS**

SCREENING / QUALITY

This product is manufactured:

- according to TCS upscreening standard.

LOGIC BLOCK DIAGRAM



A. GENERAL DESCRIPTION

1. INTRODUCTION

The TSPC932 provides individual output enable control. The enables are synchronized to the internal clock such that upon assertion the shut down signals will hold the clocks LOW without generating a runt pulse on the outputs. The shut down pins provide a means of powering down certain portions of a system or a means of disabling outputs when the full compliment are not required for a specific design. The shut down pins will disable the outputs when driven LOW. A common shut down pin is provided to disable all of the outputs (except the feedback output) with a single control signal.

Two feedback select pins are provided to select the multiplication factor of the PLL. The TSPC932 provides six multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3. In the 1.25 and 2.5 modes, The QFP output will not provide a 50% duty cycle. The phase detector of the TSPC932 only monitor rising edge of its feedback signal, thus for this function a 50% duty cycle is not required. As the QFB signal can also be used to drive other clocks in a system, it is important the user understands that the duty cycle will not be 50%. In the x1 and x1.5 modes, QFB output will produce a 50% duty cycle signal.

The TSPC932 provides two pins for use in a system test and debug operations. The $\overline{MR}$/OE input will force all of the outputs into a high–impedance state for outputs back driving during system test. In addition, the PLL_EN pin allows user to bypass the PLL and to drive directly through the REF_CLK input. Note that the REF_CLK signal will be routed through the dividers so that it will take several transitions on the REF_CLK input to create a transition on outputs.

The TSPC932 is fully 3.3V compatible and requires no external loop filter components. All of the inputs are LVCMOS/LVTTL compatible and the outputs produce rail–to–rail 3.3V swings. For series terminated application, each output can drive two series terminated 50Ω transmission lines. For parallel terminated lines, the device can drive terminations of 50Ω into VCC/2. The device is packaged in a 32–lead TQFP package to provide the optimum combination of performance, board density and cost.

2. PIN ASSIGNMENTS

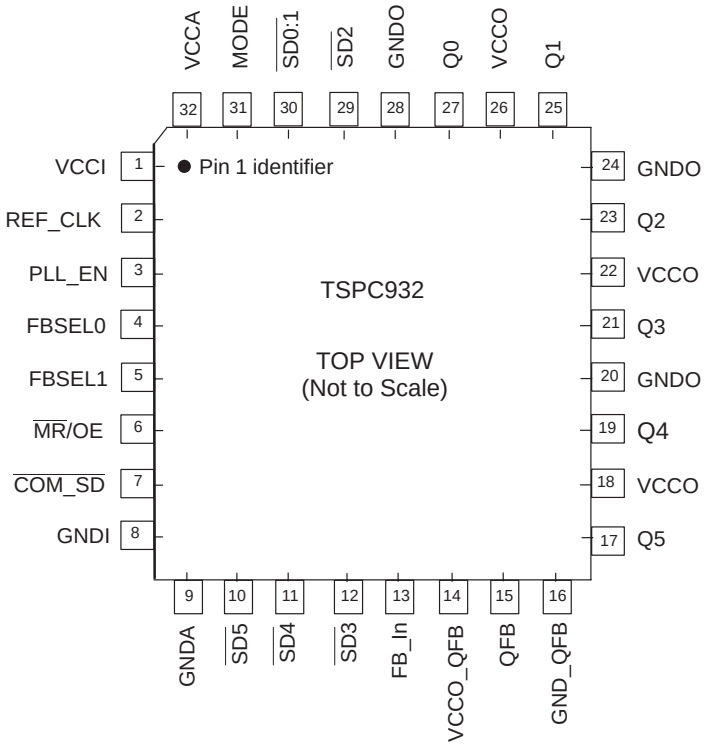


Figure 1 : 32–Lead TQFP package pinout

3. SIGNALS DESCRIPTION

Pin	Name	Function
14, 18, 22, 26	VCCO, VCCO_QFB	Digital +3.3V Output Buffers Power Supply
32	VCCA	Analog +3.3V PLL Power Supply
1	VCCI	Digital +3.3V Core Power Supply
8, 9, 16, 20, 24, 28	GNDO, GNDO_QFB, GNDA, GNDI	Ground
2	REF_CLK	Reference Clock Input
3	PLL_EN	PLL Enable
4, 5	FB_SEL[0;1]	Outputs multiplication factor selection
6	$\overline{MR}$/OE	Asserted: Outputs enable. Negated: Outputs in tri–state mode
7	$\overline{COM\_SD}$	Common outputs shut down
10, 11, 12, 29, 30	$\overline{SDx}$	Individual outputs shut down
13	FB_In	PLL Feedback Input
15	QFB	PLL Feedback Output
17,19,21,23,25,27	Qx	Clock Outputs
31	MODE	Outputs multiplication factor selection

B. DETAILED SPECIFICATIONS

1. SCOPE

This drawing describes the specific requirements for the microprocessor TSPC932, in compliance withTCS standard screening.

2. REQUIREMENTS

2.1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	–0.3	4.6	V
Input voltage	V_{in}	–0.3	V_{CC} + 0.3	V
Input Current	I_{IN}		$\pm$ 20	mA
Storage temperature range	T_{stg}	–55	150	°C

Note : Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

2.2. Mechanical and environment

The microcircuits shall meet all environmental requirements of TCS standard screening.

2.3. Design and construction

The terminal connections shall be as shown in § A.2 PIN ASSIGNMENT

2.4. Marking

Each microcircuit are legible and permanently marked with the following information as minimum :

– Motorola initial marking including P/N and date–code

– XT label for TCS Extended Temperature Upscreening

2.5. Package

The precise case outlines are described at the end of this specification (§ 5. OUTLINES DIMENSIONS).

3. ELECTRICAL CHARACTERISTICS

3.1. DC CHARACTERISTICS (TC = –55°C to 125°C, Vcc = 3.3V ± 5%)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Input HIGH Voltage	V_{IH}		2.0		3.6	V
Input LOW Voltage	V_{IL}				0.8	V
Output HIGH Voltage	V_{OH}	I_{OH}=–20mA (Note 1.)	2.4			V
Output LOW Voltage	V_{OL}	I_{OL}=+20mA (Note 1.)			0.5V	V
Input Current	I_{IN}	Note 2.			± 120	µA
Maximum Core Supply Current	I_{cc}				100	mA
Maximum PLL Supply Current	I_{CCPLL}			15	20	mA
Maximum Output Buffers Supply Current	I_{CCO}				150	mA
Input Capacitance	C_{IN}				4	pF
Output Capacitance	C_{PD}	Per output		25		pF

Note 1: The TSPC932 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Information section).

Note 2: Inputs have pull–up/pull–down resistors which affect current.

3.2. PLL INPUT REFERENCE CHARACTERISTICS (TC = –55°C to 125°C, Vcc = 3.3V ± 5%)

Parameter	Symbol	Comments	Min.	Max.	Unit
TCLK Input Rise/Fall Time	t_r, t_f			3.0	ns
Reference Input Frequency	f_{ref}		Note 3.	Note 3.	MHz
Reference Input Duty Cycle	f_{refDC}		25	75	

Note 3: Minimum and Maximum input reference frequency is limited by the VCO lock range and feedback divider.

3.3. AC CHARACTERISTICS (TC = –55°C to 125°C, Vcc = 3.3V ± 5%)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Reference Input Frequency	f_{ref}		Note 4.		Note 4.	MHz
Output–to–Output Skew	t_{OS}	Note 5.		200	300	ps
VCO Lock Range	f_{VCO}		200		400	MHz
Maximum Output Frequency	f_{Qn}				100	MHz
Output Duty Cycle	t_{pw}	Note 5.				ps
Output Rise/Fall Time	t_r,t_f	0.8 to 2.0V	0.1		1.0	ns
Output Disable Time	t_{PLZ},t_{PHZ}	50Ω to V_{CC}/2	2.0		8.0	ns
Output Enable Time	t_{PZL}	50Ω to V_{CC}/2	2.0		10.0	ns
Cycle–to–Cycle Jitter	t_{jitter}	Note 6.		± 150		ps
Maximum PLL Lock Time	t_{lock}				10	ms

Note 4: Input reference frequency is bounded by VCO lock range and feedback divide selection.

Note 5: Measured with 50Ω to V_{CC}/2 termination.

Note 6: See Application Information section for more jitter information.

4. APPLICATION INFORMATION

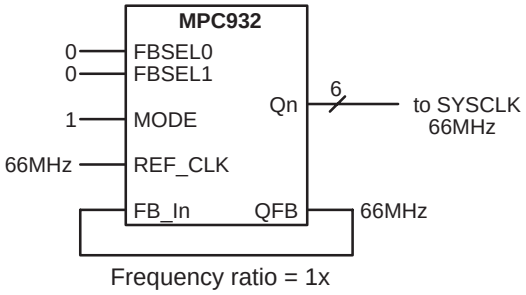
4.1. Output frequency selection

TSPC932 provides three independent pins to select the multiplication factor of the PLL. MODE pin and FBSEL[0–1] pins allow to select different paths through dividers (see logic diagram for more information).

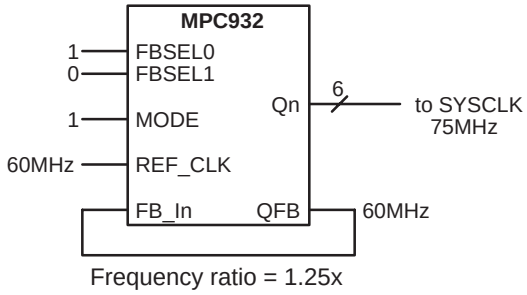
MODE	FBSEL1	FBSEL0	Qn	QFB	PLL multiplication factor
0	0	0	VCO/4	VCO/8	2x
0	0	1	VCO/4	VCO/10	2.5x
0	1	0	VCO/4	VCO/12	3x
0	1	1	NA	NA	–
1	0	0	VCO/4	VCO/4	1x
1	0	1	VCO/4	VCO/5	1.25x
1	1	0	VCO/4	VCO/6	1.5x
1	1	1	NA	NA	–

4.2. Driving PowerPC microprocessors SYSCLK input

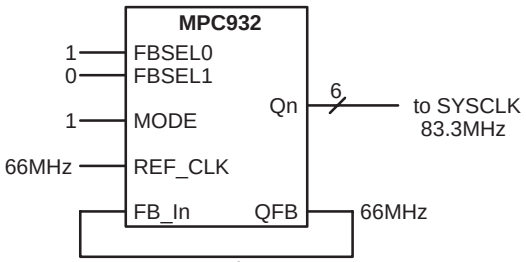
TSPC932 was designed to fit TSPC603, TSPC740/750 and TSPC2605 high performances clock input characteristics. The following figure highlights some possible configurations to drive SYSCLK input of these devices.



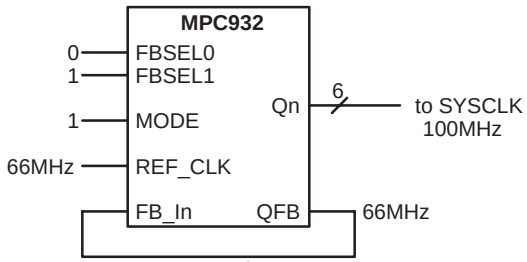
Frequency ratio = 1x



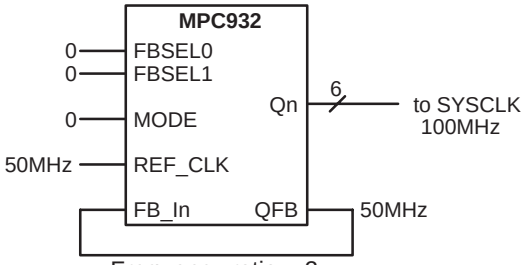
Frequency ratio = 1.25x



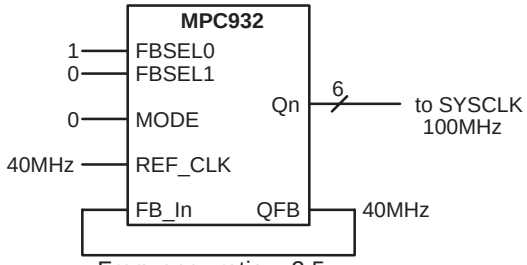
Frequency ratio = 1.25x



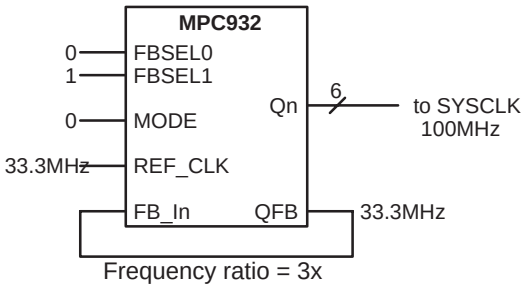
Frequency ratio = 1.5x



Frequency ratio = 2x



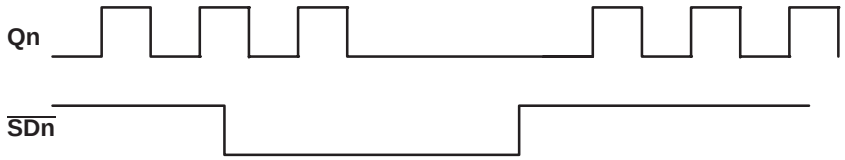
Frequency ratio = 2.5x



Frequency ratio = 3x

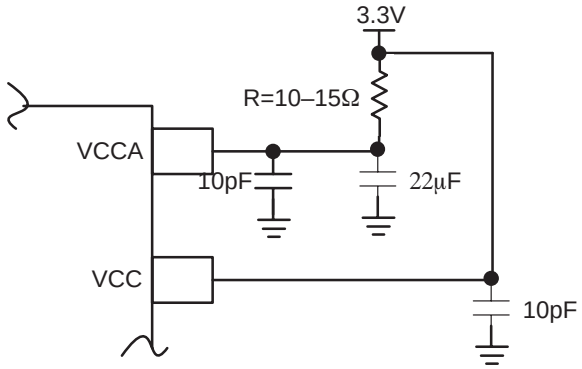
4.3. Output Shut–Down pins

TSPC932 provides 6 shut–downs to disable a single or multiple parts of a system.



4.4. Power Supply Filtering

The TSPC932 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on power supply pins. The TSPC932 provides separate power supplies for the output buffers (VCCO) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop.In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin.



The TSPC932 is most susceptible to noise with spectral content in the 1kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter is the DC voltage drop that will be seen between the Vcc supply and the VCCA pin of the TSPC932. From the datasheet, the current sourced through the VCCA pin is typically 15mA (20mA maximum). Assuming that a minimum of 3.0V must be maintained on the VCCA pin, very little DC voltage drop can be tolerated when a 3.3V power supply is used. The resistor shown in figure above must have a resistance of 10 to 15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall performance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL

Although the TSPC932 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter scheme discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

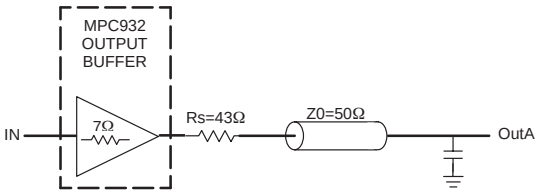
4.5. Jitter Performance on TSPC932

With clock raqtes of today's digital systems continuing to increase, more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and hiw that affects the overall system timing budget. The TSPC932 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design.
The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment, there is no way to measure this parameter for jitter performance in the class demonstrated by the TSPC932. As a result, different methods are used which approximate cycle–to–cycle jitter.The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviation of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is no the case, the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data form a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a consevative estimate of cycle–to–cycle jitter.
Moreover, there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost, always configure the device such that the VCO runs sa fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep updates at the phase detector will help to reduce jitter. Note that if there is a dradeoff between higher reference frequencies and higher VCO frequencies, always chose the higher VCO frequency to minimize jitter. The third guidelines is to try to shut down outputs that are unused. Minimizing the number of switching outputs will minimize output jitter.

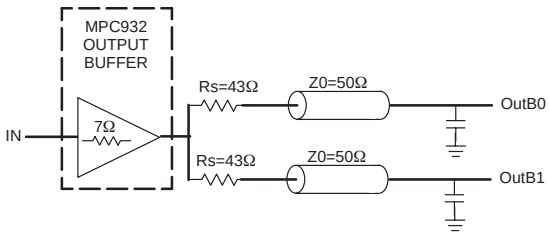
4.6. Driving Trnamission Lines

The TSPC932 Clock Driver was designed to drive high speed signals in a terminated transmission lines environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω, output drivers are able to drive either parallel or series termintated transmission lines. For more information on transmission lines, please refer to the Motorola Application Note AN1091.

In most high performance clock networks, point–to–point signals distribution is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to Vcc/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the TSPC932 Clock Driver.



For the series terminated case, no DC current is drawn, thus the outputs can drive multiple series terminated lines in parallel. When taken to its extreme, the fanout of the TSPC932 Clock Driver is effectively doubled due to its capability to drive multiple lines.



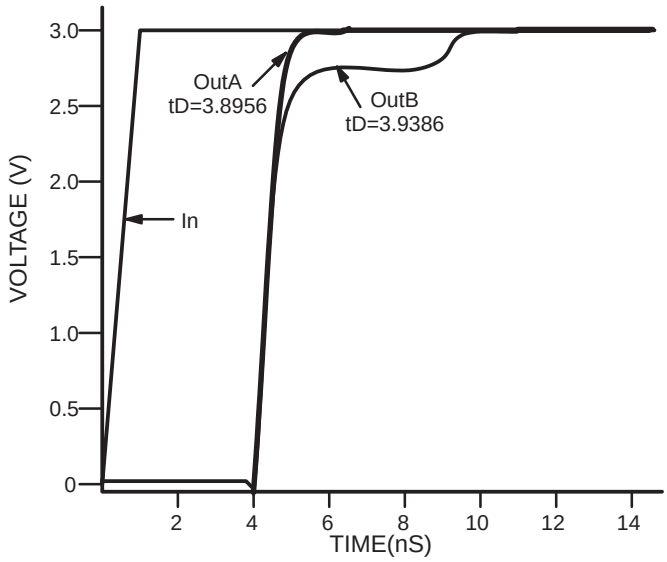
The waveform plot below shows the simulation results of an output driving a single line vs two lines. In both cases, driving capability of the TSPC932 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. This waveform shows a step caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedance. The voltage wave launched down the two lines will equal:

VL=VS(Zo/(Rs+Ro+Zo))

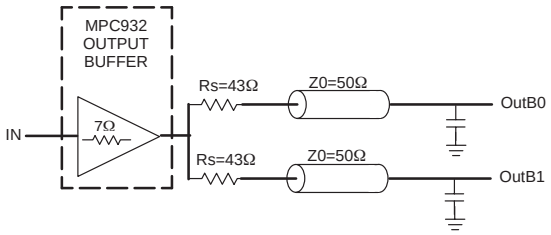
Zo=50Ω || 50Ω
Rs=43Ω || 43Ω
Ro=7Ω

VL=3.0(25/(21.5+7+25)=1.40V

At the load end the voltage will double, due to near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).



Since this step is well above the threshold region, it will not cause any false clock triggering, however designers may be uncomfortable with anwanted reflections on the line. To better match the impedances when driving multiple lines, the situation depicted below should be preferred. In this case, series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.

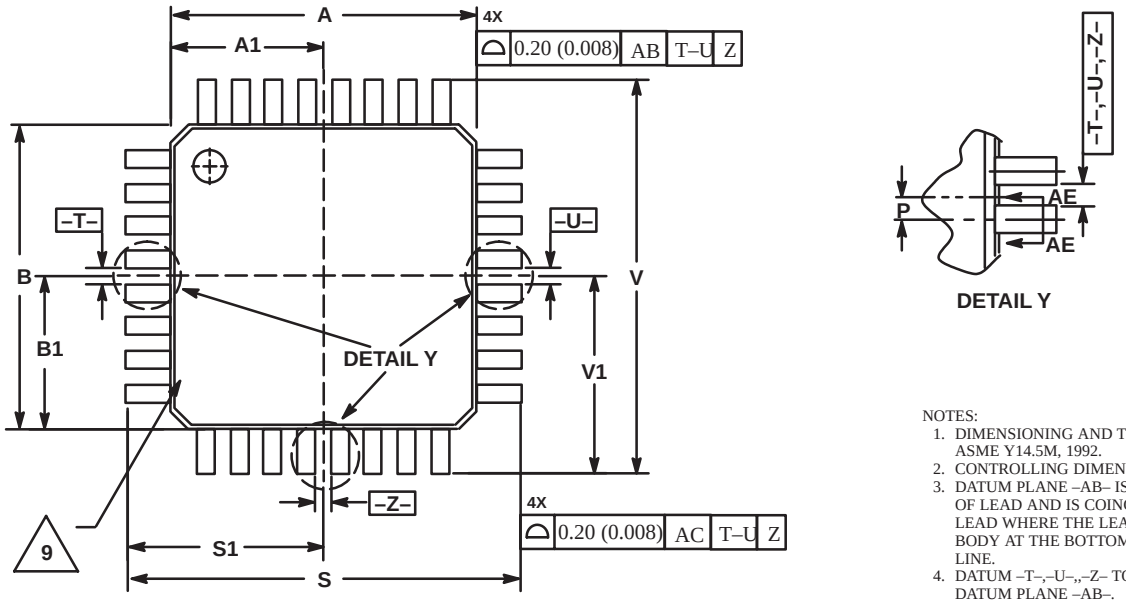


7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

5. OUTLINES DIMENSIONS

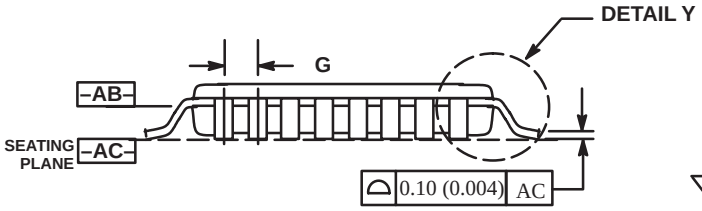
■ **TQFP 32 - Plastic Thin Quad Flat Package (dimensions in inches and (mm))**

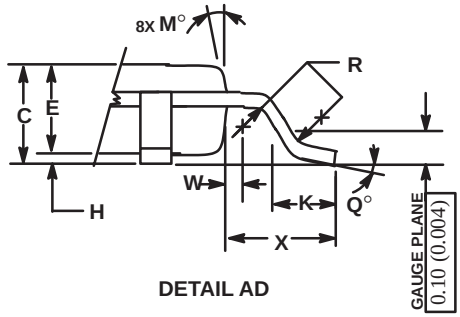
TD package
TQFP
CASE 873A–02
ISSUE A



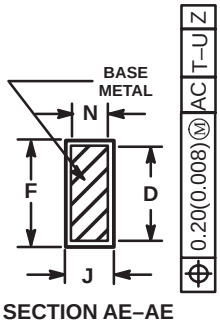
TOP VIEW

DETAIL Y





DETAIL AD

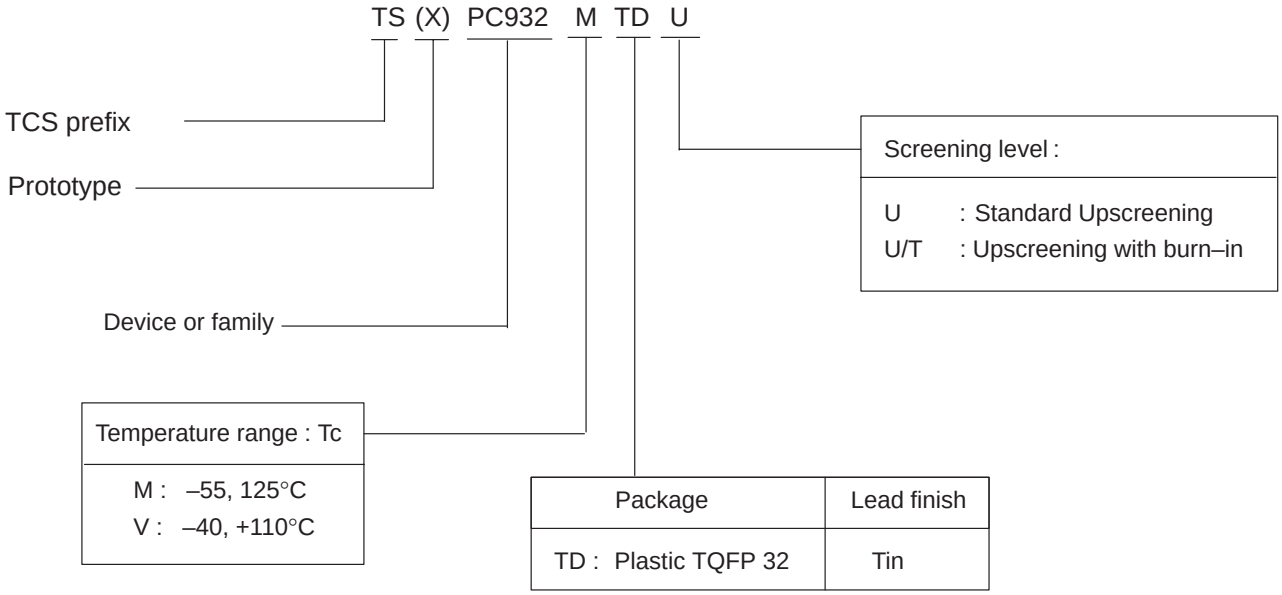


SECTION AE–AE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1992.
2. CONTROLLING DIMENSION: MILLIMETER..
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXISTS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM –T–,–U–,,–Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEALING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSION. ALLOWABLE PROTUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTUSION. DAMBAR PROTUSION SHALL NO CAUSE THE D DIMENSION TO NOT EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076(0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 BSC		0.008 BSC	
X	1.000 BSC		0.039 BSC	

6. ORDERING INFORMATION



This product is manufactured and commercialized by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - PO Box 123 - 38521 SAINT-EGREVE Cedex - FRANCE.

For further information please contact :

THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - Route Départementale 128 - PO Box 46 - 91401 ORSAY Cedex - FRANCE - Phone +33 (0)1 69 33 00 00 - Fax +33 (0)1 69 33 03 21 - Télex 616780 F - E-mail : lafrique@tcs.thomson.fr