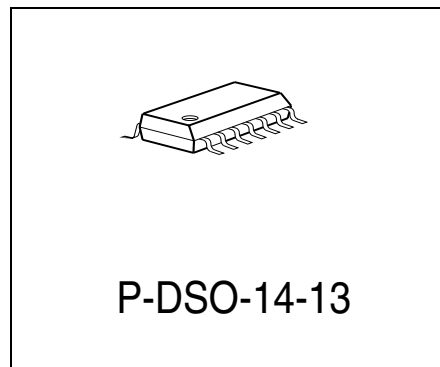


Preliminary Data Sheet

1 Features

- Data transmission rate up to 125 kBaud
- Very low current consumption in stand-by and sleep operation mode
- Implemented receive-only mode
- Optimized EMC behavior
- Wake-up input pin, dual edge sensitive
- Battery fail flag
- Extended bus failure management to guarantee safe operation during all bus line failure events
- Full support of dual failure conditions
- Fully wake-up capability during all bus line failures conditions
- Supports one-wire transmission mode with ground offset voltages up to 1.5 V
- Prevention from bus occupation in case of CAN controller failure
- Thermal protection
- Bus line error protection against transients in automotive environment



Type	Ordering Code	Package
TLE 6254-2G	Q67006-A9549	P-DSO-14-13 (SMD)

2 Description

The CAN-Transceiver TLE 6254 works as the interface between the CAN protocol controller and the physical CAN bus-lines.

It is optimized for low-speed data transmission (up to 125 kBaud) in automotive and industrial applications.

While no data is transferred, the power consumption can be minimized by multiple low power modes.

In normal operation mode a differential signal is transmitted/received. When bus wiring failures are detected the device automatically switches in a dedicated single-wire mode to maintain communication.

3 Pin Configuration (top view)

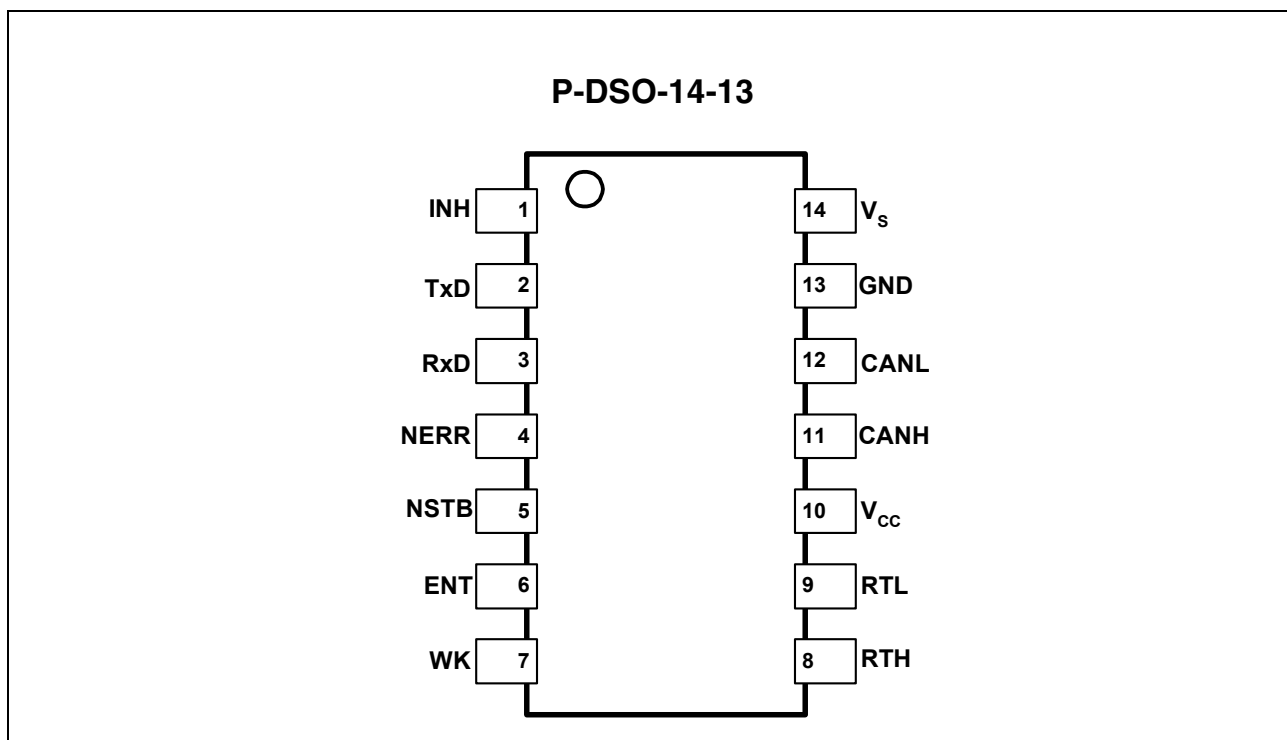


Figure 1

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	INH	Inhibit output ; for controlling an external voltage regulator
2	TxD	Transmit data input ; integrated pull up, LOW: bus becomes dominant, HIGH: bus becomes recessive
3	RxD	Receive data output ; integrated pull up, LOW: bus is dominant, HIGH: bus is recessive
4	NERR	Error flag output ; integrated pull up, LOW: bus error (in normal operation mode), further functions see Table 3
5	NSTB	Not stand-by input ; digital control inputs to select operation modes, see Figure 4
6	ENT	Enable transfer input ; digital control input to select operation modes, see Figure 4

Pin Configuration (top view)

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
7	WK	Wake-Up input; if level of V_{WAKE} changes the device indicates a wake-up from low power mode by switching the RxD and INT outputs LOW and switching the INH output HIGH (in sleep mode), see Table 3
8	RTH	Termination resistor output; connect to CANH bus-line via termination resistor ($500\ \Omega < R_{RTH} < 16\ k\Omega$), controlled by internal failure management
9	RTL	Termination resistor output; connect to CANL bus-line via termination resistor ($500\ \Omega < R_{RTL} < 16\ k\Omega$), controlled by internal failure and mode management
10	V_{CC}	Supply voltage input; + 5 V, block to GND directly at the IC with ceramic capacitor
11	CANH	CAN bus line H; HIGH: dominant state
12	CANL	CAN bus line L; LOW: dominant state
13	GND	Ground
14	V_S	Battery voltage supply input; block to GND directly at the IC with ceramic capacitor

Functional Block Diagram

4 Functional Block Diagram

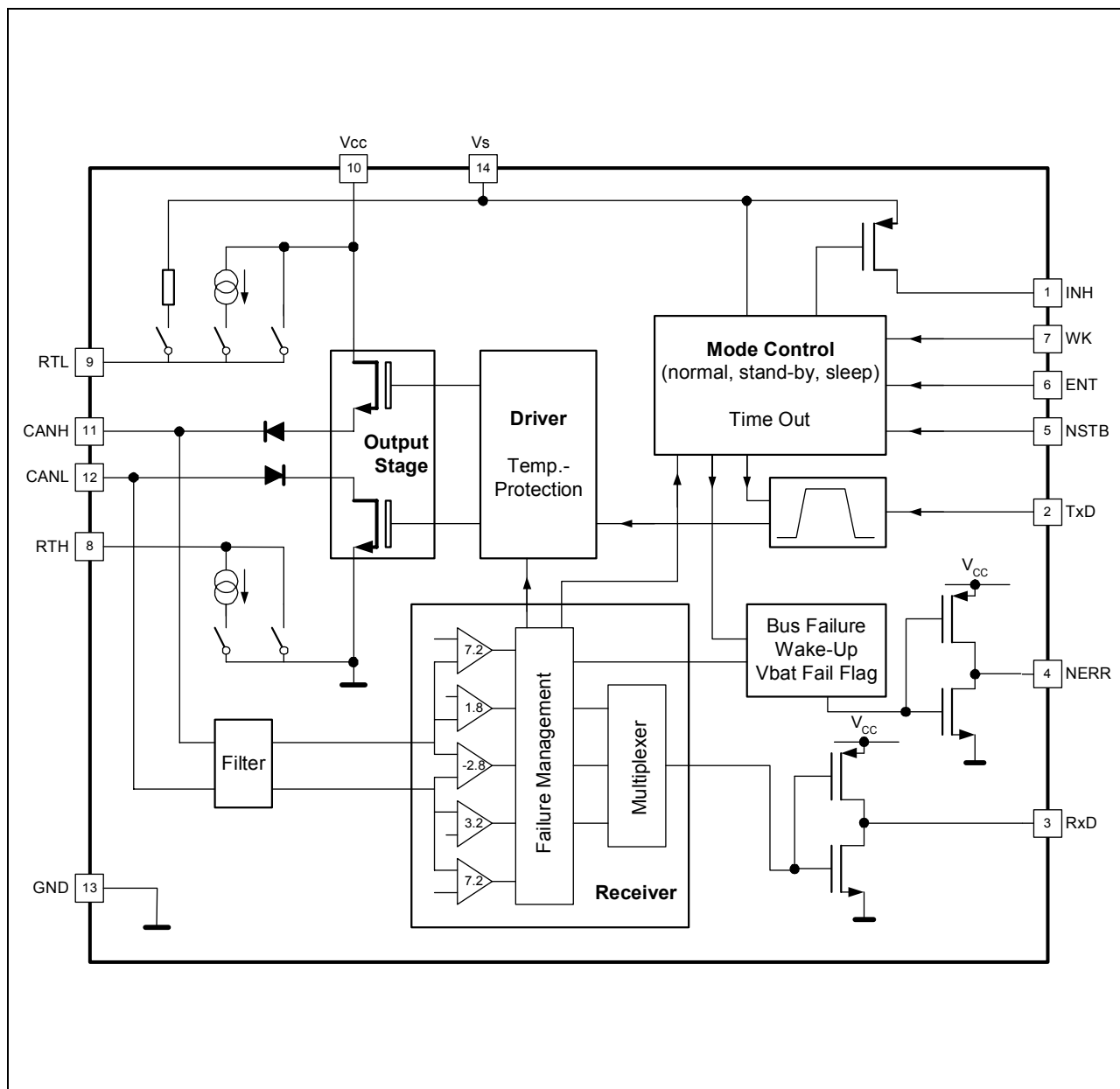


Figure 2 Block Diagram

5 Circuit Description

The CAN transceiver TLE 6254 works as the interface between the CAN protocol controller and the physical CAN bus-lines. **Figure 3** shows the principle configuration of a CAN network.

The TLE 6254 is optimized for low-speed data transmission (up to 125 kBaud) in automotive and industrial applications.

In normal operation mode a differential signal is transmitted/received. When bus wiring failures are detected the device automatically switches in a dedicated single-wire mode to maintain communication.

While no data is transferred, the power consumption can be minimized by multiple low power operation modes. Further a receive-only mode is implemented.

To reduce radiated electromagnetic emission (EME) the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (one of the bus lines is affected by a bus line failure) the EME performance of the system is degraded from the differential mode.

In case the transmission data input TxD is permanently dominant, both, the CANH and CANL transmitting stage are disabled after a certain delay time. This is necessary to prevent the bus from being blocked by a defective protocol unit or short to GND at the TxD input.

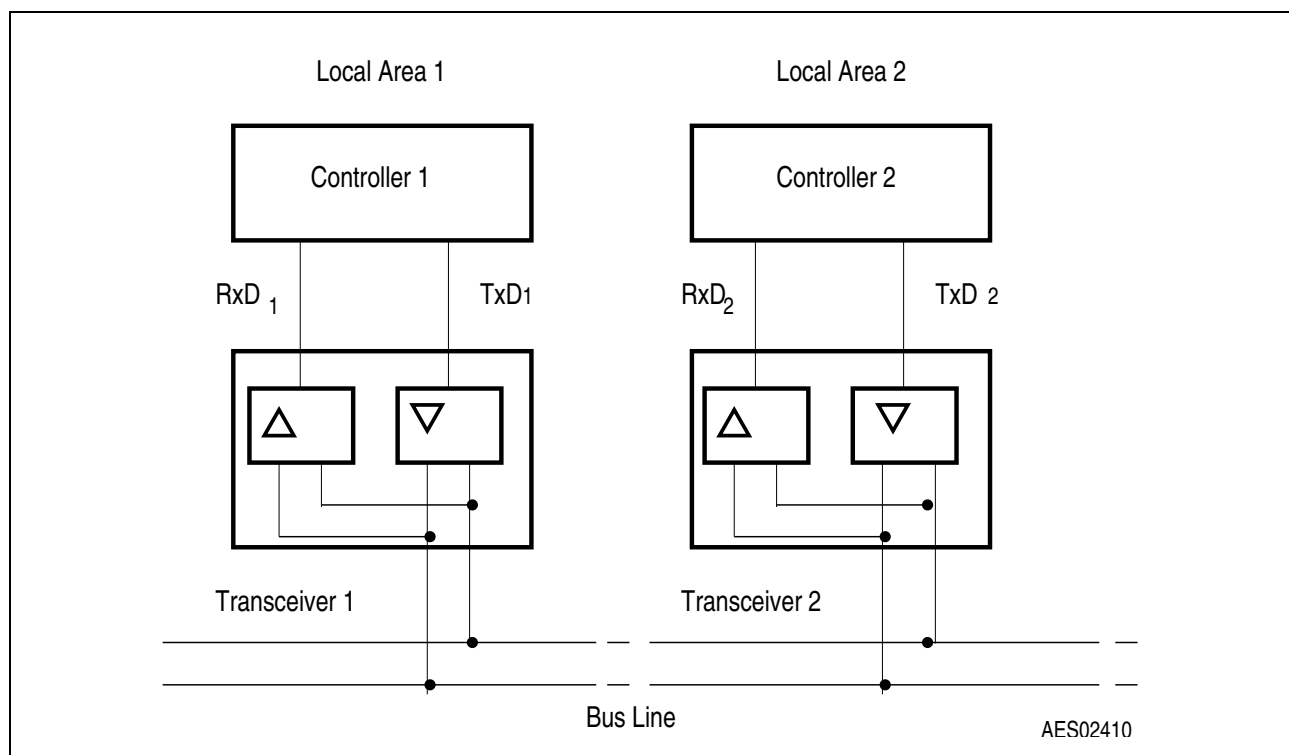


Figure 3 CAN Network Example

Circuit Description

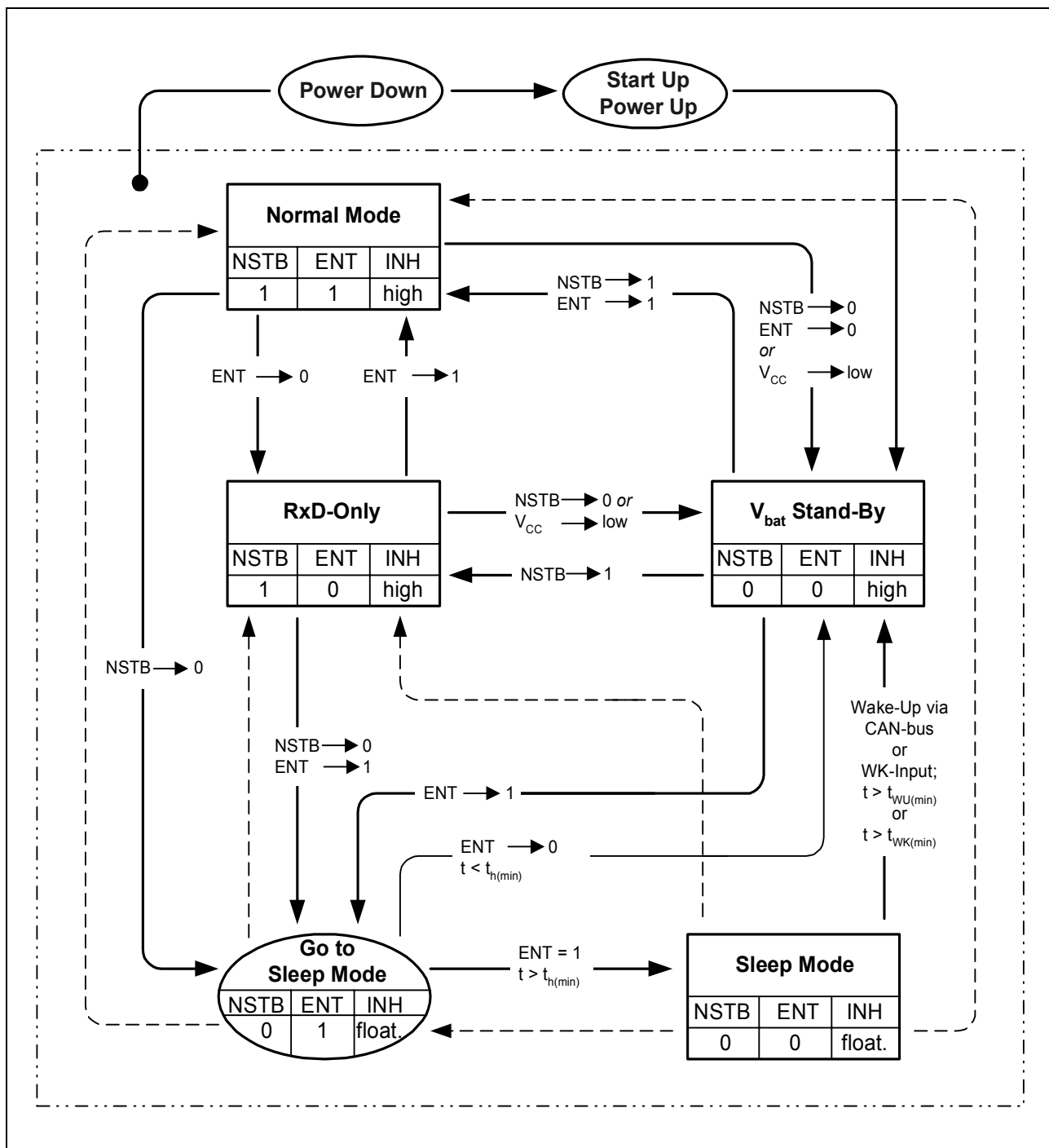


Figure 4 State Diagram

5.1 Operation Modes, Wake-Up

In addition to the normal operation mode, the TLE 6254 offers a receive-only mode as well as two low power operation modes to save power during periods that do not require communication on the CAN bus: sleep mode, V_{Bat} stand-by mode (see **Table 5** and **Figure 4**). Via the control input pins NSTB and ENT the operation modes are selected by the microcontroller. In the low power modes neither receiving nor transmitting of messages is possible.

In sleep operation mode the lowest power consumption is achieved. In order to minimize the overall current consumption of the ECU (electronic control unit) the external voltage regulator (5 V supply) is deactivated by the INH output in this mode, when connected. For that purpose the INH output is switched to high impedance. In parallel the CANL line is pulled-up to the battery supply voltage via the RTL output and the pull-up paths at the input pins TxD and RxD are disabled from the internal supply.

To enter the sleep operation mode the transition mode “Go-to-Sleep” has to be selected (**Figure 4**) for a minimum time $t_{\text{h(min)}}$. After the minimum hold time $t_{\text{h(min)}}$ the sleep mode can be actively selected. Otherwise the TLE 6254 will automatically fall in sleep mode because of the not powered microcontroller.

On a wake-up request either by bus line activities or via the WAKE input, the transceiver is automatically set in V_{Bat} -stand-by mode. Now the voltage regulator (5 V supply) is enabled by the INH output. The WAKE input reacts to both, transition from high to low voltage level as well as the other way round. To avoid faulty wake-ups due to transients on the bus lines or the WAKE input circuitry respectively, a certain filter time is implemented. As soon as V_{CC} is provided, the wake-up request is monitored on both, the NERR and RxD outputs, by setting them low. Upon this the microcontroller can activate the normal operation mode by setting the control inputs NSTB and ENT high.

The V_{Bat} stand-by mode corresponds to the sleep mode, but a voltage regulator connected to the INH output will remain active. Wake-up requests via the WAKE pin or the bus lines are immediately reported to the microcontroller by setting RxD and NERR low. A power-on condition (V_{BAT} pin is supplied) automatically switches the TLE 6254 to V_{Bat} stand-by mode.

In the receive-only mode data on the CAN-bus are transversed to the RxD output, but both output stages, CANH as well as CANL are disabled. This means that data at the TxD input are not transmitted to the CAN bus. This mode is useful in combination to a dedicated network-management software that allows separate diagnosis for all nodes.

A wake-up request in the receive-only mode is only reported at the RxD-output. The NERR output in this mode is used to indicate a battery fail condition. When entering the normal mode the V_{bat} -flag is reset and the NERR output becomes high again. This feature is useful e.g. when changing the ECU and therefore a presetting routine of the microcontroller has to be started.

Circuit Description

If either of the supply voltages drops below the specified limits, the transceiver is automatically switched to V_{BAT} stand-by mode or power down mode respectively.

Table 2 Truth Table of the CAN Transceiver

NSTB	ENT	Mode	INH	NERR	RxD	RTL
0	0	V_{BAT} stand-by mode ¹⁾	V_{bat}	active LOW wake-up interrupt if V_{CC} is present		switched to V_{BAT}
0	0	sleep mode ²⁾	floating			switched to V_{BAT}
0	1	go to sleep command	becomes floating			switched to V_{BAT}
1	0	Receive-only mode	V_{bat}	active LOW V_{BAT} power-on flag ³⁾	HIGH = recessive receive data; LOW = dominant receive data	switched to V_{CC}
1	1	normal mode	V_{bat}	active LOW bus error flag	HIGH = recessive receive data; LOW = dominant receive data	switched to V_{CC}

¹⁾ Wake-up interrupts are released when entering normal operation mode.

²⁾ If go to sleep command was used before, ENT may turn LOW as V_{CC} drops, without affecting internal functions.

³⁾ V_{BAT} power-on flag will be reseted when entering normal operation mode.

5.2 Bus Failure Management

The TLE 6254 detects the bus failures as described in **table 3**, and automatically switches to a dedicated CANH or CANL single wire mode to maintain data transmission if necessary. Therefore, the device is equipped with one differential receiver and 4 single ended receivers, two for each bus line. To avoid false triggering by external RF influences the single wire modes are only activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay. Bus failures are indicated in the normal operation mode by setting the NERR output low.

The differential receiver threshold is typ. – 2.8 V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2 and 4 with a noise margin as high as possible. For these failures, further failure management is not necessary. Detection of the failure cases 1, 2, 3a and 4 is only possible when the bus is dominant. Nevertheless, they are reported on the NERR output until transmission of the next CAN word on the bus begins.

Circuit Description

When one of the bus failures 3, 5, 6, 6a and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and the respective output stage. A wake-up from sleep mode via the bus is possible either via a dominant CANH or CANL line. This ensures that a wake-up is possible even if one of the failures 1 to 7 occurs.

Table 3 **CAN bus-line failures** (according to ISO 11519-2)

failure #	failure description
1	CANL line interrupted
2	CANH line interrupted
3	CANL line shorted to V_{BAT}
3a	CANL line shorted to V_{CC}
4	CANH line shorted to GND:
5	CANL line shorted to GND:
6	CANH line shorted to V_{BAT}
6a	CANH line shorted to V_{CC}
7	CANL line shorted to CANH line

A current limiting circuit protects the CAN transceiver output stages from damage by short-circuit to positive and negative battery voltages.

The CANH and CANL pins are protected against electrical transients which may occur in the severe conditions of automotive environments.

The transmitter output stages generate the majority of the power dissipation. Therefore they are disabled if the junction temperature exceeds the maximum value. This effectively reduces power dissipation, and hence will lead to a lower chip temperature, while other parts of the IC can remain operating. In temperature shut-down condition the TLE 6254 is still able to receive CAN-bus messages.

5.3 Comparison TLE 6254 versus TLE 6252

In the following table (**table 4**) the min differences between the TLE 6252 and TLE 6254 are listed.

Circuit Description

Table 4 TLE 6254 versus TLE 6252

TLE 6254	TLE 6252
Receive-only mode	Vcc-stand-by mode
improved EMC susceptibility	-
improved bus failure handling for shorts of the CAN-bus lines to Vcc	-
Threshold for Power-On flag: typ: 2.7 V	Threshold for Power-On flag: typ: 1.0 V
A transition from Vbat-stand-by mode to the go-to sleep command is possible also after a wake-up from sleep mode.	Internal wake flag after wake-up from sleep mode is deleted by transition to normal mode. This flag needs to be deleted before entering the go-to-sleep command again.
all dual failure conditions are handled	some dual failure conditions are not correctly handled
Improved leakage current behavior of RTL pin in power down state.	

5.4 Application Hints

Table 5 Not Needed Pins

Pin Symbol	Recommendation
INH	Leave open
NERR	Leave open
NSTB	Connect to V_{CC}
ENT	Connect to V_{CC}
WAKE	Connect to V_{BAT} , if not possible connect to GND: increases current consumption by approx. 5 μA

The transceiver will stay in a present operating mode until a suitable condition disposes a state change. If not otherwise defined all conditions are AND-combined. The signals V_{CC} and V_{BAT} show if the supply is available (e.g. $V_{CC} = 1$: V_{CC} voltage is present). If at minimum one supply voltage is switched on, the start-up procedure begins (not figured). After a delay time the device changes to normal operating or stand-by mode.

Absolute Maximum Ratings

6 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input voltage at V_{BAT}	V_S	– 0.3	40	V	–
Logic supply voltage V_{CC}	V_{CC}	– 0.3	6	V	–
Input voltage at TxD, RxD, NERR, NSTB and ENT	V_{IN}	– 0.3	$V_{CC} + 0.3$	V	–
Input voltage at CANH and CANL	V_{BUS}	– 40	40	V	–
Transient voltage at CANH and CANL	V_{BUS}	– 150	100	V	1)
Input voltage at WAKE	V_{WK}	–	40	V	–
Output current at WAKE	I_{WK}	–	5	mA	–
Input voltage at INH	V_{INH}	– 0.3	$V_{BAT} + 0.3$	V	–
Input voltage at RTH and RTL	$V_{RTH/L}$	– 0.3	40	V	–
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 55	155	°C	–
Electrostatic discharge voltage at pin CANH, CANL, RTH, RTL, V_{BAT}	V_{esd}	– 4	4	kV	2)
Electrostatic discharge voltage at any other pin	V_{esd}	– 2	2	kV	3)

1) See ISO 7637

2) Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

7 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Logic input voltage	V_{CC}	4.75	5.25	V	–
Battery input voltage	V_S	6	27	V	–
Termination resistances at RTL and RTH	$R_{RTL/H}$	0.5	16	k Ω	–
Junction temperature	T_j	– 40	140	°C	–

Thermal Resistance

Junction ambient	R_{thja}	–	120	K/W	–
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Thermal Shutdown

Junction temperature	T_{jSH}	140	–	°C	–
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Wake Input Voltage

Wake input voltage	V_{WK}	– 0.3	27	V	–
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Note: In the operating range, the functions given in the circuit description are fulfilled.

Static Characteristics

8 Static Characteristics

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		

Supplies V_{CC} , V_S

Supply current	I_{CC}	–	5.0	8.0	mA	recessive; $TxD = V_{CC}$
		–	6.5	10	mA	dominant; $TxD = 0\text{ V}$; no load
Supply current (Receive-only mode)	I_{CC}	–	3.5	5.0	mA	
Supply current (V_{BAT} stand-by)	I_{CC}	–	25	50	μA	$V_{CC} = 5\text{ V}$; $V_S = 12\text{ V}$
	I_S	–	40	60	μA	
Supply current (sleep operation mode)	I_S	–	35	60	μA	$V_{CC} = 0\text{ V}$; $V_S = 12\text{ V}$;
Battery voltage for setting power-on flag	V_S	1.5	2.5	3.5	V	V_{CC} stand-by mode guaranteed by design
Battery voltage low time for setting power-on flag	$t_{pw(on)}$		10		μs	Receive-only mode

Receiver Output RxD and Error Detection Output NERR

HIGH level output voltage (pin NERR)	V_{OH}	$V_{CC} - 0.9$	–	V_{CC}	V	$I_0 = -100\text{ }\mu\text{A}$
HIGH level output voltage (pin RxD)	V_{OH}	$V_{CC} - 0.9$	–	V_{CC}	V	$I_0 = -250\text{ }\mu\text{A}$
LOW level output voltage	V_{OL}	0	–	0.9	V	$I_0 = 1.25\text{ mA}$

Static Characteristics

8 Static Characteristics (cont'd)

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		

Transmission Input TxD, Not Stand-By NSTB and Enable Transfer ENT

HIGH level input voltage	V_{IH}	$0.7 \times V_{CC}$	–	$V_{CC} + 0.3$	V	–
LOW level input voltage	V_{IL}	– 0.3	–	$0.3 \times V_{CC}$	V	–
HIGH level input current (pins NSTB and ENT)	I_{IH}	–	30	60	μA	$V_i = 4\text{ V}$
LOW level input current (pins NSTB and ENT)	I_{IL}	0.7	6	–	μA	$V_i = 1\text{ V}$
HIGH level input current (pin TxD)	I_{IH}	– 150	– 40	– 10	μA	$V_i = 4\text{ V}$
LOW level input current (pin TxD)	I_{IL}	– 600	– 200	– 40	μA	$V_i = 1\text{ V}$
Forced battery voltage stand-by mode (fail safe)	V_{CC}	2.75	–	4.5	V	–

Wake-up Input WAKE

Input current	I_{IL}	– 3	– 2	– 1	μA	–
Wake-up threshold voltage	$V_{WK(min)}$	2.2	3.2	3.9	V	$V_{NSTB} = 0\text{ V}$

Inhibit Output INH

HIGH level voltage drop $\Delta V_H = V_S - V_{INH}$	ΔV_H	–	0.3	0.8	V	$I_{INH} = -0.18\text{ mA}$;
Leakage current	$I_{INH,ik}$	– 5.0	–	5.0	μA	sleep operation mode; $V_{INH} = 0\text{ V}$

Static Characteristics

8 Static Characteristics (cont'd)

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		

Bus Lines CANL, CANH

Differential receiver recessive-to-dominant threshold voltage	$V_{dRxD(rd)}$	-2.8	-2.5	-2.2	V	$V_{CC} = 5.0\text{ V}$
Differential receiver dominant-to-recessive threshold voltage	$V_{dRxD(dr)}$	-3.2	-2.9	-2.6	V	$V_{CC} = 5.0\text{ V}$
CANH recessive output voltage	$V_{CANH,r}$	0.10	0.15	0.30	V	$TxD = V_{CC}$; $R_{RTH} < 4\text{ k}\Omega$
CANL recessive output voltage	$V_{CANL,r}$	$V_{CC} - 0.2$	—	—	V	$TxD = V_{CC}$; $R_{RTL} < 4\text{ k}\Omega$
CANH dominant output voltage	$V_{CANH,d}$	$V_{CC} - 1.4$	$V_{CC} - 1.0$	V_{CC}	V	$TxD = 0\text{ V}$; $I_{CANH} = -40\text{ mA}$
CANL dominant output voltage	$V_{CANL,d}$	—	1.0	1.4	V	$TxD = 0\text{ V}$; $I_{CANL} = 40\text{ mA}$
CANH output current	I_{CANH}	-110	-80	-50	mA	$V_{CANH} = 0\text{ V}$; $TxD = 0\text{ V}$
		-5	0	5	μA	sleep operation mode; $V_{CANH} = 12\text{ V}$
CANL output current	I_{CANL}	50	80	110	mA	$V_{CANL} = 5\text{ V}$; $TxD = 0\text{ V}$
		-5	0	5	μA	sleep operation mode; $V_{CANL} = 0\text{ V}$; $V_S = 12\text{ V}$

Static Characteristics

8 Static Characteristics (cont'd)

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{\text{det(th)}}$	6.5	7.3	8.0	V	–
Voltage detection threshold for short-circuit to battery voltage on CANH	$V_{\text{det(th)}}$	$V_{\text{BAT}} - 2.5$	$V_{\text{BAT}} - 2$	$V_{\text{BAT}} - 1$	V	stand-by/ sleep operation mode
CANH wake-up voltage threshold	$V_{\text{CANH,wu}}$	1.2	1.9	2.7	V	–
CANL wake-up voltage threshold	$V_{\text{CANL,wu}}$	2.2	3.1	3.9	V	–
Wake-up voltage threshold hysteresis	ΔV_{wu}	0.2	–	–	V	$\Delta V_{\text{wu}} = V_{\text{CANL,wu}} - V_{\text{CANH,wu}}$
CANH single-ended receiver threshold	V_{CANH}	1.6	2.1	2.6	V	failure cases 3, 5 and 7
CANL single-ended receiver threshold	V_{CANL}	2.4	2.9	3.4	V	failure case 6 and 6a
CANL leakage current	$I_{\text{CANL,lk}}$	– 5	0	5	μA	$V_{CC} = 0\text{ V}$; $V_S = 0\text{ V}$; $V_{\text{CANL}} = 12\text{ V}$; $T_j < 85\text{ }^{\circ}\text{C}$
CANH leakage current	$I_{\text{CANH,lk}}$	– 5	0	5	μA	$V_{CC} = 0\text{ V}$; $V_S = 0\text{ V}$; $V_{\text{CANH}} = 5\text{ V}$; $T_j < 85\text{ }^{\circ}\text{C}$

Static Characteristics

8 Static Characteristics (cont'd)

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		

Termination Outputs RTL, RTH

RTL to V_{CC} switch-on resistance	R_{RTL}	–	20	95	Ω	$I_o = -10\text{ mA}$
RTL output voltage	V_{oRTL}	$V_{CC} - 1.0$	$V_{CC} - 0.7$	–	V	$ I_o < 1\text{ mA}$; V_{CC} stand-by mode
RTL to BAT switch series resistance	R_{oRTL}	5	15	28	k Ω	V_{BAT} stand-by or sleep operation mode
RTH to ground switch-on resistance	R_{RTH}	–	20	95	Ω	$I_o = 10\text{ mA}$
RTH output voltage	V_{oRTH}	–	0.7	1.0	V	$I_o = 1\text{ mA}$; low power mode
RTH pull-down current	$I_{RTH,pd}$	40	75	120	μA	failure cases 6 and 6a
RTL pull-up current	$I_{RTL,pu}$	– 120	– 75	– 40	μA	failure cases 3, 3a, 5 and 7
RTH leakage current	$I_{RTH,lk}$	– 5	0	5	μA	$V_{CC} = 0\text{ V}$; $V_S = 0\text{ V}$; $V_{RTH} = 5\text{ V}$; $T_j < 85\text{ }^{\circ}\text{C}$
RTL leakage current	$I_{RTL,lk}$	– 5	0	5	μA	$V_{CC} = 0\text{ V}$; $V_S = 0\text{ V}$; $V_{RTL} = 12\text{ V}$; $T_j < 85\text{ }^{\circ}\text{C}$

Dynamic Characteristics

9 Dynamic Characteristics

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
CANH and CANL bus output transition time recessive-to-dominant	t_{rd}	0.6	1.2	2.1	μs	10% to 90%; $C_1 = 10\text{ nF}$; $C_2 = 0$; $R_1 = 100\text{ }\Omega$
CANH and CANL bus output transition time dominant-to-recessive	t_{dr}	0.3	0.6	1.3	μs	10% to 90%; $C_1 = 1\text{ nF}$; $C_2 = 0$; $R_1 = 100\text{ }\Omega$
Minimum dominant time for wake-up via CANL or CANH	$t_{wu(min)}$	15	25	40	μs	stand-by modes; $V_S = 12\text{ V}$
Minimum wake-up time on pin WAKE	$t_{WK(min)}$	15	25	50	μs	Low power modes; $V_S = 12\text{ V}$
Failure cases 3, 6 detection time	t_{fail}	30	45	80	μs	–
Failure case 6a detection time		2	4.8	6	ms	–
Failure cases 5, 6, 6a, 7 recovery time		30	45	80	μs	–
Failure cases 3 recovery time		250	500	750	μs	–
Failure cases 5, 7 detection time		1.0	2.0	4.0	ms	–
Failure cases 5 detection time		0.4	1.0	2.4	ms	stand-by modes; $V_S = 12\text{ V}$
Failure cases 6, 6a, 7 detection time		0.8	4.0	8.0	ms	stand-by modes; $V_S = 12\text{ V}$
Failure cases 5, 6, 6a, 7 recovery time		0.4	1.0	2.4	ms	stand-by modes; $V_S = 12\text{ V}$

Dynamic Characteristics

9 Dynamic Characteristics (cont'd)

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{PD(L)}$	–	1.5	2.1	μs	$C_1 = 100\text{ pF}$; $C_2 = 0$; $R_1 = 100\text{ }\Omega$; no failures and bus failure cases 1, 2, 3a, 4
		–	1.7	2.4	μs	$C_1 = C_2 = 3.3\text{ nF}$; $R_1 = 100\text{ }\Omega$; no bus failure and failure cases 1, 2, 3a, 4
		–	1.8	2.5	μs	$C_1 = 100\text{ pF}$; $C_2 = 0$; $R_1 = 100\text{ }\Omega$; bus failure cases 3, 5, 6, 6a, 7
		–	2.0	2.6	μs	$C_1 = C_2 = 3.3\text{ nF}$; $R_1 = 100\text{ }\Omega$; bus failure cases 3, 5, 6, 6a, 7
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{PD(H)}$	–	1.5	2.0	μs	$C_1 = 100\text{ pF}$; $C_2 = 0$; $R_1 = 100\text{ }\Omega$; no failures and bus failure cases 1, 2, 3a, 4
		–	2.5	3.5	μs	$C_1 = C_2 = 3.3\text{ nF}$; $R_1 = 100\text{ }\Omega$; no bus failure and failure cases 1, 2, 3a, 4

Dynamic Characteristics

9 Dynamic Characteristics (cont'd)

$4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$; $6\text{ V} \leq V_S \leq 27\text{ V}$; normal operation mode; $-40 \leq T_j \leq +125\text{ }^{\circ}\text{C}$ (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{PD(H)}$	–	1.0	2.1	μs	$C_1 = 100\text{ pF}$; $C_2 = 0$; $R_1 = 100\text{ }\Omega$; bus failure cases 3, 5, 6, 6a, 7
		–	1.5	2.6	μs	$C_1 = C_2 = 3.3\text{ nF}$; $R_1 = 100\text{ }\Omega$; bus failure cases 3, 5, 6, 6a, 7
Minimum hold time to go sleep command	$t_{h(min)}$	15	25	50	μs	–
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a, 4 detection NERR becomes LOW	n_e	–	4	–	–	–
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a, 4 recovery		–	2	–	–	–
TxD permanent dominant disable time	t_{TxD}	1.3	2.0	3.5	ms	–

10 Test and Application

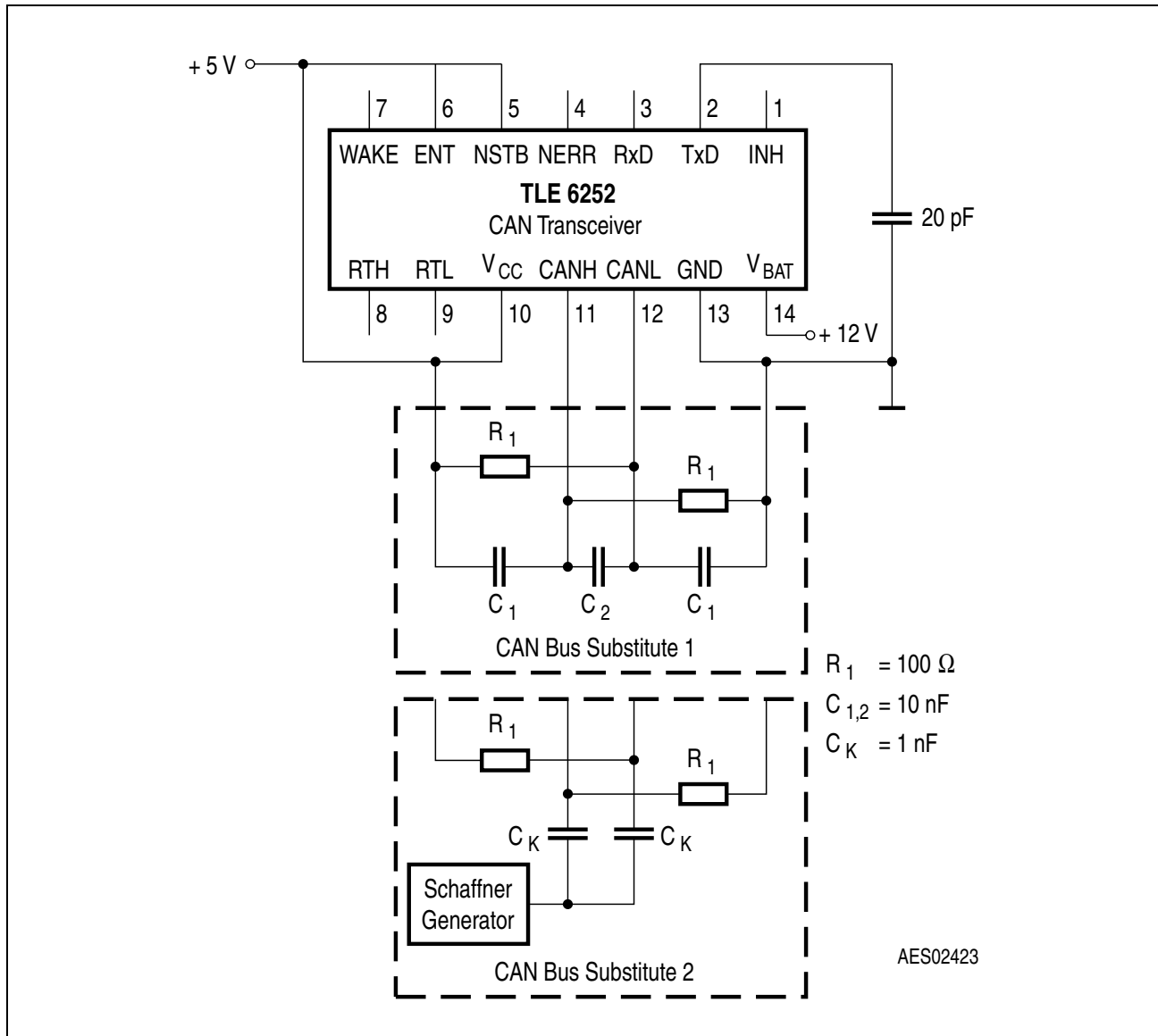


Figure 5 Test Circuits

For isolated testing the CAN Bus Substitute 1 is connected to the CAN Transceiver (see **Figure 5**). The capacitors $C_{1,2}$ simulate the cable. Allowed minimum values of the termination resistors R_{RTH} and R_{RTL} are 500 Ω. Electromagnetic interference on the bus lines is simulated by switching to CAN Bus Substitute 2. The waves of the applied transients will be in accordance with ISO 7637 part 1, test 1, test pulses 1, 2, 3a and 3b.

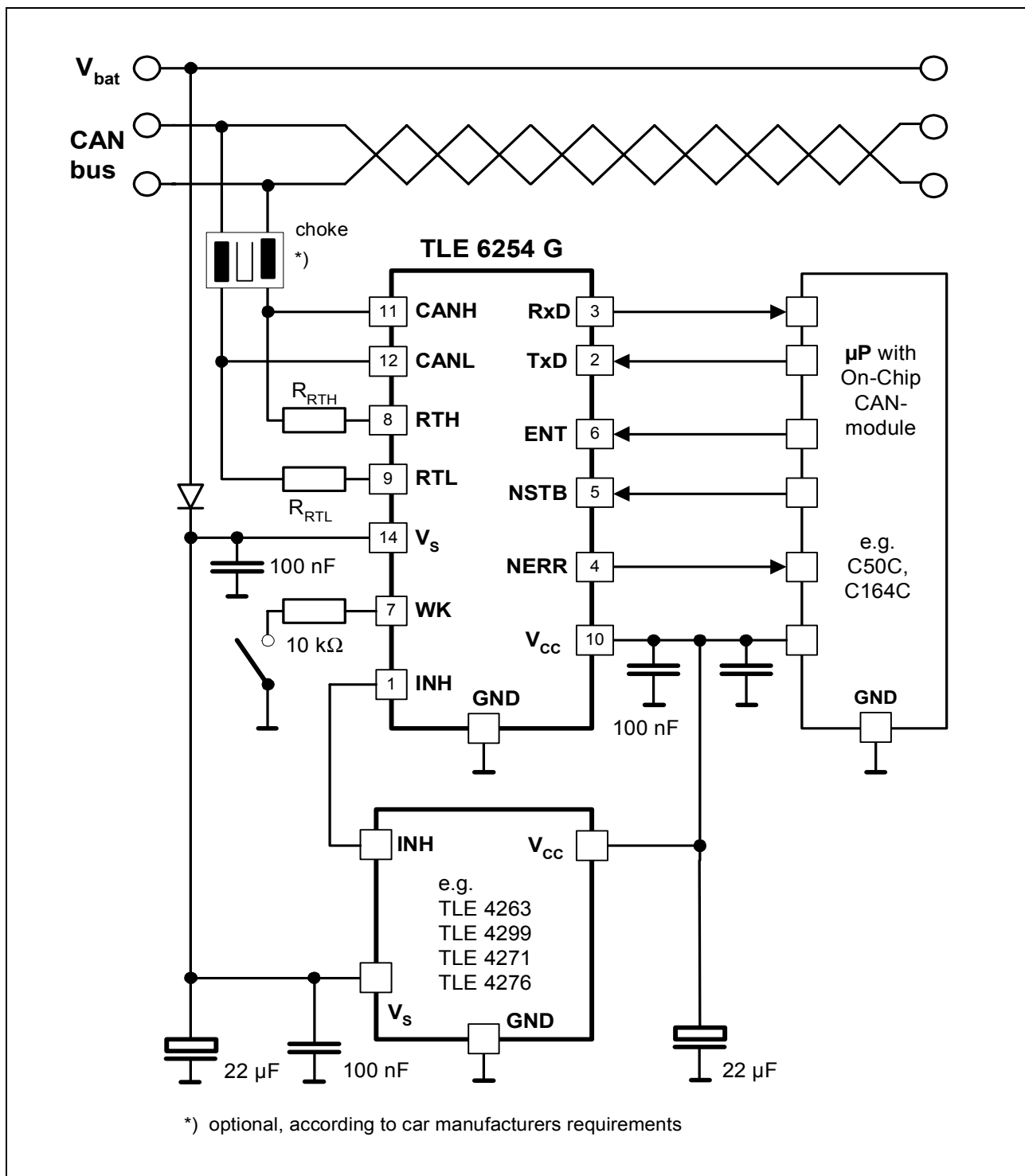
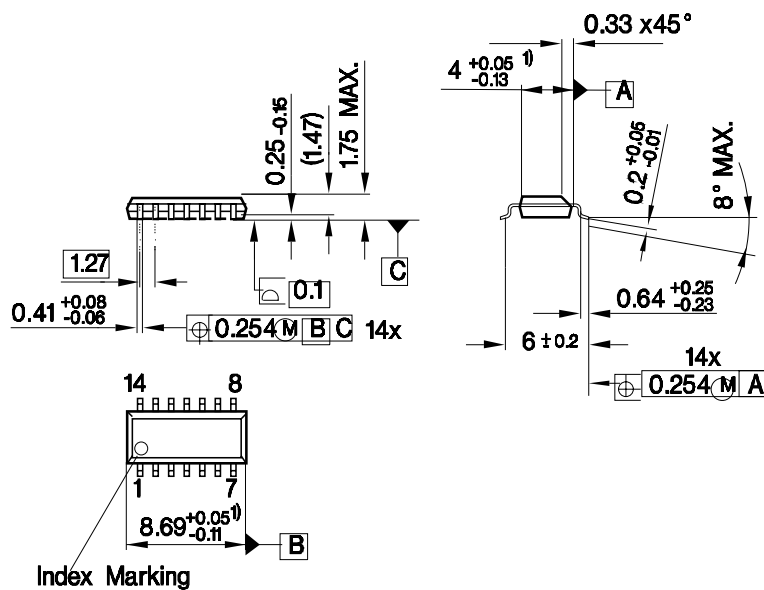


Figure 6 Application Circuit

11 Package Outlines

P-DSO-14-13

(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPS09330

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm

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