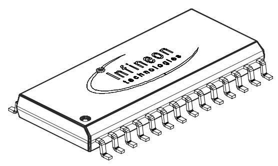
Kormoran II

TLE 6266 G

Target Data Sheet

1 Features

- Standard Fault Tolerant differential CAN-Transceiver
- Bus failure management
- Low current consumption mode <70µA
- CAN data transmission rate up to 125 kBaud
- Low-Dropout Voltage Regulator 5V ± 2%
- Two Low Side Switches
- Three High Side Switches with internal Charge Pump
- Power on and under-voltage Reset Generator
- Vcc Supervisor
- Window Watchdog
- Programable Cyclic Wake Timing via SPI
- Integrated fail-safe mechanism
- Standard 16 bit SPI-Interface
- Wide input voltage and temperature range
- Thermal protection
- Enhanced power P-DSO-Package
- Wakeup input pin



P-DSO-28-6
Enhanced Power

Type	Ordering Code	Package
TLE 6266 G	on request	P-DSO-28-6

2 Description

The TLE 6266 G is a monolithic integrated circuit in an enhanced power P-DSO-28-6 package, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a 16 bit SPI interface to control and monitor the IC. Further there are integrated additional features like three high side switches, two low side switches, a window watchdog circuit and a reset circuit. The IC offers a low current consumption mode, that reduces the current to typ. 70µA.

The IC is designed to withstand the severe conditions of automotive applications and is optimized for low-speed data transmission (up to 125 kBaud).

3 Pin Configuration

(top view)

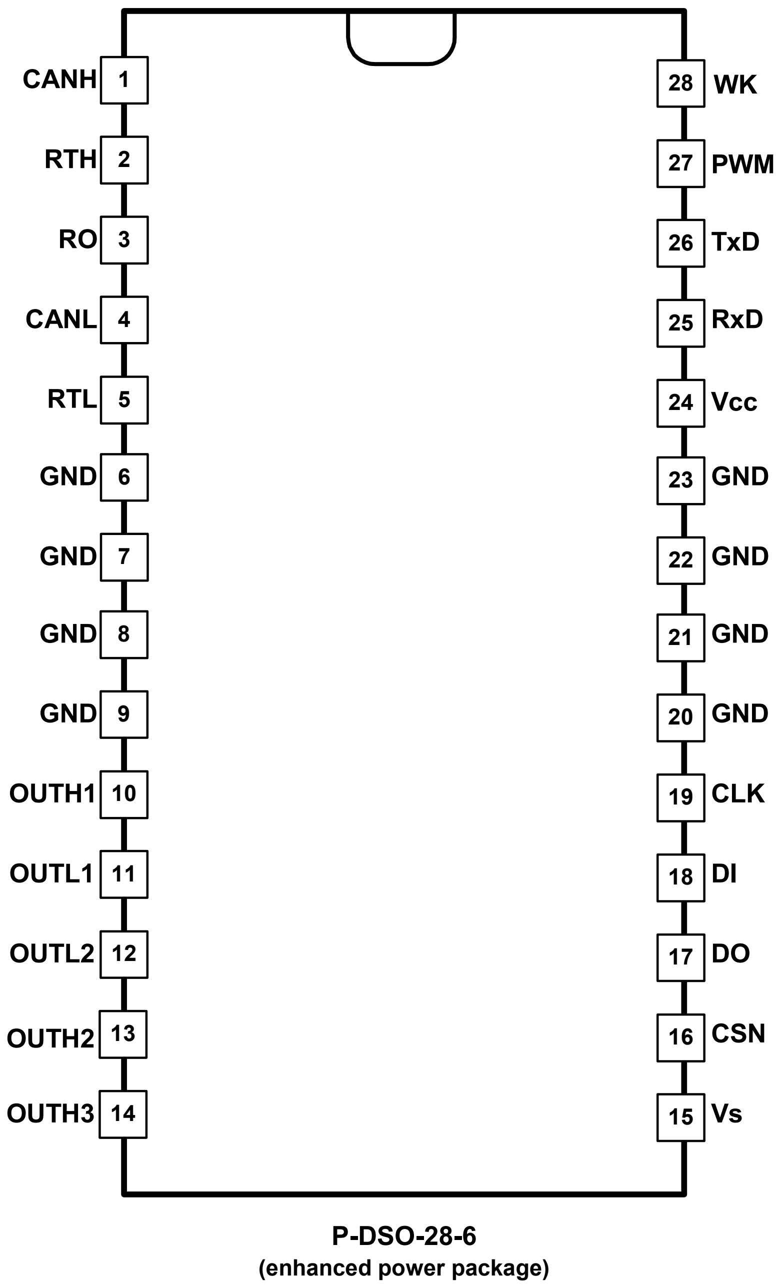


Figure 1 TLE 6266 Block Diagram

4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	CANH	**CAN-H bus line**; HIGH in dominant state
2	RTH	**Termination input** for CANH
3	RO	**Reset output**; open drain output; integrated pull up; active LOW
4	CANL	**CAN-L bus line**; LOW in dominant state
5	RTL	**Termination input** for CANL
6, 7, 8, 9, 20, 21, 22, 23	GND	**Ground**; to reduce thermal resistance place cooling areas on PCB close to this pins.
10	OUTH1	**High side output 1**; controlled via PWM input and/or SPI input, short circuit protected
11	OUTL1	**Low side output 1**; SPI controlled, with active zener
12	OUTL2	**Low side output 2**; SPI controlled, with active zener
13	OUTH2	**High side output 2**; SPI controlled
14	OUTH3	**High side output 3**; SPI controlled, in cyclic wake mode controlled by an internal autotiming function
15	V_S	**Power supply**; block to GND directly at the IC with ceramic capacitor
16	CSN	**SPI interface chip select not**; CSN is an active low input; serial communication is enabled by pulling the CSN terminal LOW; CSN input should only be transitioned when CLK is LOW; CSN has an internal active pull up and requires CMOS logic level inputs
17	DO	**SPI interface data out**; this tristate output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a LOW on Chip-Select-Not (CSN); see **Table 7** for diagnosis protocol
18	DI	**SPI interface data in**; receives serial data from the control device; serial data transmitted to DI is a 16 bit control word with the Least Significant Bit (LSB) being transferred first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **Table 6** for input data protocol

4 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
19	CLK	**SPI interface clock input**; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs
24	V_{CC}	**Output voltage regulator**; 5V logic supply, block to GND with an 100nF external ceramic capacitor directly at the IC + external capacitor $C_Q \geq 22\ \mu F$
25	RxD	**CAN Receive data output;** integrated pull up, LOW: bus becomes dominant, HIGH: bus becomes recessive
26	TxD	**CAN Transmit data input;** integrated pull up, LOW: bus becomes dominant, HIGH: bus becomes recessive
27	PWM	**Pulse Width Modulation control**; for high side switch 1
28	WK	**Wake-Up input**; for detection of external wake-up events within cyclic wake mode, active LOW

5 Functional Block Diagram

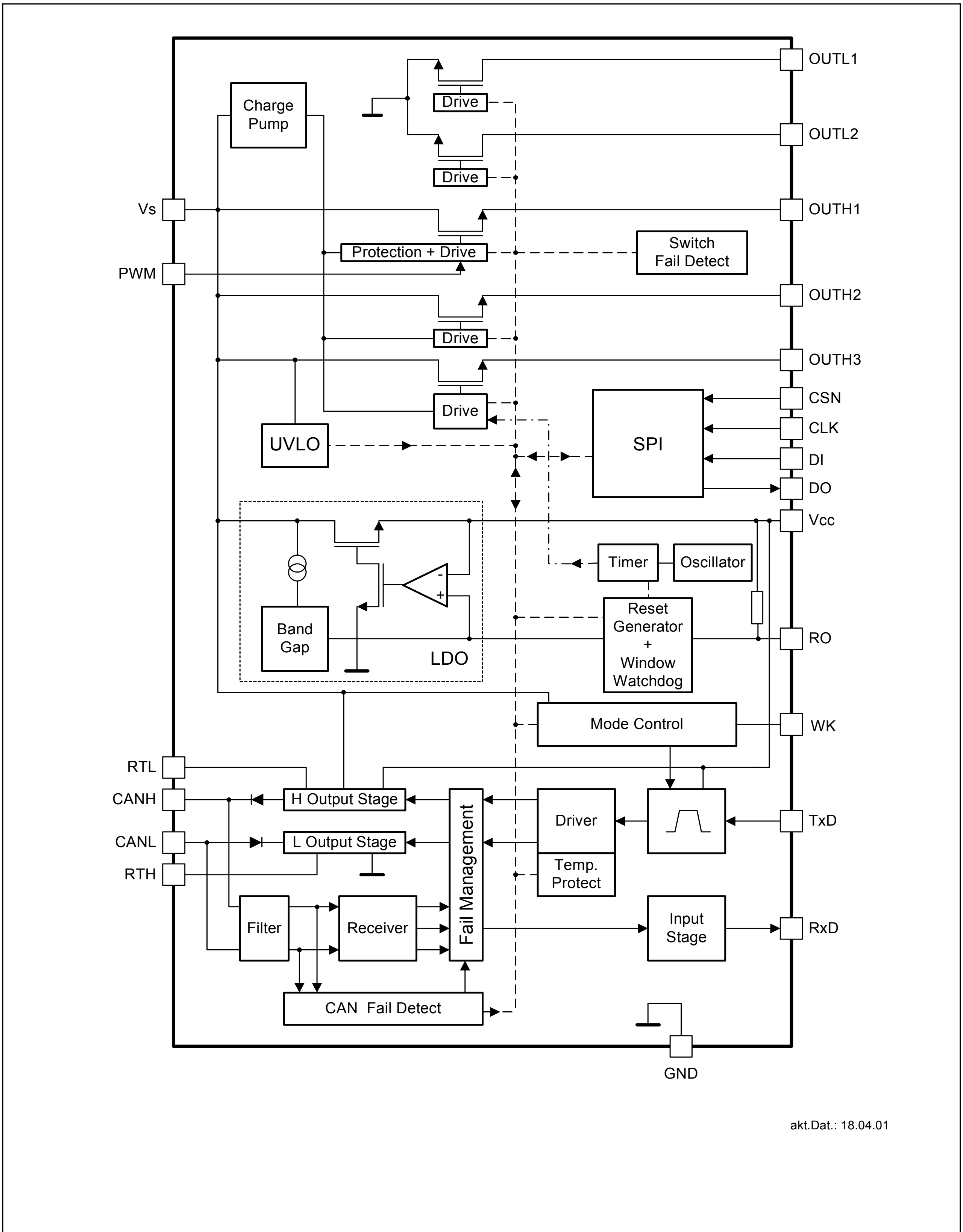


Figure 2 TLE 6266 G Functional Block Diagram

6 Circuit Description

The TLE 6266 G is a monolithic IC, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a SPI interface to control and monitor the IC. Further there are three high side switches, two low side switches, a window watchdog circuit and a reset circuit integrated. **Figure 2** shows the block diagram of the TLE 6266.

The CAN transceiver TLE 6266 works as the interface between the CAN protocol controller and the physical CAN bus-lines. **Figure 3** shows the principle configuration of a CAN network.

In normal operation mode a differential signal is transmitted/received. When bus wiring failures are detected the device automatically switches in a dedicated single-wire mode to maintain communication.

While no data is transferred, the power consumption can be minimized by multiple low power operation modes. Further a receive-only mode is implemented that allows a separate CAN node diagnosis.

To reduce radiated electromagnetic emission (EME) the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (one of the bus lines is affected by a bus line failure) the EME performance of the system is degraded from the differential mode.

In case the transmission data input TxD is permanently dominant, both, the CANH and CANL transmitting stage are disabled after a certain delay time. This is necessary to prevent the bus from being blocked by a defective protocol unit or short to GND at the TxD input.

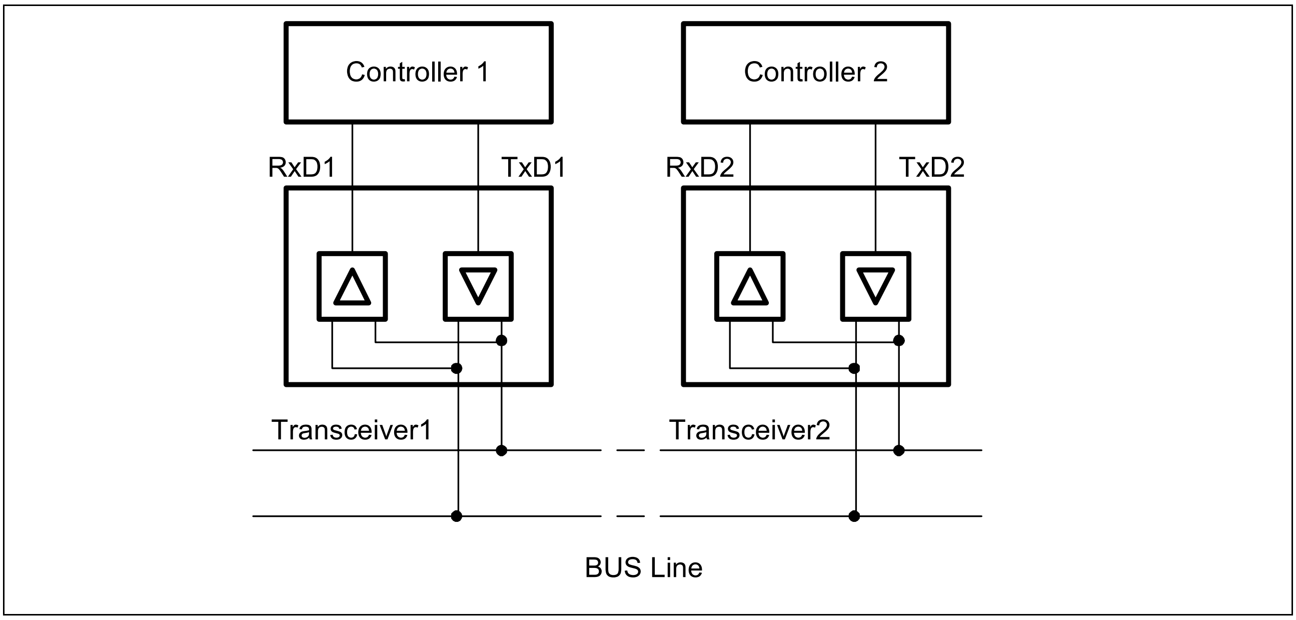


Figure 3 CAN Network Example

6.1 Operation Modes

The TLE 6266 offers four different operation modes (see **Figure 4**) that are controlled via the SPI input bits 9,10 (mode bits M0,M1) as shown in **Table 1**: the normal operation mode, the receive-only mode, the V_{bat} stand-by mode and the cyclic wake operation mode. The cyclic wake mode itself is subdivided into two modes: the cyclic HS OFF and the cyclic HS ON mode. Both, cyclic wake and V_{bat} stand-by are designed for periods that do not require communication on the CAN-Bus but offer a low power mode, especially the cyclic wake mode (<70µA). There is also a so called 3V supervisor feature, that monitors if the output voltage V_{CC} has fallen below the supervisor threshold V_{ST}. This feature can be activated in every operation mode via SPI (see **6.7**).

Table 1 Operation modes bit settings

	Mode Bit M1 (SPI Bit 10)	**Mode Bit M0 (SPI Bit 9)**
Normal operation	1	1
RxD only	1	0
Cyclic Wake	0	1
V_{bat} stand-by	0	0

Normal operation mode

The normal operation mode is designed to receive and transmit data messages.

Cyclic Wake Modes

In the cyclic wake operation mode the lowest power consumption is achieved. This mode consists of two states, the Cyclic HS ON and the Cyclic HS OFF mode.

In the **HS OFF state**, almost all functions of the IC are deactivated. Only the wake-up input, the oscillator and the Power On Reset circuit are activated. The voltage regulator is switched on as soon as the voltage at V_{CC} falls below the load-threshold to charge an external capacitor for 1ms (see **Figure 5**). When the nominal voltage level is reached again, the voltage regulator is automatically deactivated to minimize the current consumption. The oscillator is used to realize the HS3-autotiming function that allows the HS3-switch to be automatically enabled after the programed time (via SPI input bits 12,13 see **Table 2**). The CANL line is pulled-up to the battery supply voltage via the RTL output in this mode.

There are three possibilities to enter the cyclic HS ON mode from the HS OFF mode:

- the cyclic wake time function
- a falling edge at the wake-up pin
- a CAN bus wake

In the **HS ON state** all deactivated functions from the HS-OFF mode are activated. A wake-up via CAN bus sets the RxD output to LOW. In the HS ON state, a long open window is started. If there is no valid trigger or transition into the HS OFF state during this time, a watchdog reset is activated. A correct trigger signal on the PWM Pin causes a transition into the cyclic HS OFF state. This behavior grants the watchdog feature also in the cyclic wake mode, but with a longer period of time. This is called the ´failsafe PWM feature´.

Table 2 SPI Bit settings for the cyclic wake period

Input Bit 13	Input Bit12	Period
0	0	48ms
0	1	96ms
1	0	192ms
1	1	no cyclic wake-up

V_{bat} stand-by mode

In the V_{bat} stand-by mode the voltage regulator remains active. The CANL line is pulled-up to battery supply voltage via the RTL output. Wake-up requests via the Wake-Up pin or the bus lines are immediately reported to the microcontroller by setting RxD=LOW. A power-on condition (V_{bat} pin is supplied) or a watchdog reset, automatically switches the TLE 6266 to V_{bat} stand-by mode. Also if the supply voltage drops below the specified limits (undervoltage reset), the transceiver is automatically switched to V_{bat} stand-by mode or power down mode, respectively.

RxD-only mode

In the receive-only mode data on the CAN-bus are transferred to the RxD output, but both output stages, CANH as well as CANL are disabled. This means that data at the TxD input are not transmitted to the CAN bus. The CANL line is pulled-up to 5V via the RTL output. This mode is useful in combination to a dedicated network-management software that allows separate diagnosis for all nodes.

Table 3 shows an overview about the different features of the TLE 6266 and their activation status in all operation modes.

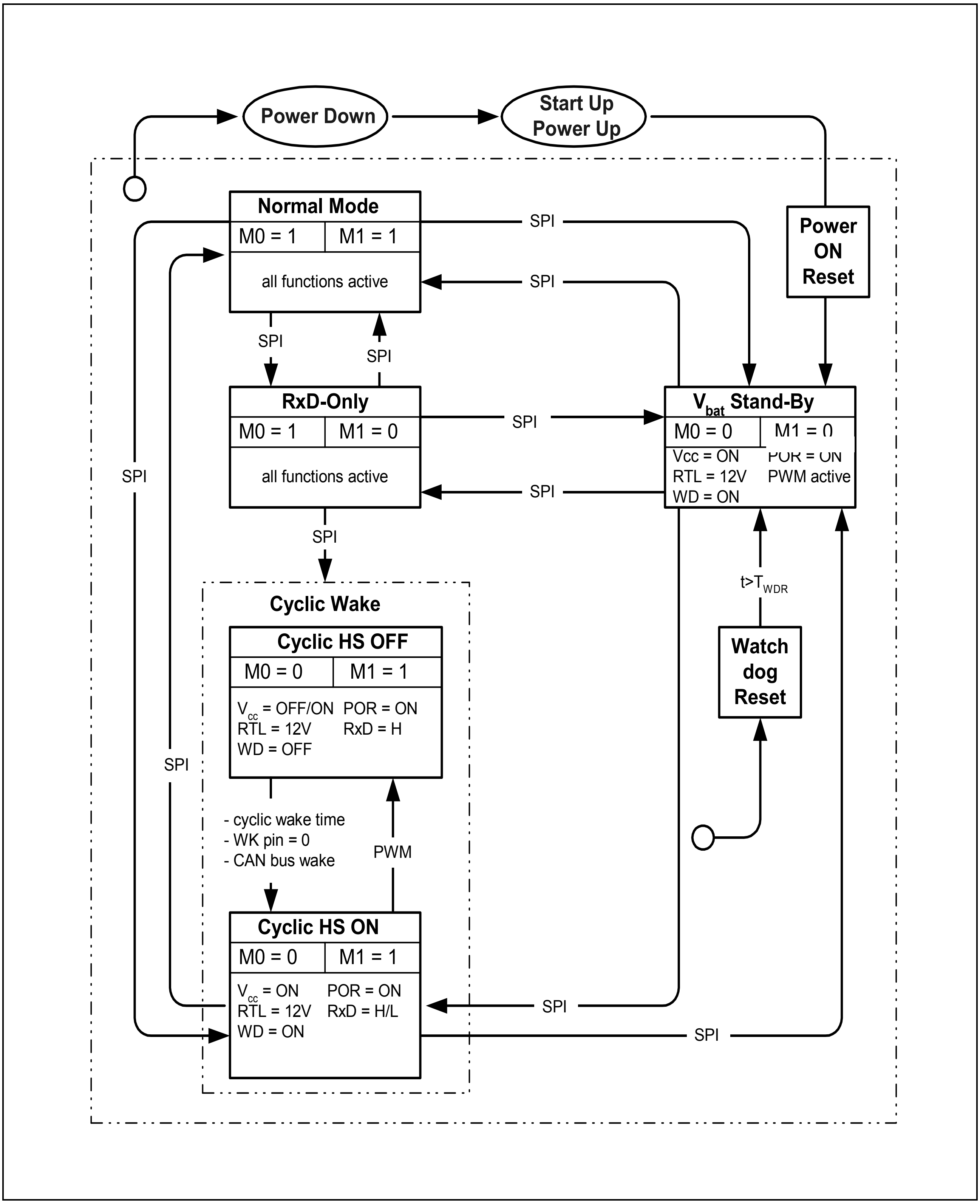


Figure 4 State Diagram

Table 3 Operation mode table

Feature	Normal mode	RxD stand-by mode	V_{bat} stand-by mode	Cyclic Wake HS ON	Cyclic Wake HS OFF
LDO	ON	ON	ON	ON	OFF/ON
Reset	ON	ON	ON	ON	ON
Watchdog	ON	ON	ON	ON	OFF
SPI	ON	ON	ON	ON	OFF
Oscillator	ON	ON	ON	ON	ON
CAN transmit	ON	OFF	OFF	OFF	OFF
CAN receive	ON	ON	OFF	OFF	OFF
OUTHS 1[1) 2) 3)]	ON	ON	ON	OFF	OFF
OUTHS 2[1) 3)]	ON	ON	ON	OFF	OFF
OUTHS 3[1) 3)]	ON	ON	ON	OFF	OFF
OUTHS 3 cycl. HS ON[1) 3)]	OFF	OFF	OFF	ON	OFF
OUTLS 1[1) 4)]	ON	ON	ON	OFF	OFF
OUTLS 2[1) 4)]	ON	ON	ON	OFF	OFF
OUT HS 3 Timebase-Test	ON	ON	ON	OFF	OFF
Failsafe PWM	OFF	OFF	OFF	ON	OFF
3V Supervisor [1)]	1)	1)	1)	1)	1)
RTL output	switched to Vcc	switched to Vcc	switched to Vs	switched to Vs	switched to Vs
RxD output	L = bus dominant; H = bus recessive	L = bus dominant; H = bus recessive	active low wake-up interrupt	active low wake-up interrupt	active low wake-up interrupt

[1)] only active when selected via SPI

[2)] also active when driven via the PWM input

[3)] automatically disabled when a reset occures

[4)] automatically disabled when a reset resp. watchdog reset occures

6.2 Bus Failure Management

Normally a differential signal is transmitted resp. received. When a bus wiring failure (see **Table 4**) is detected the device automatically switches to a dedicated CANH or CANL single-wire mode to maintain the communication if necessary. Therefore it is equipped with one differential receiver and four single ended comparators (two for each bus line).

To avoid false triggering by external RF influences, the single wire modes are activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay.

The bus failures are monitored via the diagnosis protocoll of the SPI. Therefore it is possible to distinguish 6 CAN bus failures or failure groups on the SPI output bits 8 to 13 (see **Table 4** and **5**). The failures are reported until transmission of the next CAN word begins.

The differential receiver threshold is set to typ. -2.5V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2, 3a and 4 with a noise margin as high as possible.

When one of the bus failures 3, 5, 6, 6a, and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and output stage. Simultaneously the multiplexing output of the receiver circuit is switched to the unaffected single ended comparator.

Table 4 CAN bus line failure cases (according to ISO 11519-2)

Failure #	**Failure Description**
1	CANL line interrupted
2	CANH line interrupted
3	CANL shorted to V_{bat}, CANL > 7.2 V
3a (no ISO failure)	CANL shorted to V_{CC}; 3.2 V < CANL < 7.2 V
4	CANH shorted to GND
5	CANL shorted to GND
6	CANH shorted to V_{bat}; CANH > 7.2 V
6a (no ISO failure)	CANH shorted to V_{CC}; 1.8 V < CANH < 7.2 V
7	CANL shorted to CANH

To reduce radiated electromagnetic emission (EME) the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (one of the bus lines is affected by a bus line failure) the EME performance of the system is degraded from the differential mode.

In case the transmission data input TxD is permanently dominant, both, the CANH and CANL transmitting stage are disabled after a certain delay time t_{TxD}. This is necessary to prevent the bus from being blocked by a defective protocol unit or short to GND at the TxD input.

The CANH and CANL pins are protected against electrical transients which may occur in the severe conditions of automotive environments.

In order to protect the transceiver output stages from being damaged by shorts on the bus lines, current limiting circuits are integrated. The CANL and CANH output stage respectively are protected by an additional temperature sensor, that disables them as soon as the junction temperature exceeds the maximum value. In the temperature shutdown condition of the CAN output stages receiving messages from the bus lines is still possible. A thermal shutdown of the CAN-transceiver circuit is monitored via the SPI output bit 15.

Table 5 SPI output bits for bus failure diagnosis

OBIT	Bus Failure
13	CAN Failure 2 and 4
12	CAN Failure 1 and 3a
11	CAN Failure 6
10	CAN Failure 6a
9	CAN Failure 5 and 7
8	CAN Failure 3
0	CAN Bus Failure

6.3 Low Dropout Voltage Regulator

The TLE6266 is able to drive external 5V loads up to 45 mA. Its output voltage tolerance is less than ± 2%. In addition the regulator circuit drives the internal loads like the CAN-transceiver circuit. In the cyclic wake operation mode the voltage regulator is switched on and off by a control mechanism (see **Figure 5**).

The current limitation of the LDO is set to typ. 180mA, to grant that the external capacitor can be charged quickly. In normal operating mode the external current should be less then 45mA. This has to guaranteed by the system architecture.

An external reverse current protection is recommended to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors $C_{VCC} \geq 100$ nF. Nevertheless a lot of applications require a much larger output capacitance to buffer the output voltage in case of low input voltage or negative transients. Furthermore the due function of e.g. the reset and 3V-supervisor circuit are supported by a larger output capacitance because of their reaction times. Therefore a output capacitance $C_{VCC} \geq 22$ µF is recommended.

During the cyclic wake HS OFF mode, the LDO is switched on and off, depending on the output voltage level. **Figure 5** shows a detailed flowchart of the V_{cc} control loop and also a graph of the V_{cc} voltage and the thresholds in this mode.

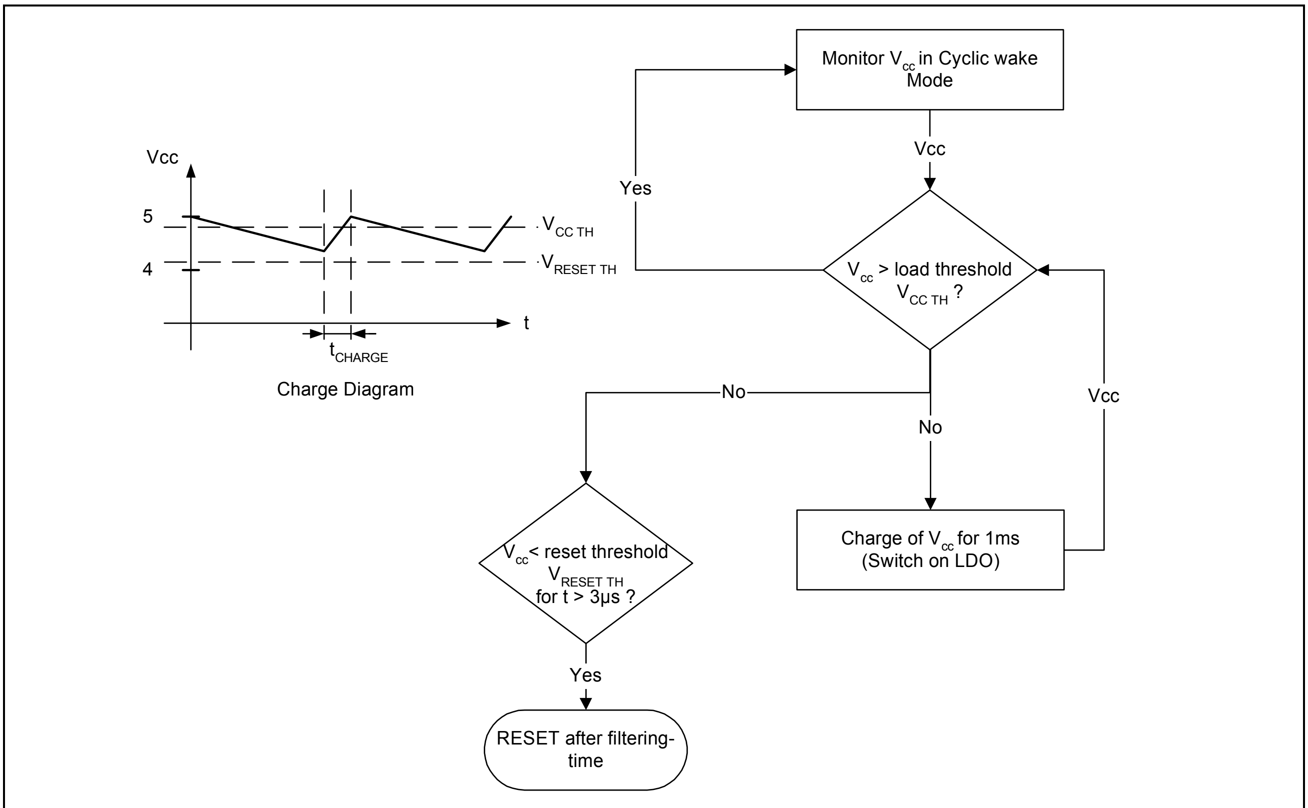


Figure 5 Cyclic wake flowchart for the LDO

6.4 SPI (serial peripheral interface)

The 16-bit wide programming word or input word (see **Table 6**) is read in via the data input DI, and this is synchronized with the clock input CLK supplied by the µC. The diagnosis word appears synchronously at the data output DO (see **Table 7**).

The transmission cycle begins when the chip is selected by the chip select not input CSN (H to L). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus for other usage.

The SPI output bit 0 for CAN bus wiring failure can be read out without SPI transmission directly via the CSN pin (CSN=LOW). A transition of the CSN pin signal from LOW to HIGH resets the SPI diagnosis bit 0.

The TLE 6266 offers a feature to monitor the SPI clock signal (CLK pin) during the cyclic wake mode. If there are edges on this signal, the IC performs a reset and the RO pin is set to LOW. This feature is activated if the CSN pin is set to HIGH.

For details of the SPI timing please refer to **Figure 7 to 11**.

Table 6 SPI Input Data Protocol

IBIT	Input Data
15	Disable 3V Reset Comparator
14	not used
13	Cyclic Wake Time Bit2
12	Cyclic Wake Time Bit1
11	PWM Enable HS1
10	Mode 1
9	Mode 0
8	not used
7	Supervisor Enable
6	LS-Switch 2
5	LS-Switch 1
4	Timebase Test
3	HS-Switch 3
2	HS-Switch 2
1	HS-Switch 1
0	Watchdog Trigger

H=ON
L=OFF

Table 7 SPI Output Data Protocol

OBIT	Output Data
15	Thermal Shutdown Transceiver
14	Thermal Shutdown Switches
13	CAN Failure 2 and 4
12	CAN Failure 1 and 3a
11	CAN Failure 6
10	CAN Failure 6a
9	CAN Failure 6a, 5 and 7
8	CAN Failure 3
7	3V Supervisor (Vcc < 3V)
6	Status LS2
5	Status LS1
4	Temperature Prewarning for all Switches
3	Vs Undervoltage Lockout
2	Window Watchdog Reset
1	Overcurrent HS1
0	CAN Bus Failure

H=ON
L=OFF

6.5 Oscillator

The TLE 6266 has an internal oscillator +/-15% accuracy. The frequency of the oscillator can be measured within the normal, the V_{bat} stand-by and the RxD-only mode. This is a timebase test, activated via SPI input bit 3 and 4. During this test, the HS3-switch will be activated cyclically.

6.6 Window Watchdog and Reset

When the output voltage V_{CC} exceeds the reset threshold voltage V_{RT} the reset output RO is switched HIGH after a delay time t_{RD}. This is necessary for a defined start of the microcontroller when the application is switched on. As soon as an under-voltage condition of the output voltage ($V_{CC} < V_{RT}$) appears, the reset output RO is switched LOW again. The LOW signal is guaranteed down to an output voltage $V_{CC} \geq 1V$. Please refer to **Figure 16**, reset timing diagram.

After the delayed reset (LOW to HIGH transition of RO) the window watchdog circuit is started by opening a long open window. The long open window allows the microcontroller to run his set-up and to trigger the watchdog via the SPI afterwards. Within the long open window period a watchdog trigger is alternating detected as a "rising" or "falling edge" by sampling a HIGH on the SPI input bit 0. The trigger is accepted when the CSN input becomes HIGH after the transmission of the SPI word. After each reset as well as after a power on condition the default value of the SPI input bit 0 is LOW.

After every reset condition (watchdog reset, undervoltage reset) as well as a transition in the cyclic wake mode from HS OFF to HS ON, the watchdog starts the long open window.

A correct watchdog trigger immediately results in starting the window watchdog by opening the closed window followed by the open window (see **Figure 14**). From now on the microcontroller has to service the watchdog trigger by inverting the SPI input bit 0 alternating. The "negative" or "positive" edge has to meet the open window time. A correct watchdog service immediately results in starting the next closed window. Please refer to **Figure 15**, watchdog timing diagram.

If the trigger signal does not meet the open window a watchdog reset is created by setting the reset output RO low for t_{WDR}. Then the watchdog starts again by opening the long open window. In addition, the SPI output bit 2 is set HIGH until the next successful watchdog trigger, to monitor a watchdog reset. SPI output bit 2 is also HIGH until the watchdog is correctly triggered after power-up/start-up. For fail safe reasons the TLE6266 is automatically switched in V_{bat} stand-by mode if a watchdog trigger failure occurs.

In the cyclic wake HS OFF mode, the watchdog circuit is automatically disabled.Both, the undervoltage reset and the watchdog reset set all SPI input bits LOW.

6.7 3V-Supervisor

If the output voltage falls below the 3V-supervisor threshold V_{ST}, an internal flip-flop is set LOW. The SPI output bit 7 monitors this. In normal operation this flip-flop has to be activated via the SPI input bit 7. This feature is useful e.g. to monitor that the RAM data of the microcontroller might be damaged or the application is connected to V_S the first time.

The 3V supervisor uses a comparator to monitor the voltage. Additional, there is a possibility to disable this comparator in order to reduce the current consumption. To do this, set SPI input bit 15 first and in the next step set SPI input bit 7.

6.8 High Side Switch 1

The high side output OUTH1 is able to switch loads up to 250 mA. Its on-resistance is 1.0 Ω typ. @ 25°C. This switch can be controlled either via the PWM input or the SPI input bit 1. When the input PWM is used it has to be enabled by setting the SPI input bit 11 HIGH. In case of both control inputs being active the PWM signal is masked by the SPI signal (see **Figure 12**, High Side Switch 1 Timing Diagram).

The SPI output bit 14 monitors a thermal shutdown of the switches, whereas output bit 4 flags a thermal prewarning. By this, the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. Further OUTH1 is protected against short circuit and overload. The SPI output bit 1 indicates an overload of OUTH1. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI output bit 3. Moreover the switches are disabled when a reset occurs.

6.9 High Side Switch 2

The high side output OUTH2 is able to switch loads up to 250 mA. Its on-resistance is 1.0 Ω typ. @ 25°C. This switch is controlled via the SPI input bit 2.

The SPI output bit 14 monitors a thermal shutdown of the switches, whereas output bit 4 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI output bit 3. Moreover the switches are disabled when a reset occurs.

6.10 High Side Switch 3

The high side output OUTH3 is able to switch loads up to 250 mA. Its ON-resistance is 1.0 Ω typ. @ 25°C. This switch is controlled via the SPI input bits 3 and 4. To supply external wake-up circuits in low power mode (cyclic wake - HS ON mode or Vbat-stand-by mode), the output OUTH3 is periodically activated by entering the cyclic wake mode. The autotiming period is programable via SPI (see **Table 2**).This has to be done, to minimize the current consumption depending on the cyclic wake time (see **Figure 17**).

In the cyclic wake mode, the PWM signal is used to switches HS3 from the cyclic HS ON to the cyclic HS OFF state, if correctly triggered within the long open window (see **Table 13**). This is called the ´fail-safe feature´

The SPI output bit 14 monitors a thermal shutdown of the switches, whereas output bit 4 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI output bit 3. Moreover the switches are disabled when a reset occurs.

6.11 Low Side Switches 1 & 2

The two low side outputs OUTL1 and OUTL2 are able to switch loads up to 100 mA. Their on-resistance is 1.5 Ω typ. @ 25°C. This switches are controlled via the SPI input bits 5 and 6. In case of high inrush currents a built in zener circuit (typ. 37 V) activates the switches to protect them.

The SPI diagnosis bit 14 monitors a thermal shutdown of the switches, whereas bit 4 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6266 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. The SPI output bits 5/6 are giving a feedback about current status of OUTL1/OUTL2. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI diagnosis bit 3. In addition the outputs OUTL1 and OUTL2 are disabled when a reset occurs. After the second correct triggered watchdog, the switches are released for usage.

6.12 Wake Up Pin

This pin is used to wake up the TLE 6266 with an external signal from the µC. The feature is active during cyclic HS OFF mode to switch the transceiver into the cyclic HS ON mode before starting up the µC.

6.13 Timebase Test

This test is useful to measure the internal cycle time of the TLE 6266. The µC may use this information to activate special functions or routines (e.g. to switch on/off the LED) after a certain number of cyclic HS ON conditions in the cyclic wake mode, that depends on timing.

To measure the internal cyclic timing, the SPI input bit 4 has to be set HIGH. Then the HS3 switch is automatically enabled for 3 times during the closed window of the watchdog (see **Figure 6**).

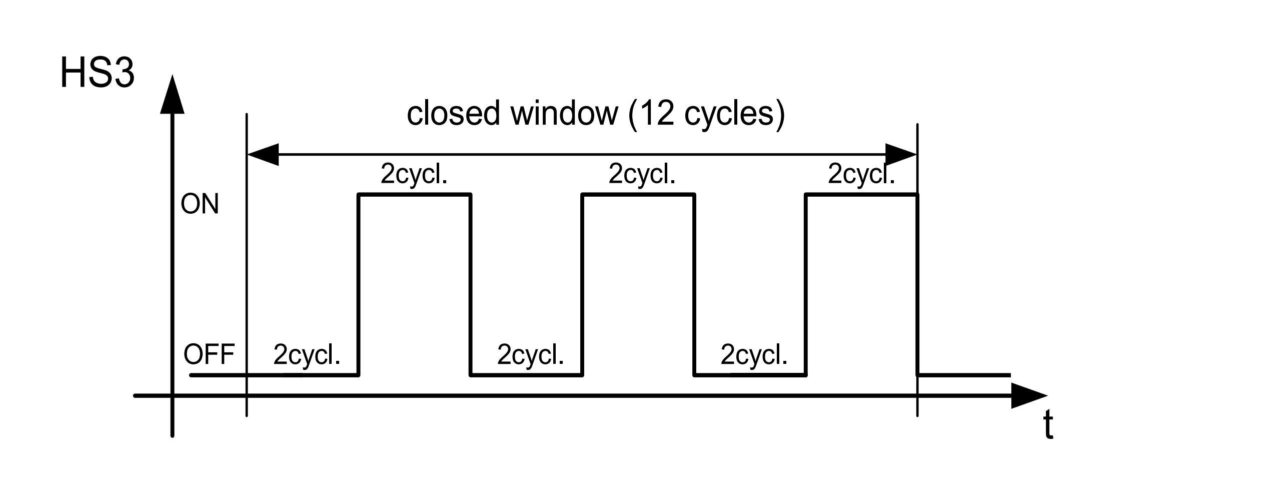


Figure 6 Timebase Test Diagram

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	-0.3	28	V	
Supply voltage	V_S	-0.3	40	V	t_p< 0.5s; t_p/T < 0.1
Regulator output voltage	V_{CC}	-0.3	5.5	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	-10	28	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	-40	40	V	V_S >0 V t_p< 0.5s; t_p/T < 0.1
Transient voltage at CANH and CANL	V_{BUS}	– 150	100	V	see ISO 7637
Logic input voltages (DI, CLK, CSN, WK, PWM, TxD)	V_I	-0.3	V_{CC} +0.3	V	
Logic output voltage (DO, RO, RxD)	$V_{DO/RO/RD}$	-0.3	V_{CC} +0.3	V	
Termination input voltage (RTH, RTL)	$V_{TL\ /TH}$	-0.3	V_S +0.3	V	
Electrostatic discharge voltage at pin CANH, CANL	V_{ESD}	-4000	4000	V	human body model; C = 100pF, R = 1.5kΩ
Electrostatic discharge voltage to any other pin	V_{ESD}	-2000	2000	V	human body model; C = 100pF, R = 1.5kΩ
Currents					
Output current; Vcc	I_{CC}	*	0,2	A	* internally limited
Output current; OUTH1	I_{OUTH1}	*	0.3	A	* internally limited
Output current; OUTH2	I_{OUTH2}	-0.7	0.3	A	t_p< 0.5s; t_p/T < 0.1
Output current; OUTH3	I_{OUTH3}	-0.7	0.3	A	t_p< 0.5s; t_p/T < 0.1
Output current; OUTL1	I_{OUTL1}	-0.2	0.4	A	t_p< 0.5s; t_p/T < 0.1
Output current; OUTL2	I_{OUTL2}	-0.2	0.4	A	t_p< 0.5s; t_p/T < 0.1

7.1 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Temperatures					
Junction temperature	T_j	-40	150	°C	
Storage temperature	T_{stg}	-50	150	°C	

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	27	V	After V_S rising above $V_{UV\ ON}$
Supply voltage slew rate	dV_S/dt	-0.5	5	V/µs	
Supply voltage increasing	V_S	-0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	V_S	-0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (DI, CLK, CSN, PWM, TxD)	V_I	-0.3	V_{CC}	V	
Output current	I_{CC}		45	mA	
Output capacitor	C_{CC}	22		µF	
SPI clock frequency	f_{CLK}	–	1	MHz	
Junction temperature	T_j	-40	150	°C	

Thermal Resistances

Junction pin	$R_{thj\text{-}pin}$	–	25	K/W	measured to pin 7
Junction ambient	$R_{thj\text{-}a}$	–	65	K/W	

Thermal Prewarning and Shutdown (junction temperatures)

Thermal prewarning ON temperature	T_{jPW}	120	170	°C	bit 0 of SPI diagnosis word; hysteresis 30°K (typ.)
Thermal shutdown temp.	T_{jSD}	150	200	°C	hysteresis 30°K (typ.)
Ratio of SD to PW temp.	T_{jSD} / T_{jPW}	1.05	–	–	
Thermal shutdown temp. CAN	T_{jSD}	135	160	°C	hysteresis 10°K (typ.)

7.3 Electrical Characteristics

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current Pin V_S						
Current consumption	I_S	–	8	10	mA	normal mode
Quiescent current $I_{SSB1} = I_S - I_{CC}$	I_{SSB1}	–	75	100	µA	cycl. wake 48ms; V_S=12V; T_j=25°C
Static quiescent current	I_{STAT}	–	–	70	µA	
Voltage Regulator; Pin V_{cc}						
Output voltage	V_{CC}	4.9	5.0	5.1	V	0.1mA < I_{CC}< 30mA
Output voltage	V_{CC}	4.8	5.0	5.5	V	0A < I_{CC} < 100µA
Line regulation	ΔV_{CC}	-20		20	mV	9 V < V_S < 15 V; I_{CC} = 10mA
Load regulation	ΔV_{CC}	-25		25	mV	0.1mA < I_{CC}< 30mA; V_S = 9V
Power supply ripple rejection	$PSRR$		40		dB	V_S < 1 Vss; $C_Q \geq$ 22µF; 100Hz< f <100kHz
Output current limit	I_{CCmax}	155	-	-	mA	1)
Dropvoltage $V_{DR} = V_S - V_{CC}$	V_{DR}		0.15	0.45	V	I_{CC} = 30 mA; see note 1)
Wake-up Input WK						
Input current	I_{IL}	– 3	– 2	– 1	µA	
H-input voltage threshold	V_{IH}	–	–	$0.7 \times V_{CC}$	V	
L-input voltage threshold	V_{IL}	$0.2 \times V_{CC}$	–	–	V	
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	
Input filtering time	t_{IFT}	–	–	3	µs	

1) measured when output voltage V_{CC} dropped 100 mV from the nom. value obtained at 13.5 V inp. voltage V_S

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reset Generator; Pin RO						
Reset threshold voltage	V_{RT}	4.0	4.3	4.65	V	
Reset low output voltage	V_{RO}		0.2	0.4	V	I_{RO} = 1mA ($V_{CC} \geq V_{RT}$) or $V_{CC} \geq$ 1V (I_{RO} = 200 µA)
Reset high output voltage	V_{RO}	4.0		V_{CC}+ 0.1	V	
Reset pull up current	I_{RO}	20	150	500	µA	V_{RO} = 0V
Reset reaction time	t_{RR}	1	3	10	µs	$V_{CC} < V_{RT}$ to RO = L; normal, RxD, stand-by mode
Reset reaction time	t_{RR}	–	–	50	µs	$V_{CC} < V_{RT}$ to RO = L; cyclic wake mode
Reset delay time (16 cyl.)	t_{RD}	6.1	8.1	10.2	ms	
3 V Supervisor; (bit 7 of SPI output word)						
Supervisor threshold voltage	V_{ST}	2.3	2.7	3.1	V	
Supervisor reaction time	t_{SR}	2	8	20	µs	$V_{CC} < V_{ST}$ to diagnosis bit 7 = L
Watchdog Generator						
Watchdog trigger time	t_{WD}	7.6	10	12.3	ms	
Closed window time (12 cyl.)	t_{CW}	4.6	6.1	7.6	ms	
Open window time (20 cyl.)	t_{OW}	7.7	10.2	12.7	ms	
Watchdog reset-puls time (4 cyl.)	t_{WDR}	1.5	2.0	2.6	ms	
Long open window (128 cyl.)	t_{LOW}		65		ms	

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Switches

Under-Voltage Lockout (bit 3 of SPI output word)

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.35	6.00	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.50	4.85	5.20	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$

High Side Output OUTH1; (controlled by PWM or bit 1 of SPI input word)

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Static Drain-Source ON-Resistance; I_{OUTH1} = -0.25 A	$R_{DSON\ H1}$	–	1.0	2.0	Ω	
			1.5	4.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTH1}	-5.0	-3.0	-0.5	V	I_{OUTH1} = – 0.25 A
Clamp diode forward voltage	V_{OUTH1}		0.8	1	V	I_{OUTH1} = 0.25 A
Leakage current	I_{OLH1}	-100	-5	–	µA	V_{OUTH1} = 0 V
Switch ON delay time	t_{dONH1}		10	100	µs	PWM to OUTH1; R_L = 100 Ω
Switch OFF delay time	t_{dOFFH1}		20	100	µs	PWM to OUTH1; R_L = 100 Ω
Overcurrent shutdown threshold	I_{SDH1}	-1.0	-0.6	-0.3	A	
Shutdown delay time	t_{dSDH1}	10	25	50	µs	
Current limit	I_{OCLH1}	-2.0	-1.0	-0.5	A	

PWM Input to control OUTH1; Pin PWM (high active)

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
H-input voltage threshold	V_{IH}	–	–	0.7 × V_{CC}	V	
L-input voltage threshold	V_{IL}	0.2 × V_{CC}	–	–	V	

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	
Pull down current	I_I	5	25	180	µA	$V_I = 0.2 * V_{CC}$
Input capacitance	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V

High Side Output OUTH2; (controlled by bit 2 of SPI input word)

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Static Drain-Source ON-Resistance; I_{OUTH2} = -0.25 A	$R_{DSON\ H2}$	–	1.0	2.0	Ω	
			1.5	4.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTH2}	-5.0	-3.0	-0.5	V	I_{OUTH2} = – 0.25 A
Clamp diode forward voltage	V_{OUTH2}		0.8	1	V	I_{OUTH2} = 0.25 A
Leakage current	I_{OLH1}	-100	-5	–	µA	V_{OUTH2} = 0 V
Switch ON delay time	t_{dONH1}		10	100	µs	CSN high to OUTH2; R_L = 100 Ω
Switch OFF delay time	t_{dOFFH1}		20	100	µs	CSN high to OUTH2; R_L = 100 Ω

High Side Output OUTH3; (controlled by bit 3 and bit 4 of SPI input word)

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Static Drain-Source ON-Resistance; I_{OUTH3} = -0.25 A	$R_{DSON\ H3}$	–	1.0	2.0	Ω	
			1.5	4.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTH3}	-5.0	-3.0	-0.5	V	I_{OUTH3} = – 0.25 A
Clamp diode forward voltage	V_{OUTH3}		0.8	1	V	I_{OUTH3} = 0.25 A
Leakage current	I_{OLH3}	-100	-5	–	µA	V_{OUTH3} = 0 V
Switch ON delay time	t_{dONH3}		10	100	µs	CSN high to OUTH3; R_L = 100 Ω
Switch OFF delay time	t_{dOFFH3}		20	100	µs	CSN high to OUTH3; R_L = 100 Ω

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Low Side Output OUTL1 (bit 5 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTL1} = 0.1 A	$R_{DSON\ L1}$	–	1.5	3.0	Ω	
			2.0	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener clamp voltage	V_{OUTL1}	32	37	42	V	I_{OUTL1} = + 0.1 A
Leakage current	I_{OLL1}			5	µA	V_{OUTL1} =15 V; T_j < 85°C
Switch ON delay time	t_{dONL1}		5	50	µs	CSN high to OUTL1; R_L = 100 Ω
Switch OFF delay time	t_{dOFFL1}		5	50	µs	CSN high to OUTL1; R_L = 100 Ω
Low Side Output OUTL2 (bit 6 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTL2} = 0.1 A	$R_{DSON\ L2}$	–	1.5	3.0	Ω	
			2.0	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener clamp voltage	V_{OUTL2}	32	37	42	V	I_{OUTL2} = + 0.1 A
Leakage current	I_{OLL2}			5	µA	V_{OUTL2} =15 V; T_j < 85°C
Switch ON delay time	t_{dONL2}		5	50	µs	CSN high to OUTL2; R_L = 100 Ω
Switch OFF delay time	t_{dOFFL2}		5	50	µs	CSN high to OUTL2; R_L = 100 Ω
Timebase Test TBT(bit 4 of SPI input word)						
HS3 ON timing	t_{TBON}			2	cycl.	
HS3 OFF timing	t_{TBOFF}			2	cycl.	
# of HS activations for TBT	n_{TBT}		2			

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CAN-Transceiver						
Receiver Output R×D						
HIGH level output voltage	V_{OH}	V_{CC} – 0.9	–	V_{CC}	V	I_0 = – 250µA
LOW level output voltage	V_{OL}	0	–	0.9	V	I_0 = 1.25mA
Transmission Input T×D						
HIGH level input voltage threshold	V_{IH}	0.7 × V_{CC}	–	V_{CC} + 0.3	V	
LOW level input voltage threshold	V_{IL}	-0.3	–	0.3 × V_{CC}	V	
HIGH level input current	I_{IH}	-200	-50	-10	µA	V_i = 4 V
LOW level input current	I_{IL}	-800	-200	-40	µA	V_i = 1 V
Bus Lines CANL, CANH						
Differential receiver recessive-to-dominant threshold voltage	$V_{dRxD(rd)}$	– 2.8	– 2.5	– 2.2	V	V_{CC} = 5.0 V
Differential receiver dominant-to-recessive threshold voltage	$V_{dRxD(dr)}$	– 3.2	– 2.9	– 2.6	V	V_{CC} = 5.0 V
CANH recessive output voltage	$V_{CANH,r}$	0.10	0.15	0.30	V	TxD = V_{CC}; R_{RTH} < 4 kΩ
CANL recessive output voltage	$V_{CANL,r}$	V_{CC} – 0.2	–	–	V	TxD = V_{CC}; R_{RTL} < 4 kΩ
CANH dominant output voltage	$V_{CANH,d}$	V_{CC} – 1.4	V_{CC} – 1.0	V_{CC}	V	TxD = 0 V; I_{CANH} = – 40 mA

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CANL dominant output voltage	$V_{CANL,d}$	–	1.0	1.4	V	TxD = 0 V; I_{CANL} = 40 mA
CANH output current	I_{CANH}	– 110	– 80	– 50	mA	V_{CANH} = 0 V; TxD = 0 V
		– 5	0	5	µA	cycl. wake mode; V_{CANH} = 12 V
CANL output current	I_{CANL}	50	80	110	mA	V_{CANL} = 5 V; TxD = 0 V
		– 5	0	5	µA	cycl. wake mode; V_{CANL} = 0 V; V_S = 12 V
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{det(th)}$	6.5	7.3	8.0	V	
Voltage detection threshold for short-circuit to battery voltage on CANH	$V_{det(th)}$	V_{BAT} – 2.5	V_{BAT} – 2	V_{BAT} – 1	V	stand-by/ cycl. wake mode
CANH wake-up voltage threshold	$V_{CANH,wu}$	1.2	1.9	2.7	V	
CANL wake-up voltage threshold	$V_{CANL,wu}$	2.2	3.1	3.9	V	
Wake-up voltage threshold hysteresis	ΔV_{wu}	0.2	–	–	V	$\Delta V_{wu} = V_{CANL,wu} - V_{CANH,wu}$
CANH single-ended receiver threshold	V_{CANH}	1.6	2.1	2.6	V	failure cases 3, 5 and 7
CANL single-ended receiver threshold	V_{CANL}	2.4	2.9	3.4	V	failure case 6 and 6a
CANL leakage current	$I_{CANL,lk}$	– 5	0	5	µA	V_{CC} = 0 V; V_S = 0 V; V_{CANL} = 12 V; T_j < 85 °C
CANH leakage current	$I_{CANH,lk}$	– 5	0	5	µA	V_{CC} = 0 V; V_S = 0 V; V_{CANH} = 5 V; T_j < 85 °C

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Termination Outputs RTL, RTH						
RTL to V_{CC} switch-on resistance	R_{RTL}	–	40	95	Ω	I_o = – 10 mA
RTL output voltage	V_{oRTL}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	$\lvert I_o \rvert$ < 1 mA;
RTL to BAT switch series resistance	R_{oRTL}	5	15	30	kΩ	V_{BAT} stand-by or cycl. wake mode
RTH to ground switch-on resistance	R_{RTH}	–	40	95	Ω	I_o = 10 mA
RTH output voltage	V_{oRTH}	–	0.7	1.0	V	I_o = 1 mA; low power mode
RTH pull-down current	$I_{RTH,pd}$	40	75	120	µA	failure cases 6 and 6a
RTL pull-up current	$I_{RTL,pu}$	– 120	– 75	– 40	µA	failure cases 3, 3a, 5 and 7
RTH leakage current	$I_{RTH,lk}$	– 5	0	5	µA	V_{CC} = 0 V; V_S = 0 V; V_{RTH} = 5 V; T_j < 85 °C
RTL leakage current	$I_{RTL,lk}$	– 5	0	5	mA	V_{CC} = 0 V; V_S = 0 V; V_{RTL} = 12 V; T_j < 85 °C
CAN-Transceiver						
Dynamic Characteristics						
CANH and CANL bus output transition time recessive-to-dominant	t_{rd}	0.6	1.2	2.1	µs	10% to 90%; C_1 = 10 nF; C_2 = 0; R_1 = 100 Ω
CANH and CANL bus output transition time dominant-to-recessive	t_{dr}	0.3	0.6	1.3	µs	10% to 90%; C_1 = 1 nF; C_2 = 0; R_1 = 100 Ω

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Minimum dominant time for wake-up on CANL or CANH	$t_{wu(min)}$	8	22	38	µs	stand-by mode; V_S = 12 V
Minimum wake-up time on pin WK (wake-up)	$t_{WK(min)}$	15	25	50	µs	Low power mode; V_S = 12 V
Failure cases 3 and 6 detection time	t_{fail}	10	45	80	µs	normal operating mode
Failure case 6a detection time		2	4	8	ms	normal operating mode
Failure cases 5, 6, 6a and 7 recovery time		10	45	80	µs	normal operating mode
Failure cases 3 recovery time		250	500	750	µs	normal operating mode
Failure cases 5 and 7 detection time		1.0	2.0	4.0	ms	normal operating mode
Failure cases 5 detection time		0.4	1.0	2.4	ms	stand-by mode; V_S = 12 V
Failure cases 6, 6a and 7 detection time		0.8	4.0	8.0	ms	stand-by mode; V_S = 12 V
Failure cases 5, 6, 6a and 7 recovery time		–	2	–	µs	stand-by mode; V_S = 12 V
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{PD(L)}$	–	1.5	2.1	µs	C_1 = 100 pF; C_2 = 0; R_1 = 100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	1.7	2.4	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.8	2.5	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	2.0	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 =100 Ω; bus failure cases 3, 5, 6, 6a and 7

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Propagation delay TxD-to-RxD HIGH (dominanat to recessive)	$t_{PD(H)}$	–	1.2	2.0	µs	C_1 = 100 pF; C_2 = 0; R_1 =100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	2.5	3.5	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.0	2.1	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	1.5	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
Minimum hold time to go sleep command	$t_{h(min)}$	15	25	50	µs	
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a and 4 detection	n_e	–	4	–	–	normal operating mode
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a and 4 recovery		–	2	–	–	
TxD permanent dominant disable time	t_{TxD}	1.0	2.0	3.5	ms	normal mode

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
SPI-Interface						
Logic Inputs DI and CSN						
H-input voltage threshold	V_{IH}	–	–	0.7 × V_{CC}	V	
L-input voltage threshold	V_{IL}	0.2 × V_{CC}	–	–	V	
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	
Pull up current at pin CSN	I_{ICSN}	-100	-25	-5	µA	V_{CSN} = 0.7 × V_{CC}
Pull down current at pin DI	$I_{ICLK/DI}$	5	25	100	µA	V_{DI} = 0.2 × V_{CC}
Input capacitance at pin CSN, DI	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V
Logic Output DO						
H-output voltage level	V_{DOH}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	I_{DOH} = 1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA
Tri-state leakage current	I_{DOLK}	-10	–	10	µA	V_{CSN} = V_{CC} 0 V < V_{DO} < V_{CC}
Tri-state input capacitance	C_{DO}	–	10	15	pF	V_{CSN} = V_{CC} 0 V < V_{CC} < 5.25 V
Data Input Timing						
Clock period	t_{pCLK}	1000	–	–	ns	
Clock high time	t_{CLKH}	500	–	–	ns	
Clock low time	t_{CLKL}	500	–	–	ns	
Clock low before CSN low	t_{bef}	500	–	–	ns	
CSN setup time	t_{lead}	500	–	–	ns	

7.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CLK setup time	t_{lag}	500	–	–	ns	
Clock low after CSN high	t_{beh}	500	–	–	ns	
DI setup time	t_{DISU}	250	–	–	ns	
DI hold time	t_{DIHO}	250	–	–	ns	
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	200	ns	
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	200	ns	
Data Output Timing						
DO rise time	t_{rDO}	–	50	100	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	50	100	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	250	ns	low impedance
DO disable time	t_{DISDO}	–	–	250	ns	high impedance
DO valid time	t_{VADO}	–	100	250	ns	V_{DO} < 0.2 V_{CC}; V_{DO} > 0.7V_{CC}; C_L = 100 pF

8 Timing Diagrams

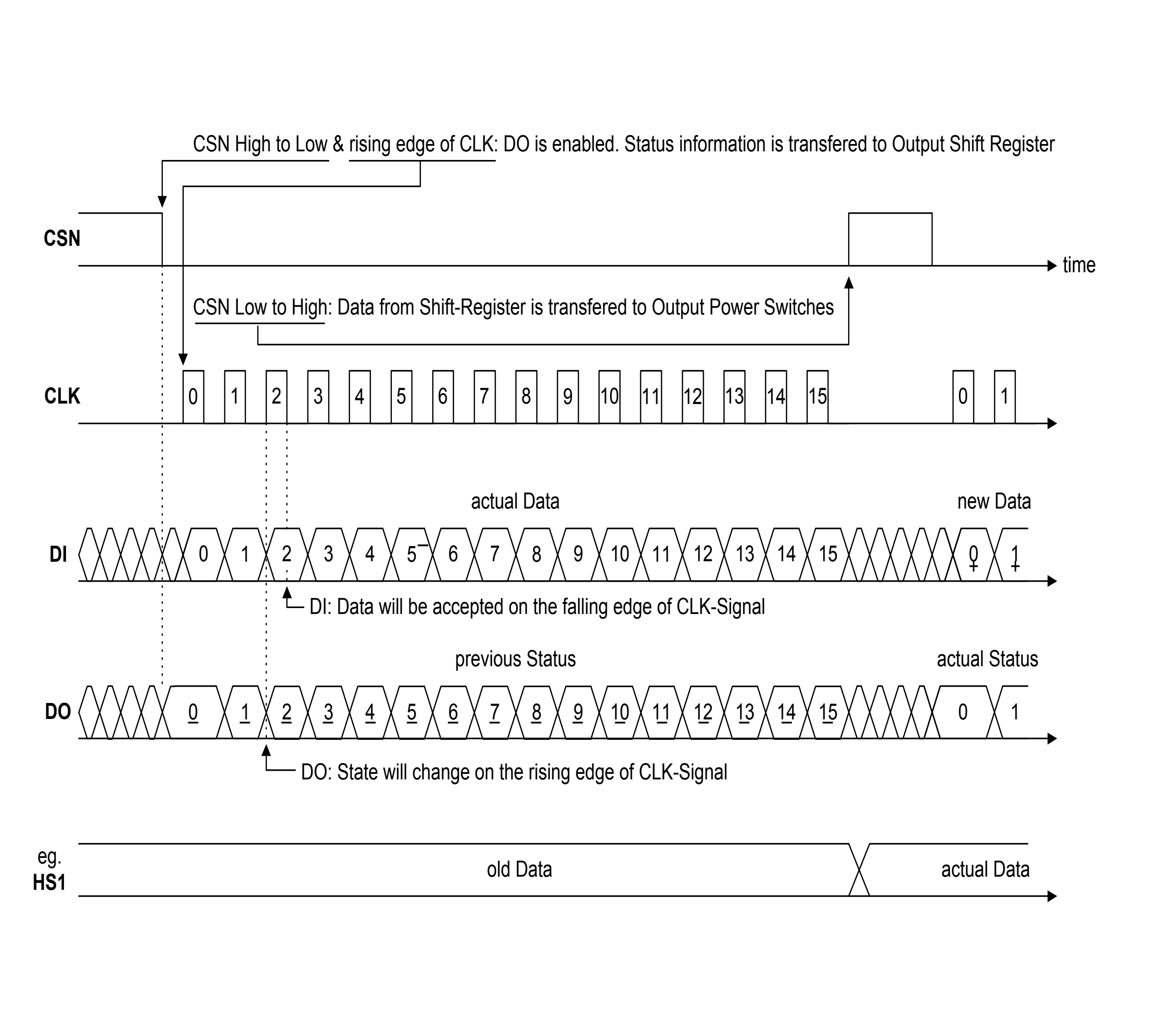


Figure 7 Data Transfer Timing

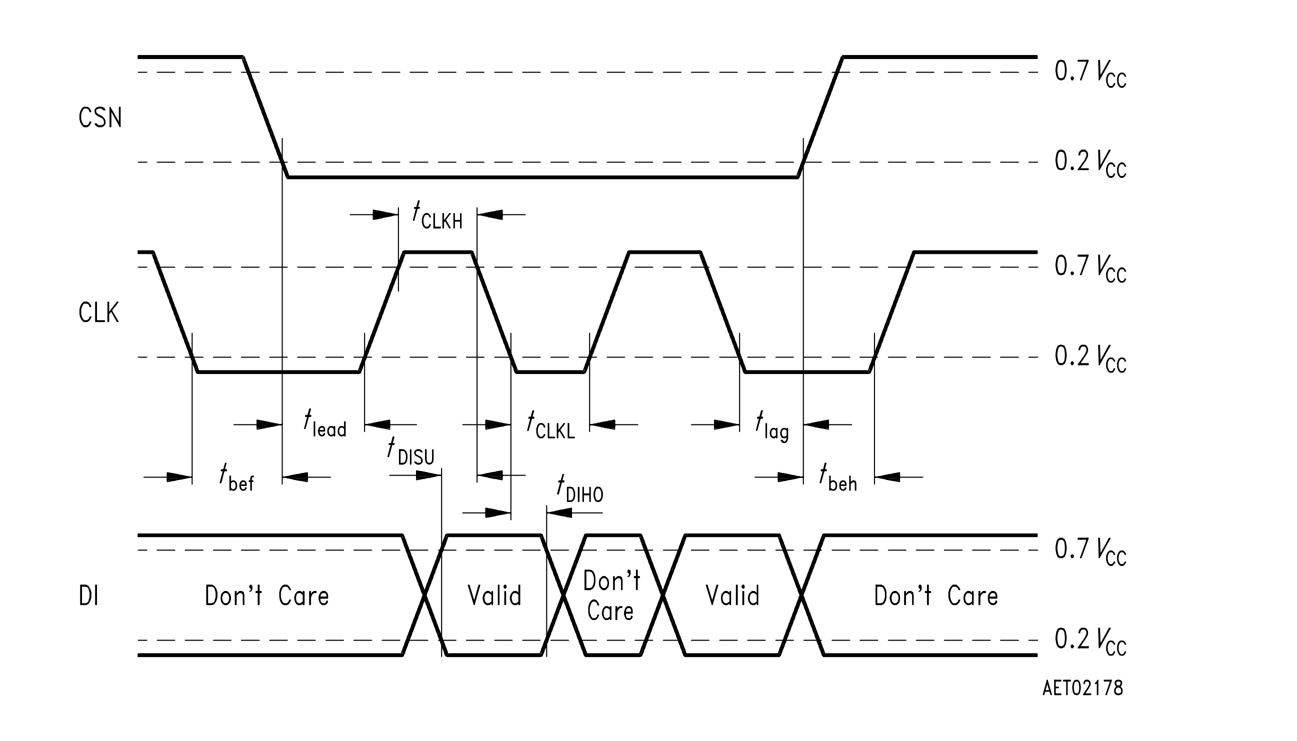


Figure 8 SPI-Input Timing

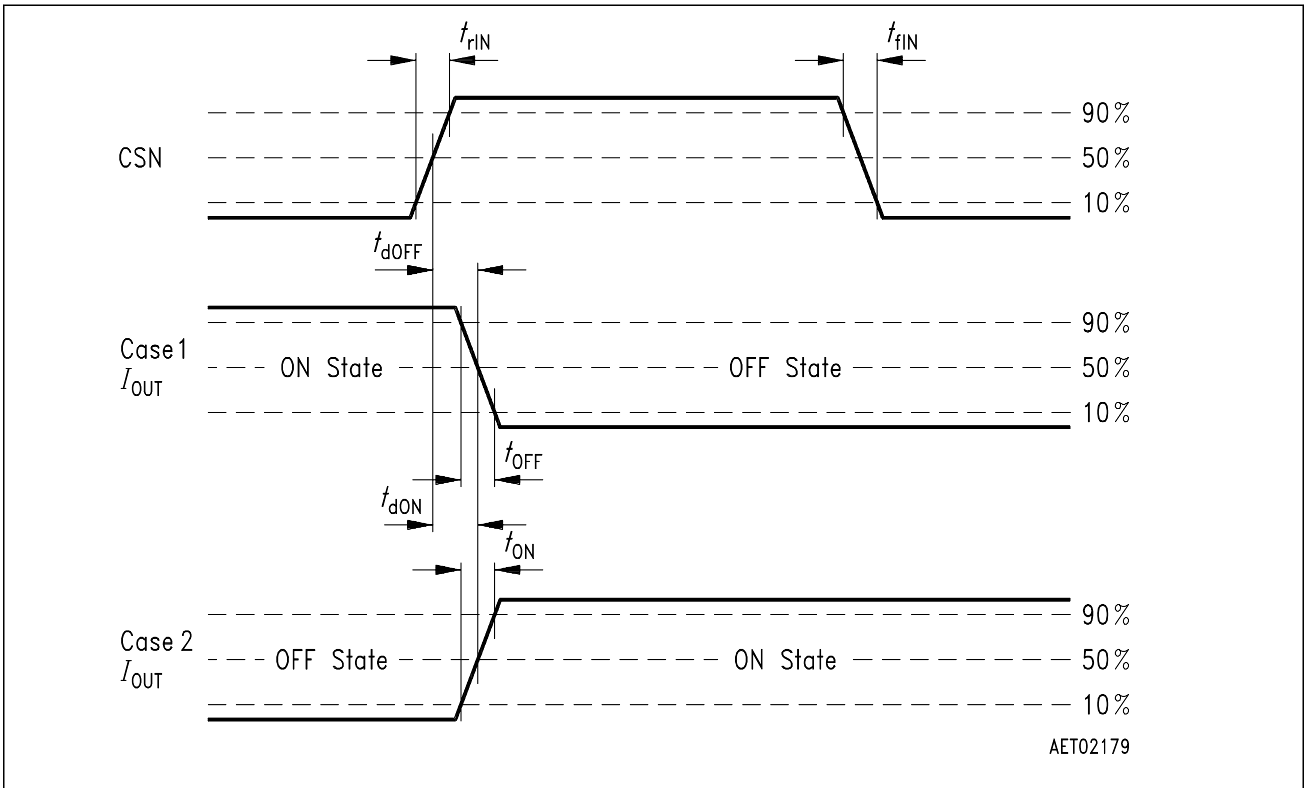


Figure 9 Turn OFF/ON Time

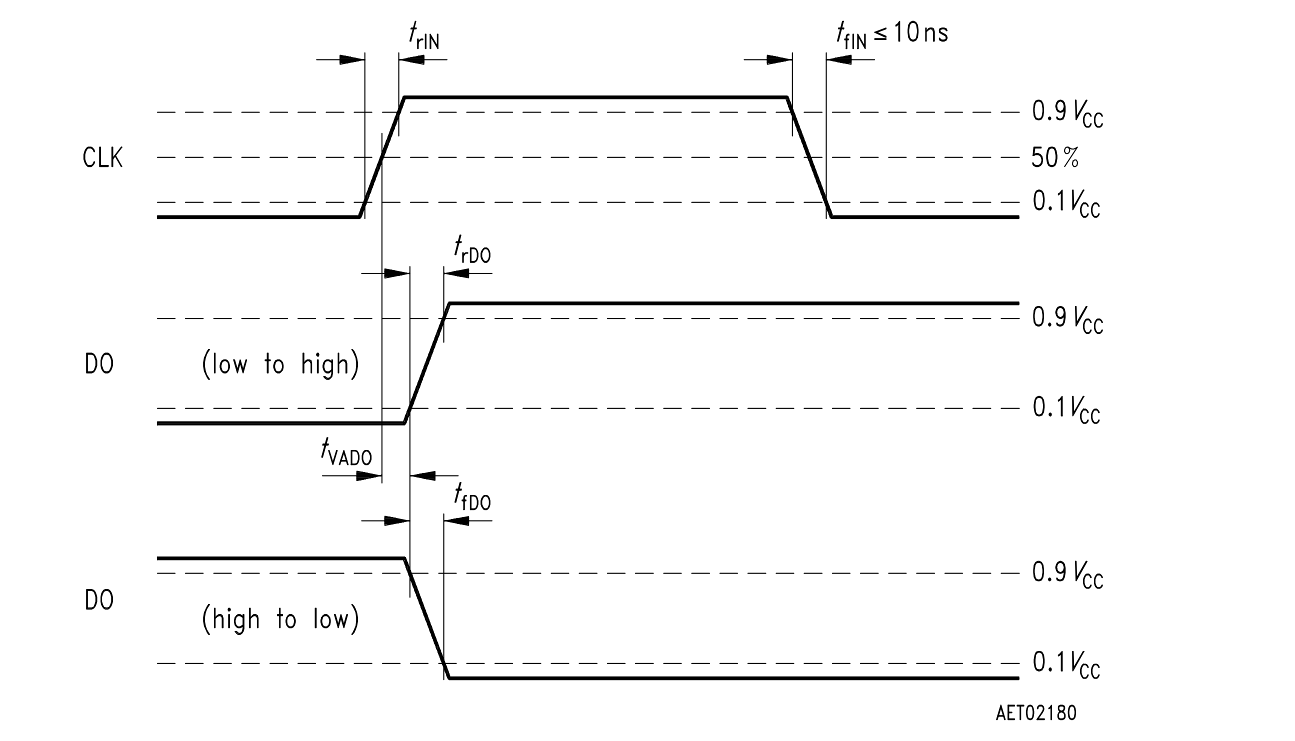


Figure 10 DO Valid Data Delay Time and Valid Time

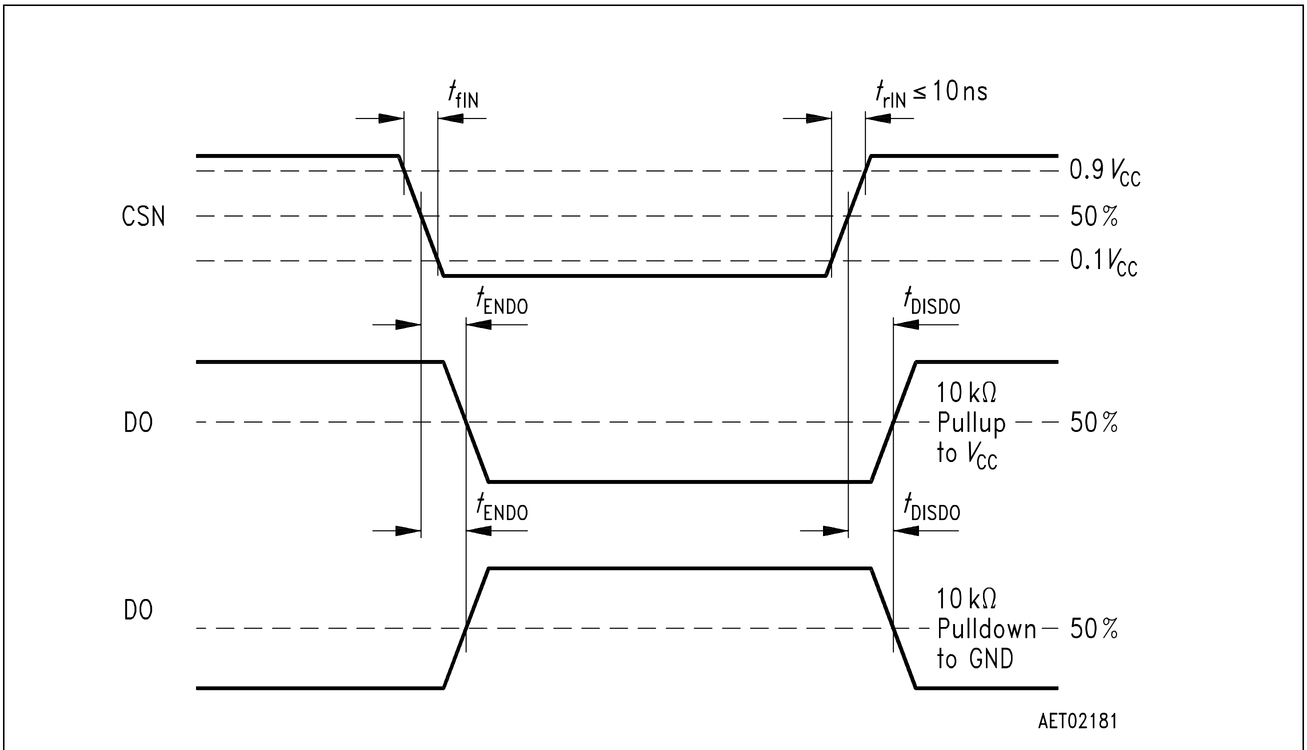


Figure 11 DO Enable and Disable Time

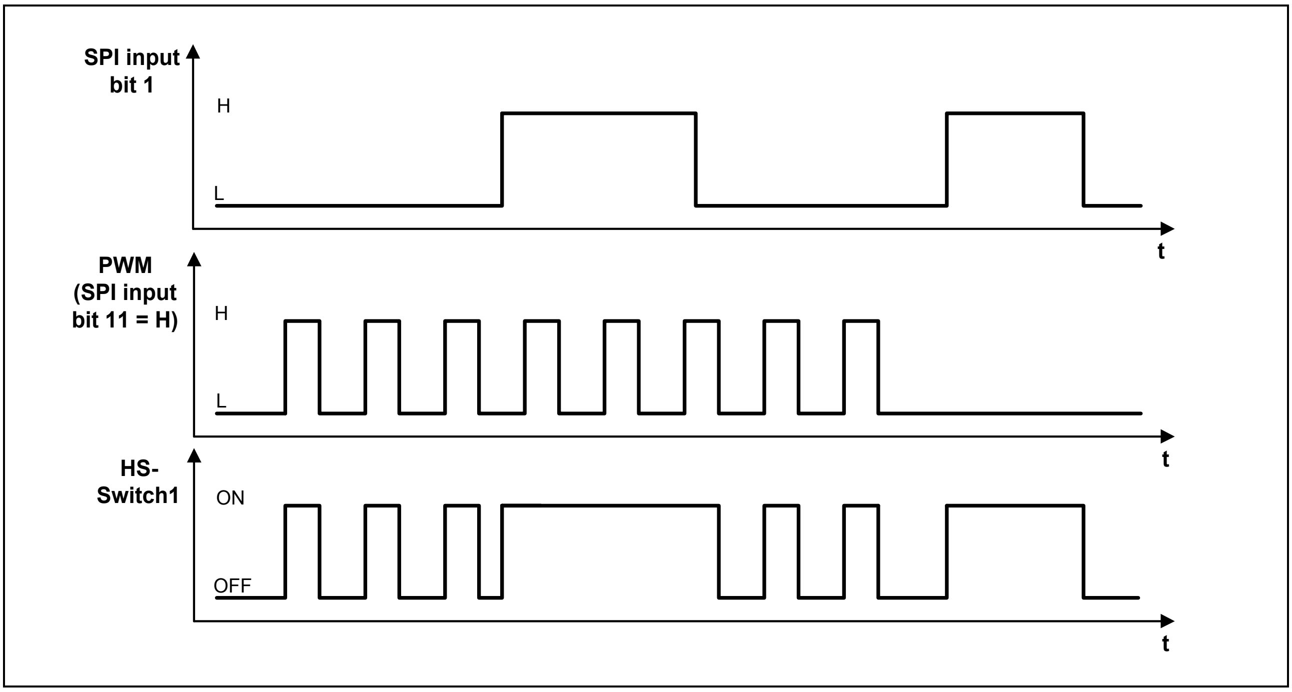


Figure 12 High Side Switch1 Timing Diagram

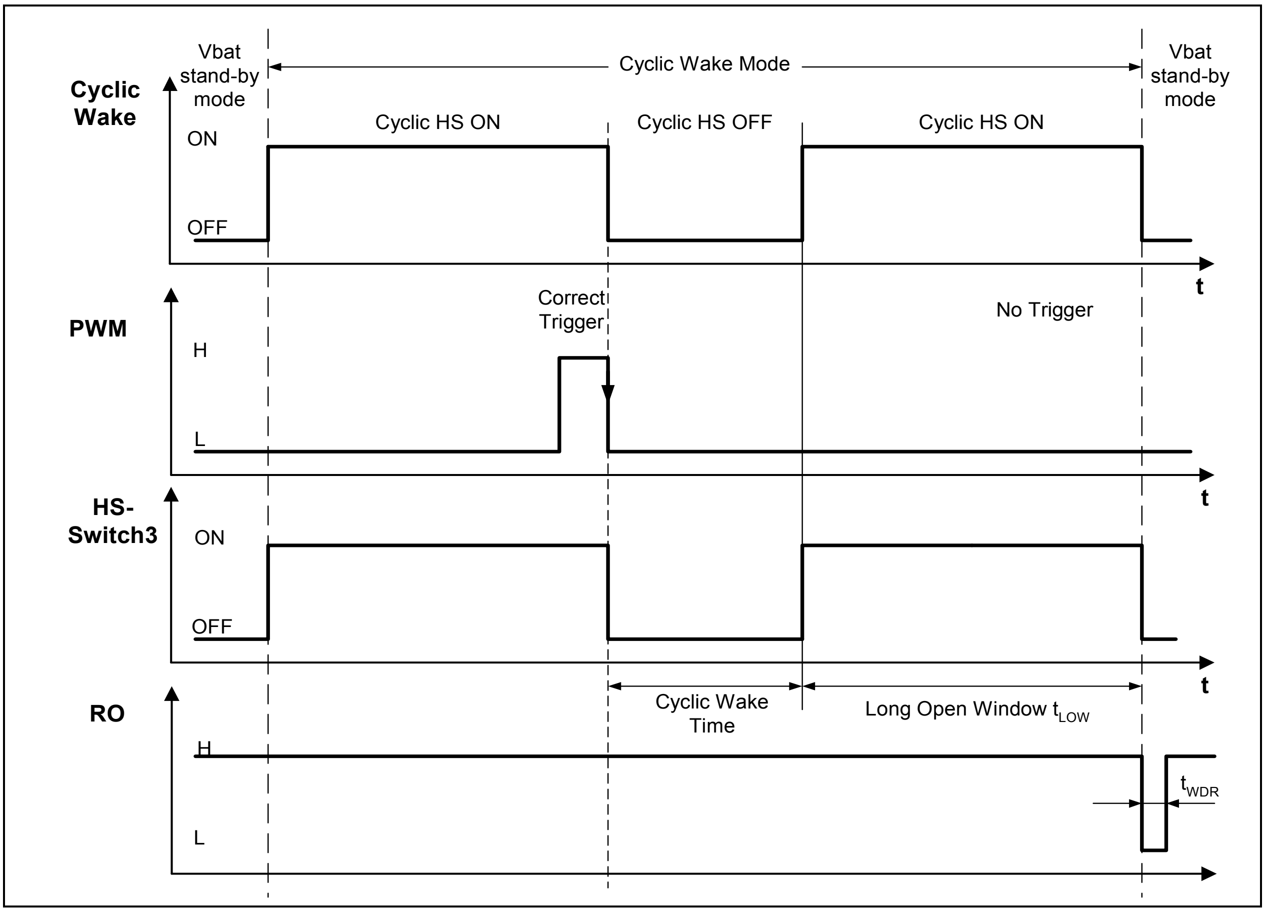


Figure 13 Cyclic Wake Timing Diagram

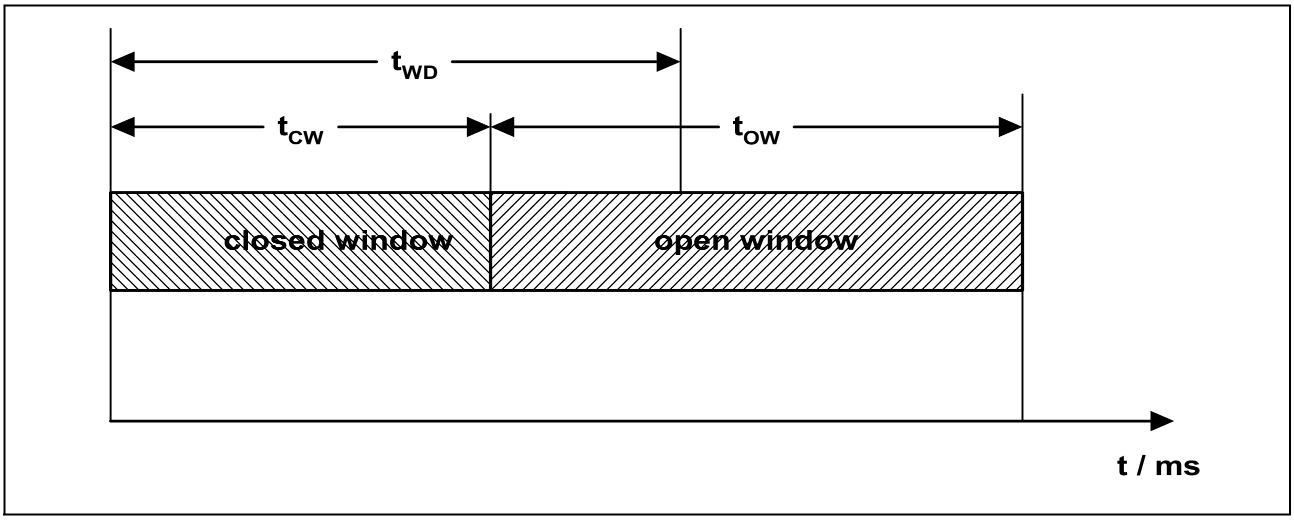


Figure 14 Watchdog Timeout Definitions

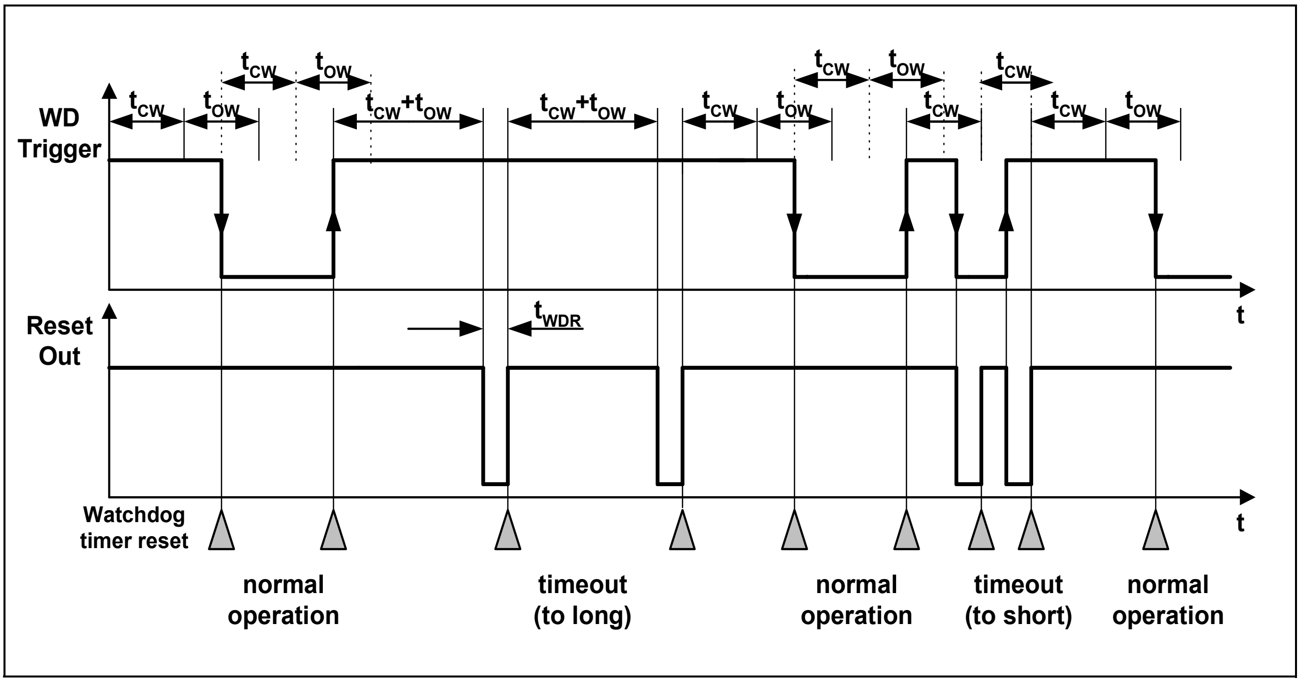


Figure 15 Watchdog Timing Diagram

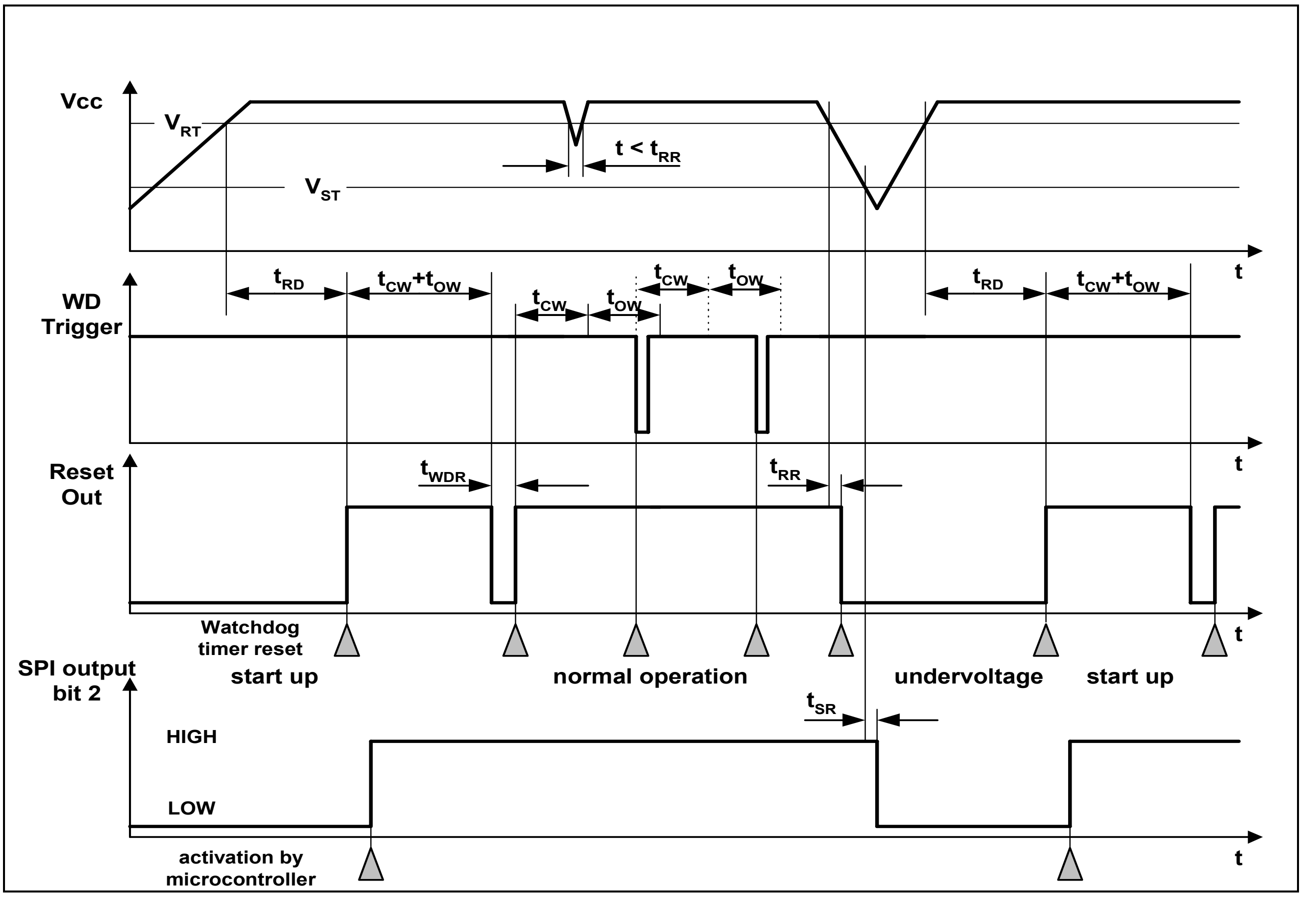


Figure 16 Reset Timing Diagram

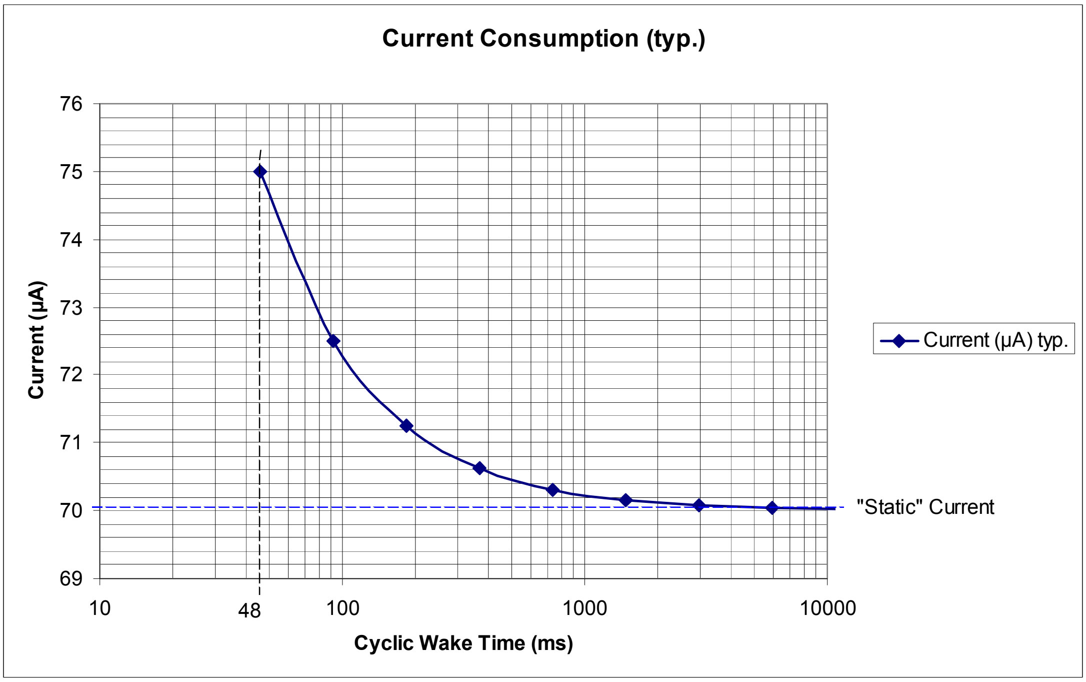


Figure 17 Current Consumption during Cyclic Wake Mode

9 Application

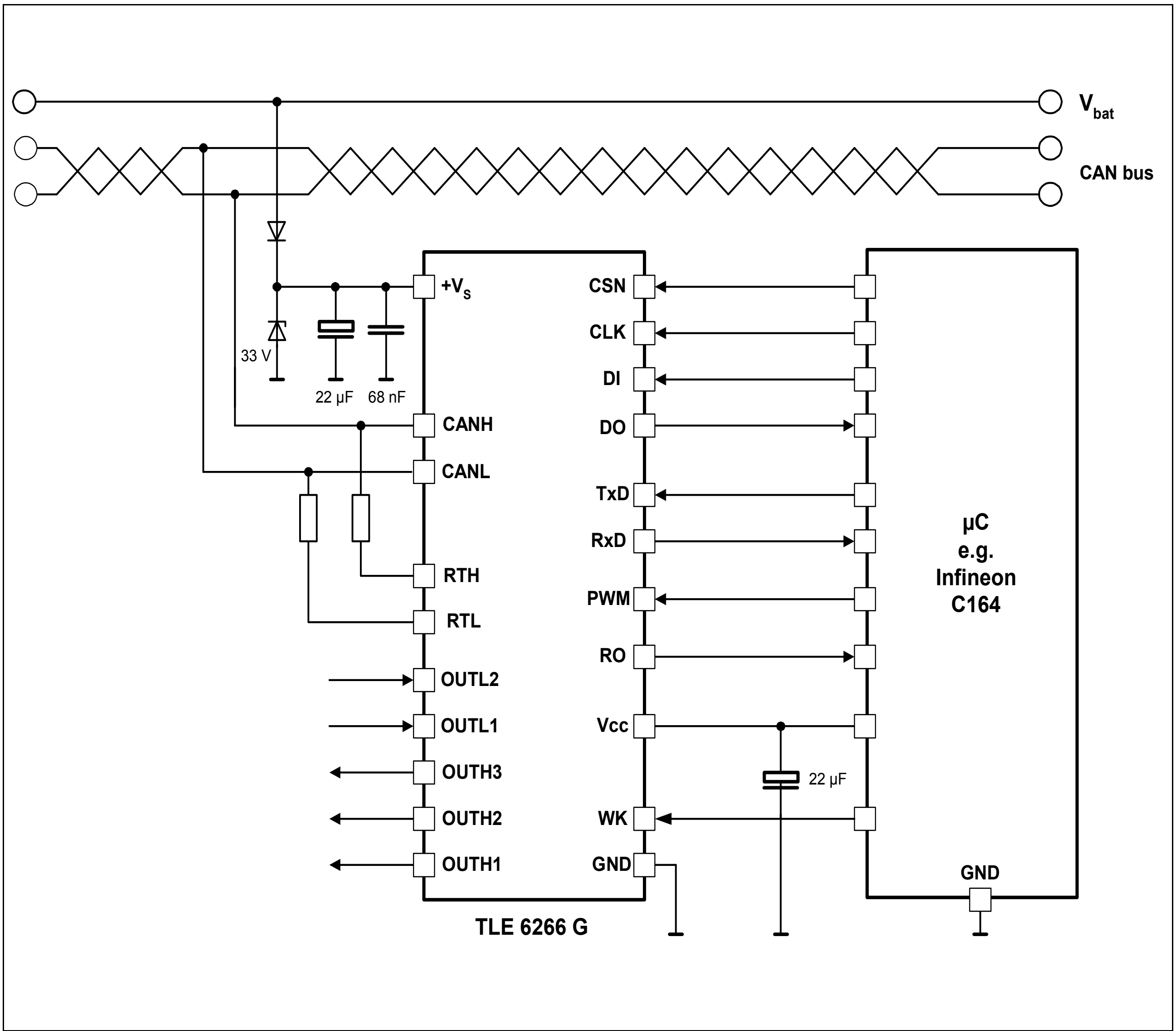
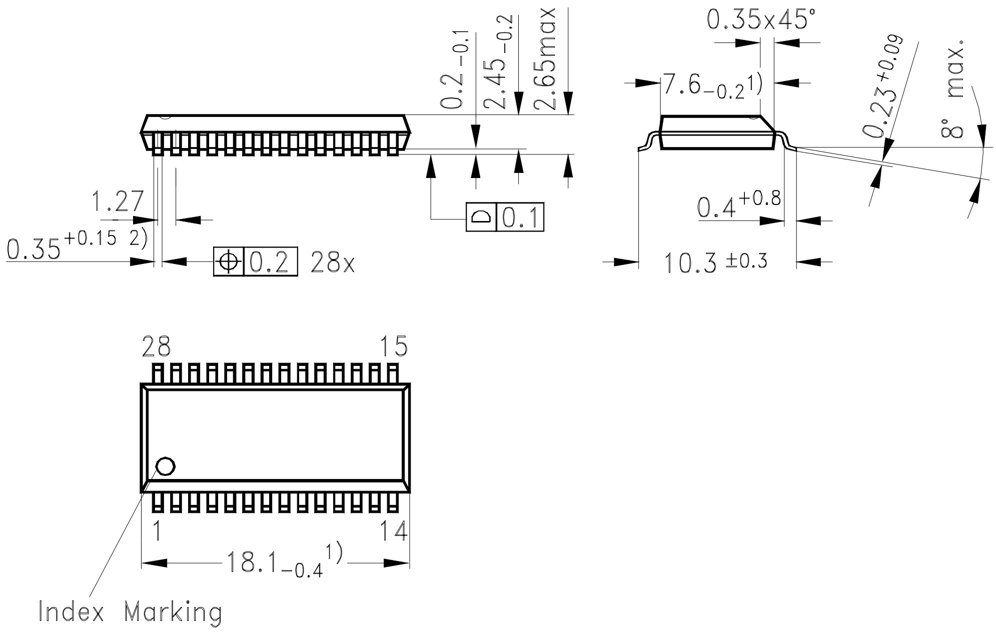


Figure 18 Application Circuit

10 Package Outlines

P-DSO-28-6
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

Figure 19 The P-DSO-28-6 package

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

Edition 1999-10-12

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