Step-Down DC/DC Controller

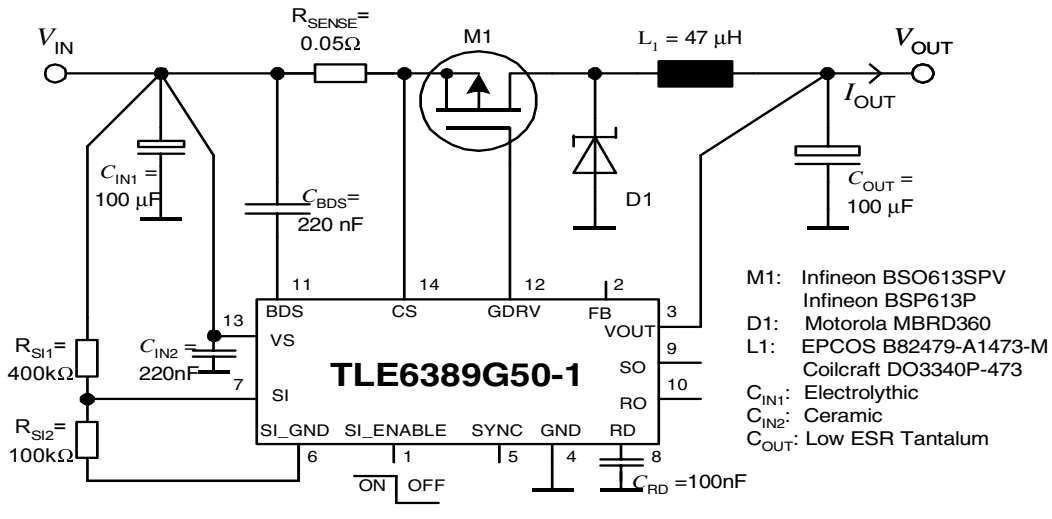
TLE 6389

Preliminary data sheet

1 Overview

1.1 Features

- Input voltage range from < 5V up to 60V
- Output voltage versions: 5V fixed and adjustable
- Output voltage accuracy: 3%
- Load current peak determined by sense resistor
- Output power up to 15W and above
- 100% maximum duty cycle
- Less than 100µA quiescent current at low loads
- 2µA max. shutdown current at device off
- Fixed 350kHz switching frequency
- Frequency synchronization input for external clocks
- Current Mode control scheme
- Integrated output under voltage Reset circuit with adjustable delay time
- On chip low battery detector (on chip comparator)
- Automotive temperature range

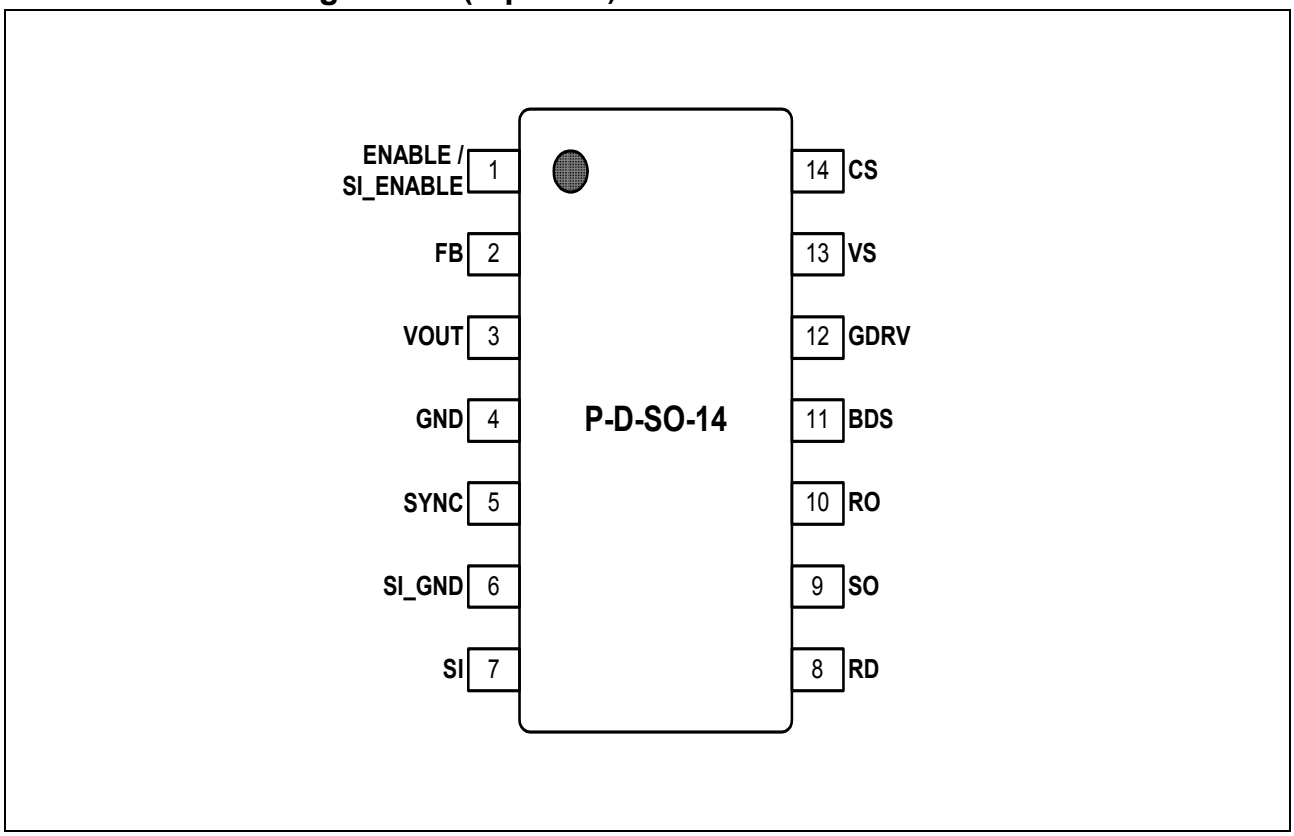


Type	Ordering Code	Package	Description
TLE 6389 GV	Q67006-A9542	P-DSO-14-3	adjustable
TLE 6389 G50	Q67006-A9545	P-DSO-14-3	5V, RO-Hysteresis <<
TLE 6389 G50-1	Q67006-A9635	P-DSO-14-3	5V, RO-Hysteresis 1V

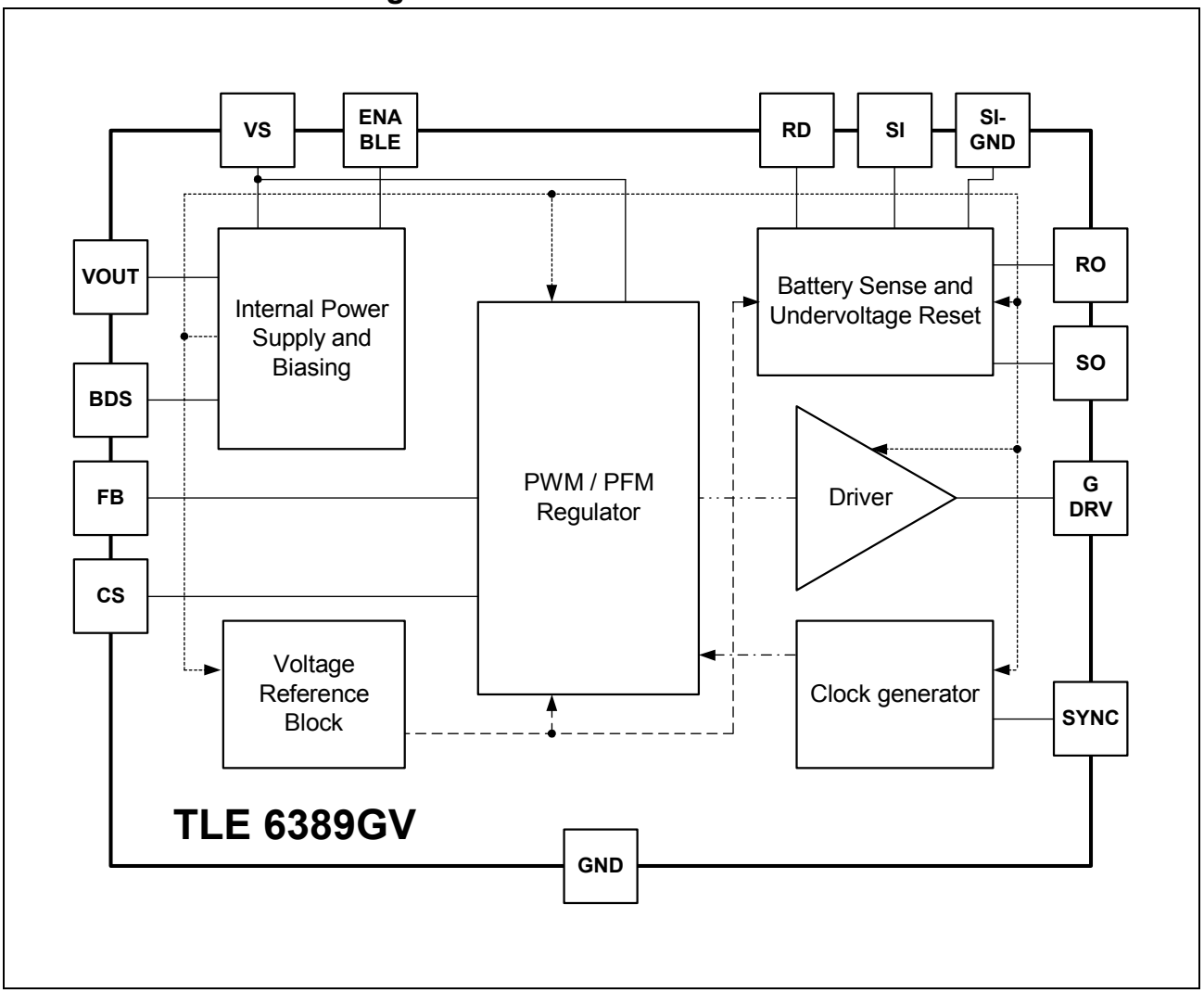
1.2 Short functional description

The **TLE6389** step-down DC-DC switching controllers provide high efficiency over loads ranging from 1mA up to 3A. A unique PWM/PFM control scheme operates with up to a 100% duty cycle, resulting in very low dropout voltage. This control scheme eliminates minimum load requirements and reduces the supply current under light loads to 100µA. For the start up procedure a slow start feature is implemented to avoid overshoots at the output. The TLE6389 step-down controllers drive an external P-channel MOSFET, allowing design flexibility for applications up to 15W of output power. A high switching frequency and operation in continuous-conduction mode allow the use of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs. The output voltage is preset at 5V (**TLE6389G50-1** and **TLE6389G50**) and adjustable for the **TLE6389GV**. Input voltages can be up to 60V.

1.3 Pin Configuration (top view)



1.4 Basic block diagram



1.5 Pin Definitions and Functions

Pin No SO-14	Symbol	Function
1	ENABLE	**Active-High enable input (only at adjustable version, TLE6389GV) for the device.** The device is shut down when ENABLE is driven low. In this shut down-mode the reference, the output and the external MOSFET are turned off. Connect to logic high for normal operation.
1	SI_ENABLE	**Active-High enable input (only at 5V version, TLE6389G50-1 and TLE6389G50) for SI_GND input.** SI_GND is switched to high impedance when SI_ENABLE is low. High level at SI_ENABLE connects SI_GND to GND with low impedance. SO is undefined when SI_ENABLE is low.
2	FB	**Feedback input.** 1. For adjustable version (GV) connect this pin to an external voltage divider from the output to GND (see the determining the output voltage, application section). 2. At the 5V fixed output voltage version (G50-1 and G50) the FB is connected internally to an on-chip voltage divider. It does not have to be connected externally to the output.
3	VOUT	**Buck output voltage input.** Input for the internal supply. Connect to the output capacitance of the buck converter.
4	GND	**Ground connection.** Analog signal ground.
5	SYNC	**Input for external frequency synchronization.** An external clock signal connected to this pin allows switching frequency synchronization of the device. The internal oscillator is clocked then by the frequency applied at the SYNC input.
6	SI_GND	**SI-Ground input.** Ground connection for SI comparator resistor divider. Depending on SI_ENABLE this input is switched to high impedance or low ohmic to GND.
7	SI	**Sense comparator input.** Input of the low-battery comparator. This input is compared to an internal 1.25V reference where SO gives the result of the comparison. Can be used for any comparison, not necessarily as battery sense.
8	RD	**Reset delay input.** Connect a ceramic capacitor to GND for power on reset delay time adjustment.

Pin No SO-14	Symbol	Function
9	SO	**Sense comparator output.** Open drain output from SI comparator at the adjustable version (TLE6389GV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (TLE6389G50-1 and TLE6389G50).
10	RO	**Reset output.** Open drain output from undervoltage reset comparator at the adjustable version (TLE6389GV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (TLE6389G50-1 and TLE6389G50).
11	BDS	**Buck driver supply input.** Connect a ceramic capacitor between BDS and VS to generate clamped gate-source voltage to supply the driver of the PMOS power stage.
12	GDRV	**Gate drive output.** Connect to the gate of the external P-Channel MOSFET**.** The voltage at GDRV swings between the levels of VS and BDS.
13	VS	**Device supply input.** Connect a 220nF ceramic cap close to the pin in addition to the low ESR tantalum input capacitance.
14	CS	**Current-sense input.** Connect current-sense resistor between VS and CS. The voltage drop over the sense-resistor determines the peak current flowing in the buck circuit. The external MOSFET is turned off when the peak current is exceeded.

2 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Device supply input VS					
2.1	Voltage	V_{VS}	-0.3	61	V	–
2.2	Current	I_{VS}	–	–	–	
	Current sense input CS					
2.3	Voltage	V_{CS}	-0.3	61	V	–
2.4	Current	I_{CS}	–	–	–	
	Gate drive output GDRV					
2.5	Voltage	V_{GDRV}	– 0.3	6.8	V	$\lvert V_{VS} - V_{GDRV}\rvert < 6.8V$
2.6	Current	I_{GDRV}	–	–	–	limited internally
	Buck driver supply input BDS					
2.7	Voltage	V_{BDS}	– 0.3	55	V	$\lvert V_{VS} - V_{BDS}\rvert < 6.8V$
2.8	Current	I_{BDS}	–	–	–	
	Feedback input FB					
2.9	Voltage	V_{FB}	– 0.3	6.8	V	
2.10	Current	I_{FB}	–	–	–	
	Enable input SI_ENABLE					
2.11	Voltage	V_{SI_ENABLE}	– 0.3	61	V	(TLE6389G50-1 and TLE6389G50)
2.12	Current	I_{SI_ENABLE}	–	–	–	
	SI-Ground input SI_GND					
2.13	Voltage	V_{SI_GND}	– 0.3	61	V	(TLE6389G50-1 and TLE6389G50)
2.14	Current	I_{SI_GND}	–	–	–	
	Enable input ENABLE					
2.15	Voltage	V_{ENABLE}	– 0.3	61	V	(TLE6389GV only)
2.16	Current	I_{ENABLE}	–	–	–	

2 Absolute Maximum Ratings (cont'd)

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Sense comparator input SI					
2.17	Voltage	V_{SI}	– 0.3	61	V	
2.18	Current	I_{SI}	–	–	–	
	Sense comparator output SO					
2.19	Voltage	V_{SO}	– 0.3	6.8	V	
2.20	Current	I_{SO}	–	–	–	limited internally
	Buck output voltage input VOUT					
2.21	Voltage	V_{VOUT}	– 0.3	15	V	(TLE6389GV only)
2.22	Voltage	V_{VOUT}	– 0.3	6.8	V	(TLE6389G50-1 and TLE6389G50)
2.23	Current	I_{VOUT}	–	–	mA	
	Reset delay input RD					
2.24	Voltage	V_{RD}	– 0.3	6.8	V	
2.25	Current	I_{RD}	–	–	mA	
	Reset output RO					
2.26	Voltage	V_{RO}	– 0.3	6.8	V	
2.27	Current	I_{RO}	–	–	mA	limited internally
	Frequency synchronization input SYNC					
2.28	Voltage	V_{SYNC}	– 0.3	6.8	V	
2.29	Current	I_{SYNC}	–	–	mA	
	ESD-Protection (Human Body Model; R=1,5kΩ; C=100pF)					
2.30	Electrostatic discharge voltage	V_{ESD}	–2	2	kV	HBM

2 Absolute Maximum Ratings (cont'd)

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Temperatures					
2.31	Junction temperature	T_j	– 40	150	°C	–
2.32	Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3 Operating Range

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
3.1	Supply voltage range	V_{VS}	5	60	V	
3.2	Sense Resistor	R_{SENSE}	5	-	mΩ	Calculation see section 6
3.3	PMOS, on+off delay	$t_{on+off\ delay}$	-	t_{min}-300	ns	$t_{min}=V_{VOUT}/(V_{VS}*f_{SW})$
3.4	Buck driver supply capacitor	C_{BDS}	220	-	nF	
3.5	Buck inductance	L1	47	-	µH	recommended value
3.6	Buck inductance	L1	22	100	µH	
3.7	Buck output capacitor	C_{OUT}	100	-	µF	
3.8	Junction temperature	T_j	– 40	150	°C	
	Thermal Resistance					
3.9	Junction ambient	R_{thj-a}		140	K/W	Footprint only
3.10	Junction pin	R_{thj-p}		50	K/W	–

4 Electrical Characteristics

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Current Consumption[1] TLE6389G50-1 and TLE6389G50						
4.1	Current consumption of VS	I_{VS}		75	90	µA	V_{VS} = 48V; PFM mode; T_j = 25°C
4.2				70	85	µA	V_{VS} = 13.5V; PFM mode; T_j = 25 °C
4.3					115	µA	V_{VS} = 48V; PFM mode
4.4	Current consumption of SI_ENABLE	I_{SI_ENABLE}		5	10	µA	V_{VS} = 48V; V_{SI_ENABLE} = 48V; PFM mode; T_j = 25°C
4.5	Current consumption of VOUT	I_{VOUT}		95	115	µA	V_{SI_ENABLE} = L; V_{VOUT} = 5.5V; PFM mode; T_j = 25°C
4.6				140	160	µA	V_{SI_ENABLE} = H; V_{VOUT} = 5.5V; V_{SI} > $V_{SI, high}$; PFM mode; T_j = 25°C
4.7	Current consumption of SI	I_{SI}		0.2	0.5	µA	V_{VS} = 13.5V; V_{SI_ENABLE} = H; V_{SI} = 10V ; PFM mode;

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Current Consumption[1] TLE6389GV (variable)						
4.8	Current consumption of VS	I_{VS}		75	90	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode; T_j = 25°C; $V_{OUT} \geq$ 7V
4.9				70	85	µA	V_{VS} = 13.5V; V_{ENABLE} = H; PFM mode; T_j = 25 °C; $V_{OUT} \geq$ 7V
4.10					125	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode; $V_{OUT} \geq$ 7V
4.11					2	µA	V_{ENABLE}=0V
4.12	Current consumption of ENABLE	I_{EN}		5	10	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode; T_j = 25°C
4.13	Current consumption of VOUT	I_{VOUT}		140	160	µA	V_{OUT} = 10V; V_{ENABLE} = H; $V_{SI} > V_{SI, high}$; PFM mode; T_j = 25°C; $V_{OUT} \geq$ 7V
4.14	Current consumption of SI	I_{SI}		0.2	0.5	µA	V_{VS} = 13.5V; V_{ENABLE} = H; V_{SI} = 10V ; PFM mode; T_j = 25°C

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.15	Current consumption of FB	I_{FB}		0.2	0.5	µA	V_{VS} = 13.5V; V_{FB} = 1.25V; V_{ENABLE} = H; PFM mode; T_j = 25°C
	Buck Controller						
4.16	Output voltage	V_{VOUT}	4.85	5.00	5.15	V	TLE6389G50-1, TLE6389G50; V_{VS} = 13.5V & 48V; I_{OUT} = 0.5 to 2A; PWM Mode; R_{SENSE} = 0.01Ω; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.17			4.75	5.00	5.25	V	TLE6389G50-1, TLE6389G50; V_{VS} = 24V; I_{OUT} = 15mA; PFM Mode; R_{SENSE} = 0.01Ω; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.18			3.8			V	TLE6389G50-1; V_{VS} decreasing from 5.8V to 4.2V; I_{LOAD} = 0mA to 500mA; R_{SENSE} = 0.01Ω; R_{M1} = 0.4Ω; R_{L1} = 0.1Ω;

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.19	FB threshold voltage	$V_{FB, th}$	1.225	1.25	1.275	V	TLE6389GV
4.20	Output voltage	V_{VOUT}	9.7	10.0	10.3	V	TLE6389GV; Calibrated divider, see section 7.3; V_{VS} = 13.5V & 48V; I_{OUT} = 0.5 to 2A; PWM Mode; R_{SENSE} = 0.01Ω; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.21	Output voltage	V_{VOUT}	9.5	10.0	10.5	V	TLE6389GV; Calibrated divider, see section 7.3; V_{VS} = 24V; I_{OUT} = 15mA; PFM Mode; R_{SENSE} = 0.01Ω; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.22	Buck output voltage adjust range	V_{VOUT}	$V_{FB, th}$		7	V	TLE6389GV, supplied by VS only, complete current to supply the IC drawn from VS, 2)

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.23	Buck output voltage adjust range	V_{VOUT}	7		15	V	TLE6389GV, current to supply the IC drawn from VS and VOUT, as specified, 2)
4.24	Buck output voltage accuracy	V_{VOUT}	0.97 *V_{OUT_nom}		1.03 *V_{OUT_nom}	V	TLE6389GV, PWM mode, 2)
4.25	Buck output voltage accuracy	V_{VOUT}	0.95 *V_{OUT_nom}		1.05 *V_{OUT_nom}	V	TLE6389GV, PFM mode, 2)
4.26	Line regulation	$\Delta V_{VOUT}/\Delta V_{VS}$		0.7	2	mV/V	V_{VS} = 5.8 V to 48V; I_{OUT} = 0.5 to 2A; PWM mode
4.27	Load regulation	$\Delta V_{VOUT}/\Delta I_{LOAD}$		40		mV/A	TLE6389G50-1, TLE6389G50, I_{OUT} = 0.5 to 2A; PWM mode; V_{VS} = 5.8 V and 48V; R_{SENSE}=0.01Ω
4.28				8* V_{OUT_nom}		mV/A	TLE6389GV, I_{OUT} = 0.5 to 2A; PWM mode; V_{VS} = 13.5 V and 48V; R_{SENSE}=0.01Ω
4.29	Gate driver, PMOS off	$V_{VS} - V_{GDRV}$	0		0.2	V	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.30	Gate driver, PMOS on	$V_{VS} - V_{GDRV}$	6		8.2	V	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.31	Gate driver, UV lockout	$V_{VS} - V_{BDS}$	2.5		4	V	Decreasing (V_{VS}-V_{BDS}) until GDRV is permanently at VS level
4.32	Gate driver, peak charging current	I_{GDRV}		1		A	PMOS dependend; [2]
4.33	Gate driver, peak discharging current	I_{GDRV}		1		A	PMOS dependend; [2]
4.34	Gate driver, gate voltage, rise time	t_r		45	60	ns	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.35	Gate driver, gate voltage, fall time	t_f		50	65	ns	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.36	Peak current limit threshold voltage	$V_{LIM} = V_{VS} - V_{CS}$	50	80	100	mV	
4.37	Oscillator frequency	f_{OSC}	290	360	420	kHz	PWM mode only
4.38	Maximum duty cycle	d_{MAX}	100			%	PWM mode only
4.39	Minimum on time	t_{MIN}		220	400	ns	PWM mode only
4.40	SYNC capture range		250		530	kHz	PWM mode only

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Reset Generator						
4.41	Reset threshold	$V_{VOUT, RT}$	3.5	3.65	3.8	V	TLE6389G50-1; V_{VOUT} decreasing
4.42			4.5	4.65	4.8	V	TLE6389G50-1; V_{VOUT} increasing
4.43	Reset threshold	$V_{VOUT, RT}$	4.5	4.65	4.8	V	TLE6389G50; V_{VOUT} increasing/ decreasing
4.44	Reset threshold hysteresis	$\Delta V_{VOUT, RT}$		50		mV	TLE6389G50;
4.45	Reset threshold	$V_{FB, RT}$		1.12		V	TLE6389GV; V_{VOUT} decreasing
4.46				1.17		V	TLE6389GV; V_{VOUT} increasing
4.47	Reset output pull up resistor	R_{RO}	10	20	40	kΩ	TLE6389G50-1, TLE6389G50; Internally connected to V_{OUT}
4.48	Reset output High voltage	$V_{RO, H}$	0.8* V_{VOUT}			V	TLE6389G50-1, TLE6389G50; I_{ROH}=0mA
4.49	Reset output Low voltage	$V_{RO,L}$		0.2	0.4	V	$I_{RO, L}$=1mA; 2.5V < V_{VOUT} < V_{RT}

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.50	Reset output Low voltage	$V_{RO,L}$		0.2	0.4	V	$I_{RO,L}$=0.2mA; 1V < V_{VOUT} < 2.5V
4.51	Reset delay charging current	$I_{RD, ch}$	5		10	µA	V_{RD} = 0V
4.52	Reset delay discharging current	$I_{RD, dis}$	3		13	mA	
4.53	Upper reset timing threshold	$V_{RD, UT}$	2.6		4.8	V	
4.54	Lower reset timing threshold	$V_{RD, LT}$	0		0.2	V	
4.55	Reset delay time	t_{rd}	26		96	ms	Calculated with C_{RD} = 100nF;[2)]; see section 6
4.56	Reset reaction time	t_{rr}			10	µs	
	Overvoltage Lockout						
4.57	Overvoltage threshold	$V_{VOUT, OV}$		V_{OUT_nom} +0.1		V	TLE6389G50-1, TLE6389G50; V_{VOUT} increasing
4.58	Overvoltage threshold	$V_{FB, OV}$		V_{FB,th_nom} +0.02		V	TLE6389GV; V_{VOUT} increasing
	ENABLE Input						
4.59	Enable ON-threshold	$V_{ENABLE, ON}$	4.5			V	
4.60	Enable OFF-threshold	$V_{ENABLE, OFF}$			0.8	V	

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	SI_ENABLE Input						
4.61	Enable ON-threshold	$V_{ENABLE, ON}$	4.5			V	
4.62	Enable OFF-threshold	$V_{ENABLE, OFF}$			0.8	V	
	SI_GND Input						
4.63	Switch ON resistance	R_{SW}	50	100	230	Ω	V_{SI_ENABLE}=5V; I_{SI_GND} = 3mA;
	Battery Voltage Sense						
4.64	Sense threshold	$V_{SI, low}$	1.22	1.25	1.28	V	V_{VS} decreasing
4.65	Sense threshold	$V_{SI, high}$		1.33		V	V_{VS} increasing
4.66	Sense threshold hysteresis	$V_{SI, hys}$	50	80	120	mV	
4.67	Sense output pull up resistor	R_{SO}	10	20	40	kΩ	TLE6389G50-1, TLE6389G50; Internally connected to V_{VOUT}
4.68	Sense out output High voltage	$V_{SO, H}$	0.8* V_{VOUT}			V	$I_{SO, H}$=0mA
4.69	Sense out output Low voltage	$V_{SO, L}$		0.2	0.4	V	$I_{SO, L}$=1mA; 2.5V < V_{VOUT}; V_{SI} < 1.13 V
4.70				0.4	V_{VOUT}	V	I_{SOL}=0.2mA; 1V < V_{VOUT} <2.5V; V_{SI} < 1.13 V

4 Electrical Characteristics (cont'd)

5V< V_S <48V; - 40°C< T_j <150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

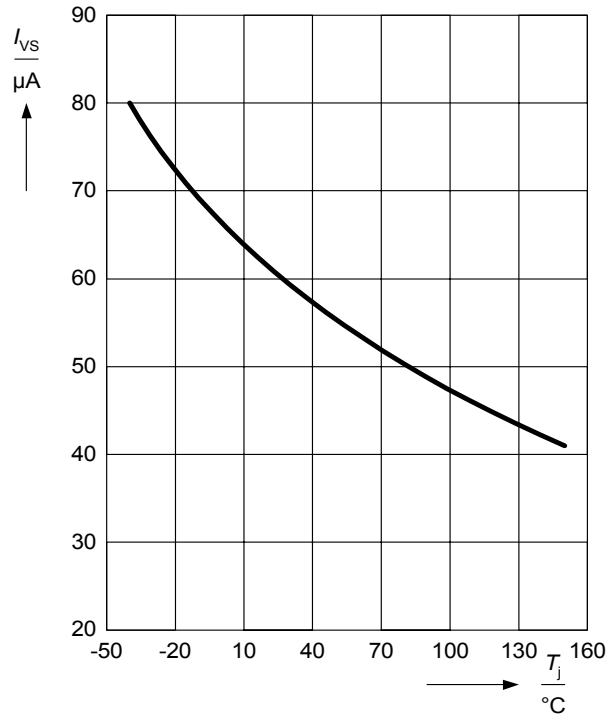
Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Thermal Shutdown						
4.71	Thermal shutdown junction temperature	T_{jSD}	151	175	200	°C	
4.72	Temperature hysteresis	ΔT		30		K	

1) The device current measurements for I_{VS} and I_{FB} exclude MOSFET driver currents.

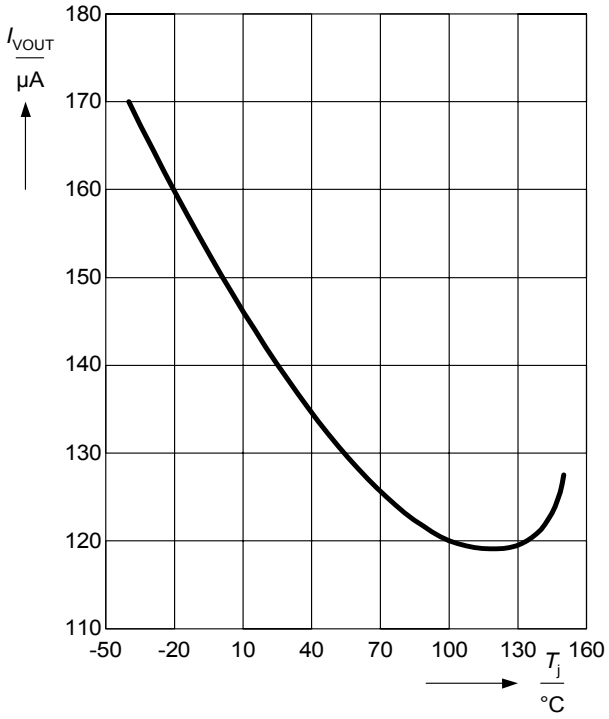
2) Not subject to production test - specified by design

5 Typical performance characteristics

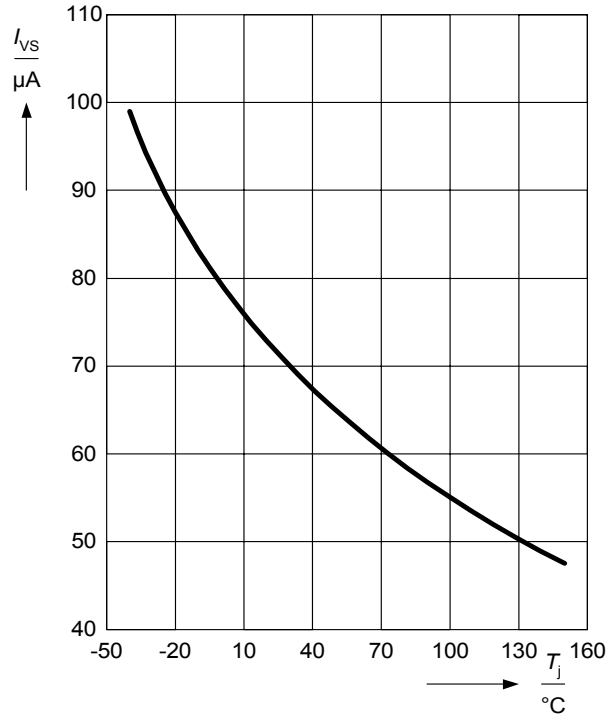
Current consumption I_{VS} vs. temperature T_j at enabled device and V_{VS}=13.5V



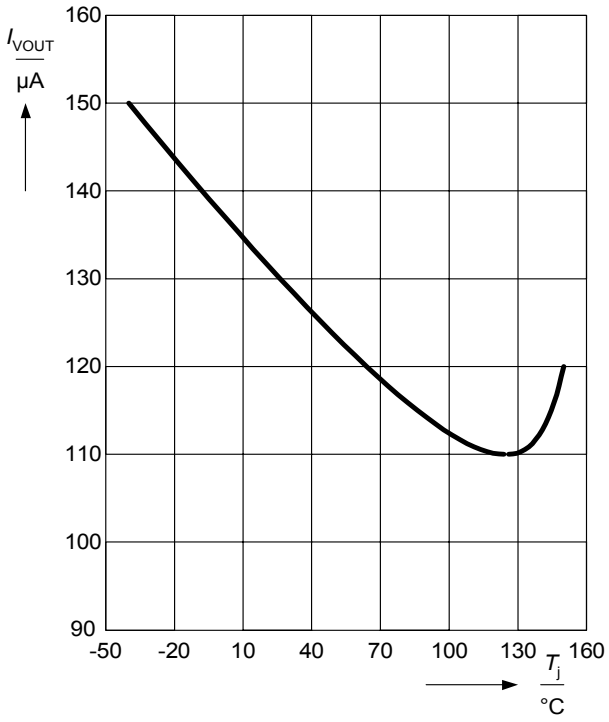
Current consumption I_{VOUT} vs. temperature T_i at enabled device and V_{VOUT}=5.5V



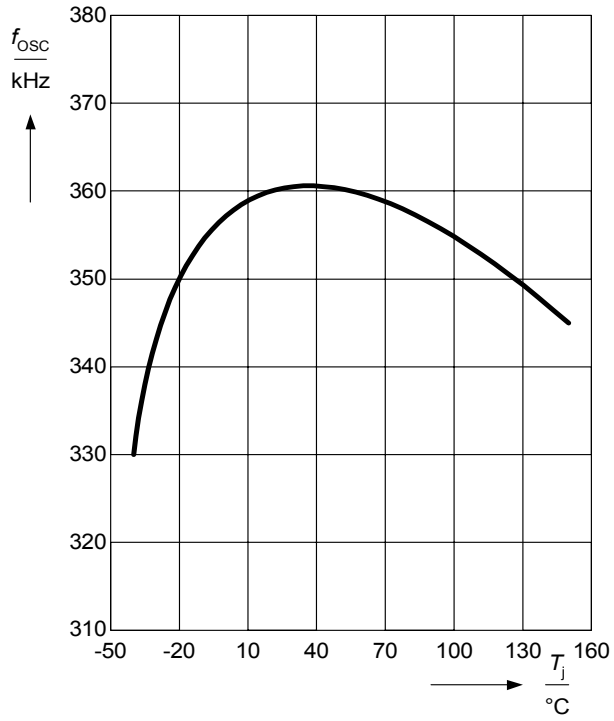
Current consumption I_{VS} vs. temperature T_j at enabled device and V_{VS}=48V



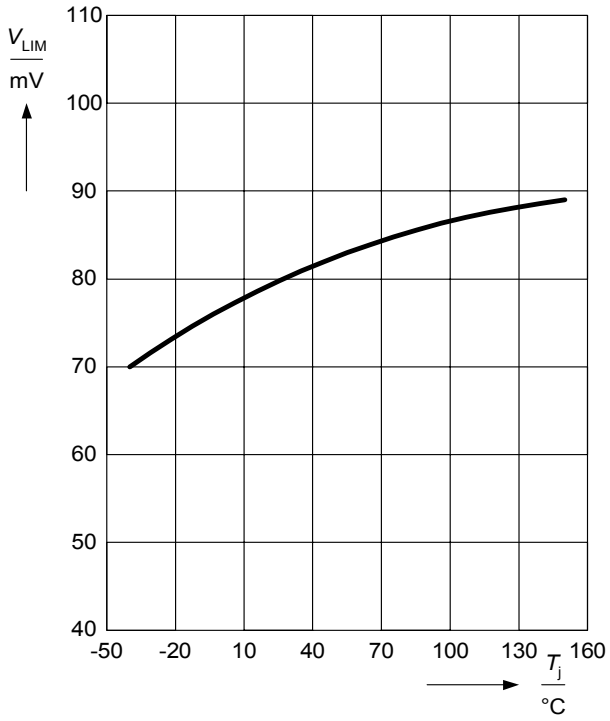
Current consumption I_{VOUT} vs. temperature T_i at enabled device and V_{VOUT}=10V (GV)



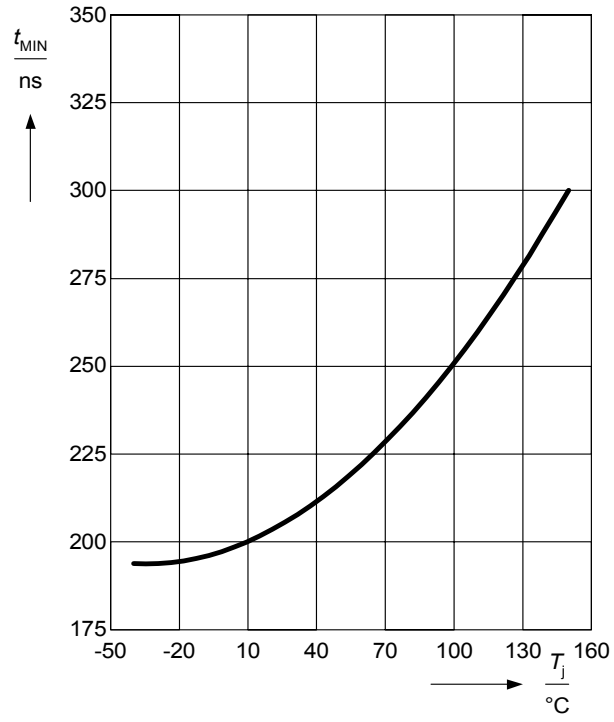
Internal oscillator frequency f_{OSC} vs. temperature T_i



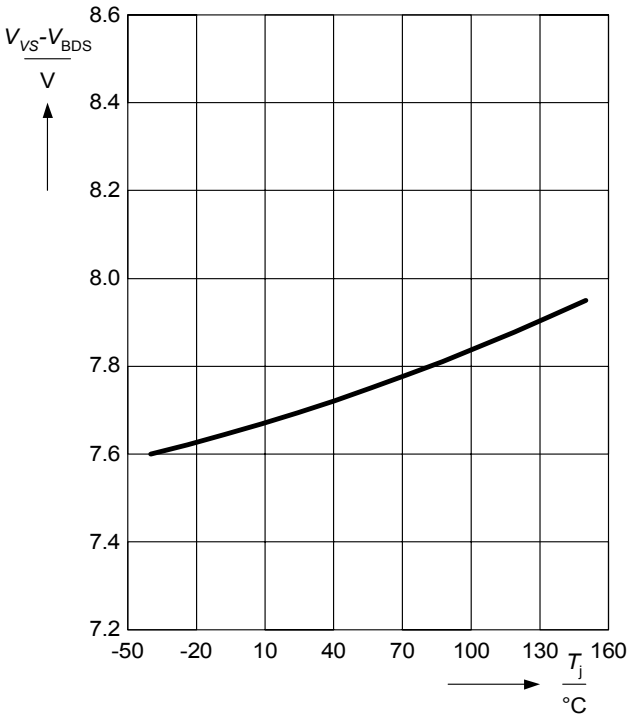
Peak current limit threshold voltage V_{LIM} vs. temperature T_i)



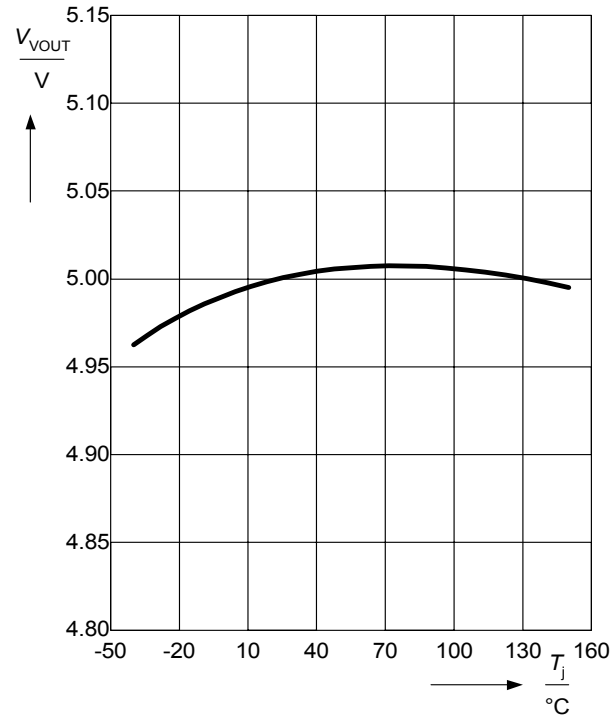
Minimum on time t_{MIN} (blanking) vs. temperature T_i



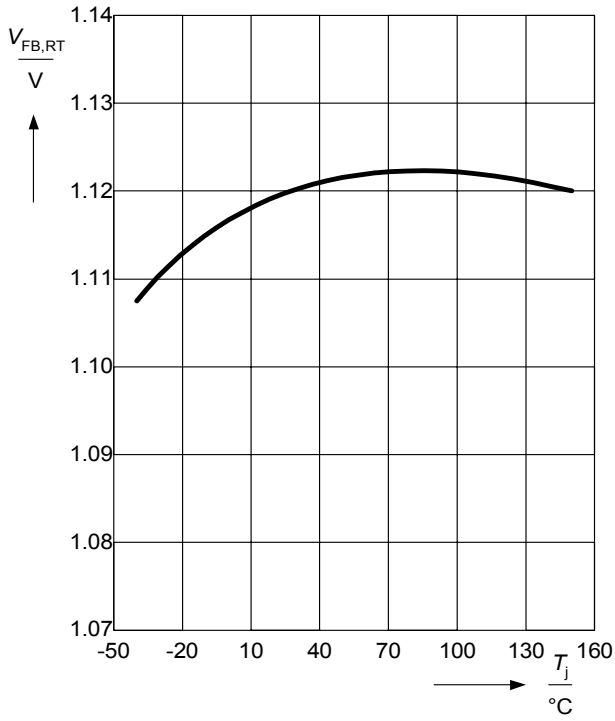
Gate driver supply V_{VS} - V_{BDS} vs. temperature T_i



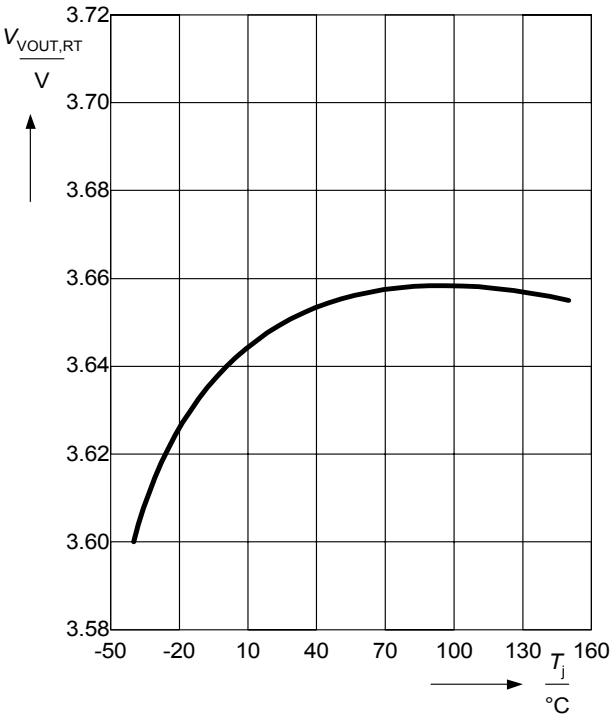
Output voltage V_{VOUT} vs. temperature T_j in PFM mode (V_{VS}=24V, I_{Load}=15mA, G50-1)



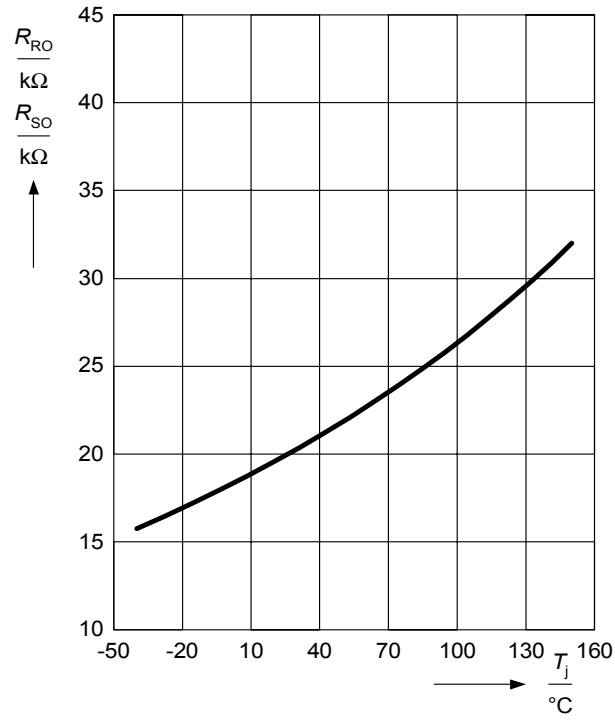
Lower Reset threshold $V_{FB,RT}$ vs. temperature T_i (GV)



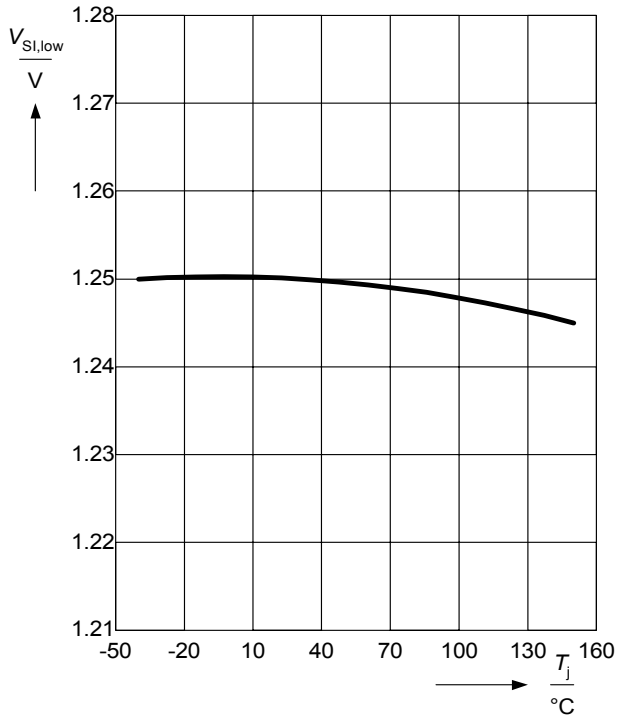
Lower Reset threshold $V_{VOUT,\ RT}$ vs. temperature T_i (G50-1)



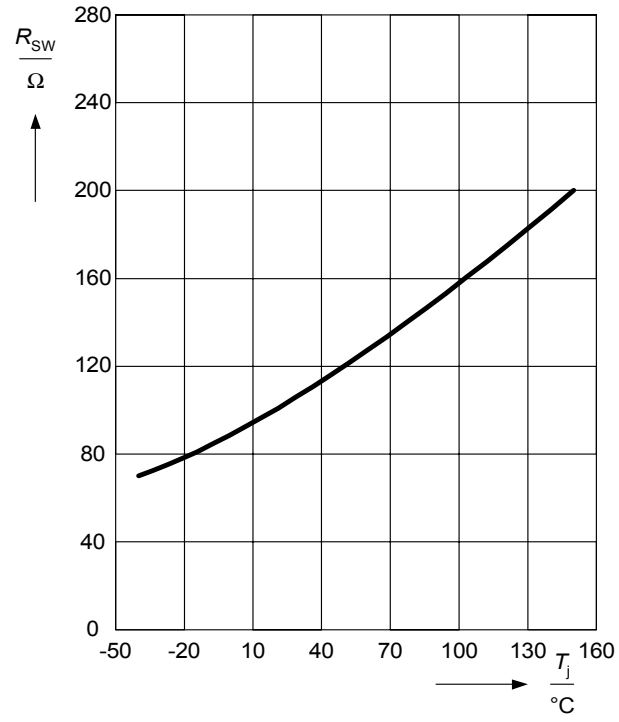
Internal pull up resistors R_{RO} and R_{SO} vs. temperature T_i (G50-1)



Lower Sense threshold $V_{SI,\ low}$ vs. temperature T_j



On resistance of SI_GND switch R_{SW} vs. temperature T_j



6 Detailed circuit description

In the following, some internal blocks of the TLE6389 are described in more detail. For the right choice of the external components please refer to the section application infomation.

6.1 PFM/PWM Step-down regulator

To meet the strict requirements in terms of current consumption demanded by all Body- and 42V PowerNet applications a special PFM (Pulse Frequency Modulation) - PWM (Pulse Width Modulation) control scheme for highest efficiency is implemented in the TLE6389 regulators. Under light load conditions the output voltage is able to increase slightly and at a certain threshold the controller jumps into PFM mode. In this PFM operation the PMOS is triggered with a certain on time (depending on input voltage, output voltage, inductance- and sense resistor value) whenever the buck output voltage decreases to the so called WAKE-threshold. The switching frequency of the step down regulator is determined in the PFM mode by the load current. It increases with increasing load current and turns finally to the fixed PWM frequency at a certain load current depending on the input voltage, current sense resistor and inductance. The diagram below shows the buck regulation circuit of the TLE6389 .

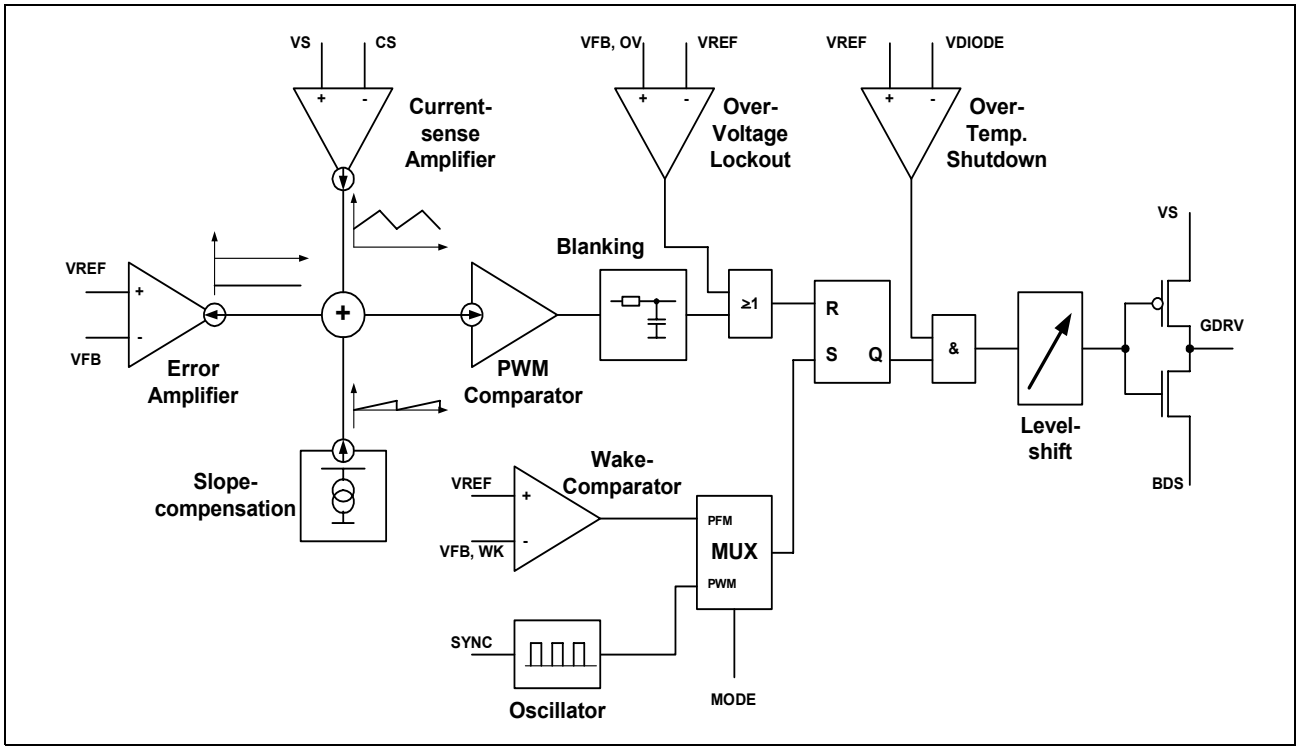


Figure 1 Buck control scheme

The TLE6389 uses a slope-compensated peak current mode PWM control scheme in which the feedback or output voltage of the step down cirucit and the peak current of the current through the PMOS are compared to form the OFF signal for the external PMOS.

The ON-trigger is set periodically by the internal oscillator when acting in PWM mode and is given by the output of the WAKE-comparator when operating in PFM mode. The Multiplexer (MUX) is switched by the output of the MODE-detector which distinguishes between PFM and PWM by tracking the output voltage (goto PFM) and by tracking the gate trigger frequency (goto PWM). In PFM mode the peak current limit is reduced to prevent overshoots at the output of the buck regulator. In order to avoid a gate turn off signal due to the current peak caused by the parasitric capacitance of the catch diode the blanking filter is necessary. The blanking time is set internally to 200ns and determines (together with the PMOS turn on and turn off delay) the minimum duty cycle of the device. In addition to the PFM/PWM regulation scheme an overvoltage lockout and thermal protection are implemented to guarantee safe operation of the device and of the supplied application circuit.

6.2 Battery voltage sense

To detect undervoltage conditions at the battery a sense comparator block is available within the TLE6389. The voltage at the SI input is compared to an internal reference of typ. 1.25V. The output of the comparator drives a NMOS structure giving a low signal at SO as soon as the voltage at SI decreases below this threshold. In the 5V fixed version an internal pull up resistor is connected from the drain of the NMOS to the output of the buck converter, in the variable version SO is open drain.

The sense in voltage divider can be switched to high impedance by a low signal at the SI_ENABLE to avoid high current consumption to GND (TLE6389G50-1 and TLE6389G50 only).

Of course the sense comparator can be used for any input voltage and does not have to be used for the battery voltage sense only.

6.3 Undervoltage Reset

The output voltage is monitored continously by the internal undervoltage reset comparator. As soon as the output voltage decreases below the thresholds given in the characteristics the NPN structure pulls RO low (latched). In the 5V fixed version an internal pull up resistor is connected from the collector of the NPN to the output of the buck converter, in the variable version RO is open collector.

At power up RO is kept low until the the output voltage has reached its reset threshold and stayed above this threshold for the power on reset delay time. This delay time can be determined by the appropriate choice of the external delay capacitance (see application information).

7 Application information

7.1 General

The **TLE6389** step-down DC-DC controllers are designed primarily for use in Automotive applications where high input voltage range requirements have to be met. Using an external P-MOSFET and current-sense resistor allows design flexibility and the improved efficiencies associated with high-performance P-channel MOSFETs. The unique, peak current-limited, PWM/PFM control scheme gives these devices excellent efficiency over wide load ranges, while drawing around 100µA current from the battery under no load condition. This wide dynamic range optimizes the **TLE6389** for automotive applications, where load currents can vary considerably as individual circuit blocks are turned on and off to conserve energy. Operation to a 100% duty cycle allows the lowest possible dropout voltage, maintaining operation during cold cranking. High switching frequencies and a simple circuit topology minimize PC board area and component costs.

7.2 Typical application circuits

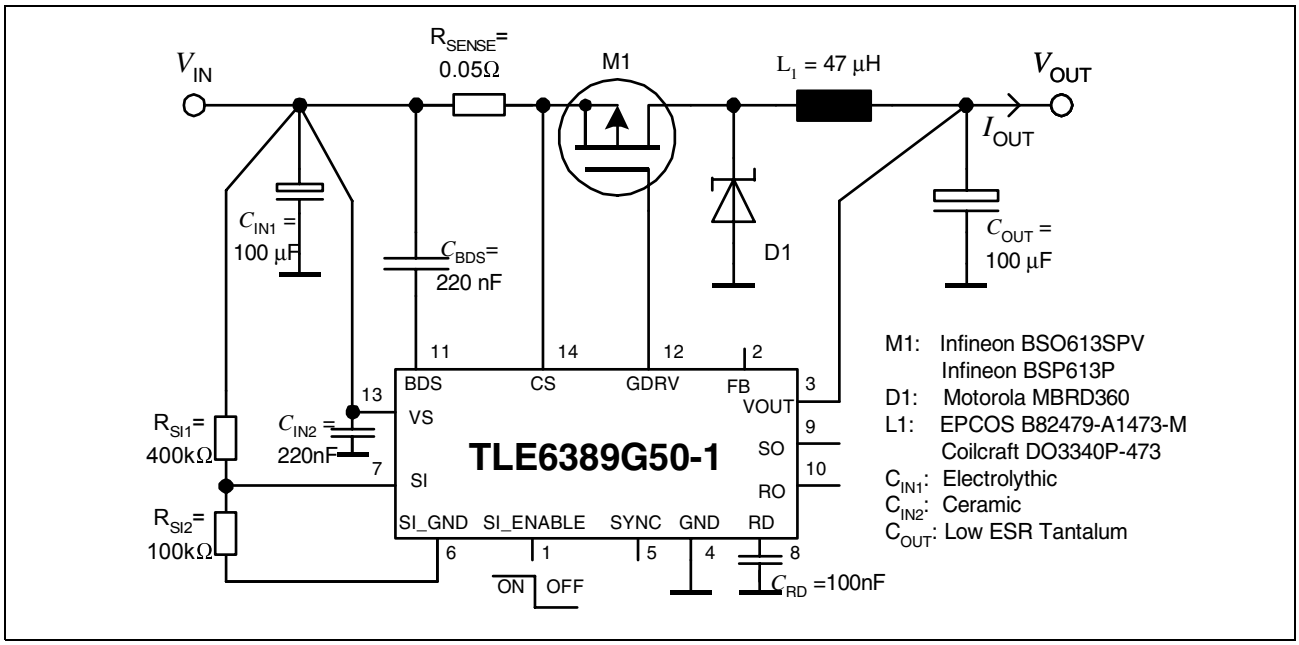


Figure 2 Application circuit TLE6389G50-1 and TLE6389G50

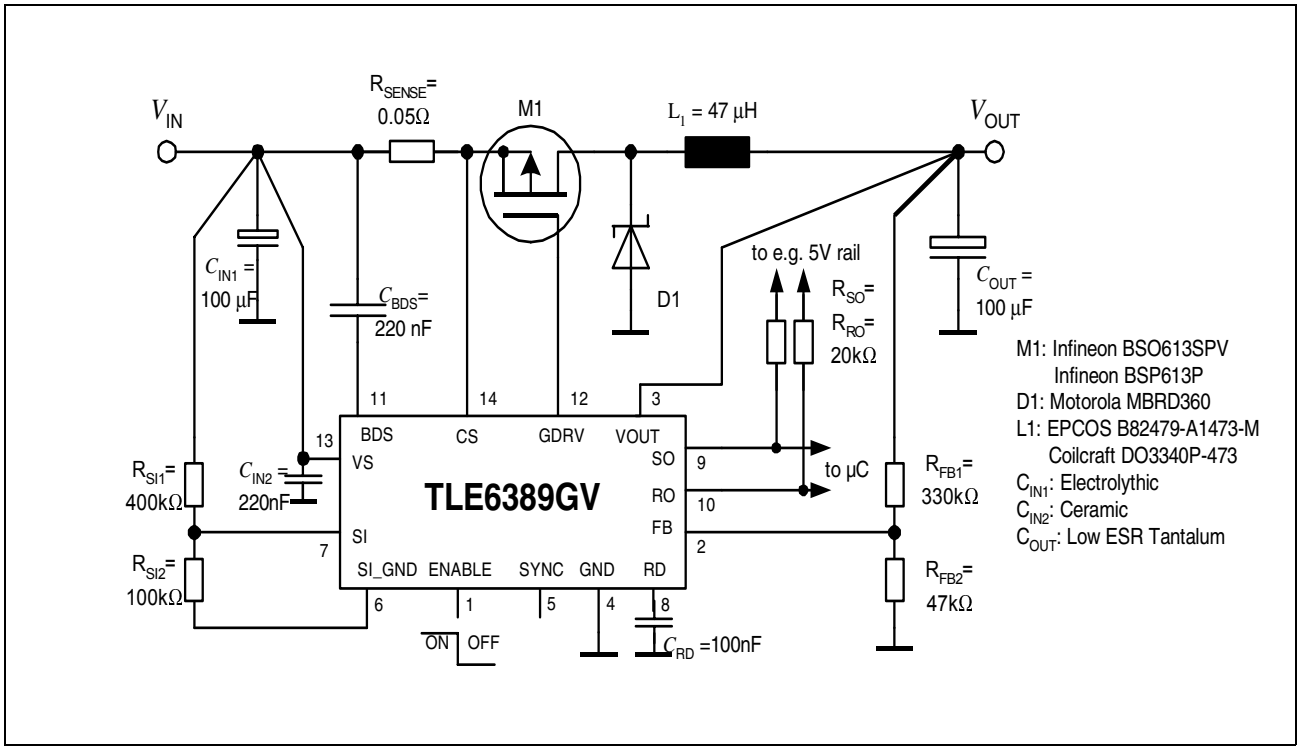


Figure 3 Application circuit TLE6389GV

7.3 Output voltage at adjustable version - feedback divider

The output voltage is sensed either by an internal voltage divider connected to the VOUT pin (**TLE6389G50-1** and **TLE6389G50,** fixed 5V versions) or an external divider from the Buck output voltage to the FB pin (**TLE6389GV**, adjustable version).

To determine the resistors of the feedback divider for the desired output voltage V_{OUT} at the TLE6389GV select R_{FB2} between 5kΩ and 500kΩ and obtain R_{FB1} with the following formula:

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{OUT}}{V_{FB,\,th}} - 1 \right)$$

V_{FB} is the threshold of the error amplifier with its value of typical 1.25V which shows that the output voltage can be adjusted in a range from 1.25 to 15V. Keep in mind that the current consumption will be increased in PFM mode in the range between 1.25 and 7V. To filter spikes at the FB input connect a small ceramic cap (10nF) in parallel to R_{FB2}.

7.4 SI_Enable

Connecting SI_ENABLE to 5V causes SI_GND to have low impedance. Thus the SI comparator is in operation and can be used to monitor the battery voltage. SO output signal is valid. Connecting SI_ENABLE to GND causes SI_GND to have high impedance. Thus the SI comparator is not able to monitor the battery voltage. SO output signal is invalid.

7.5 Battery sense comparator - voltage divider

The formula to calculate the resistor divider for the sense comparator is basically the same as for the feedback divider in section before. With the selected resistor R_{SI2}, the desired threshold of the input voltage $V_{IN, UV}$ and the lower sense threshold $V_{SI, low}$ the resistor R_{SI1} is given to:

$$R_{SI1} = R_{SI2} \cdot \left(\frac{V_{IN, UV}}{V_{SI, low}} - 1 \right)$$

For high accuracy and low ohmic resistor divider values the On-resistance of the SI_GND NMOS (typ. 100Ω) has to be added to R_{SI2}.

7.6 Undervoltage reset - delay time

The diagram below shows the typical behavour of the reset output in dependency on the input voltage V_{IN}, the output voltageV_{VOUT} or V_{FB} and the reset delay voltage V_{RD}.

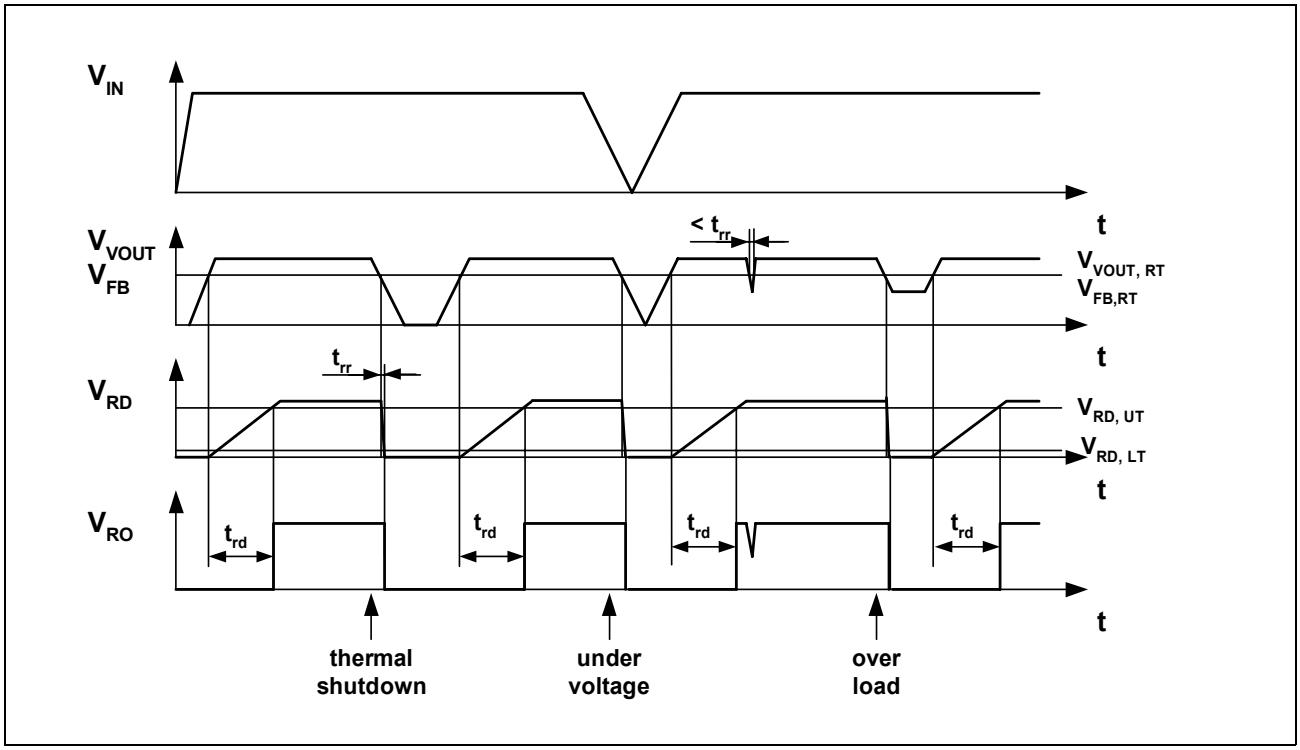


Figure 4 Reset timing

The reset delay time can be calculated with the following:

$$t_{rd} = \frac{V_{RD,\,UT}}{I_{RD,\,ch}} \cdot C_{RD}$$

where C_{RD} is the value of the delay capacitance, $V_{RD,UT}$ the upper reset timing threshold and $I_{RD,\,ch}$ the reset delay charging current.

7.7 100% duty-cycle operation and dropout

The **TLE6389** operates with a duty cycle up to 100%. This feature allows to operate with the lowest possible drop voltage at low battery voltage as it occurs at cold cranking. The MOSFET is turned on continuously when the supply voltage approaches the output voltage level, conventional switching regulators with less than 100% duty cycle would fail in that case.

The drop- or dropout voltage is defined as the difference between the input and output voltage levels when the input is low enough to drop the output out of regulation. Dropout

depends on the MOSFET drain-to-source on-resistance, the current-sense resistor and the inductor series resistance. It is proportional to the load current:

$$V_{drop} = I_{LOAD} \cdot (R_{DS(ON)PMOS} + R_{SENSE} + R_{INDUCTANCE})$$

7.8 SYNC Input and Frequency Control

The **TLE6389**'s internal oscillator is set for a fixed PWM switching frequency of 360kHz or can be synchronized to an external clock at the SYNC pin. When the internal clock is used SYNC has to be connected to GND. SYNC is a negative-edge triggered input that allows synchronization to an external frequency ranging between 270kHz and 530kHz. When SYNC is clocked by an external signal, the converter operates in PWM mode until the load current drops below the PWM to PFM threshold. Thereafter the converter continues operation in PFM mode.

7.9 Shutdown Mode

Connecting ENABLE to GND places the **TLE6389GV** in shutdown mode. In shutdown, the reference, control circuitry, external switching MOSFET, and the oscillator are turned off and the output falls to 0V. Connect ENABLE to voltages higher than 4.5V for normal operation.

7.10 Buck converter circuit

A typical choice of external components for the buck converter circuit is given in figure 2 and 3. For basic operation of the buck converter the input capacitors C_{IN1}, C_{IN2}, the driver supply capacitor C_{BDS}, the sense resistor R_{SENSE}, the PMOS device, the catch diode D1, the induuctance L1 and the output capacitor C_{OUT} are necessary. In addition for low electromagnetic emission a Pi-filter at the input and/or a small resistor in the path between GDRV and the gate of the PMOS may be necessary.

7.10.1 Buck inductance (L1) selection in terms of ripple current:

The internal PWM/PFM control loop includes a slope compensation for stable operation in PWM mode. This slope compensation is optimzed for inductance values of 47µH and

Sense resistor values of 50mΩ for the 5V output voltage versions. When choosing an inductance different from 47µH the Sense resistor has to be changed also.

$$\frac{R_{SENSE}}{L1} = 1{,}064 \times 10^{3}$$

To achieve the same effect of slope compensation in the adjustable voltage version also the inductance in µH is given by

$$(94 \cdot V_{VOUT} \cdot R_{SENSE}) < L1 < (188 \cdot V_{VOUT} \cdot R_{SENSE})$$

The inductance value determines together with the input voltage, the output voltage and the switching frequency the current ripple which occurs during normal operation of the step down converter. This current ripple is important for the all over ripple at the output of the switching converter. .

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{f_{SW} \cdot V_{IN} \cdot L1}$$

When picking finally the inductance of a certain supplier (Epcos, Coilcraft etc.) the saturation current has to be considered. The saturation current value of the desired inductance has to be higher than the maximum load current which can appear in the actual application.

7.10.2 Determining the current limit

The peak current which the buck converter is able to provide is determined by the peak current limit threshold voltage V_{LIM} and the sense resistor R_{SENSE}. With a maximum peak

current given by the application ($I_{PEAK, PWM}=I_{LOAD}+0.5\Delta I$) the sense resistor is calculated to

$$R_{SENSE} = \frac{V_{LIM}}{2 \cdot I_{PEAK, PWM}}$$

7.10.3 PFM and PWM thresholds

The crossovering thresholds PFM to PWM and vice versa strongly depend on the input voltage V_{IN}, the Buck converter inductance L1, the sense resistor value R_{SENSE} and the turn on and turn off delays of the external PMOS.

For more details on the PFM to PWM and PWM to PFM thresholds please refer to the application note “TLE6389 - Determining PFM/PWM current thresholds”.

7.10.4 Buck output capacitor (C_{OUT}) selection:

The choice of the output capacitor effects straight to the minimum achievable ripple which is seen at the output of the buck converter. In continuous conduction mode the ripple of the output voltage equals:

$$V_{Ripple} = \Delta I \cdot \left(R_{ESRCOUT} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right)$$

From the formula it is recognized that the ESR has a big influence in the total ripple at the output, so low ESR tanatlum capacitors are recommended for the application.

One other important thing to note are the requirements for the resonant frequency of the output LC-combination. The choice of the components L and C have to meet also the specified range given in section 3 otherwise instabilities of the regulation loop might occur.

7.10.5 Input capacitor (C_{IN1}) selection:

At high load currents, where the current through the inductance flows continuously, the input capacitor is exposed to a square wave current with its duty cycle V_{OUT}/V_I. To

prevent a high ripple to the battery line a capacitor with low ESR should be used. The maximum RMS current which the capacitor has to withstand is calculated to:

$$I_{RMS} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{2 \cdot I_{LOAD}}\right)^2}$$

For low ESR an e.g. Al-electrolythic capacitance in parallel to an ceramic capacitance could be used.

7.10.6 Freewheeling diode / catch diode (D1)

For lowest power loss in the freewheeling path Schottky diodes are recommended. With those types the reverse recovery charge is neglectible and a fast handover from freewheeling to forward conduction mode is possible. Depending on the application (12V battery systems) 40V types could be also used instead of the 60V diodes. Also for high temperature operation select a Schottky-diode with low reverse leakage.

A fast recovery diode with recovery times in the range of 30ns can be also used if smaller junction capacitance values (smaller spikes) are desired.

7.10.7 Buck driver supply capacitor (C_{BDS})

The voltage at the ceramic capacitor is clamped internally to 7V, a ceramic type with a minimum of 220nF and voltage class 16V would be sufficient.

7.10.8 Input pi-filter components for reduced EME

At the input of Buck converters a square wave current is observed causing electromagnetical interference on the battery line. The emission to the battery line consists on one hand of components of the switching frequency (fundamental wave) and its harmonics and on the other hand of the high frequency components derived from the current slope. For proper attenuation of those interferers a π-type input filter structure is recommended which is built up with inductive and capacitive components in addition to the Input caps C_{IN1} and C_{IN2}. The inductance can be chosen up to the value of the Buck converter inductance, higher values might not be necessary, the additional capacitance should be a ceramic type in the range up to 100nF.

Inexpensive input filters show due to their parasitrics a notch filter characteristic, which means basically that the lowpass filter acts from a certain frequency as a highpass filter and means further that the high frequency components are not attenuated properly. To slower down the slopes at the gate of the PMOS switch and get down the emission in the high frequency range a small gate resistor can be put between GDRV and the PMOS gate.

7.11 Components recommendation - overview

Device	Type	Supplier	Remark
C_{IN1}	Electrolythic /Foil type	various	100µF, 60V
C_{IN2}	Ceramic	various	220nF, 60V
L1	B82464-A4473	EPCOS	47µH, 1.6A, 145mΩ
	B82479-A1473-M	EPCOS	47µH, 3.5A, 47mΩ
	DO3340P-473	Coilcraft	47µH, 3.8A, 110mΩ
	DO5022P-683	Coilcraft	68µH, 3.5A, 130mΩ
	DS5022P-473	Coilcraft	47µH, 4.0A, 97mΩ
M1	BSO 613SPV	Infineon	60V, 3.44A, 130mΩ, NL
	BSP 613P	Infineon	60V, 2.9A, 130mΩ, NL
	SPD09P06PL	Infineon	60V, 9A, 250mΩ, LL
C_{BDS}	Ceramic	various	220nF, 16V
D1	MBRD360	Motorola	Schottky, 60V, 3A
	MBRD340	Motorola	Schottky, 40V, 3A
	SS34	various	Schottky, 40V, 3A
C_{OUT}	B45197-A2107	EPCOS	Low ESR Tantalum, 100µF, 10V

7.12 Layout recommendation

The most sensitive points for Buck converters - when considering the layout - are the nodes at the input, output and the gate of the PMOS transistor and the feedback path.

For proper operation and to avoid stray inductance paths the external catch diode, the Buck inductance and the input capacitor C_{IN1} have to be connected as close as possible to the PMOS device. Also the GDRV path from the controller to the MosFet has to be as short as possible. Best suitable for the connection of the cathode of the catch diode and one terminal of the inductance would be a small plain located next to the drain of the PMOS.

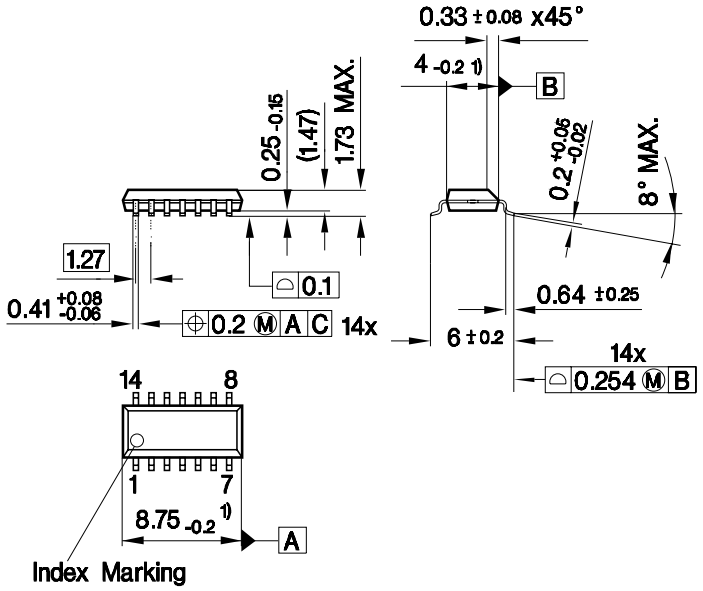
The GND connection of the catch diode must be also as short as possible. In general the GND level should be implemented as surface area over the whole PCB as second layer, if necessary as third layer. The feedback path has to be well grounded also, a ceramic capacitance might help in addition to the output cap to avoid spikes.

To obtain the optimum filter capability of the input pi-filter it has to be located also as close as possible to the input. To filter the supply input of the device (VS) the ceramic cap should be connected directly to the pin.

As a guideline an EMC optimized application board / layout is available.

8 Package Outlines:

Dimensions in mm



1) Does not include plastic or metal protrusion of 0.15 max. per side

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