

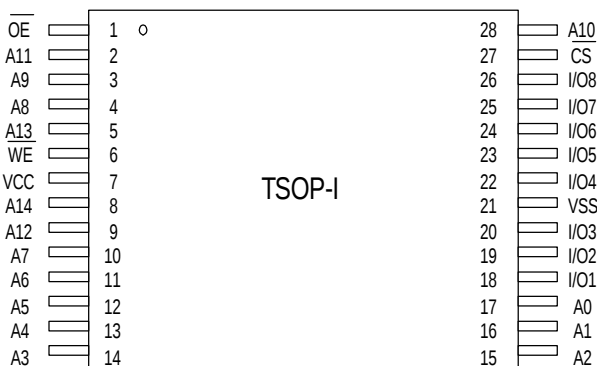
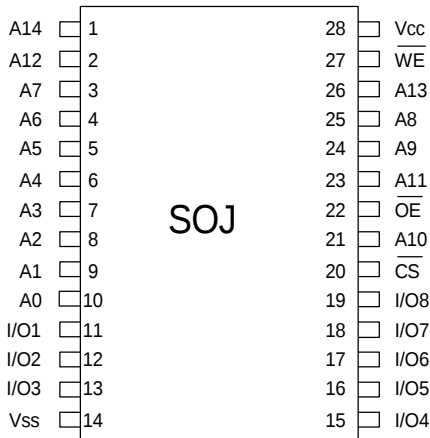
SRAM

32K X 8 HIGH SPEED
CMOS STATIC RAM

FEATURES

- High speed access time: 8/10/12/15ns(max.)
- Low power consumption : Active 300 mW (typ.)
- Single + 3.3 power supply
- Fully static operation – No clock or refreshing required
- All inputs and outputs directly LVTTTL compatible
- Common I/O capability
- Available packages :28-pin 300 mil, SOJ and TSOP-I (forward type).
- Output enable ($\overline{OE}$) available for very fast access

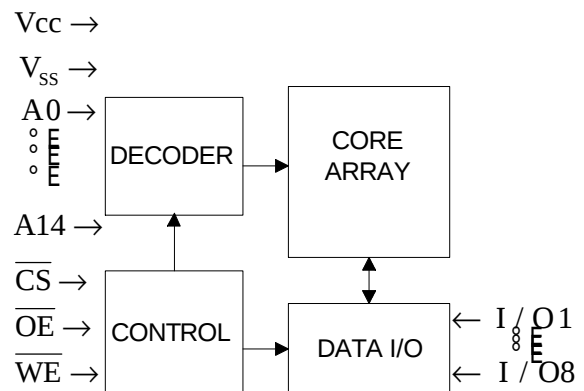
PIN CONFIGURATION



GENERAL DESCRIPTION

The T14L256A is a high speed, low power CMOS static RAM organized as 32,768 x 8 bits that operates on a single 3.3-volt power supply. This device is packaged in a standard 28-pin 300 mil SOJ or TSOP-I forward.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground

PART NUMBER EXAMPLES

	PACKAGE	SPEED
T14L256A-8J	SOJ	8ns
T14L256A-8P	TSOP-I	8ns

DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to + 4.6	V
Inputs to Vss Potential	-0.5 to Vcc +0.5	V
Power Dissipation	1.0	W
Storage Temperature	-60 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	Typ-5%	3.3	Typ+5%	V
Input Voltage, low	V _{IL}	-0.3	-	0.8	V
Input Voltage, high	V _{IH}	2.1	-	Vcc+0.3	V
Ambient Temperature	T _A	0	-	70	°C

TRUTH TABLE

CS	OE	WE	MODE	I/O1- I/O8	Vcc
H	X	X	Not Selected	High-Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High-Z	Icc
L	L	H	Read	Data Out	Icc
L	X	L	Write	Data In	Icc

OPERATING CHARACTERISTICS

(Vcc = 3.3V± 5%, Vss = 0V, Ta = 0 to 70°C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Leakage Current	I _{LI}	Vin=Vss to Vcc		-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} =Vss to Vcc , $\overline{CS} = V_{IH}$ or OE= V _{IH} or $\overline{WE} = V_{IL}$		-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = + 8.0mA		-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = - 4.0mA		2.4	-	-	V
Operating Power Supply Current	I _{CC}	$\overline{CS} = V_{IL}$, I/O=0mA	8	-	-	110	mA
		Cycle = MIN. Duty = 100%	10	-	-	100	mA
			12	-	-	90	mA
			15	-	-	80	mA
Standby Power Supply Current	I _{SB}	$\overline{CS} = V_{IH}$, Cycle=MIN, Duty=100%		-	-	15	mA
	I _{SB1}	$\overline{CS} \geq V_{CC}$ -0.2V		-	-	2	mA

Note: Typical characteristics are at Vcc = 3.3V, Ta = 25°C

CAPACITANCE

(V_{CC} = 3.3V, T_a = 25°C, f = 1 MHz)

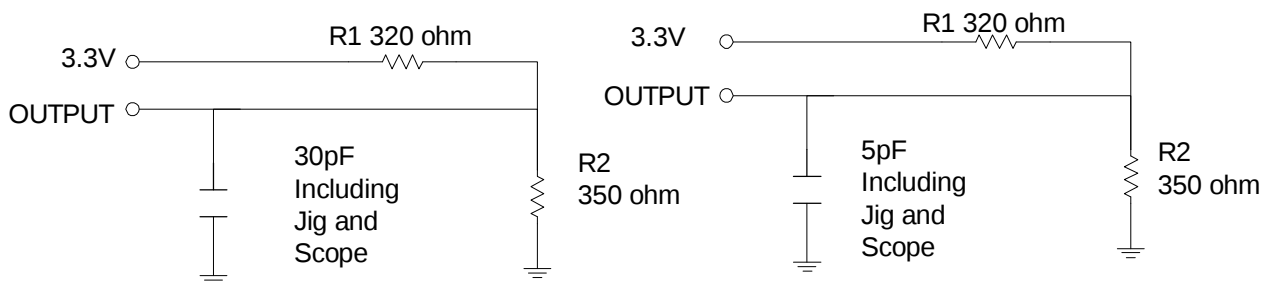
PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/ Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

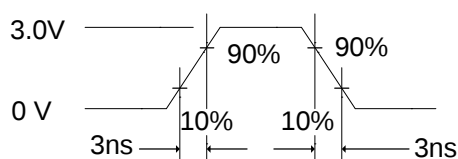
AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 30pF, I _{OH} /I _{OL} = -4mA/8mA

AC TEST LOADS AND WAVEFORM



(For T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ}, T_{WHZ}, T_{OW})



AC CHARACTERISTICS

($V_{CC}=3.3V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^{\circ}C$)

(1) READ CYCLE

PARAMETER	SYM.	T14L256A-8		T14L256A-10		T14L256A-12		T14L256A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	8	ϕW	10	ϕW	12	ϕW	15	ϕW	ns
Address Access Time	T_{AA}	ϕW	8	ϕW	10	ϕW	12	ϕW	15	ns
Chip Select Access Time	T_{ACS}	ϕW	8	ϕW	10	ϕW	12	ϕW	15	ns
Output Enable to Output Valid	T_{AOE}	ϕW	5	ϕW	6	ϕW	7	ϕW	7	ns
Chip Selection to Output in Low Z	T_{CLZ}^*	3	ϕW	3	ϕW	3	ϕW	3	ϕW	ns
Output Enable to Output in Low Z	T_{OLZ}^*	0	ϕW	0	ϕW	0	ϕW	0	ϕW	ns
Chip Deselection to Output in High Z	T_{CHZ}^*	ϕW	4	ϕW	5	ϕW	6	0	7	ns
Output Disable to Output in High Z	T_{OHZ}^*	ϕW	4	ϕW	5	ϕW	6	0	7	ns
Output Hold from Address Change	T_{OH}	2.5	ϕW	3	ϕW	3	ϕW	3	ϕW	ns

* These parameters are sampled but not 100% tested.

(2)WRITE CYCLE

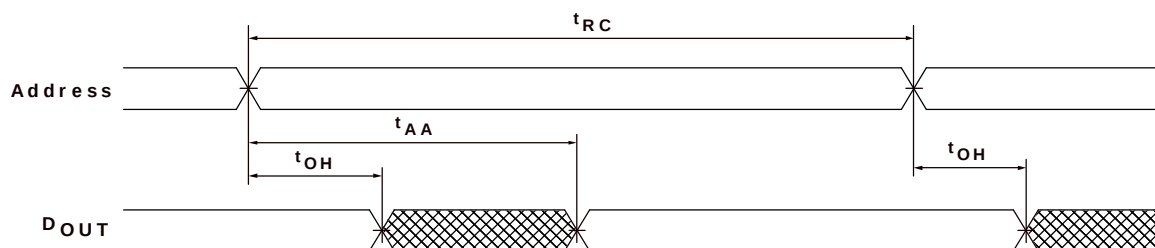
PARAMETER	SYM.	T14L256A-8		T14L256A-10		T14L256A-12		T14L256A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	T_{WC}	8	ϕW	10	ϕW	12	ϕW	15	ϕW	ns
Chip Selection to End of Write	T_{CW}	6	ϕW	8	ϕW	10	ϕW	11	ϕW	ns
Address Valid to End of Write	T_{AW}	6	ϕW	8	ϕW	10	ϕW	11	ϕW	ns
Address Setup Time	T_{AS}	0	ϕW	0	ϕW	0	ϕW	0	ϕW	ns
Write Pulse Width	T_{WP}	6	ϕW	8	ϕW	10	ϕW	11	ϕW	ns
Write Recovery Time	T_{WR}	0	ϕW	0	ϕW	0	ϕW	0	ϕW	ns
Data Valid to End of Write	T_{DW}	5	ϕW	6	ϕW	8	ϕW	8	ϕW	ns
Data Hold from End of Write	T_{DH}	0	ϕW	0	ϕW	0	ϕW	0	ϕW	ns
Write to Output in High Z	T_{WHZ}^*	ϕW	4	ϕW	5	ϕW	6	ϕW	6	ns
Output Disable to Output in High Z	T_{OHZ}^*	ϕW	4	ϕW	5	ϕW	6	ϕW	7	ns
Output Active from End of Write	T_{OW}	0	ϕW	0	ϕW	0	ϕW	0	ϕW	ns

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

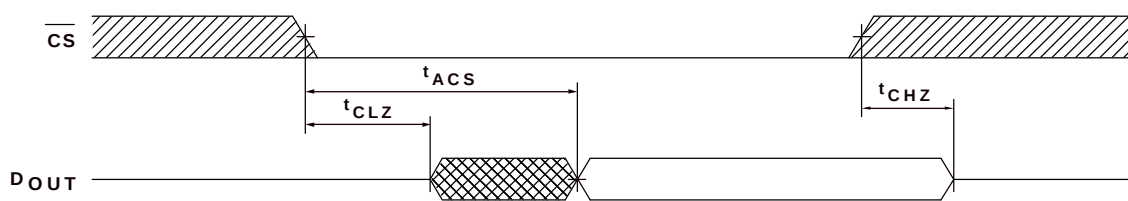
READ CYCLE 1

(Address Controlled)



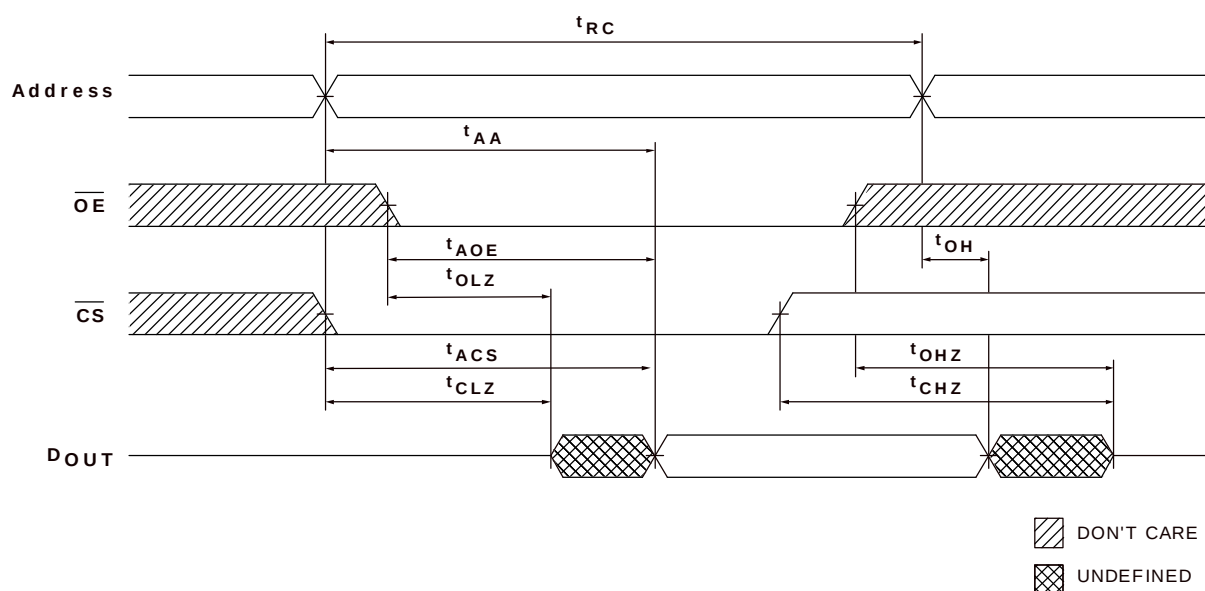
READ CYCLE 2

(Chip Select Controlled)

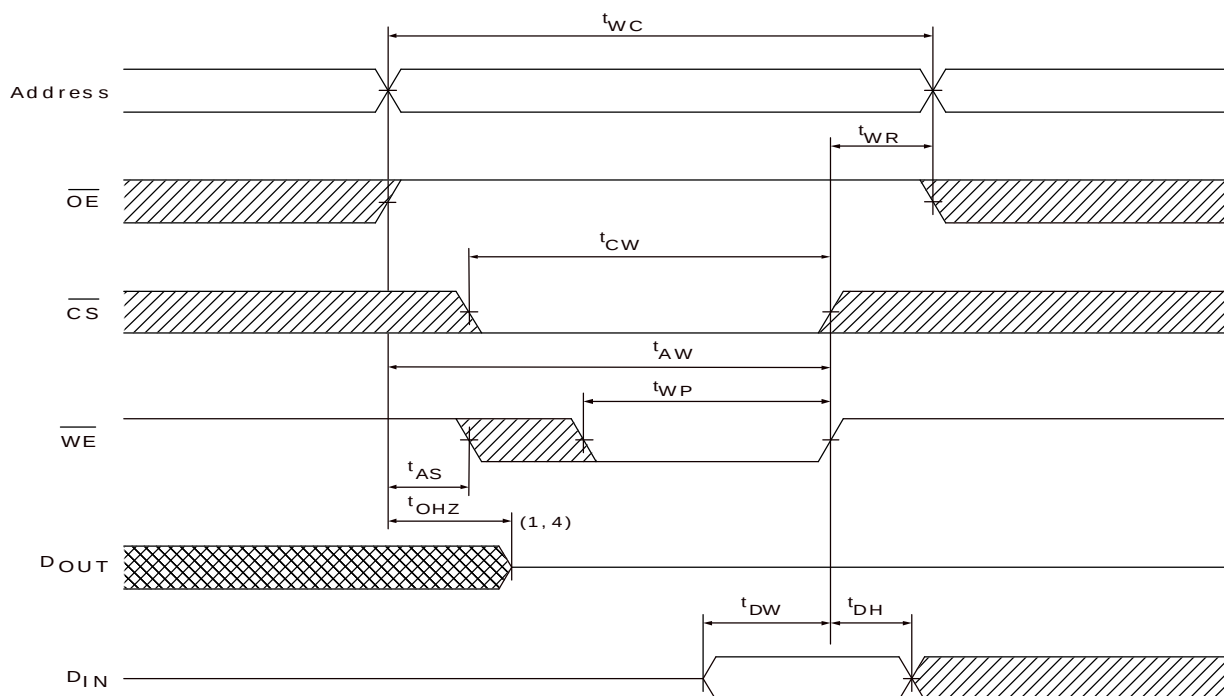


READ CYCLE 3

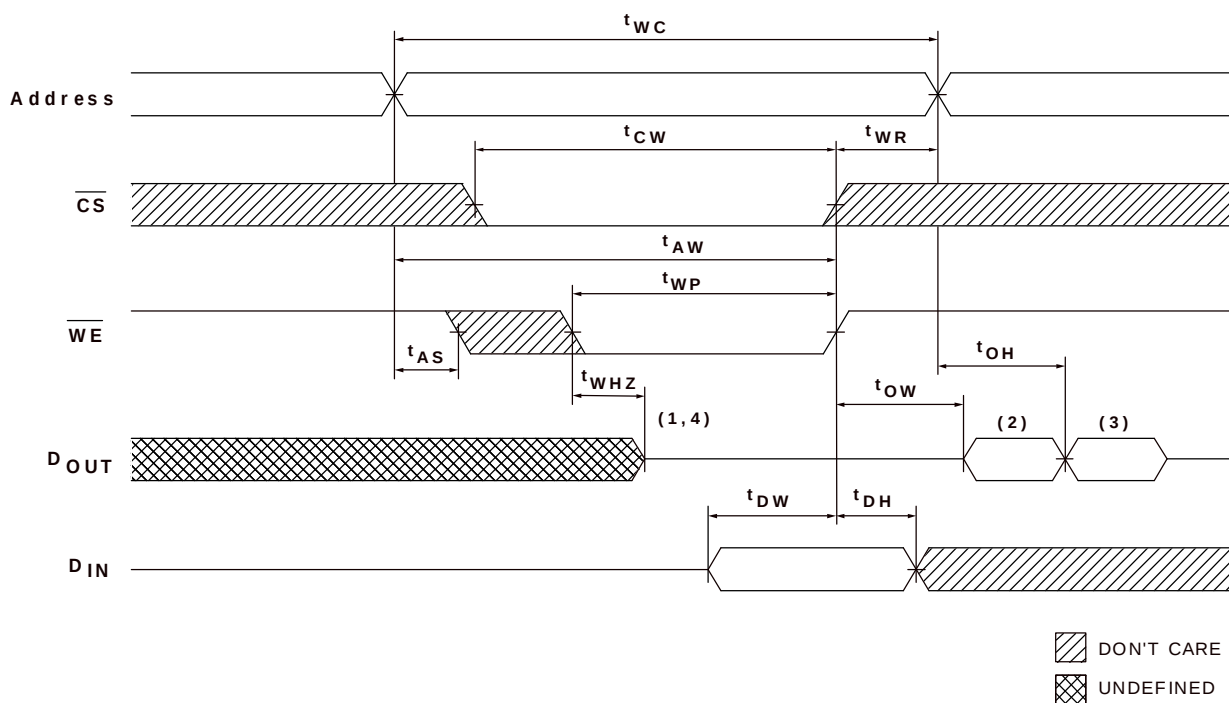
(Output Enable Controlled)



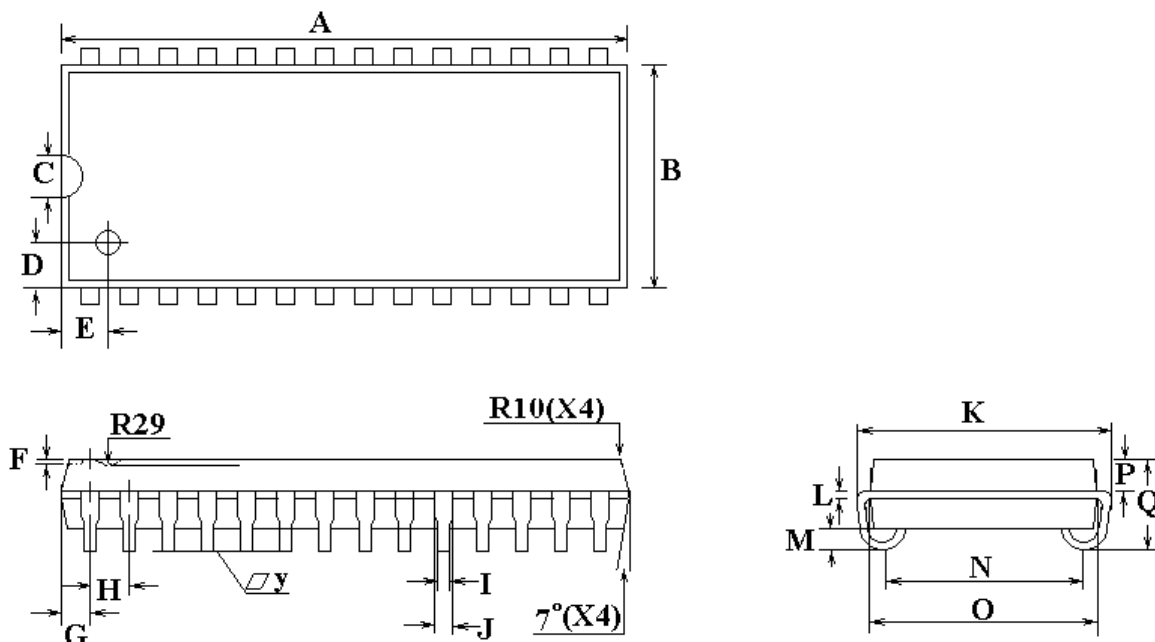
WRITE CYCLE 1 ($\overline{\text{OE}}$ CLOCK)



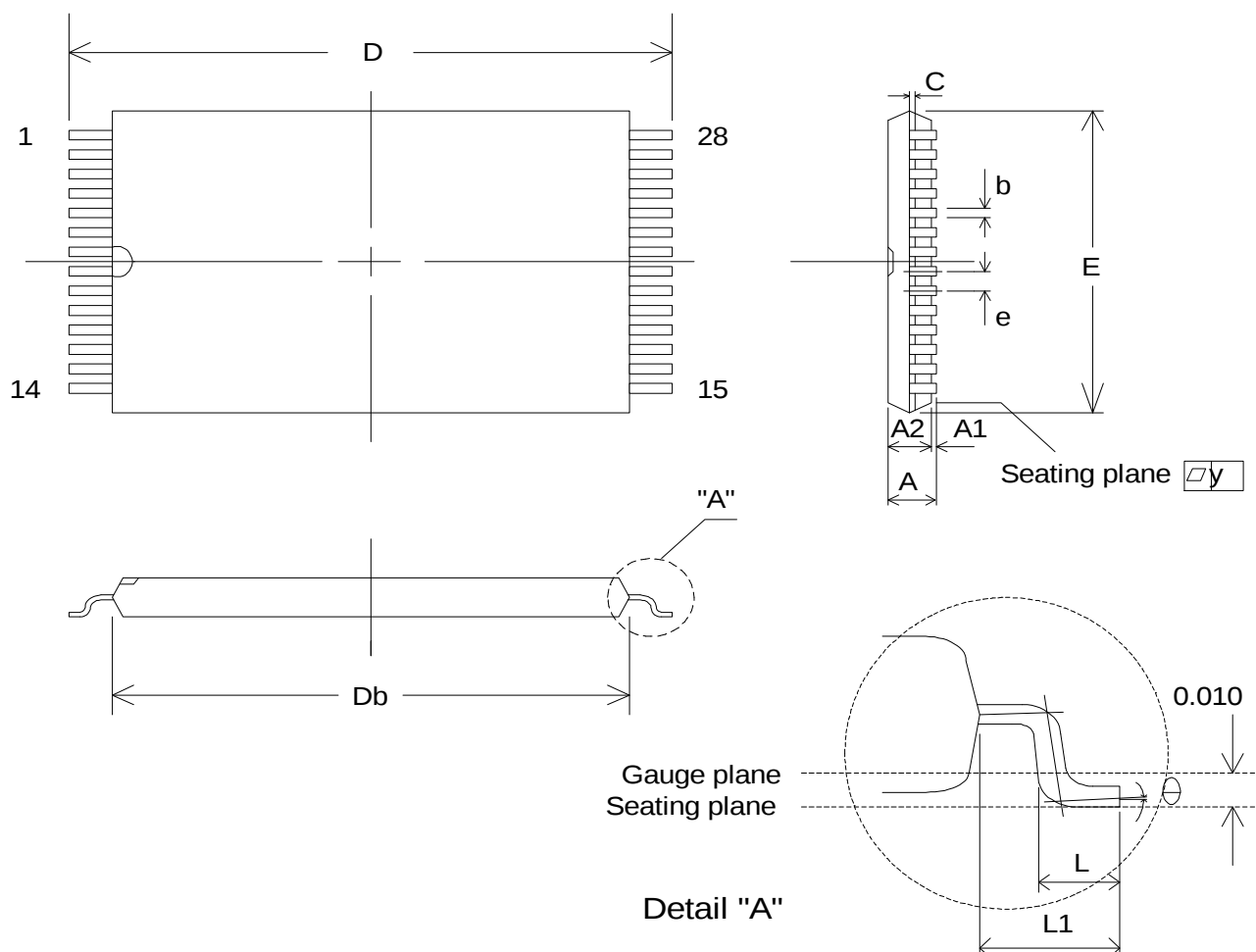
WRITE CYCLE 2 ($\overline{\text{OE}} = V_{\text{IL}}$ Fixed)



- Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5\text{pF}$. This parameter is guaranteed but not 100% tested.
5. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

PACKAGE DIMENSIONS
28-LEAD SOJ SRAM (300 mil)


SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.710±0.002	18.03±0.05
B	0.336±0.003	8.53±0.08
C	0.060±0.002	1.52±0.05
D	0.050±0.001	1.27±0.03
E	0.063±0.001	1.63±0.03
F	0.015±0.002	0.38±0.05
G	0.030±0.002	0.76±0.05
H	0.050±0.002	1.27±0.05
I	0.018±0.002	0.46±0.05
J	0.028±0.002	0.71±0.05
K	0.337±0.002	8.56±0.05
L	0.010±0.001	0.25±0.03
M	0.026±0.002	0.66±0.05
N	0.268±0.003	6.81±0.08
O	0.300±0.002	7.62±0.05
P	0.053±0.001	1.35±0.03
Q	0.140±0.004	3.56±0.10
y	0.004(MAX)	0.10(MAX)

PACKAGE DIMENSIONS
28-LEAD TSOP-I SRAM (8X13.4mm)


SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(max.)	1.20(max.)
A1	0.004 ° Ø.002	0.10 ° Ø.05
A2	0.039 ° Ø.002	1.00 ° Ø.05
b	0.008(typ.)	0.20(typ.)
c	0.006(typ.)	0.15(typ.)
Db	0.465 ° Ø.004	11.80 ° Ø.10
E	0.315 ° Ø.004	8.00 ° Ø.10
e	0.022(typ.)	0.55(typ.)
D	0.528 ° Ø.008	13.40 ° Ø.20
L	0.020 ° Ø.004	0.50 ° Ø.10
L1	0.0315 ° Ø.004	0.80 ° Ø.10
y	0.004(max.)	0.10(max.)
£ K	0 £ 5 £ X	0 £ 5 £ X

