TLV431A, TLV431B

Low Voltage Precision Adjustable Shunt Regulator

The TLV431A and B series are precision low voltage shunt regulators that are programmable over a wide voltage range of 1.24V to 16V. The TLV431A series features a guaranteed reference accuracy of ±1.0% at 25°C and ±2.0% over the entire industrial temperature range of -40°C to 85°C. For TLV431B series, the accuracy is even higher, it's ±0.5% and ±1.0% respectively. These devices exhibit a sharp low current turn-on characteristic with a low dynamic impedance of 0.20 Ω over an operating current range of 100μA to 20mA. This combination of features makes this series an excellent replacement for zener diodes in numerous applications circuits that require a precise refrence voltage. When combined with an optocoupler, the TLV431A/B can be used as an error amplifier for controlling the feedback loop in isolated low output voltage (3.0 V to 3.3 V) switching power supplies. These devices are available in economical TO-92 and micro size TSOP-5 and SOT-23-3 packages.

Features

- Programmable Output Voltage Range of 1.24 V to 16 V
- Voltage Reference Tolerance ± 1.0% for A Series and ± 0.5%for B Series
- Sharp Low Current Turn-On Characteristic
- Low Dynamic Output Impedance of 0.20 Ω from 100 μA to 20 mA
- Wide Operating Current Range of 50 μA to 20 mA
- Micro Miniature TSOP-5, SOT-23-3 and TO-92 Packages

Applications

- Low Output Voltage (3.0 V to 3.3 V) Switching Power Supply Error Amplifier
- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Analog and Digital Circuits Requiring Precision References
- Low Voltage Zener Diode Replacements

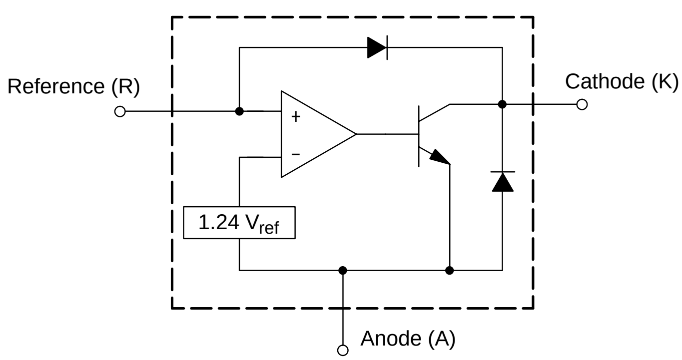
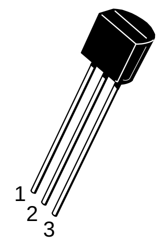


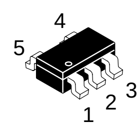
Figure 1. Representative Block Diagram

ON Semiconductor®

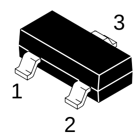
http://onsemi.com



TO-92
LP SUFFIX
CASE 29



TSOP-5
SN SUFFIX
CASE 483



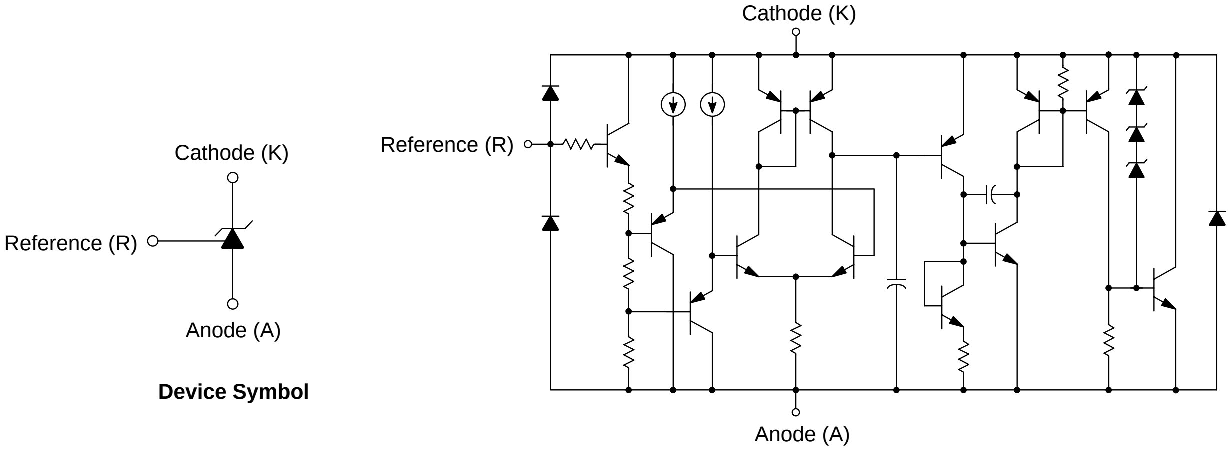
SOT-23-3
SN1 SUFFIX
CASE 318

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

DEVICE MARKING INFORMATION AND PIN CONNECTIONS

See general marking information in the device marking section on page 11 of this data sheet.



The device contains 13 active transistors.

Figure 2. Representative Device Symbol and Schematic Diagram

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	18	V
Cathode Current Range, Continuous (Note 1)	I_K	-20 to 25	mA
Reference Input Current Range, Continuous	I_{ref}	–0.05 to 10	mA
Thermal Characteristics LP Suffix Package, TO-92 Package Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case SN Suffix Package, TSOP-5 Package Thermal Resistance, Junction-to-Ambient SN1 Suffix Package, SOT-23-3 Package Thermal Resistance, Junction-to-Ambient	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 178 83 226 491	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range (Note 1)	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C

1. Maximum package power dissipation limits must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V.

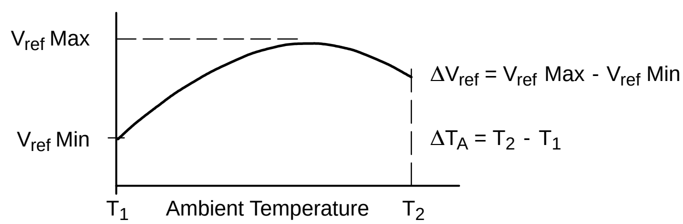
RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	16	V
Cathode Current	I_K	0.1	20	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	TLV431A Min	TLV431A Typ	TLV431A Max	TLV431B Min	TLV431B Typ	TLV431B Max	Unit
Reference Voltage (Figure 3) ($V_{KA} = V_{ref}$, I_K = 10 mA, T_A = 25°C) ($T_A = T_{low}$ to T_{high}, Note 2)	V_{ref}	1.228 1.215	1.240 -	1.252 1.265	1.234 1.228	1.240 -	1.246 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) ($V_{KA} = V_{ref}$, I_K= 10 mA, $T_A = T_{low}$ to T_{high}, Note 2)	ΔV_{ref}	-	7.2	20	-	7.2	20	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) ($V_{KA} = V_{ref}$ to 16 V, I_K= 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	-	-0.6	-1.5	-	-0.6	-1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open)	I_{ref}	-	0.15	0.3	-	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, Notes 2, 3)	ΔI_{ref}	-	0.04	0.08	-	0.04	0.08	μA
Minimum Cathode Current for Regulation (Figure 3)	$I_{K(min)}$	-	55	80	-	55	80	μA
Off-State Cathode Current (Figure 5) (V_{KA} = 6.0 V, V_{ref} = 0) (V_{KA} = 6.0 V, V_{ref} = 0)	$I_{K(off)}$	- -	0.01 0.012	0.04 0.05	- -	0.01 0.012	0.04 0.05	μA
Dynamic Impedance (Figure 3) ($V_{KA} = V_{ref}$, I_K =0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 4)	$\lvert Z_{KA} \rvert$	-	0.25	0.4	-	0.25	0.4	Ω

2. Ambient temperature range: T_{low} = −40°C, T_{high} = 85°C.
3. The deviation parameters ΔV_{ref} and ΔI_{ref} are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{(\Delta V_{ref})}{V_{ref}\ (T_A = 25°C)} \times 10^6\right)}{\Delta T_A}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV_{ref} = 7.2 mV and the slope is positive,
V_{ref} @ 25°C = 1.241 V
ΔT_A = 125°C

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\frac{0.0072}{1.241} \times 10^6}{125} = 46\ ppm/°C$$

4. The dynamic impedance Z_{KA} is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$\left|Z_{KA}'\right| = \left|Z_{KA}\right| \times \left(1 + \frac{R1}{R2}\right)$$

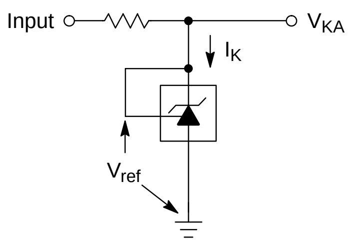


Figure 3. Test Circuit for $V_{KA} = V_{ref}$

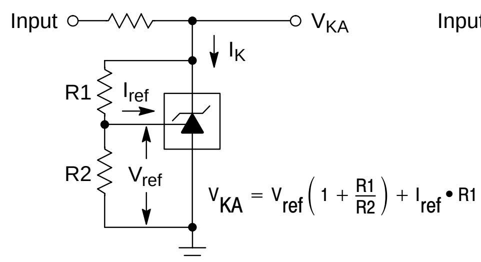


Figure 4. Test Circuit for $V_{KA} > V_{ref}$

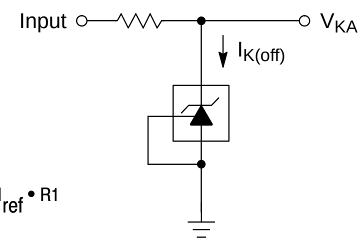


Figure 5. Test Circuit for $I_{K(off)}$

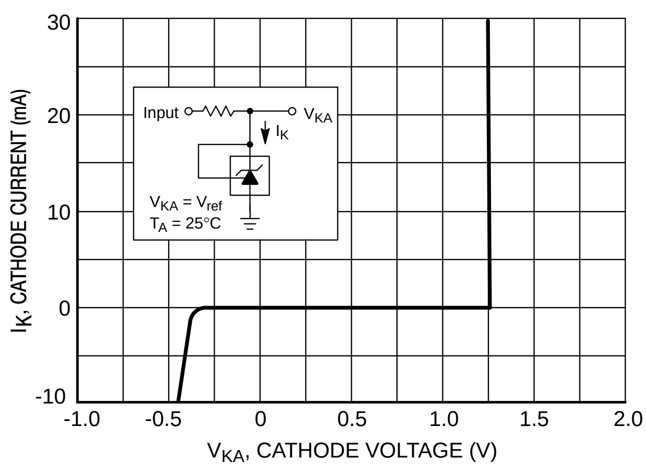


Figure 6. Cathode Current vs. Cathode Voltage

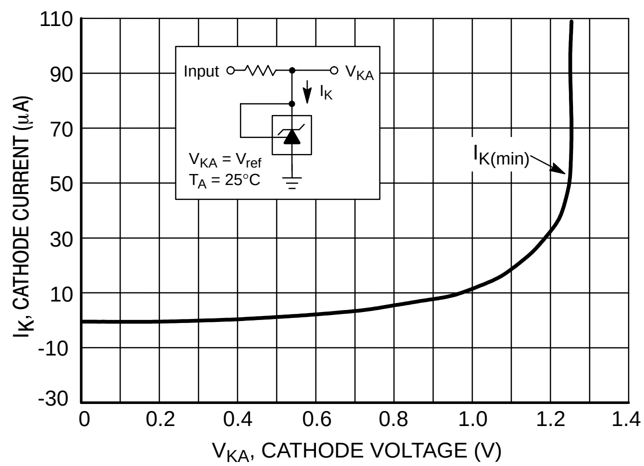


Figure 7. Cathode Current vs. Cathode Voltage

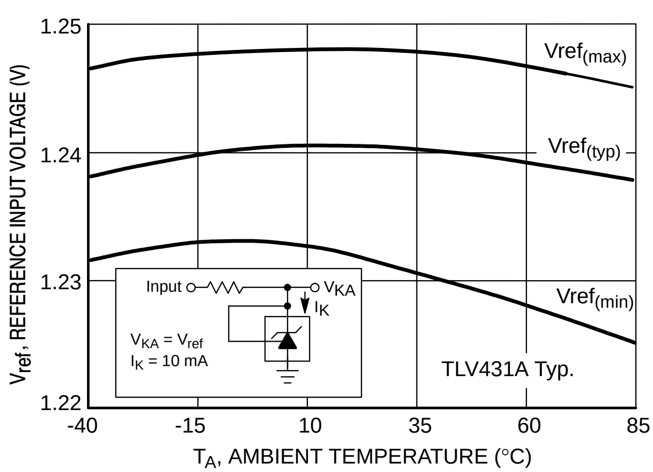


Figure 8. Reference Input Voltage versus Ambient Temperature

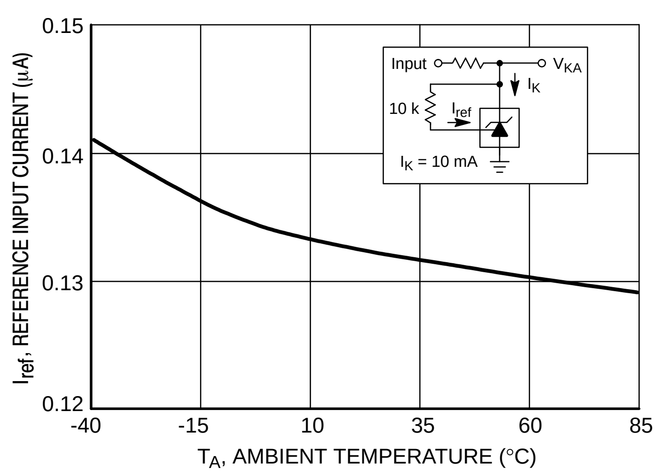


Figure 9. Reference Input Current versus Ambient Temperature

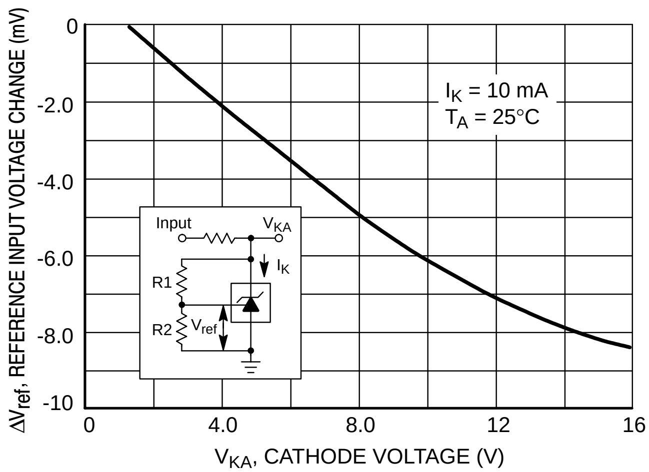


Figure 10. Reference Input Voltage Change versus Cathode Voltage

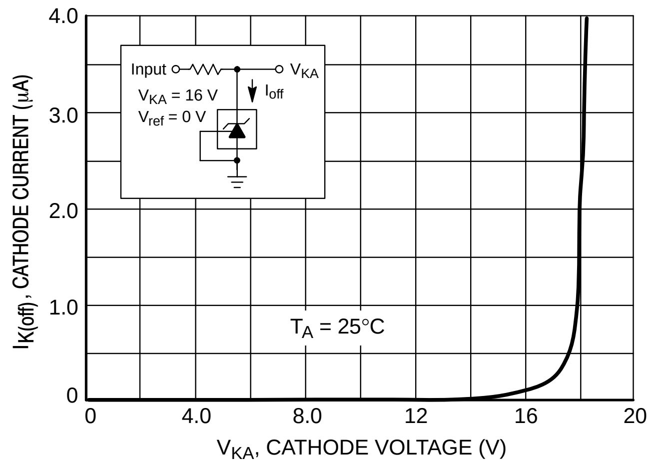


Figure 11. Off-State Cathode Current versus Cathode Voltage

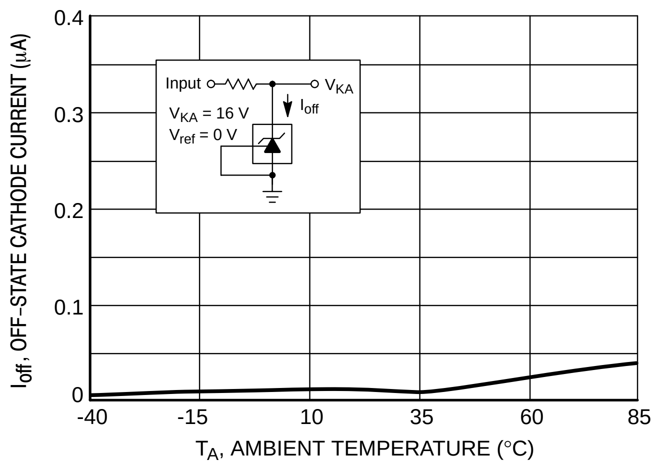


Figure 12. Off-State Cathode Current versus Ambient Temperature

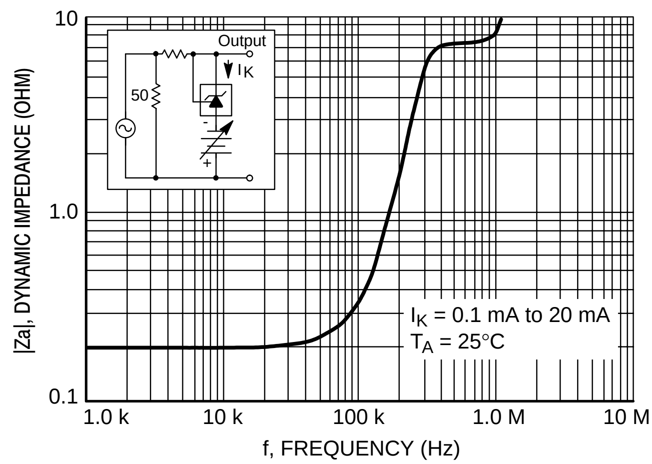


Figure 13. Dynamic Impedance versus Frequency

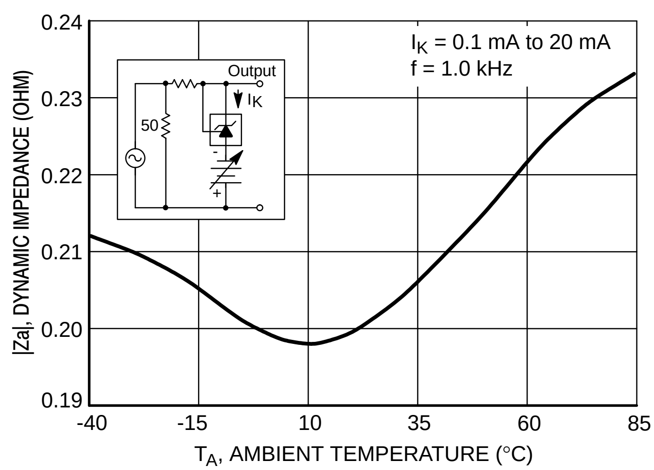


Figure 14. Dynamic Impedance versus Ambient Temperature

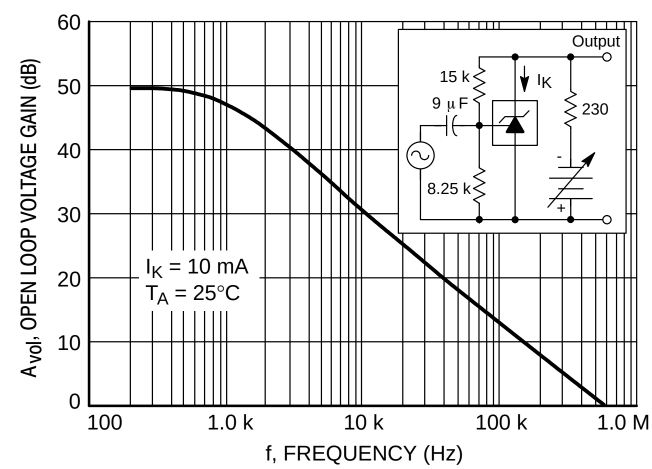


Figure 15. Open-Loop Voltage Gain versus Frequency

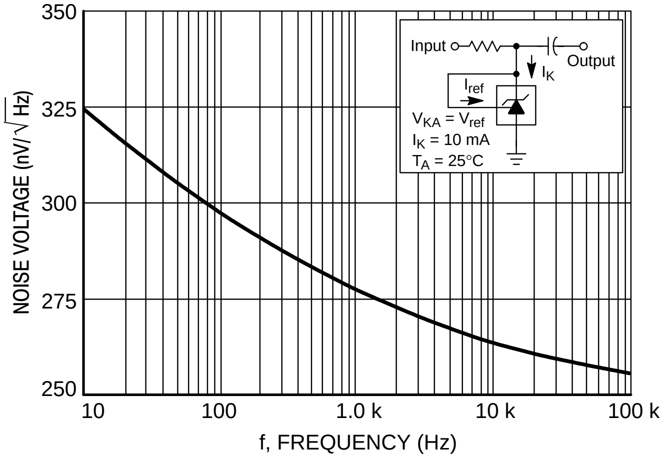


Figure 16. Spectral Noise Density

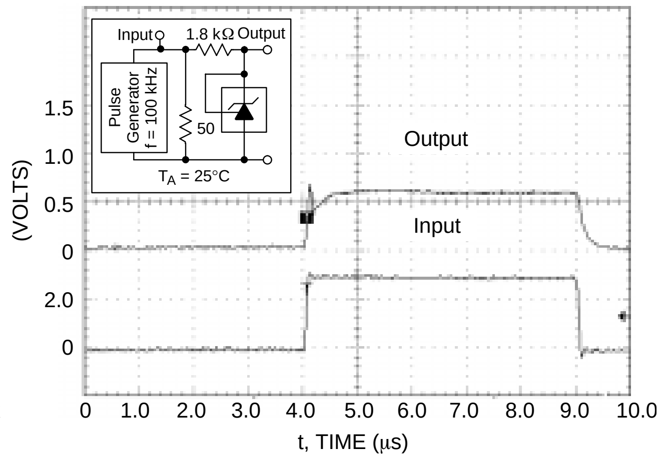


Figure 17. Pulse Response

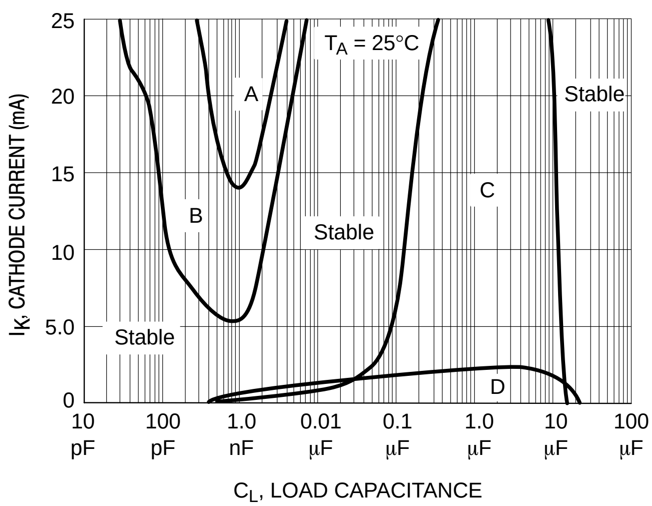
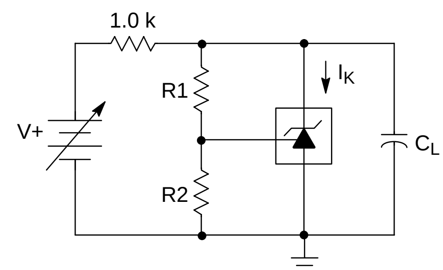


Figure 18. Stability Boundary Conditions



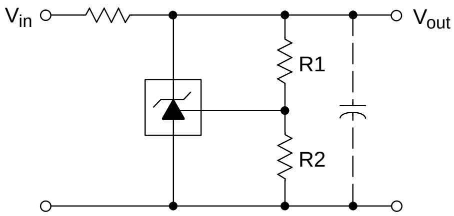
Unstable Regions	V_{KA} (V)	R1 (kΩ)	R2 (kΩ)
A, C	V_{ref}	0	∞
B, D	5.0	30.4	10

Figure 19. Test Circuit for Figure 18

Stability

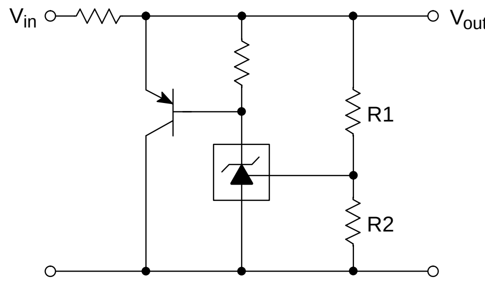
Figures 18 and 19 show the stability boundaries and circuit configurations for the worst case conditions with the load capacitance mounted as close as possible to the device. The required load capacitance for stable operation can vary depending on the operating temperature and capacitor equivalent series resistance (ESR). Ceramic or tantalum surface mount capacitors are recommended for both temperature and ESR. The application circuit stability should be verified over the anticipated operating current and temperature ranges.

TYPICAL APPLICATIONS



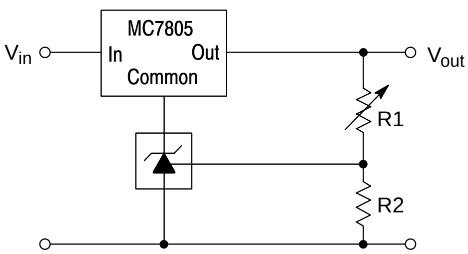
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 20. Shunt Regulator



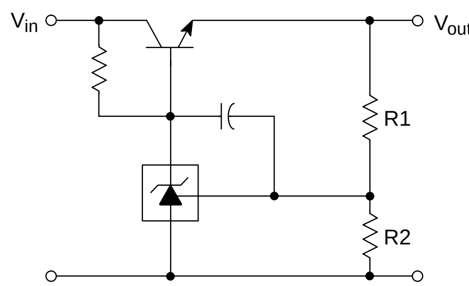
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 21. High Current Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$
$$V_{out(min)} = V_{ref} + 5.0\ V$$

Figure 22. Output Control for a Three Terminal Fixed Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$
$$V_{out(min)} = V_{ref} + V_{be} \approx 2.0\ V$$

Figure 23. Series Pass Regulator

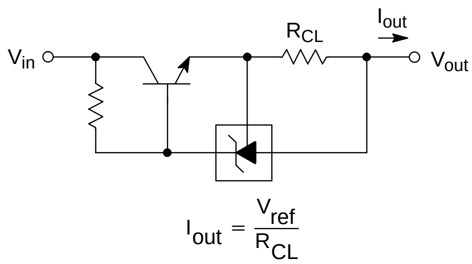


Figure 24. Constant Current Source

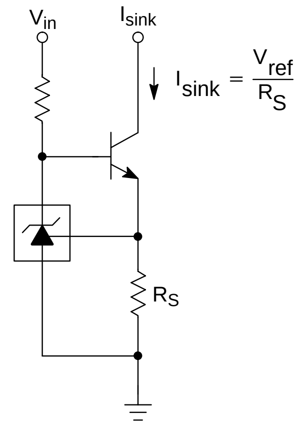


Figure 25. Constant Current Sink

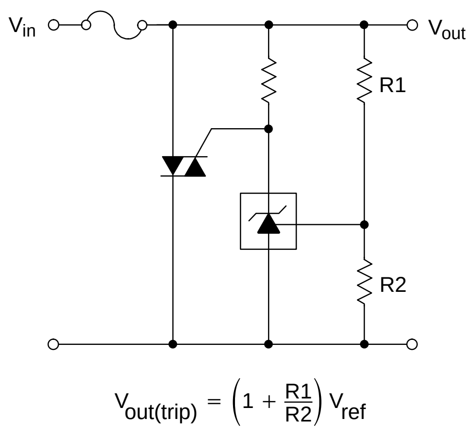


Figure 26. TRIAC Crowbar

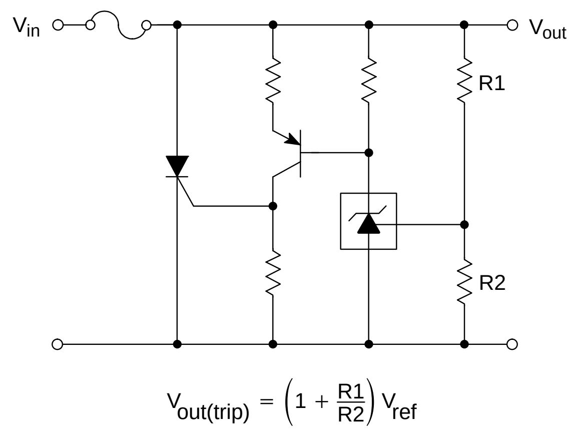
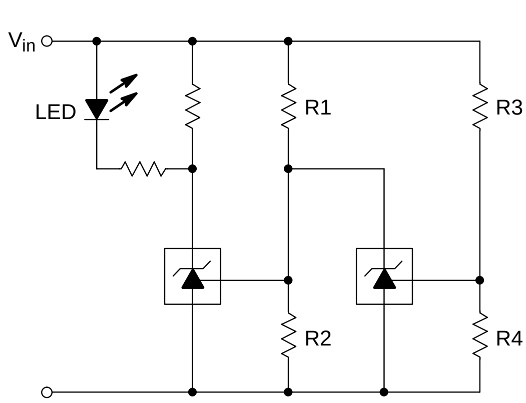


Figure 27. SCR Crowbar

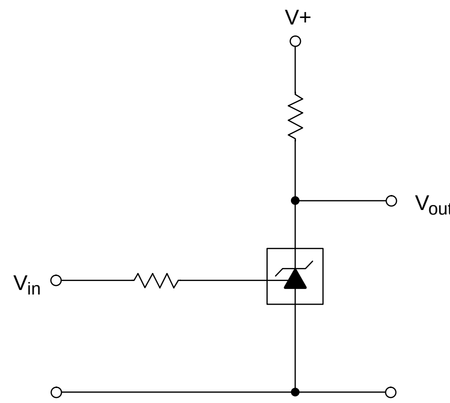


L.E.D. indicator is 'ON' when V_{in} is between the upper and lower limits,

$$\text{Lower limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 28. Voltage Monitor



V_{in}	V_{out}
$< V_{ref}$	V+
$> V_{ref}$	≈ 0.74 V

Figure 29. Single-Supply Comparator with Temperature-Compensated Threshold

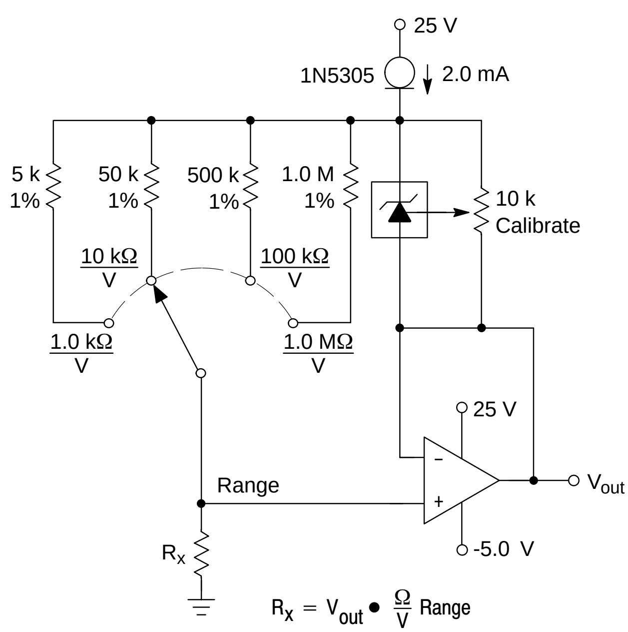


Figure 30. Linear Ohmmeter

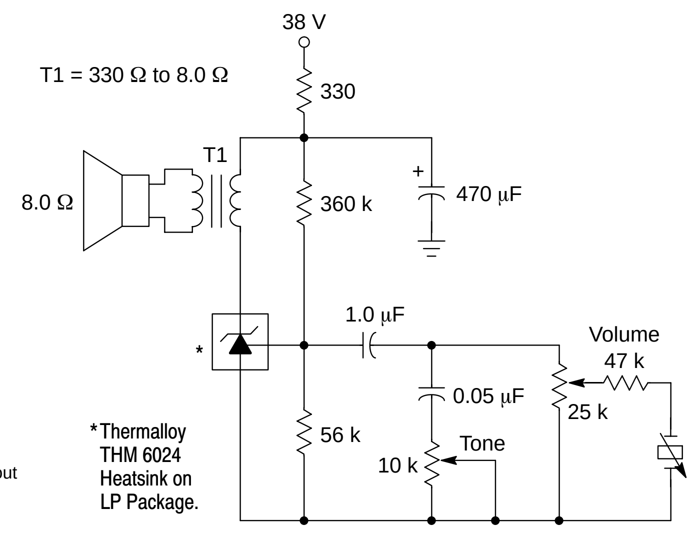


Figure 31. Simple 400 mW Phono Amplifier

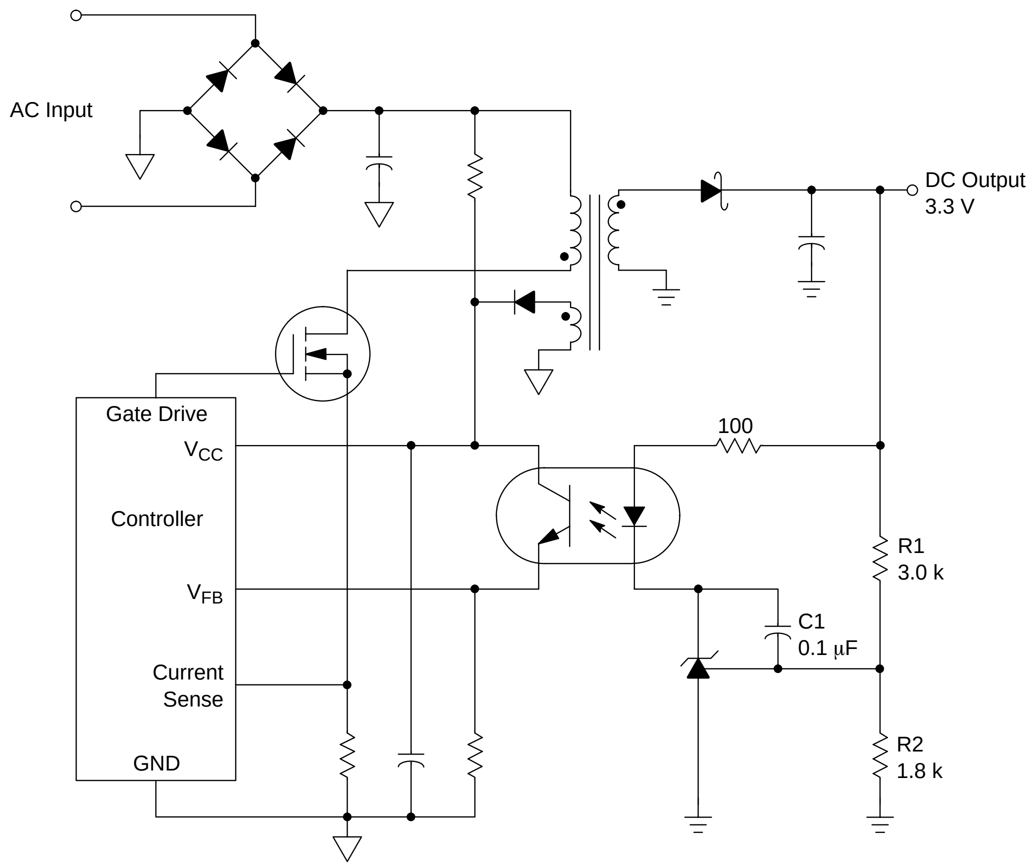
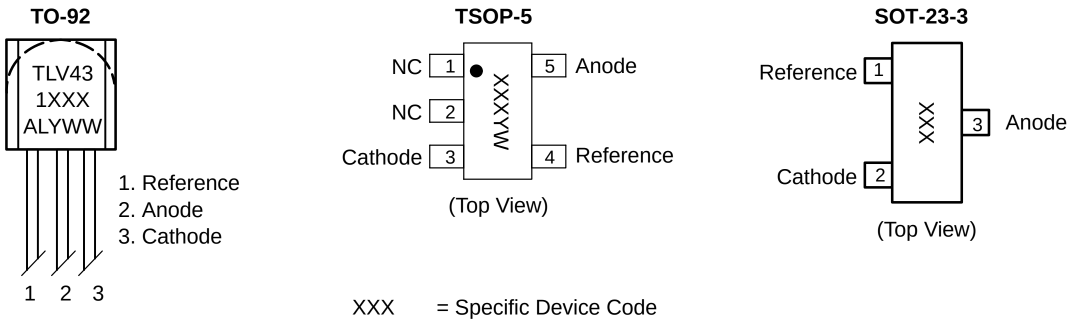


Figure 32. Isolated Output Line Powered Switching Power Supply

The above circuit shows the TLV431A/B as a compensated amplifier controlling the feedback loop of an isolated output line powered switching regulator. The output voltage is programmed to 3.3 V by the resistors values selected for R1 and R2. The minimum output voltage that can be programmed with this circuit is 2.64 V, and is limited by the sum of the reference voltage (1.24 V) and the forward drop of the optocoupler light emitting diode (1.4 V). Capacitor C1 provides loop compensation.

PIN CONNECTIONS AND DEVICE MARKING



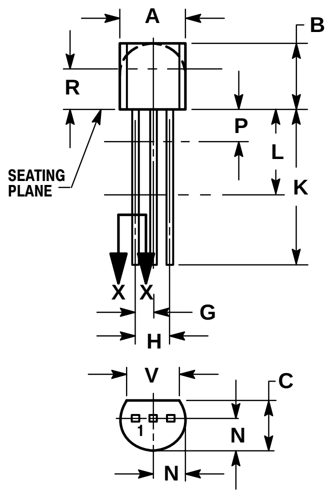
XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW, W = Work Week

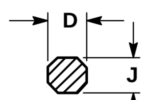
DEVICE ORDERING INFORMATION

Device	Device Code	Package	Shipping
TLV431ALP	ALP	TO-92	6000/Box
TLV431ALPRA	ALP	TO-92	2000/Tape & Reel
TLV431ALPRE	ALP	TO-92	2000/Tape & Reel
TLV431ALPRM	ALP	TO-92	2000/Ammo Pack
TLV431ALPRP	ALP	TO-92	2000/Ammo Pack
TLV431ASNT1	RAA	TSOP-5	3000/Tape & Reel
TLV431ASN1T1	RAF	SOT-23-3	3000/Tape & Reel
TLV431BLP	BLP	TO-92	6000/Box
TLV431BLPRA	BLP	TO-92	2000/Tape & Reel
TLV431BLPRE	BLP	TO-92	2000/Tape & Reel
TLV431BLPRM	BLP	TO-92	2000/Ammo Pack
TLV431BLPRP	BLP	TO-92	2000/Ammo Pack
TLV431BSNT1	RAH	TSOP-5	3000/Tape & Reel
TLV431BSN1T1	RAG	SOT-23-3	3000/Tape & Reel

PACKAGE DIMENSIONS

TO-92
LP SUFFIX
PLASTIC PACKAGE
CASE 29-11
ISSUE AL



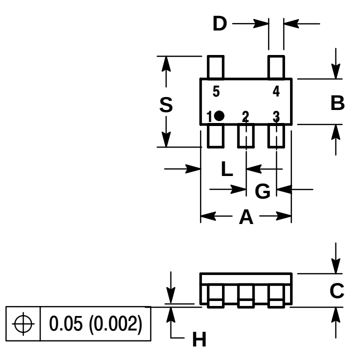


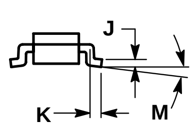
SECTION X-X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

TSOP-5
SN SUFFIX
PLASTIC PACKAGE
CASE 483-01
ISSUE B



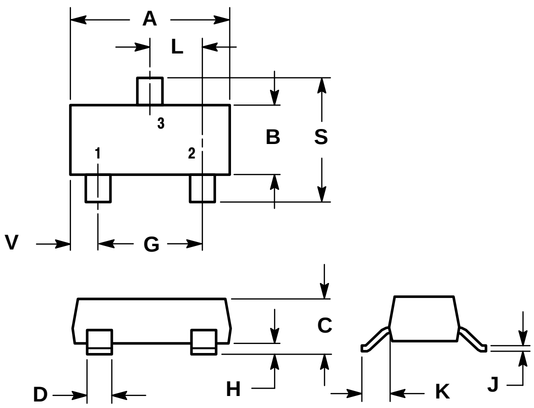


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

PACKAGE DIMENSIONS

SOT-23-3
SN1 SUFFIX
PLASTIC PACKAGE
CASE 318-09
ISSUE AH

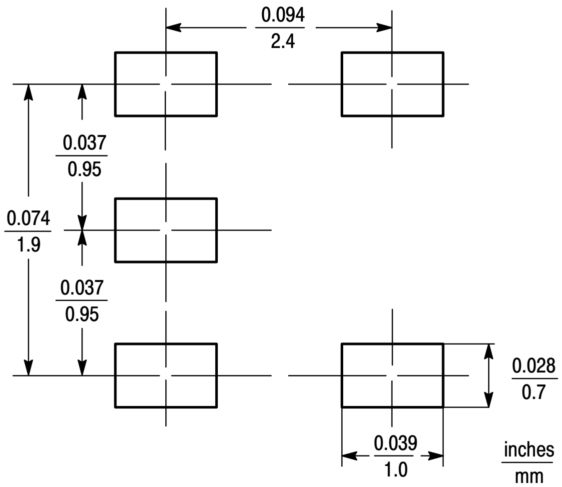


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01, −02, AND −06 OBSOLETE, NEW STANDARD 318−09.

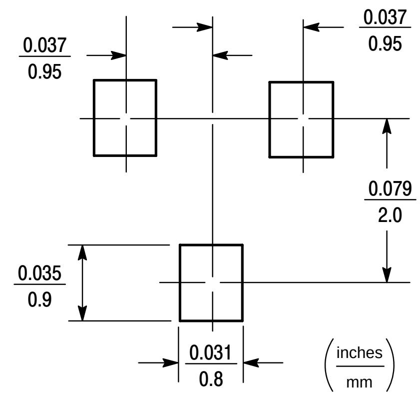
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
H	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



TSOP-5
(Footprint Compatible with SOT-23-5)



SOT-23-3

PUBLICATION ORDERING INFORMATION

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