



**PHAST-12E Device**  
**Programmable, High Performance ATM/PPP/TDM**  
**SONET/SDH Terminator for Level 12 with Enhanced Features**  
**TXC-06212**

**PRODUCT INFORMATION**

**FEATURES**

- Supports simultaneous termination of ATM, POS, and TDM (Time Division Multiplexed, e.g., VT1.5, VC-4 etc.) traffic
- Integrated clock recovery and synthesis for four 155.52 Mbit/s signals or one 622 Mbit/s signal
- STS-12/STS-12c/STM-4/STM-4c, or quad STS-3c/STM-1 framing and performance monitoring
- Complete Transport/Section Overhead processing and generation per Bellcore and ITU-T standards
- Complete Path Overhead processing and generation for one STS-12/STS-12c/STM-4/STM-4c signal or for four STS-3c/STM-1 signals for ATM/PPP
- VC-4 cross connect for STS-12, STM-4, and 4xSTS-3c/STM-1 operation
- Loop timing mode selectable from one of the four recovered clocks or from a separate reference clock input.
- APS for ATM/PPP payloads using the UTOPIA port(s)
- Cell or frame delineation function for four STS-3c/STM-1 or one STS-12/STS-12c/STM-4/STM-4c signal.
- "PPP" support per RFC1662 and RFC2615 for all inputs
- UTOPIA L2 (cell) 8/16-bit interface at 25 MHz/50 MHz
- UTOPIA L2P (frame) 16-bit interface at 50 MHz
- Quad byte-parallel Telecom Bus at 19.44 Mbyte/s
- Access to Line or Section DCC via a port
- Ring port for UPSR support
- Selectable Intel/Motorola-compatible microprocessor interface
- Boundary scan capability (IEEE 1149.1)
- +3.3 V  $\pm 5\%$  I/O and +2.5 V  $\pm 5\%$  CORE power supplies
- 2.2 W (four 155 Mbit/s interfaces),  
1.5 W (one interface at 622 Mbit/s)
- 675-lead enhanced plastic ball grid array package

**DESCRIPTION**

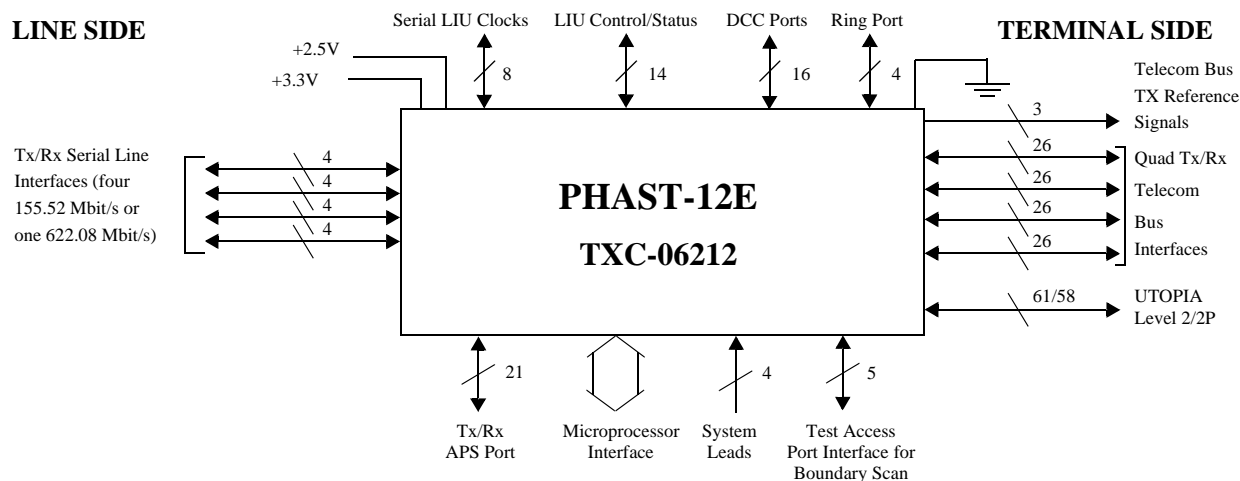
The PHAST-12E is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines or a single STS-12/12c or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s signals or single 622.08 Mbit/s serial operation.

The PHAST-12E can terminate ATM payloads from any of the above signals into a 16-bit or 8-bit UTOPIA Level 2 PHY interface. PPP payloads are terminated into a 16-bit wide UTOPIA Level 2P interface. STM (VT/TU) payloads can be terminated into four 8-bit wide Telecom Bus interfaces. The PHAST-12E facilitates multiservice applications by providing simultaneous termination of ATM, Packet over SONET/SDH (POS), and TDM traffic that are contained in separate SPEs/VCs. When terminating concatenated payloads, the four Telecom Bus interfaces act in concert as a single 32-bit wide Telecom Bus interface. Single-device APS switching or 1:N APS between multiple PHAST-12E devices is also provided for ATM and PPP payloads.

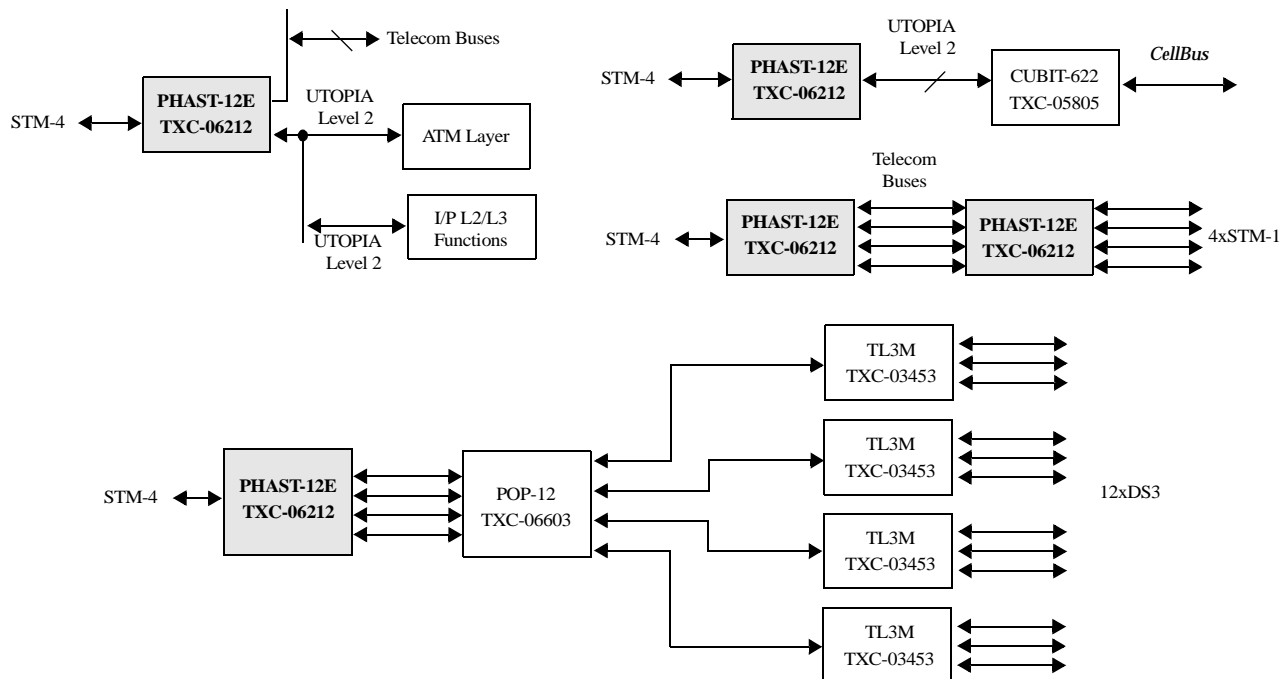
**APPLICATIONS**

- Multiservice applications
- SONET/SDH add/drop or higher order terminal multiplexers
- Transport of ATM/PPP or VT/TU payloads over SONET/SDH
- Transmission of E1/DS1, E3/DS3 or E4 over SONET/SDH
- ATM and packet switches

**LINE SIDE**



### APPLICATION DIAGRAM



Note: Instead of connecting to the 2.488 Gbit/s PHY device, the serial interfaces of each PHAST-12E device can be connected to a 622 Mbit/s fiber optic transceiver for STS-12/STS-12c/STM-4/STM-4c operation. Alternatively, four 155 Mbit/s fiber optic transceivers can be connected to the line interfaces of each PHAST-12E device for quad STS-3c/STM-1 applications.

### RELATED PRODUCTS

- TXC-03452B Level 3 Mapper/Desynchronizer VLSI Device (L3M)
- TXC-03453 Triple Level 3 Mapper VLSI Device (TL3M)
- TXC-03456 Level 4 Mapper/Desynchronizer VLSI Device (L4M)
- TXC-04222 21/28 Channel Dual Bus High Density mapper VLSI Device (TEMx28)
- TXC-04228 DS1 Mapper 28-Channel Device (T1Mx28)
- TXC-05804 CellBus Bus Switch VLSI Device (CUBIT-3)
- TXC-05805 Multi-PHY CellBus Switch access VLSI Device (CUBIT-622)
- TXC-06101 SONET STS-1 Overhead Terminator VLSI Device (PHAST-1)
- TXC-06103 STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator with Telecom Bus Interface VLSI Device (PHAST-3N)
- TXC-06112 Programmable, High-Performance ATM/Packet/Transmission SONET/SDH Terminator for Level 12 VLSI Device (PHAST-12)
- TXC-06203 STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface VLSI Device (PHAST-3P)
- TXC-06603 OC-12 SONET/SDH Path Overhead Processor, Retimer and Cross Connect VLSI Device (POP-12)

### FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products.

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Document Number:  
TXC-06212-MC  
Ed. 3, February 2002