# PHAST-3N
# STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator with Telecom Bus Interface
# TXC-06103

**PRODUCT INFORMATION**

## FEATURES

- Bit-serial SDH/SONET line interface
  - Pseudo-ECL interface with clock recovery and synthesis
- Byte-parallel SDH/SONET line interface
  - Parity detection/generation with optional frame pulse input
- Section, line, and path overhead byte processing
  - RAM access for overhead bytes
  - Line AIS, REI (FEBE) and RDI detection
  - B2 and B3 byte BIP detection with BER measurement
  - J0 byte TIM or single-byte comparison
  - S1 byte change in synchronization status
  - J1 byte TIM or 64-byte LF/CR alignment
  - C2 byte PSL, unequipped, PDI detection
  - G1 byte RDI (single-bit or three-bit), path REI (FEBE) detection
  - H4 byte multiframe detection with optional V1 pulse generation
- Section, line and path overhead byte insertion
  - From RAM, interfaces, terminal, ring (mate device) or receive side (e.g., RDI)
- Supports 1+1 or 1:N APS applications
- N1 byte tandem connection processing (STM-1 VC-4 format)
- Interfaces
  - TOH (RSOH & MSOH) bytes with programmable marker pulse
  - K1/K2 APS bytes, E1 and E2 order wire bytes
  - Section data communication (D1-D3) bytes
  - Line data communication (D4-D12) bytes
  - POH bytes (for VC-4 or each STS-1)
  - Alarm Indication Port (AIP) for line/path ring operation
  - Scan and drive leads (two each)
- Telecom Bus terminal interface
  - Clock, byte data, parity, C1J1V1, SPE, POH byte, AIS indication, bus active indication
- Tributary unequipped/AIS generation for TUG-3, TU-2/VT6, TU-12/VT2 and TU-11/VT1.5
- Telecom Bus terminal interface source timing mode
  - Transmit timing for downstream devices from reference clock and frame pulse
- Receive and transmit pointer rejustification to receive and transmit reference clock and frame pulse
- Receive pointer tracking
  - AIS, LOP, NDF and false pointer detection,
- Receive and transmit line/path AIS generation
- Motorola or Intel microprocessor interface for memory access
- Boundary scan, loopbacks, and optional PRBS generator/detector
- Single +3.3 volt, ±5% power supply; 5 volt tolerant inputs
- 256-lead, 27 mm x 27 mm, plastic ball grid array package
- Device driver:
  - Insulates application from register access details
  - Driver APIs configure and manage the PHAST-3N device
  - Default configurations are provided within the driver
  - One command configures all the control registers
  - Driver can download the firmware code into PHAST-3N
  - Similar architecture to other device drivers, such as the TL3M

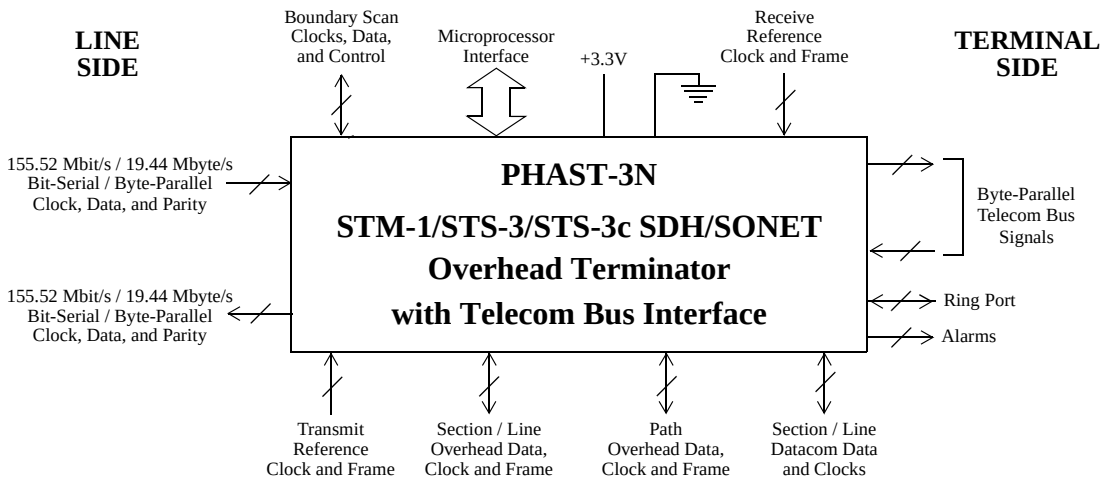
## DESCRIPTION

The TranSwitch PHAST-3N (TXC-06103) is an STM-1/STS-3/ STS-3c section, line and path overhead termination device that provides a terminal side Telecom Bus interface. The PHAST-3N device provides either a serial or parallel interface on the line side. The serial interface provides 155 MHz clock recovery and clock synthesis. Line and section overhead bytes are processed. The PHAST-3N performs pointer tracking, and receive and transmit pointer justification. The PHAST-3N also performs POH byte processing. TOH (RSOH and MSOH) and POH bytes are written into RAM locations for microprocessor access or provided via interfaces for external access. In the transmit direction, the PHAST-3N will either interface to downstream timing or provide the timing signals. The transmit POH bytes can be inserted from RAM, a serial POH interface, a mate PHAST-3N device for path and line ring applications, or directly from the terminal side.

The PHAST-3N can generate line and path AIS in the receive and transmit directions. For testing, the device provides boundary scan, a PRBS generator and analyzer, B2 and B3 byte BER measurements, programmable BIP error mask generation, line and terminal loopback, and STS-1 terminal loopback. The device provides either Motorola or Intel microprocessor access. Performance counters can be configured to be saturating or roll-over. The interrupts, with mask bits, can be programmed for activation on positive, negative, or positive and negative alarm transitions, or positive levels. A software polling register is also provided.

## APPLICATIONS

- Telecom Bus applications for TU/VT mappers
- Line and path ring applications
- Add/drop multiplexers
- Cross connect systems
- Data communications systems







Document Number:
TXC-06103-MC
Ed. 4, November 2001



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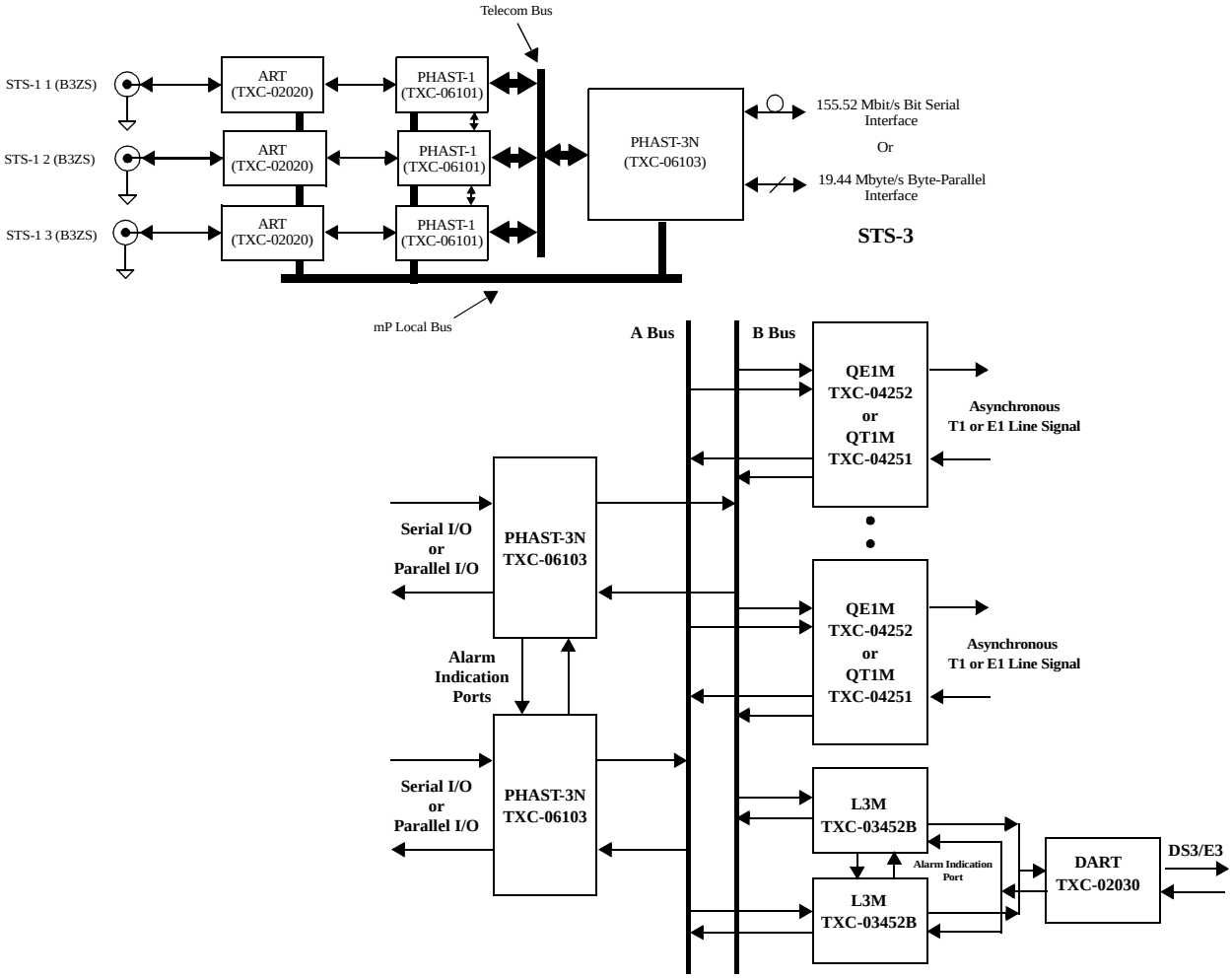
## APPLICATION DIAGRAMS




## RELATED PRODUCTS

- TXC-02020 Advanced STS-1/DS3 Receiver/Transmitter VLSI Device (ART)
- TXC-02030 Advanced E3/DS3/STS-1 Receiver/Transmitter VLSI Device (DART)
- TXC-03452B Level 3 Mapper VLSI Device (L3M)
- TXC-03453 Triple Level 3 Mapper VLSI Device (TL3M)
- TXC-03456 Level 4 Mapper VLSI Device (L4M)
- TXC-04201 DS1 Mapper 7-Channel VLSI Device (DS1MX7)
- TXC-04216 Sixteen channel E1 to AU-4/VT2 or TU-12 Async Mapper-Desync Device (E1Mx16)
- TXC-04228 DS1 Mapper 28-Channel Device (T1Mx28)
- TXC-04251 Quad T1 Mapper VLSI Device (QT1M)
- TXC-04252 Quad E1 Mapper VLSI Device (QE1M)
- TXC-06101 SONET STS-1 Overhead Terminator VLSI Device (PHAST-1)

## FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products.



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