- **Support for 6-Bit as Well as 8-Bit Video Inputs, With On-Chip Dithering**
- **FlatLink™ Input Interface for Low EMI and Power**
- **Mini-LVDS Intra-Panel Interface Towards Column Drivers**
- **DE-Only Mode of Operation**
- **Tolerates Spread Spectrum Clock at the Input, With SSC Pass-Thru to the Outputs**
- **Support for SSC at the Outputs by Using External SSC Generation**
- **Flexible Control Outputs With User-Programmable Timings**
- **Support for 2-Level and 3-Level Gate Drivers**
- **Optional Serial EEPROM for Fine Tuning Timing During Development**
- **Four Default Timing Sets Provided On-Chip**
- **Fail-Safe Circuit Detects Off-Spec Conditions and Generates Timing Signals Internally**
- **Operating Voltage Range: 2.7 to 3.6 V**

description

The TFP74X3 is a programmable timing controller for TFT LCD panels, supporting resolutions from XGA up to QXGA. It resides on the panel and provides the interface between graphics controllers and the TFT-LCD system, routing video data and generating timing signals for the panel.

The host interface is FlatLink, which is a proven, low-power, and low-EMI serial interface. Mini-LVDS, an advanced serial intra-panel interface, is used between the TFP74X3 and the column drivers, resulting in improved EMI performance and lower power consumption.

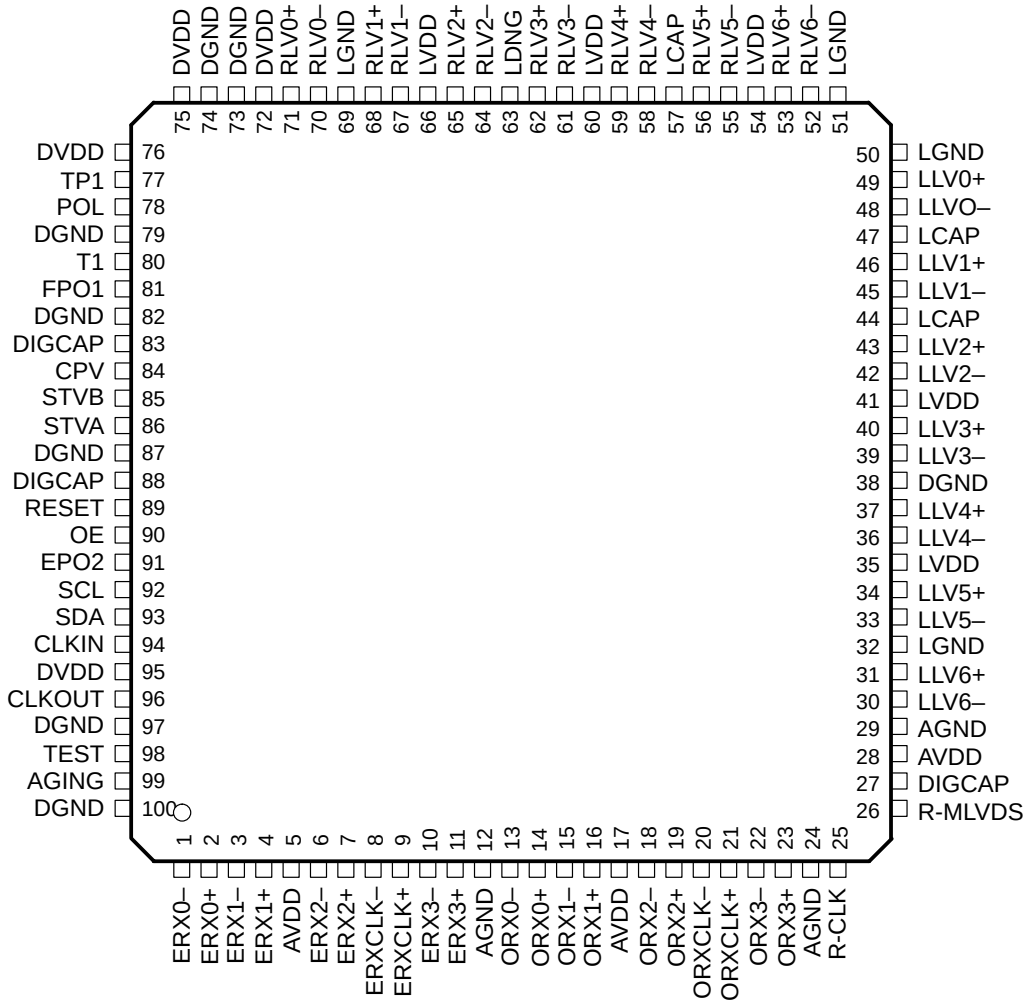
Control outputs with user-programmable timings are available to control source and gate drivers. Additional control outputs are available to sequence the panel power supplies. The TFP74X3 can be configured from an optional external serial EEPROM.

PRODUCT PREVIEW

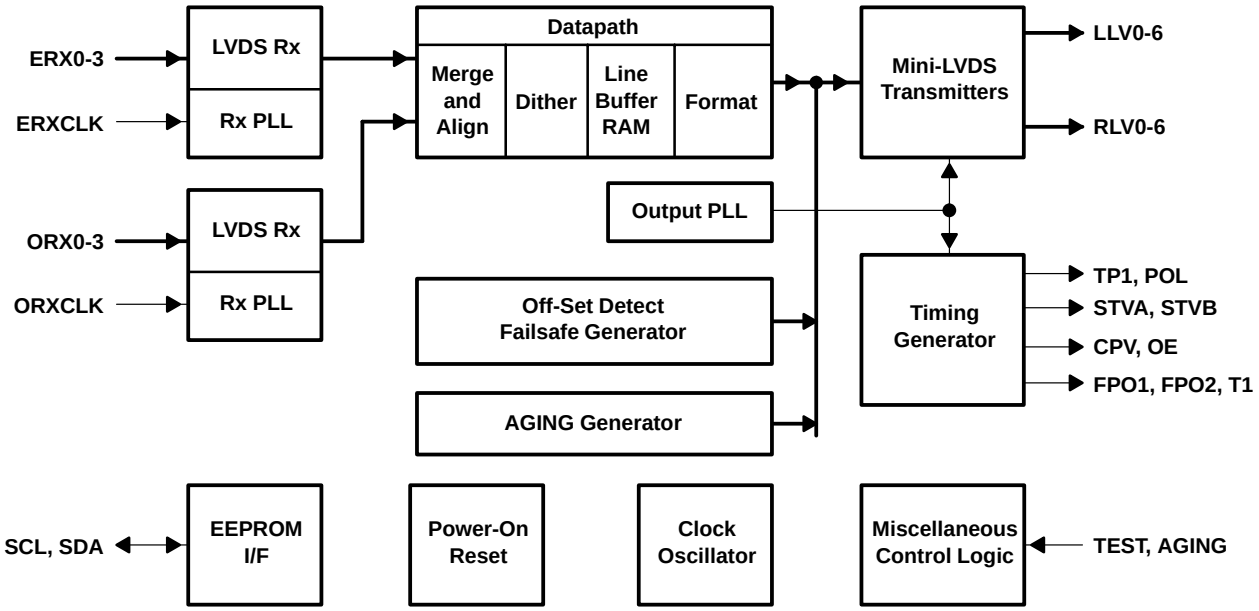
PRODUCT PREVIEW

pin assignment

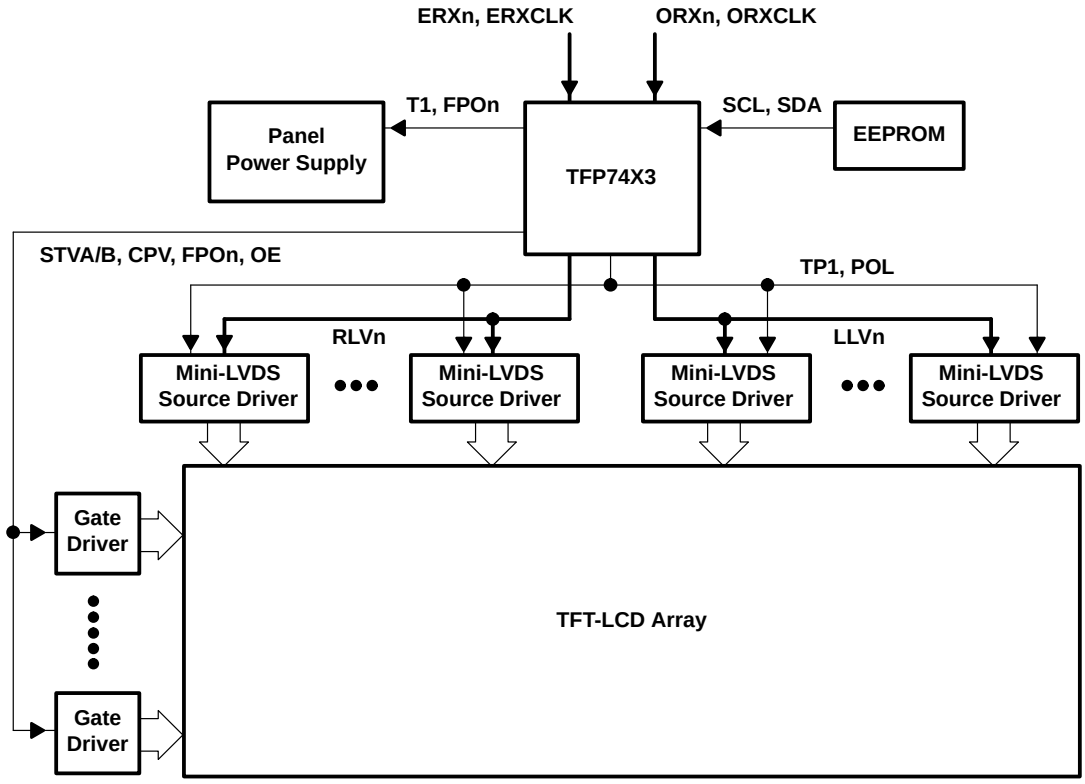
TQFP PACKAGE
(TOP VIEW)



block diagram



system diagram



PRODUCT PREVIEW

detailed description

LVDS receiver

The FlatLink receiver is a dual-port receiver. ERX0– through ERX3– and ERX0+ through ERX3+ are for the even (0, 2, 4…) pixels, ORX0– through ORX3– and ORX0+ through ORX3+ are for the odd (1, 3, 5…) pixels. In the single input port mode, ERX0– through ERX3– and ERX0+ through ERX3+ must be used. Both 18-bit color and 24-bit color are supported.

The FlatLink inputs are SSC-tolerant, and input SSC is passed on to the outputs to enable a low-EMI total solution.

data path

In the data path, video data from the two input ports are aligned and merged to form a single data stream. On-chip dithering is available to convert 24-bit color to 18 bits color. The dithering can be turned on or off by the user through the use of suitable register programming. The formatting section adds control bits to the mini-LVDS data stream and distributes data to different mini-LVDS outputs depending on resolution and mounting options. For normally-black panels, the video data can be inverted by register programming.

mini-LVDS transmitter

There are 14 pairs of mini-LVDS outputs, arranged as 7 pairs for the left half-bus (LLV0– through LLV6– and LLV0+ through LLV6+) and 7 pairs for the right half-bus (RLV0– through RLV6– and RLV0+ through RLV6+). Data and clock pairs are assigned out of these pins depending on the mode/resolution. Drive levels for data pairs are set by a resistor on R-MLVDS. The drive levels on the clock pairs can be set proportional to the data-pair drive levels by register programming. Preemphasis with register-programmable levels may be used on the mini-LVDS signals.

timing generator

The timing generator produces signals for controlling the gate drivers, source drivers and the panel power supply. The timing signals can be programmed by configuring the internal registers from an external EEPROM. Two very versatile general-purpose outputs, FPO1 and FPO2, are also available.

fail-safe circuit and clock oscillator

The TFP74X3 detects if the input signal is out of specification. In such a case, the fail-safe circuit generates timing signals and feeds data back to the panel. This prevents any damage to the panel. The fail-safe circuit works off an internal clock. The frequency of the internal oscillator is set by a single external resistor.

EEPROM interface

This block controls the reading of an external I^2C EEPROM. If an EEPROM is not connected, the TFP74X3 configures itself from one of four internal ROMs, depending on how the SCL and SDA pins are connected (pulled high/pulled low). In case an external EEPROM is connected but the read operation is not successful, the TFP74X3 remains in the reset condition.

miscellaneous control logic

This block configures the internal registers from the EEPROM (if present) and sets up the internal control depending on the contents of the EEPROM, the status of SCL, SDA, TEST, and AGING.

power-on reset

A laser-trimmed band-gap voltage sets accurate thresholds for the power-on reset. An external resistor and capacitor set the reset duration. Internal circuitry in this block also detects glitches in the power supply and initiates a reset sequence if a glitch in the power supply reduces voltage below safe levels, preventing damage to the panel.

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