TSA1401

14-BIT, 52MSPS, 250mW A/D CONVERTER

ADVANCED DATA

- 14-bit A/D converter in deep submicron technology
- Single supply voltage: 2.5V
- Digital I/O supply voltage: 2.5V/3.3V compatible
- 52 Msps sampling frequency
- Ultra low power dissipation: 250mW at 52Msps
- 100 MHz effective resolution bandwidth
- Built-in reference voltage with external bias capabilities
- Intrinsic SFDR higher than 80dB
- Dither capability
- Digital output high impedance mode

DESCRIPTION

The TSA1401 is a 14-bit, 52MHz sampling frequency Analog to Digital Converter using a deep submicron CMOS technology combining high performances and very low power consumption.

The TSA1401 is based on a pipeline structure and digital error correction to provide excellent static linearity and dynamic performances.

Typically designed for IF-sampling and multi-channel applications where low consumption is a must, the TSA1401 is part of the high speed, low power ADC family and is pin compatible to the 12bits, 50Msps TSA1201.

The dynamic range performance is enhanced by the dither capability. Dither can be inhibited through an input command pin: DYN.

Differential inputs of 1Vp-p each are applied for an optimum SNR. A tristate capability is available on the output buffers, therefore a low power dissipation is performed.

The TSA1401 is available in the industrial temperature range of -40°C to +85°C and in a small 48-lead TQFP package.

APPLICATIONS

- **Multi-channel basestations**
- **Medical imaging**
- **Wideband digital communications**
- **Communication instrumentation**

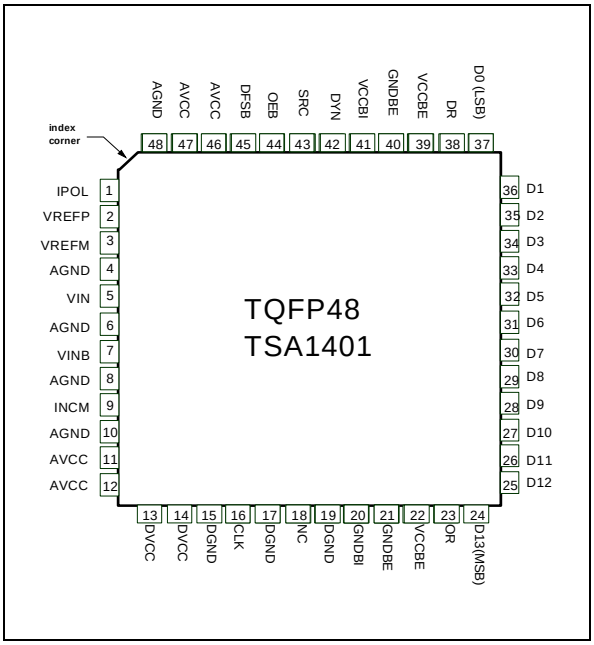
ORDER CODE

Part Number	Temperature Range	Package	Conditioning	Marking
TSA1401IF	-40°C to +85°C	TQFP48	Tray	TSA1401
TSA1401IFT	-40°C to +85°C	TQFP48	Tape & Reel	TSA1401

ORDER CODE

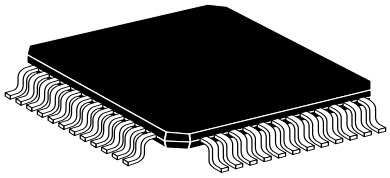
Part Number	Temperature Range	Package	Conditioning	Marking
EVAL1401/AA	Evaluation board			

PIN CONNECTIONS (top view)



PACKAGE

TQFP48



ABSOLUTE MAXIMUM RATINGS

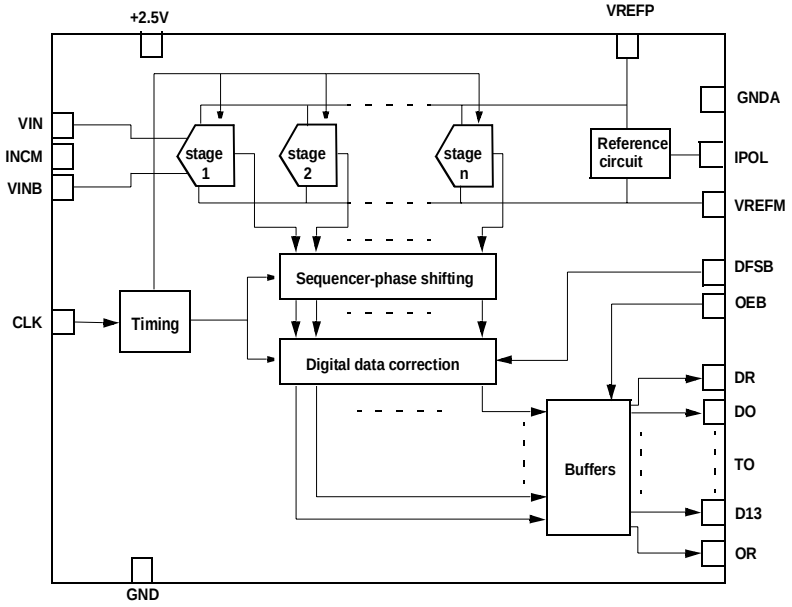
Symbol	Parameter	Values	Unit
AVCC	Analog Supply voltage [1]	0V to 3.3V	V
DVCC	Digital Supply voltage [1]	0V to 3.3V	V
VCCBI	Digital buffer Supply voltage [1]	0V to 3.6V	V
VCCBE	Digital buffer Supply voltage [1]	0V to 3.6V	V
IDout	Digital output current	-100mA to 100mA	mA
Tstg	Storage temperature	+150	°C
ESD	HBM: Human Body Model[2]	2	kV
Latch-up	Class[3]	A	

1. All voltages values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must not exceed -0.3V or VCC
2. ElectroStatic Discharge pulse (ESD pulse) simulating a human body discharge of 100 pF through 1.5kΩ
3. Corporate ST Microelectronics procedure number 0018695

OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC	Analog Supply voltage		2.25	2.5	2.7	V
DVCC	Digital Supply voltage		2.25	2.5	2.7	V
VCCBI	Digital buffer Supply voltage			3.3		V
VCCBE	Digital buffer Supply voltage			3.3		V
VREFP	Forced top voltage reference		inter-nal ref.	-	AVCC	V

BLOCK DIAGRAM



TIMING CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
FS	Sampling Frequency				52	MHz
DC	Clock Duty Cycle		45	50	55	%
TC1	Clock pulse width (high)			9.6		ns
TC2	Clock pulse width (low)			9.6		ns
Tod	Data Output Delay (Fall of Clock to Data Valid)	10pF load capacitance		5		ns
Tpd	Data Pipeline delay			8.5		cycles
Ton	Falling edge of OEB to digital output valid data			1		ns
Toff	Rising edge of OEB to digital output tri-state			1		ns

ANALOG INPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VIN-VINB	Full scale reference voltage			2.0		Vpp
Cin	Input capacitance			7.0		pF
BW	Analog Input Bandwidth (-3dB) [1)]	Full power, Vin=2.0Vpp, FS=52Msps		1000		MHz
ERB	Effective Resolution Bandwidth			100		MHz

1. Full power analog bandwidth of interest. Higher values can be achieved with smaller inputs levels.

REFERENCE VOLTAGE

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VREFP	Top internal reference voltage			1.03		V
VREFM	Bottom internal reference voltage		0		VREFP	V
Vpol	Analog bias voltage			1.27		V
Ipol	Analog bias current	Normal operating mode		tbd		µA
Ipol	Analog bias current	Shutdown mode		0		µA
VINCM	Input common mode voltage			0.56		V

POWER CONSUMPTION

Symbol	Parameter	Min	Typ	Max	Unit
ICCA	Analog Supply current		80		mA
ICCD	Digital Supply Current		10		mA
ICCBI	Digital Buffer Supply Current		5		mA
ICCBE	Digital Buffer Supply Current		5		mA
ICCBEZ	Digital Buffer Supply Current in High Impedance Mode		tbd		µA
Pd	Power consumption in normal operation mode		250		mW
PdZ	Power consumption in High Impedance mode		tbd		mW
Rthja	Thermal resistance (TQFP48)		80		°C/W
Rthjc	Thermal resistance (TQFP48)		18		°C/W

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock inputs						
VIL	Logic "0" voltage				0.8	V
VIH	Logic "1" voltage		2.0			V
IIL	Low input current	Vi=0V		0		µA
IIH	High input current	Vi=VCCD		0		µA
Digital inputs						
VIL	Logic "0" voltage				0.25 VCCBE	V
VIH	Logic "1" voltage		0.75 VCCBE			V
IIL	Low input current	Vi=0V		0		µA
IIH	High input current	Vi=VCCBE		0		µA

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Digital Outputs						
VOL	Logic "0" voltage	Iol=10µA			0.4	V
VOH	Logic "1" voltage	Ioh=10µA	2.4			V

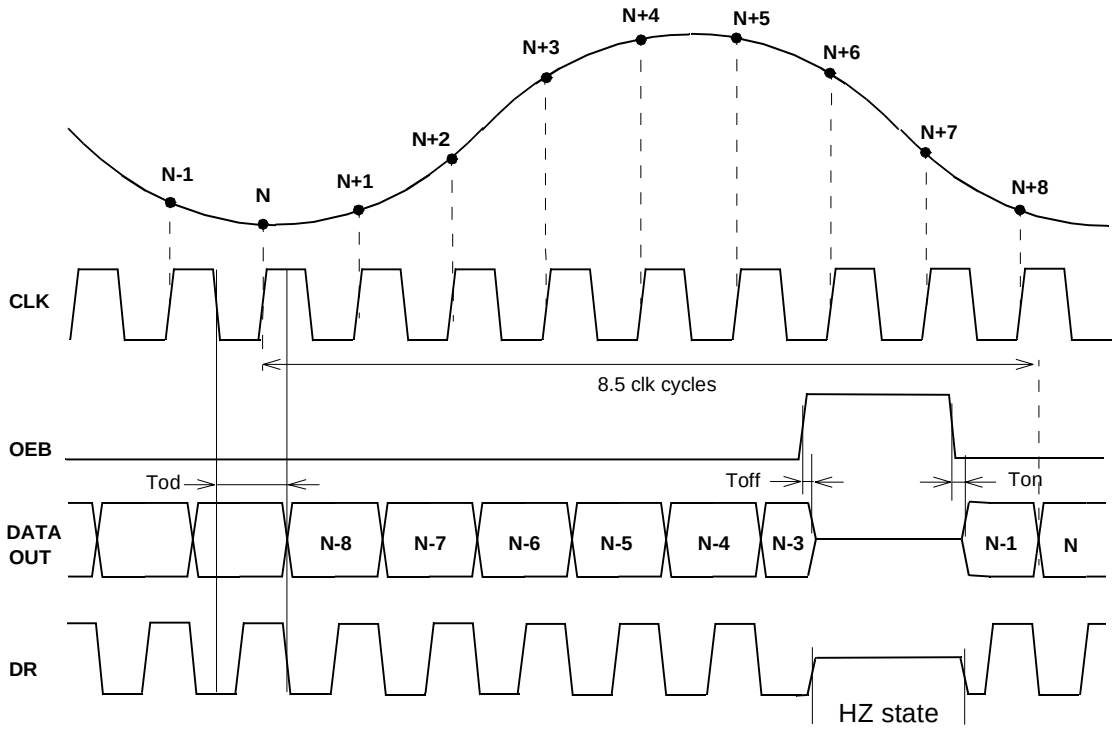
ACCURACY

Symbol	Parameter	Min	Typ	Max	Unit
OE	Offset Error				mV
GE	Gain Error				%
DNL	Differential Non Linearity		±0.5		LSB
INL	Integral Non Linearity		±1		LSB
-	Monotonicity and no missing codes	Guaranteed			

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious Free Dynamic Range	w/o dither		80		dBc
		with dither		100		dBc
SNR	Signal to Noise Ratio			75		dB
THD	Total Harmonics Distortion			tbd		dB
SINAD	Signal to Noise and Distortion Ratio			74		dB
ENOB	Effective Number of Bits			12		bits
IMD2	Two tones Intermodulation Distortion			tbd		dBc

TIMING DIAGRAM



PIN DESCRIPTION

Pin No	Name	Description	Observation	Pin No	Name	Description	Observation
1	IPOL	Analog bias current input		25	D12	Digital output	CMOS output (2.5V/3.3V)
2	VREFP	Top voltage reference	1V	26	D11	Digital output	CMOS output (2.5V/3.3V)
3	VREFM	Bottom voltage reference	0V	27	D10	Digital output	CMOS output (2.5V/3.3V)
4	AGND	Analog ground	0V	28	D9	Digital output	CMOS output (2.5V/3.3V)
5	VIN	Analog input	1Vpp	29	D8	Digital output	CMOS output (2.5V/3.3V)
6	AGND	Analog ground	0V	30	D7	Digital output	CMOS output (2.5V/3.3V)
7	VINB	Inverted analog input	1Vpp	31	D6	Digital output	CMOS output (2.5V/3.3V)
8	AGND	Analog ground	0V	32	D5	Digital output	CMOS output (2.5V/3.3V)
9	INCM	Input common mode	0.5V	33	D4	Digital output	CMOS output (2.5V/3.3V)
10	AGND	Analog ground	0V	34	D3	Digital output	CMOS output (2.5V/3.3V)
11	AVCC	Analog power supply	2.5V	35	D2	Digital output	CMOS output (2.5V/3.3V)
12	AVCC	Analog power supply	2.5V	36	D1	Digital output	CMOS output (2.5V/3.3V)
13	DVCC	Digital power supply	2.5V	37	D0(LSB)	Least Significant Bit output	CMOS output (2.5V/3.3V)
14	DVCC	Digital power supply	2.5V	38	DR	Data Ready output	CMOS output (2.5V/3.3V)
15	DGND	Digital ground	0V	39	VCCBE	Digital Buffer power supply	2.5V/3.3V
16	CLK	Clock input	2.5V compatible CMOS input	40	GNDBE	Digital Buffer ground	0V
17	DGND	Digital ground	0V	41	VCCBI	Digital Buffer power supply	2.5V
18	NC	Non connected		42	DYN	Dynamic input	2.5V/3.3C compatible CMOS input
19	DGND	Digital ground	0V	43	SRC	Slew Rate Control input	2.5V/3.3C compatible CMOS input
20	GNDBI	Digital buffer ground	0V	44	OEB	Output Enable input	2.5V/3.3C compatible CMOS input
21	GNDBE	Digital buffer ground	0V	45	DFSB	Data Format Select input	2.5V/3.3C compatible CMOS input
22	VCCBE	Digital buffer power supply	2.5V/3.3V	46	AVCC	Analog power supply	2.5V
23	OR	Over range output	CMOS output (2.5V/3.3V)	47	AVCC	Analog power supply	2.5V
24	D13(MSB)	Most Significant Bit output	CMOS output (2.5V/3.3V)	48	AGND	Analog ground	0V

OPERATION MODES DESCRIPTION

Inputs				Outputs	
Analog input differential level	**DFSB**	**OEB**	**SRC**	**OR**	**Most Significant Bit (MSB)**
(VIN-VINB) > RANGE	H	L	X	H	D13
-RANGE > (VIN-VINB)	H	L	X	H	D13
RANGE > (VIN-VINB) > -RANGE	H	L	X	L	D13
(VIN-VINB) > RANGE	L	L	X	H	D13 complemented
-RANGE > (VIN-VINB)	L	L	X	H	D13 complemented
RANGE > (VIN-VINB) > -RANGE	L	L	X	L	D13 complemented
X	X	H	X	HZ	HZ
X	X	X	H	X	26 Msps compliant slew rate
X	X	X	L	X	52 Msps compliant slew rate

Data Format Select (DFSB):

When set to a low level (VIL), DFSB provides a two's complement digital output format.

When set to a high level (VIH), DFSB provides a standard binary output coding.

Output Enable (OEB):

When set to a low level (VIL), all digital outputs remain active and in a low impedance state.

When set to a high level (VIH), all digital outputs are disconnected from device outside (high impedance state). The converter has a lower consumption but goes on sampling, which enables the data to be present on the output when the OEB is set to VIL again.

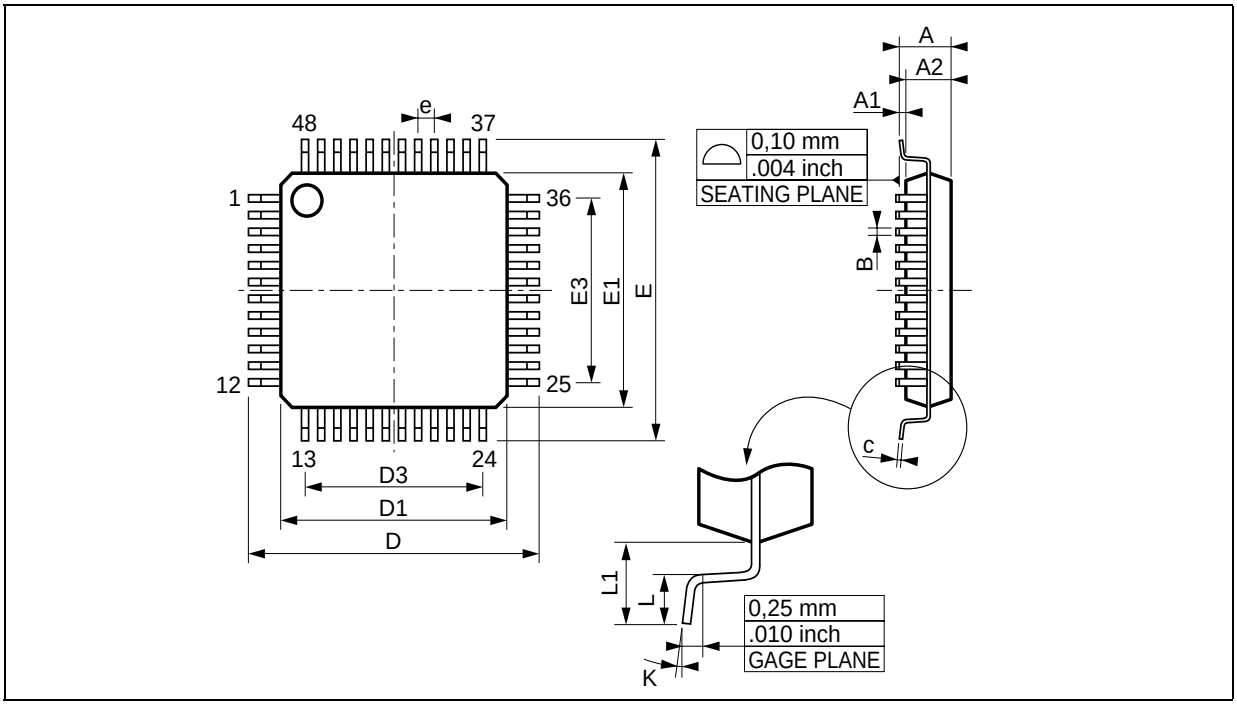
Slew Rate Control (SRC):

When set to a high level (VIH), all digital output currents are limited to a clamp value so that digital noise power is reduced to its minimum. Rise and Fall times just match the 26MHz sampling rate assuming the load capacitance on each digital output remains below 10pF

When set to a low level (VIL), the maximum digital output current is doubled compared the configuration where SRC is set to VIH. Rise and Fall times just match the 52MHz sampling rate with the lowest digital noise power, assuming the load capacitance on each digital output remains below 10pF.

Package Mechanical Data

48 PINS - PLASTIC PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (min.), 7° (max.)					