

## ULTRALOW-NOISE, HIGH PSRR, FAST RF 200-mA LOW-DROPOUT LINEAR REGULATORS

### FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **200-mA Low-Dropout Regulator With EN**
- **Available in 1.8-V, 2.5-V, 2.8-V, 2.85-V, 3-V, 3.3-V, 4.75-V, and Adjustable**
- **High PSRR (70 dB at 10 kHz)**
- **Ultralow Noise (32  $\mu$ V)**
- **Fast Start-Up Time (50  $\mu$ s)**
- **Stable With a 2.2- $\mu$ F Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (112 mV at Full Load, TPS79330)**
- **5-Pin SOT23 (DBV) Package**

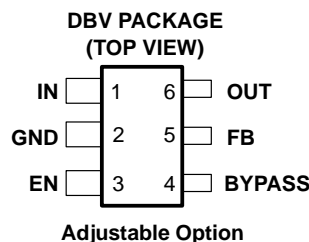
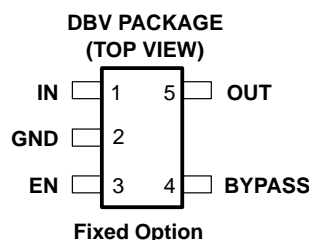
† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over specified temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### APPLICATIONS

- **VCOs**
- **RF**
- **Bluetooth™, Wireless LAN**

### DESCRIPTION

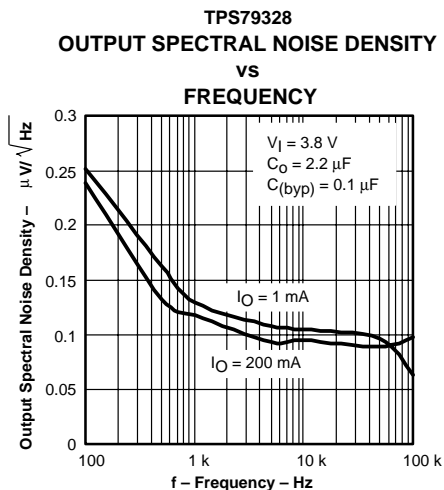
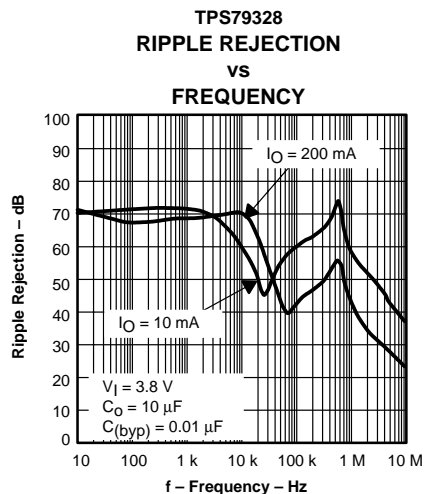
The TPS793xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT23, package. Each device in the family is stable, with a small 2.2- $\mu$ F ceramic capacitor on the output. The TPS793xx family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 112 mV at 200 mA, TPS79330). Each device achieves fast start-up times (approximately 50  $\mu$ s with a 0.001- $\mu$ F bypass capacitor) while consuming very low quiescent current (170  $\mu$ A typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1  $\mu$ A. The TPS79328 exhibits approximately 32  $\mu$ V<sub>RMS</sub> of output voltage noise with a 0.1- $\mu$ F bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.



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**AVAILABLE OPTIONS**

T <sub>J</sub>	VOLTAGE	PACKAGE	PART NUMBER	SYMBOL
–40°C to 125°C	1.2 to 5.5 V	SOT23 (DBV)	TPS79301DBVREP†	PGVE
	1.8 V		TPS79318DBVREP†	PHHE
	2.5 V		TPS79325DBVREP†	PGWE
	2.8 V		TPS79328DBVREP†‡	PGXE
	2.85 V		TPS793285DBVREP†‡	PHIE
	3 V		TPS79330DBVREP†‡	PGYE
	3.3 V		TPS793333DBVREP†	PHUE
	4.75 V		TPS793475DBVREP†‡	PHJE

† The DBVR indicates tape and reel of 3000 parts.

‡ Product preview

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Input voltage range (see Note 1)	–0.3 V to 6 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Voltage on OUT	–0.3 V to 6 V
Peak output current	internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	–40°C to 150°C
Operating ambient temperature range, $T_A$	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Low K <sup>‡</sup>	DBV	63.75 °C/W	256 °C/W	3.906 mW/°C	391 mW	215 mW	156 mW
High K <sup>§</sup>	DBV	63.75 °C/W	178.3 °C/W	5.609 mW/°C	561 mW	308 mW	224 mW

<sup>‡</sup> The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.

<sup>§</sup> The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

**TPS79301-EP, '79318-EP, '79325-EP  
'79328-EP, '793285-EP, '79330-EP  
TPS79333-EP, '793475-EP**

SGLS163 – APRIL 2003

**electrical characteristics over recommended operating free-air temperature range  $E_N = V_I$ ,  
 $T_J = -40$  to  $125^\circ\text{C}$ ,  $V_I = V_{O(\text{typ})} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $C_O = 10\text{ }\mu\text{F}$ ,  $C_{(\text{byp})} = 0.01\text{ }\mu\text{F}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>I</sub>	Input voltage (see Note 2)			2.7		5.5	V
I <sub>O</sub>	Continuous output current (see Note 3)			0		200	mA
T <sub>J</sub>	Operating junction temperature			−40		125	°C
Output voltage	TPS79301	0 μA < I <sub>O</sub> < 200 mA, (see Note 4)	1.22 V ≤ V <sub>O</sub> ≤ 5.2 V,	0.98 V <sub>O</sub>		1.02 V <sub>O</sub>	V
	TPS79318	T <sub>J</sub> = 25°C			1.8		V
		0 μA < I <sub>O</sub> < 200 mA,	2.8 V < V <sub>I</sub> < 5.5 V	1.764		1.836	
	TPS79325	T <sub>J</sub> = 25°C			2.5		V
		0 μA < I <sub>O</sub> < 200 mA,	3.5 V < V <sub>I</sub> < 5.5 V	2.45		2.55	
	TPS79328	T <sub>J</sub> = 25°C			2.8		V
		0 μA < I <sub>O</sub> < 200 mA,	3.8 V < V <sub>I</sub> < 5.5 V	2.744		2.856	
	TPS793285	T <sub>J</sub> = 25°C			2.85		V
		0 μA < I <sub>O</sub> < 200 mA,	3.85 V < V <sub>I</sub> < 5.5 V	2.793		2.907	
	TPS79330	T <sub>J</sub> = 25°C			3		V
		0 μA < I <sub>O</sub> < 200 mA,	4 V < V <sub>I</sub> < 5.5 V	2.94		3.06	
	TPS79333	T <sub>J</sub> = 25°C			3.3		V
0 μA ≤ I <sub>O</sub> < 200 mA,		4.3 V < V <sub>I</sub> < 5.5 V	3.234		3.366		
TPS793475	T <sub>J</sub> = 25°C			4.75		V	
	0 μA < I <sub>O</sub> < 200 mA,	5.25 V < V <sub>I</sub> < 5.5 V	4.655		4.845		
Quiescent current (GND current)		0 μA < I <sub>O</sub> < 200 mA,	T <sub>J</sub> = 25°C	170			μA
		0 μA < I <sub>O</sub> < 200 mA		220			μA
Load regulation		0 μA < I <sub>O</sub> < 200 mA,	T <sub>J</sub> = 25°C	5			mV
Output voltage line regulation (ΔV <sub>O</sub> /V <sub>O</sub> ) (see Note 5)		V <sub>O</sub> + 1 V < V <sub>I</sub> ≤ 5.5 V,	T <sub>J</sub> = 25°C	0.05			%V
		V <sub>O</sub> + 1 V < V <sub>I</sub> ≤ 5.5 V		0.12			
Output noise voltage (TPS79328)		BW = 200 Hz to 100 kHz, I <sub>O</sub> = 200 mA, T <sub>J</sub> = 25°C	C(byp) = 0.001 μF	55			μV <sub>RMS</sub>
			C(byp) = 0.0047 μF	36			
			C(byp) = 0.01 μF	33			
			C(byp) = 0.1 μF	32			
Time, start-up (TPS79328)		R <sub>L</sub> = 14 Ω, C <sub>O</sub> = 1 μF, T <sub>J</sub> = 25°C	C(byp) = 0.001 μF	50			μs
			C(byp) = 0.0047 μF	70			
			C(byp) = 0.01 μF	100			
Output current limit		V <sub>O</sub> = 0 V,	See Note 4	285		600	mA
Standby current		EN = 0 V,	2.7 V < V <sub>I</sub> < 5.5 V	0.07		1	μA
High level enable input voltage		2.7 V < V <sub>I</sub> < 5.5 V		2			V
Low level enable input voltage		2.7 V < V <sub>I</sub> < 5.5 V				0.7	V
Input current (EN)		EN = 0		−1		1	μA
Input current (FB) (TPS79301)		FB = 1.8 V				1	μA

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_{I(\text{min})} = V_{O(\text{max})} + V_{DO}(\text{max load})$$

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

4. The minimum  $I_N$  operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1\text{ V}$ , whichever is greater. The maximum  $I_N$  voltage is 5.5 V. The maximum output current is 200 mA.

5. If  $V_O \leq 2.5\text{ V}$  then  $V_{I\text{min}} = 2.7\text{ V}$ ,  $V_{I\text{max}} = 5.5\text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - 2.7\text{ V})}{100} \times 1000$$

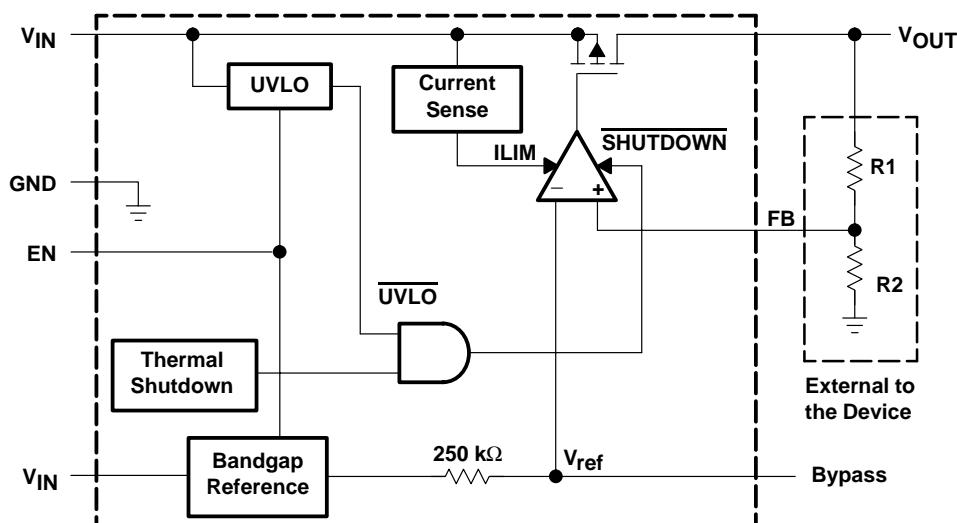
If  $V_O \geq 2.5\text{ V}$  then  $V_{I\text{min}} = V_O + 1\text{ V}$ ,  $V_{I\text{max}} = 5.5\text{ V}$ .

electrical characteristics over recommended operating free-air temperature range  $E_N = V_I$ ,  
 $T_J = -40$  to  $125^\circ\text{C}$ ,  $V_I = V_{O(\text{typ})} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $C_O = 10\text{ }\mu\text{F}$ ,  $C_{(\text{byp})} = 0.01\text{ }\mu\text{F}$  (unless otherwise noted)  
(continued)

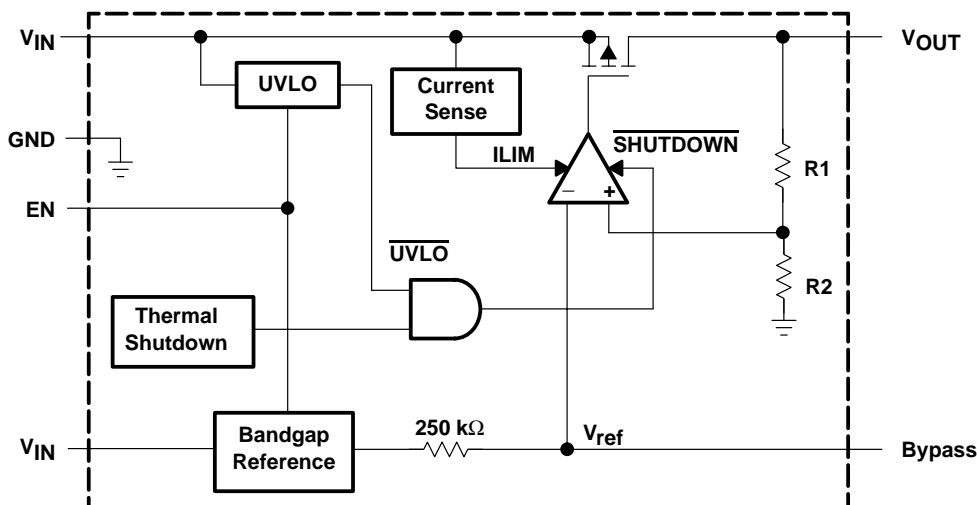
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power supply ripple rejection	TPS79328	f = 100 Hz, T <sub>J</sub> = 25°C, I <sub>O</sub> = 10 mA			70		dB
		f = 100 Hz, T <sub>J</sub> = 25°C, I <sub>O</sub> = 200 mA			68		
		f = 10 kHz, T <sub>J</sub> = 25°C, I <sub>O</sub> = 200 mA			70		
		f = 100 kHz, T <sub>J</sub> = 25°C, I <sub>O</sub> = 200 mA			43		
Dropout voltage (see Note 6)	TPS79328	I <sub>O</sub> = 200 mA, T <sub>J</sub> = 25°C			120		mV
		I <sub>O</sub> = 200 mA				200	
	TPS793285	I <sub>O</sub> = 200 mA, T <sub>J</sub> = 25°C			120		
		I <sub>O</sub> = 200 mA				200	
	TPS79330	I <sub>O</sub> = 200 mA, T <sub>J</sub> = 25°C			112		
		I <sub>O</sub> = 200 mA				200	
	TPS79333	I <sub>O</sub> = 200 mA, T <sub>J</sub> = 25°C			102		
		I <sub>O</sub> = 200 mA				180	
	TPS793475	I <sub>O</sub> = 200 mA, T <sub>J</sub> = 25°C			77		
		I <sub>O</sub> = 200 mA				125	
UVLO threshold		V <sub>CC</sub> rising		2.25		2.65	V
UVLO hysteresis		T <sub>J</sub> = 25°C	V <sub>CC</sub> rising		100		mV

NOTE 6:  $I_N$  voltage equals  $V_{O(\text{typ})} - 100\text{ mV}$ ; The TPS79325 dropout voltage is limited by the input voltage range limitations.

## functional block diagram—adjustable version



## functional block diagram—fixed version



## Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	I	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	N/A	I	This terminal is the feedback input voltage for the adjustable device.
GND	2	2		Regulator ground
IN	1	1	I	The IN terminal is the input to the device.
OUT	6	5	O	The OUT terminal is the regulated output of the device.

## TYPICAL CHARACTERISTICS

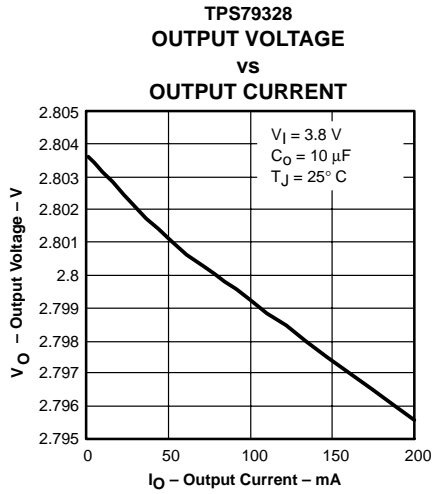


Figure 1

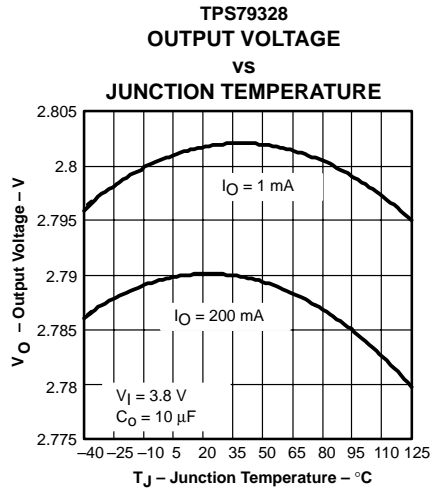


Figure 2

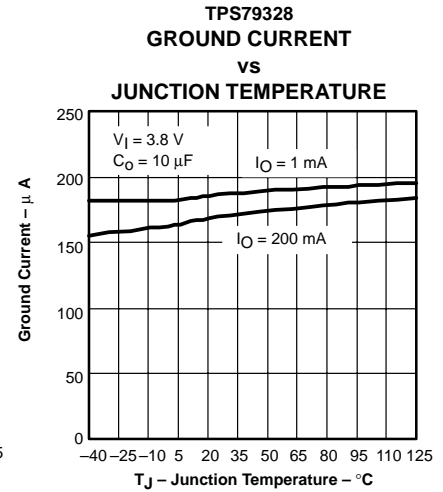


Figure 3

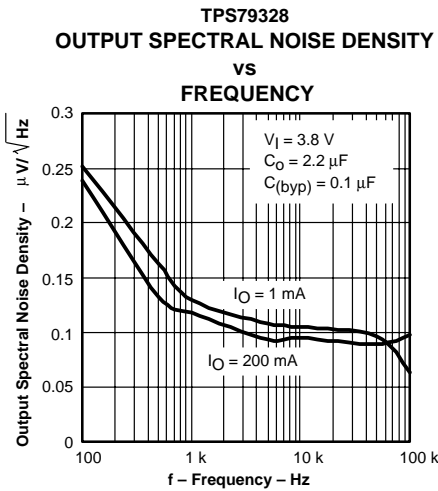


Figure 4

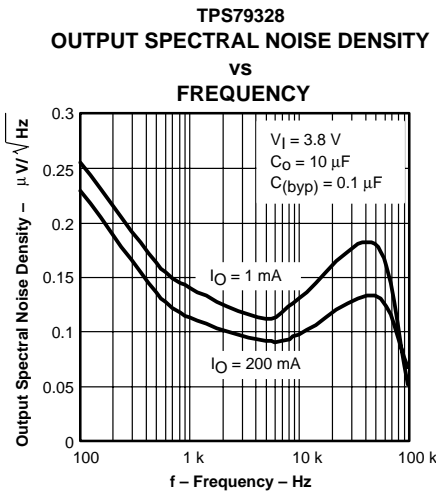


Figure 5

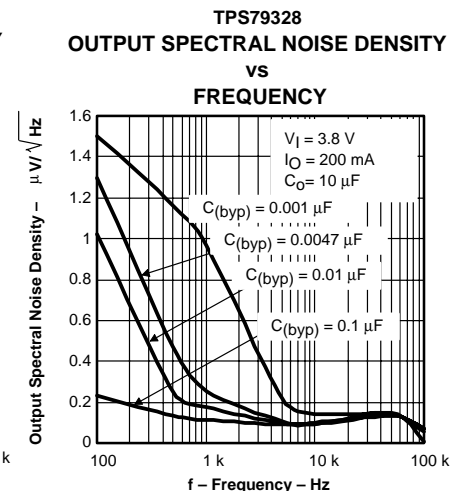


Figure 6

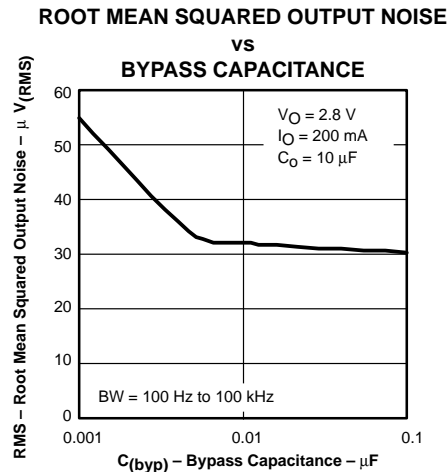


Figure 7

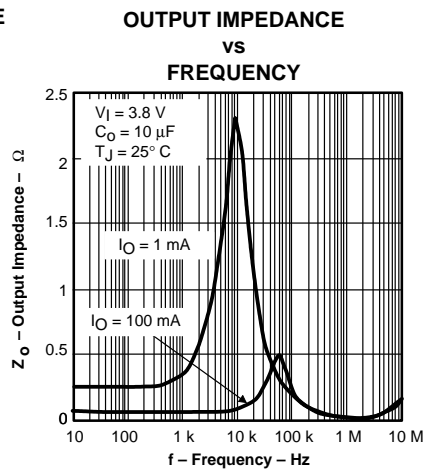


Figure 8

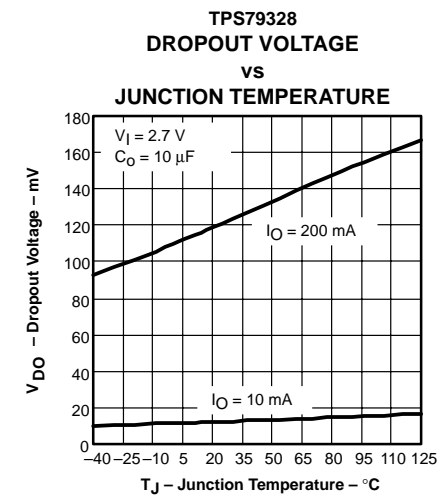


Figure 9

## TYPICAL CHARACTERISTICS

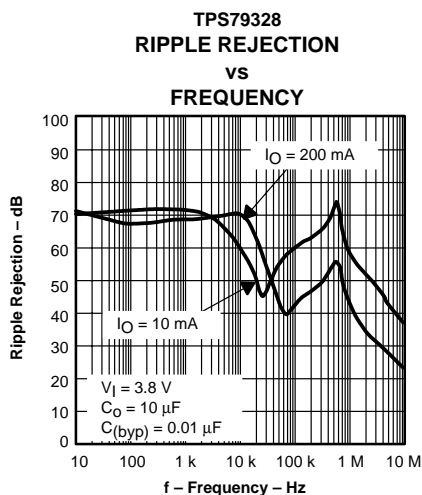


Figure 10

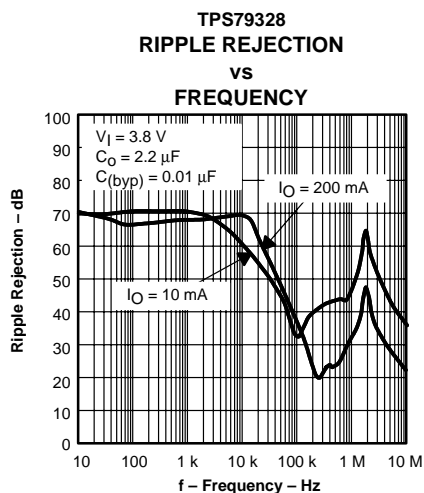


Figure 11

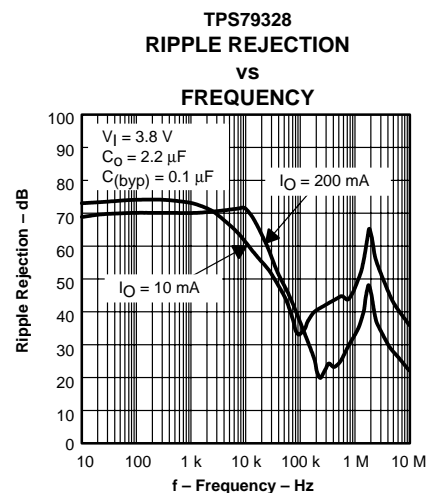


Figure 12

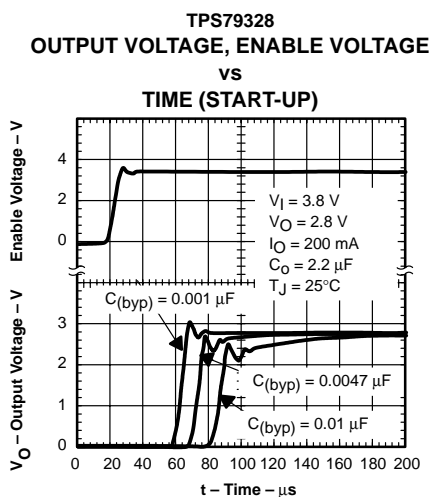


Figure 13

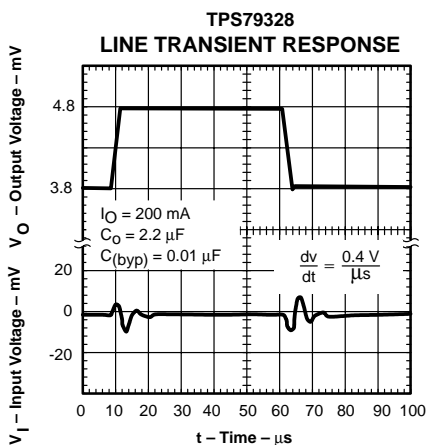


Figure 14

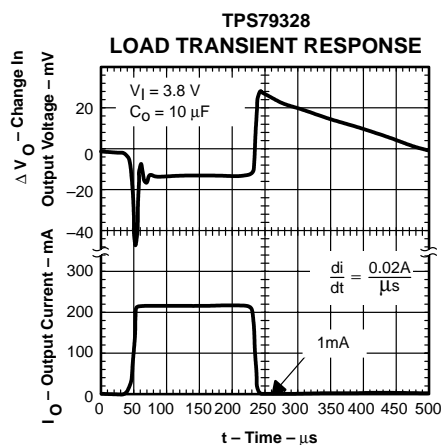


Figure 15

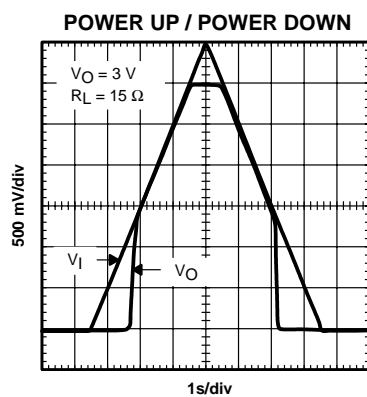


Figure 16

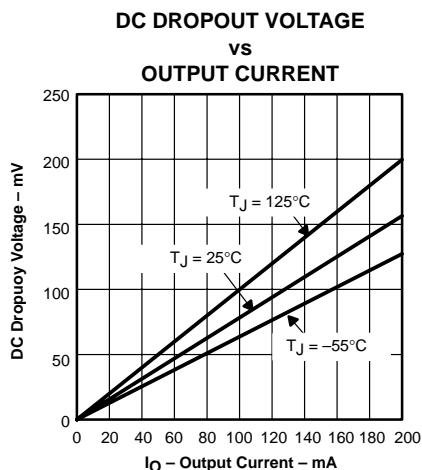


Figure 17

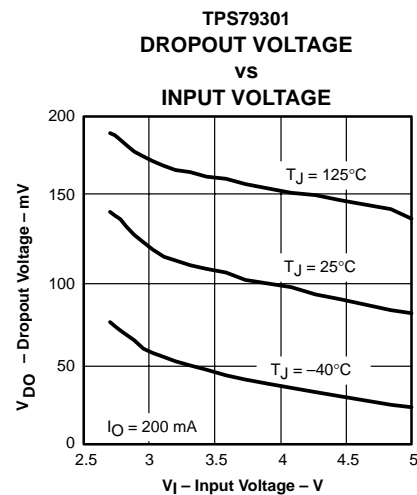
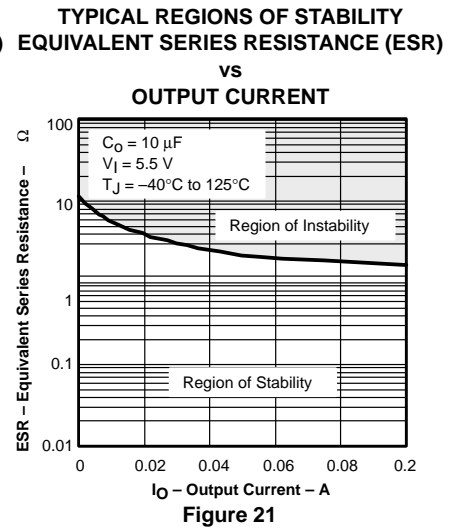
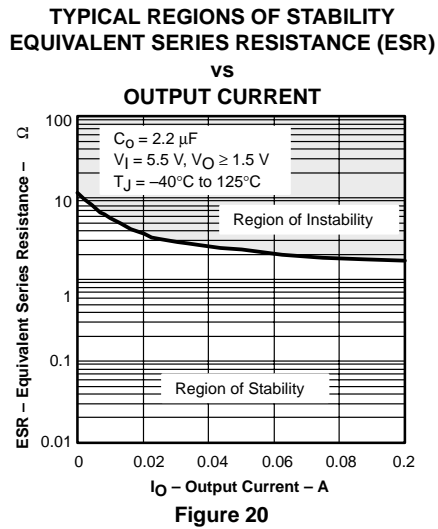
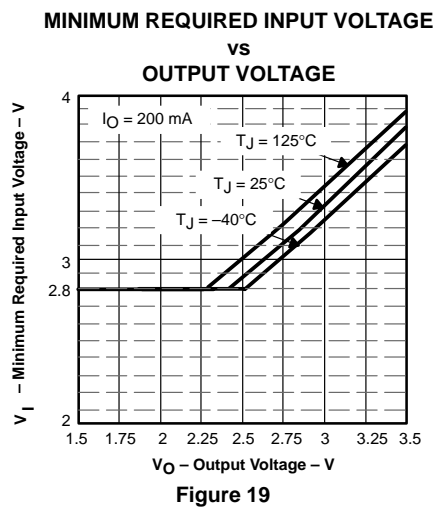


Figure 18



## TYPICAL CHARACTERISTICS



## APPLICATION INFORMATION

The TPS793xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170  $\mu\text{A}$  typically), and enable-input to reduce supply currents to less than 1  $\mu\text{A}$  when the regulator is turned off.

A typical application circuit is shown in Figure 22.

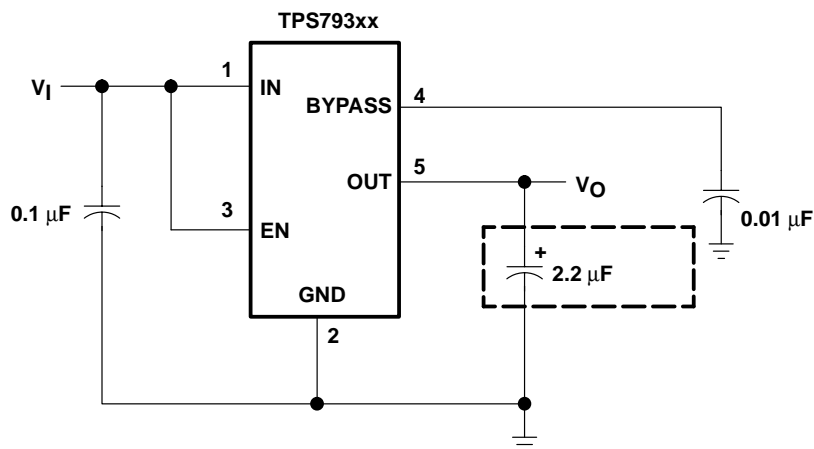


Figure 22. Typical Application Circuit

### external capacitor requirements

A 0.1- $\mu\text{F}$  or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx, is required for stability and will improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS793xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2  $\mu\text{F}$ . Any 2.2  $\mu\text{F}$  or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx has a BYPASS pin which is connected to the voltage reference through a 250-k $\Omega$  internal resistor. The 250-k $\Omega$  internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current will create an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79328 exhibits only 32  $\mu\text{V}_{\text{RMS}}$  of output voltage noise using a 0.1- $\mu\text{F}$  ceramic bypass capacitor and a 2.2- $\mu\text{F}$  ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the BYPASS pin that is created by the internal 250-k $\Omega$  resistor and external capacitor.

## APPLICATION INFORMATION

### board layout recommendation to improve PSRR and noise performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (1)$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature.

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

### programming the TPS79301 adjustable LDO regulator

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Where:

$V_{ref} = 1.2246$  V typ (the internal reference voltage)

## APPLICATION INFORMATION

### programming the TPS79301 adjustable LDO regulator (continued)

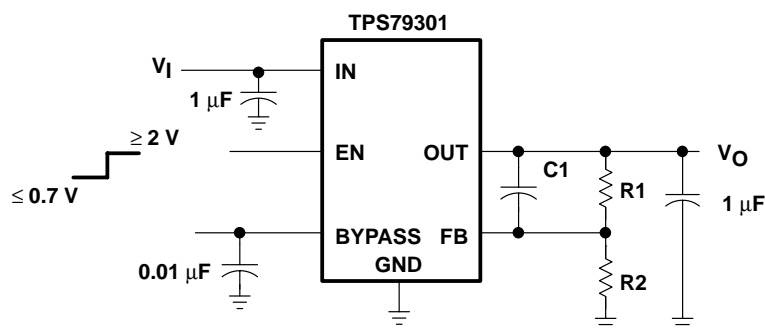
Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases  $V_O$ . The recommended design procedure is to choose  $R_2 = 30.1 \text{ k}\Omega$  to set the divider current at 50 μA,  $C_1 = 15 \text{ pF}$  for stability, and then calculate R1 using:

$$R_1 = \left( \frac{V_O}{V_{\text{ref}}} - 1 \right) \times R_2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF.



OUTPUT VOLTAGE  
PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79301 Adjustable LDO Regulator Programming

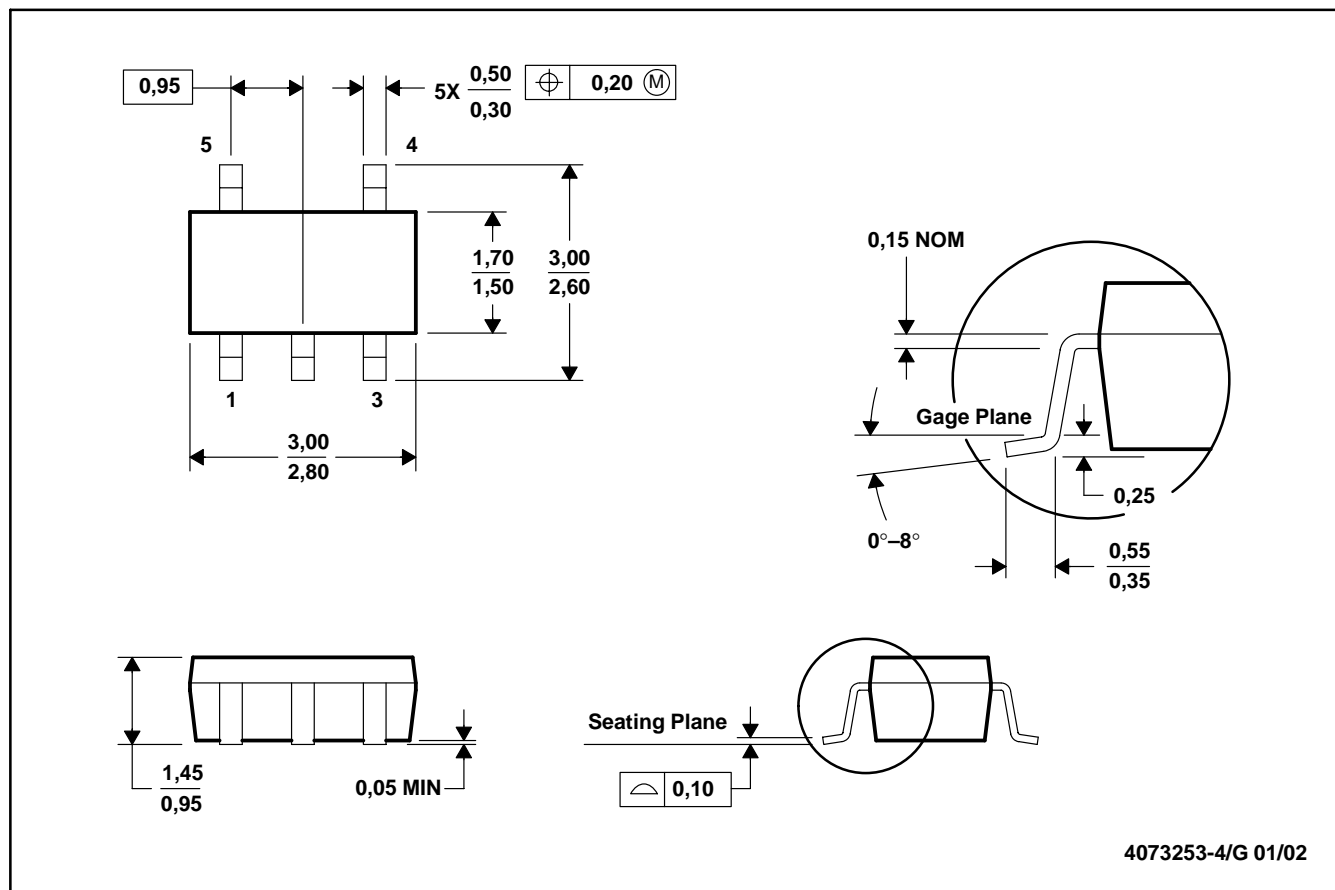
### regulator protection

The TPS793xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS793xx features internal current limiting and thermal protection. During normal operation, the TPS793xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

## DBV (R-PDSO-G5)

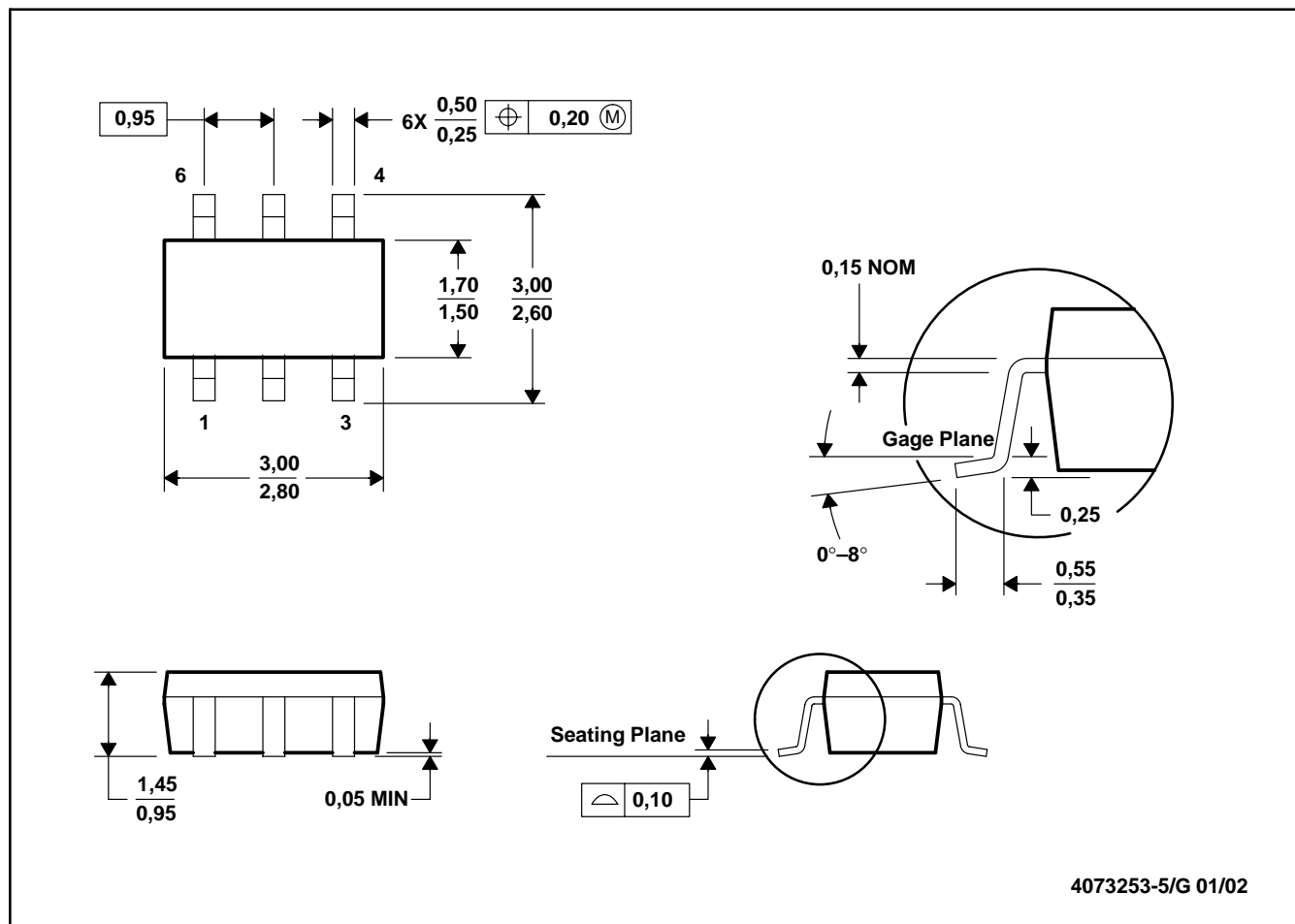
## PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-178

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

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