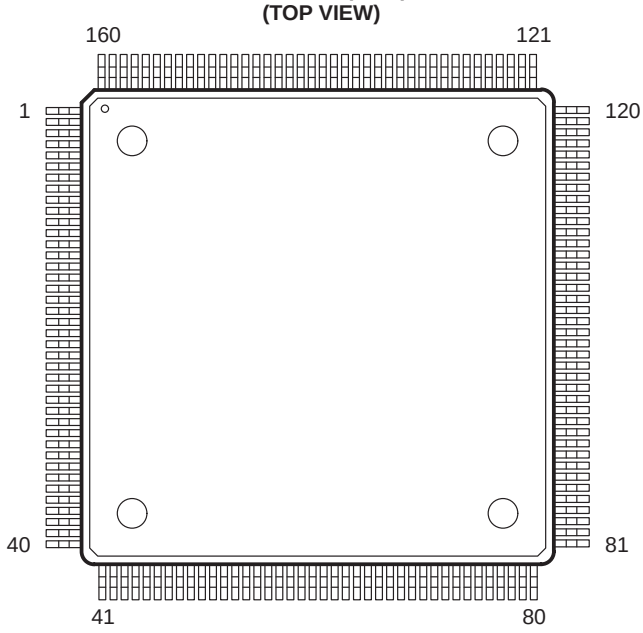
SPVS006A – FEBRUARY 1992 – REVISED JUNE 1992

- **Simplifies Design of High-Performance ISA PC Graphics Systems**
- **Single-Integrated Circuit Interfaces TMS34020 to ISA Bus**
- **Conforms to ISA Portions of the EISA Rev. 3.11 Specifications**
- **Internal Data Bus Transceivers**
- **Register Configurable I/O Mapped or Memory-Mapped Interface**
- **Register Configurable as an 8- or 16-Bit ISA Memory-Mapped Device**
- **Configurable TMS34020 Address Space Decoding**
  - **– VRAM Shift Register Transfer Decoding**
  - **– VRAM Mask Write and VRAM Color Register Write Access Decoding**
- **VGA Passthrough Support**
- **Operating Free-Air Temperature . . . 0°C to 55°C**

160-PIN PC PLASTIC QUAD-FLAT PACKAGE (EIAJ) (TOP VIEW)



description

The TMS34094 ISA Bus Interface device, a peripheral device for the TMS34020 Graphics Processor, facilitates the design of a high-performance graphics system for use in an ISA Bus-compatible PC. The device decodes ISA Bus cycles and controls the TMS34020 host interface to enable read and write accesses to the TMS34020's local memory. In addition, the TMS34094 allows the host to access the TMS34020's local memory via either I/O-mapped or memory-mapped ISA Bus accesses. The capability is software configurable, simplifying design and reducing system cost.

I/O mapped interface

The I/O mapped interface defines three I/O locations which facilitate access to the entire range of TMS34020 local memory. Two registers are used together to provide a 28-bit address to the TMS34020. The third register acts as the data port between the ISA Bus and TMS34020 local memory. This set of three registers supports the TMS34020's autoincrement modes which reduce data transfer overhead. For simplifying interrupt routines, the TMS34094 also provides read back of the address for the next host access.

memory-mapped interface

The memory-mapped interface provides four highly configurable windows between host memory space and TMS34020 memory space. Each window has four individually configurable attributes. These include: response as either an 8-bit or 16-bit device; begin address in the memory map of the host; begin address in the memory map of the TMS34020; and size. Size may range from 8K bytes to 4M bytes.

local memory decode

TMS34020 local memory map decoding is provided by the TMS34094. The TMS34094 internally decodes LAD bus addresses to generate four bank select output signals. The bank select signals may be used to control DRAM, VRAM, ROM and other devices in the TMS34020 local memory map. This programmable decoding allows designs to support multiple resolutions and color depths through software configuration.

For applications requiring synchronization of host software and TMS34020 software, the TMS34094 shadows the TMS34020 host control register low (HSTCTLL) as an ISA I/O register. This eliminates a LAD bus host access cycle, thereby reducing LAD bus traffic and increasing TMS34020 performance.

To simplify the design of VGA-compatible, single-monitor graphics systems, the TMS34094 supports VGA passthrough. Onchip passthrough logic supports designs where VGA controllers are onboard, as well as designs where a VGA-compatible auxiliary video connector is provided. The TMS34094 decodes ISA Bus accesses to standard VGA palette control registers and signals that a VGA pass-through access is occurring. Shadowing of VGA passthrough cycles may be disabled, enabled for writes only, or enabled for reads and writes.

pin assignment

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	V_{SS}	41	V_{SS}	81	V_{SS}	121	V_{SS}
2	$\overline{\text{HWRITE}}$	42	SA19	82	D14	122	SSRT
3	HBS01	43	SA18	83	D6	123	LAD31
4	HBS23	44	SA17	84	D13	124	LAD15
5	HA5	45	SA16	85	D5	125	LAD30
6	HA6	46	SA15	86	D12	126	LAD14
7	HA7	47	SA14	87	D4	127	LAD29
8	HA8	48	SA13	88	D11	128	LAD13
9	HA9	49	SA12	89	D3	129	LAD28
10	HA10	50	SA11	90	D10	130	LAD12
11	HA11	51	SA10	91	D2	131	LAD27
12	HA12	52	SA9	92	D9	132	LAD11
13	HA13	53	SA8	93	D1	133	LAD26
14	HA14	54	SA7	94	D8	134	LAD10
15	HA15	55	SA6	95	D0	135	LAD25
16	HA16	56	SA5	96	PCINT	136	LAD9
17	HA17	57	SA4	97	RESDRV	137	LAD24
18	HA18	58	SA3	98	BIOSEN	138	LAD8
19	V_{SS}	59	V_{SS}	99	V_{SS}	139	V_{SS}
20	HA19	60	SA2	100	$\overline{\text{HINT}}$	140	$\overline{\text{HOE}}$
21	V_{CC}	61	V_{CC}	101	V_{CC}	141	V_{CC}
22	HA20	62	SA1	102	IOSEL2	142	LAD23
23	HA21	63	SA0	103	IOSEL1	143	LAD7
24	HA22	64	$\overline{\text{MWTC}}$	104	IOSEL0	144	LAD22
25	HA23	65	$\overline{\text{MRDC}}$	105	HRDY	145	LAD6
26	HA24	66	$\overline{\text{SBHE}}$	106	LCLK2	146	LAD21
27	HA25	67	BALE	107	LCLK1	147	LAD5
28	HA26	68	BCLK	108	HDST	148	LAD20
29	HA27	69	$\overline{\text{REFRESH}}$	109	$\overline{\text{CAS2}}$	149	LAD4
30	HA28	70	$\overline{\text{IORC}}$	110	$\overline{\text{RAS}}$	150	LAD19
31	HA29	71	$\overline{\text{IOWC}}$	111	$\overline{\text{ALTCH}}$	151	LAD3
32	HA30	72	$\overline{\text{SMRDC}}$	112	$\overline{\text{WE}}$	152	LAD18
33	HA31	73	$\overline{\text{SMWTC}}$	113	SF	153	LAD2
34	LA17	74	AEN	114	$\overline{\text{RESET}}$	154	LAD17
35	LA18	75	$\overline{\text{IO16}}$	115	$\overline{\text{BSEL0}}$	155	LAD1
36	LA19	76	$\overline{\text{M16}}$	116	$\overline{\text{BSEL1}}$	156	LAD16
37	LA20	77	CHRDY	117	$\overline{\text{BSEL2}}$	157	LAD0
38	LA21	78	NC†	118	$\overline{\text{BSEL3}}$	158	$\overline{\text{HCS}}$
39	LA22	79	D15	119	V_{CC}	159	V_{CC}
40	LA23	80	D7	120	VGASHD	160	$\overline{\text{HREAD}}$

† NC – DO NOT CONNECT.

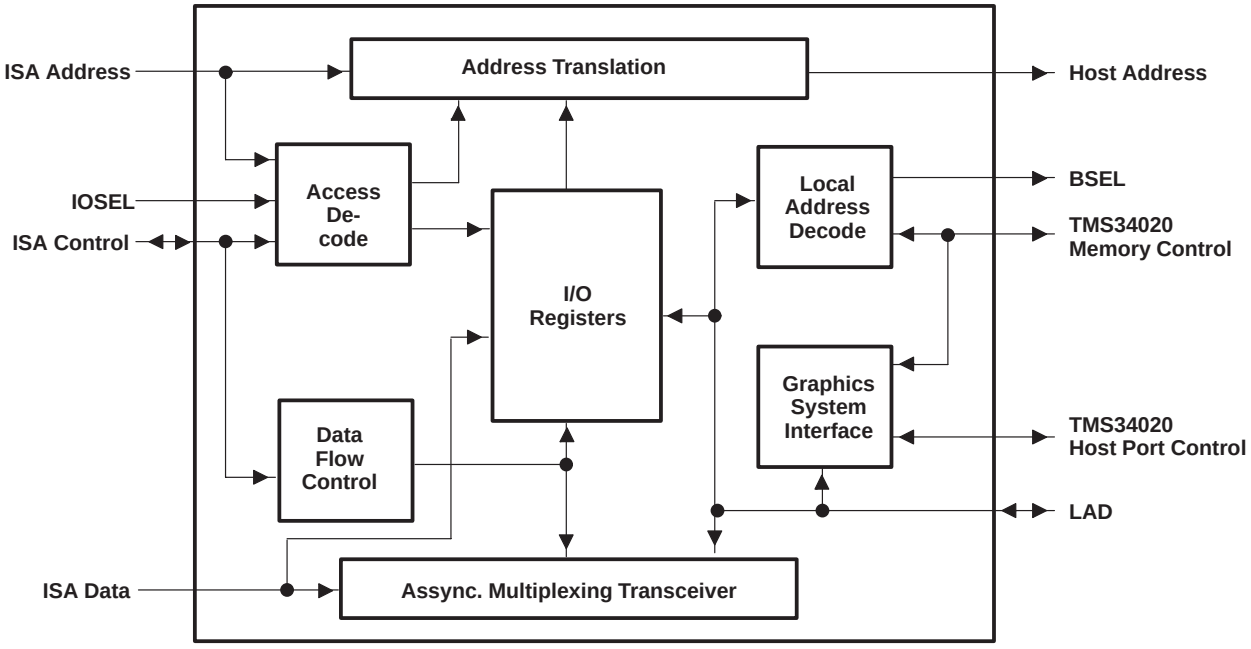
signal descriptions

SIGNAL	I/O/Z	TMS34020 INTERFACE SIGNALS
LCLK1, LCLK2	I	**Local clocks**. These signals are used to synchronize the access with the TMS34020.
LAD0–LAD31	I/O	**32-bit multiplexed local address/data bus.** These signals are used to monitor the address and status of a TMS34020 memory cycle and to read and write data from the TMS34094 to memory.
$\overline{\text{ALTCH}}$	I	**Address latch.** The high-to-low transition of the signal indicates the address value on LAD0–LAD31 is valid.
$\overline{\text{RAS}}$	I	**Row-address strobe.** The row-address strobe from the TMS34020.
$\overline{\text{CAS2}}$	I	**Column-address strobe.** This signal is used to indicate a possible access to the least significant byte of the HSTCTLL register.
$\overline{\text{WE}}$	I	**Write enable.** This signal from the TMS34020 is used to indicate a possible write access to the HSTCTLL register.
SF	I	**VRAM special function**. This signal from the TMS34020 is used in decoding LAD bus shift register transfer cycles to control the shift clock insertion indicator signal SSRT.
HDST	I	**Host data latch strobe**. The rising edge of this signal latches data on LAD0–LAD31 into the TMS34094 during a host read of TMS34020 memory.
$\overline{\text{HOE}}$	I	**Host data output enable**. Enables the TMS34094 to drive data onto LAD0–LAD31 during a host write cycle.
HRDY	I	**Host ready.** This normally low signal is asserted high by the TMS34020 to indicate that the TMS34020 is ready to complete a host-initiated cycle. It is used to generate the CHRDY output from the TMS34094.
$\overline{\text{HCS}}$	O	**Host chip select.** This signal is driven low to latch the address presented on HA5–HA31 into the TMS34020 and initiate a host access cycle. The status of this signal also configures the TMS34020 for autoincrement access. A pull-up resistor is required on $\overline{\text{HCS}}$ to ensure that the TMS34020 will reset to Host Present mode.
$\overline{\text{HREAD}}$	O	**Host read.** This active low signal is driven low to indicate a read request from the ISA bus of TMS34020 local memory.
$\overline{\text{HWRITE}}$	O	**Host write**. This active low signal is driven low to indicate a write request of TMS34020 memory from the ISA Bus.
HA5–HA31	O	**27 host-address signals.** The value represents the address of the 32-bit quantity being accessed in the TMS34020 local memory.
HBS01	O	**Host byte select 01.** This signal is connected to both HBS0 and HBS1 of the TMS34020 to indicate that the host requests an access to the even 16-bit word of the 32-bit quantity specified by HA5–HA31.
HBS23	O	**Host byte select 23**. This signal is connected to both HBS2 and HBS3 of the TMS34020 to indicate that the host requests an access to the odd 16-bit word of the 32-bit quantity specified by HA5–HA31.
$\overline{\text{RESET}}$	O	**Subsystem reset.** This signal indicates a reset to the graphics subsystem and should be connected to the $\overline{\text{RESET}}$ input of the TMS34020 and the palette. $\overline{\text{RESET}}$ will become active low after the ISA signal RESDRV has remained low for four consecutive cycles on LCLK1. It can also be asserted by setting the RS bit in the TMS34094 MODECTL register.
$\overline{\text{HINT}}$	I	**Host interrupt.** This signal is connected to the TMS34020 $\overline{\text{HINT}}$ output. The PCINT output follows the inverse of this input.
SIGNAL	**I/O/Z**	**ISA INTERFACE SIGNALS**
BCLK	I	**Bus clock**. This signal is used to synchronize some ISA Interface signals.
BALE	I	**Bus address latch enable.** The high state of this signal indicates that a valid address is presented on LA17–LA31.
SA0–SA19	I	**20-bit system address bus.** These signals form the low-order 20 bits of the 24-bit address supported by 16-bit ISA systems.
LA17–LA23	I	**7-bit latchable address bus.** These signals form the high-order 4 bits of the 24-bit ISA address. When the partial address on LA17–LA23 selects a 128 KB segment containing a TMS34094 memory map which is configured as a 16-bit memory peripheral, $\overline{\text{M16}}$ is generated. The inputs are internally pulled low and may be disconnected from the bus. This allows the TMS34094 to be installed in an 8-bit expansion slot.
D0–D15	I/O	**16-bit data bus.** These signals provide a 16-bit data path to the ISA host.
$\overline{\text{MRDC}}$	I	**Memory read command.** This signal indicates that the TMS34094 should drive its data onto D0–D15 for a valid memory mapped read access. An internal pullup holds this input deasserted when the TMS34094 is installed in an 8-bit expansion slot.
$\overline{\text{SMRDC}}$	I	**System memory read command.** This signal has a similar function as $\overline{\text{MRDC}}$ but is only activated for accesses to host memory addresses between 000000h and 0FFFFFh and for refresh cycles.

signal descriptions (concluded)

SIGNAL	I/O/Z	ISA INTERFACE SIGNALS (continued)
$\overline{\text{MWTC}}$	I	**Memory write command.** This signal is asserted to indicate that the TMS34094 should latch the data from the bus if a valid memory mapped access has been detected. The TMS34094 issues a host write request to the TMS34020 after the valid data has been latched. An internal pullup holds this input deasserted when the TMS34094 is installed in an 8-bit expansion slot.
$\overline{\text{SMWTC}}$	I	**System memory write command.** This signal has a similar function as MWTC but is activated only for accesses to host memory addresses between 000000h and 0FFFFFh.
$\overline{\text{IORC}}$	I	**I/O read command.** This signal indicates that the TMS34094 should drive its data onto D0–D15 if a valid I/O mapped access has been detected.
$\overline{\text{IOWC}}$	I	**I/O write command.** This signal indicates that the TMS34094 should latch data from D0–D15 if a valid I/O access has been detected.
$\overline{\text{SBHE}}$	I	**System byte high enable.** This signal, when low, indicates that the TMS34094, if configured and installed as a 16-bit peripheral, should drive or accept data on the high half of the data bus, D8–D15. An internal pullup resistor holds this input deasserted when the TMS34094 is installed in an 8-bit expansion slot.
AEN	I	**Address enable.** This signal indicates that the TMS34094 may respond to the I/O address and command present on the bus, when AEN = 0.
$\overline{\text{REFRESH}}$	I	**ISA refresh.** The low state of this signal indicates a refresh cycle is in progress in the ISA system. The TMS34094 ignores all ISA refresh cycles.
RESDRV	I	**Reset drive**. Assertion of RESDRV causes a reset of the TMS34094 and asserts the signal $\overline{\text{RESET}}$ low.
CHRDY	O	**Channel ready.** This is an open collector signal and is asserted whenever the TMS34094 must initiate an access to the TMS34020 local memory. In response to an ISA access cycle it indicates that the access has to be extended.
$\overline{\text{M16}}$	O	**16-bit memory data size.** This open collector signal indicates a memory window configured as a 16-bit peripheral has been accessed through the TMS34094.
$\overline{\text{IO16}}$	O	**16-bit I/O data size.** This open collector signal is asserted upon an access to any TMS34094 I/O register. Therefore, 16-bit I/O data transfer will be used whenever the TMS34094 is installed in a 16-bit bus.
PCINT	O	**PC interrupt request.** This totem pole signal issues an interrupt request to the ISA host when it goes from a low to a high state and remains there until the appropriate interrupt routine has been executed. It may be connected directly to an IRQ signal on the ISA bus.
SIGNAL	**I/O/Z**	**LOCAL BUS INTERFACE SIGNALS**
$\overline{\text{BSEL0}}$–$\overline{\text{BSEL3}}$	O	**4 bank select controls.** TheTMS34094 asserts these signals based on decoding of the LAD bus address and the type of access. These signals are typically ORed with the $\overline{\text{RAS}}$ output of the TMS34020 for use as row address strobes for four banks of memory.
SSRT	O	**Shift register transfer indicator.** This active high signal may be used to indicate to the video backend logic (such as the TLC34075) that a shift register transfer has occurred and that an inserted or relocated SCLK pulse should be triggered. This output is typically used only in systems which use VRAMs which require an SCLK pulse between a normal shift register transfer and a split shift register transfer and which enables the TMS34020s generation of split shift register transfers.
VGASHD	O	**VGA shadow indicator.** This active high signal precedes the TMS34020 host cycle caused by a VGA palette access to alert the palette access control logic of a VGA palette access on the ISA bus.
SIGNAL	**I/O/Z**	**CONFIGURATION INTERFACE**
IOSEL0–IOSEL2	I	**I/O base select pins.** Input from these pins selects the base I/O range in ISA space in which the TMS34094 I/O registers appear.
BIOSEN	I	**BIOS ROM enable pin.** Setting this input high maps the BIOS ROM in the TMS34020 local memory into ISA space after reset.

functional block diagram



memory mapped ISA interface to TMS34020 local memory

The memory mapped interface provides the option to map part or parts of the TMS34020 local memory into one or more segments of the ISA host memory space. The memory map registers (MAP0–MAP3) (page 13), base memory registers (BASE0–BASE3) (page 13), and map extension register (MAP0E) (page 8), in the TMS34094 are dedicated to memory mapped interface support. The MODECTL (page 7) register contains the configuration bits for the memory mapped interface.

Each BASEn register contains the base address and size of a segment of ISA memory. The size of each segment can be configured from 8 K-bytes to 4 M-bytes. Associated with each BASEn memory register is a MAPn register which points to a location in TMS34020 local memory. When an ISA memory access falls within one of the segments defined by BASE0–BASE3, the TMS34094 generates HA5–HA31 based on a combination of the ISA address presented and the value in the corresponding MAP0–MAP3 register, and then initiates a host access. Each window may be individually configured to respond as an 8-bit or 16-bit ISA memory mapped device.

The map extension register, MAP0E, extends MAP0 to contain all the address bits required to specify a complete host access address to the TMS34020. This will allow the ISA segment to be completely misaligned from the TMS34020 segment when an access uses the TMS34020s autoincrement mode. The ISA host may transfer up to 4 M-bytes of data without having to remap regardless of the alignment of the start address. The AI bit in the MODECTL register must have the same value as the HPFW bit of the TMS34020's HSTCTLH register, and HLB0 and HLB1 (also HSTCTLH) must both be set to 0 for the TMS34020 to properly track host addresses in autoincrement mode.

I/O mapped ISA interface to TMS34020 local memory

The I/O mapped interface presents a TMS34010-like interface between the ISA bus and the TMS34020 local memory. Communication between the ISA bus and TMS34020 local memory is controlled by three registers HADDRH, HADDRL, and HDATA (pages 11 and 12). HADDRH and HADDRL, in conjunction, hold a 28-bit address pointing to a 16-bit quantity within TMS34020 local memory.

When a read or write access to HDATA occurs, HADDRH and HADDRL values are presented on HA5–HA31 and $\overline{HCS}$ is asserted. If a software application has properly set up the HINC, HPFW, HLB0, and HLB1 bits of HSTCTLH, and has set the AI bit of MODECTL to match HPFW in HSTCTLH, successive reads or writes to HDATA cause the TMS34020 to access sequential words in local memory.

HINC	HPFW	AI	HLB0–HLB 1	TMS34020 OPERATION	TMS34094 OPERATION
0	X	0	X	No autoincrement, no LAD bus half swap	Increment HADDR and swap LAD bus halves after every host access†
0	X	1	X	No autoincrement, no LAD bus swap	Increment HADDR and swap LAD bus halves after every host write†
1	0	0	0	Autoincrement and swap LAD bus halves after every host access	Increment HADDR and swap LAD bus halves after every host access
1	1	1	0	Autoincrement and swap LAD bus halves after every host write	Increment HADDR and swap LAD bus halves after every host write
				Undefined for all other combinations	Undefined for all other combinations

† Autoincrement host reads and writes may read or write incorrect data for these settings. To prevent host accesses from failing for these settings, the TMS34094 must force $\overline{HCS}$ to rise between accesses. In I/O mapped mode (IOE[MODECTL] = 1), write or read HADDRL and/or HADDRH to force $\overline{HCS}$ high. In memory-mapped mode (IOE[MODECTL] = 0), do not use MAP0E (set XD[MAP0E] = 1) and do not perform memory-mapped host reads if AI[MODECTL] = 1.

Access to a non-sequential location requires writing the appropriate value(s) to HADDRH and HADDRL. The contents of HADDRH and HADDRL change after every host access to reflect the address of the next autoincrement access. The address stored in HADDRH and HADDRL may not properly reflect the address of the TMS34020s next host access if HINC = 0, or if HPFW, HLB0–HLB1, and AI are not set to a valid autoincrement mode shown in the table above. When the TMS34094 and TMS34020 are set up for autoincrement after writes, consecutive reads will access alternate 16-bit halves of the 32-bit data transceiver. System software should only use this mode for read-write cycles.

An I/O mapped interface is generally slower than a 16-bit memory mapped interface in making random accesses to the local memory. However, it does not take up any additional host memory or I/O locations and, in a 16-bit expansion slot, it delivers better performance than an 8-bit-only memory mapped interface. When the I/O mapped interface to GSP memory is enabled, the memory mapped interface is disabled.

operations

I/O registers

The functions of the TMS34094 are controlled through 16 registers in ISA I/O space. The registers fall into one of four categories; memory map registers (MAP0–MAP3, MAP0E, BASE0–BASE3), I/O map registers (HADDRH, HADDRL, HDATA, SHDHCTL), local memory decode registers (BKCTL, BKPORT), and a configuration register (MODECTL).

MODECTL

15	14	13	12	11	10 – 7	6	5	4	3 – 0
T16	SRE	AI	PSL	IOE	16M3–16M0	HI	SDD	RS	BE3–BE0

This register contains several of the bits which control how the TMS34094 responds to ISA bus cycles.

T16, when asserted high, allows a software test to determine whether a known add-in card sharing the 128 K-bytes used by a TMS34094 memory map is a 16-bit peripheral. The mechanism suppresses the generation of $\overline{M16}$ without enabling the byte swap logic within the TMS34094. If an 8-bit memory device shares the 128 K-byte segment, the ISA host would perform two successive 8-bit transfers on the lower half of the data bus to write a 16-bit word. Without its byte swap logic, the TMS34094 will receive both bytes with the lower half of its

data transceiver, with the odd byte overwriting the even byte. If a 16-bit peripheral is sharing the memory segment under investigation, it will issue $\overline{M16}$ and allow the TMS34094 to receive the transmission without having to respond with $\overline{M16}$. T16 is cleared after reset.

SRE, when set to 1, enables direct VGA palette reads of the local palette if SDD is set to 0. This feature is typically used when a VGA controller shares the same physical palette as the TMS34020. SRE is cleared after reset, preventing the local palette from responding to VGA palette reads.

PSL selects which half of the LAD bus is connected to a 16-bit memory device when the TMS34020's dynamic bus sizing feature is used. The TMS34094 uses this bit to determine how to swap data during accesses to the 16-bit device. When the 16-bit device is connected to LAD31–LAD16, PSL should be set to zero. When 16-bit device is connected to LAD15–LAD0, PSL should be set to one. When performing a host access to a device on the LAD bus which does not assert $\overline{SIZE16}$, the TMS34094 ignores PSL. PSL is set to zero at reset.

IOE enables the I/O mapped interface to the TMS34020 when set to 1. It should be noted that I/O mapped and memory mapped interfaces to the TMS34020 local memory are mutually exclusive. IOE is set to 0 after reset, which enables the memory mapped interface.

HI is a transparent read-through of the TMS34020 $\overline{HINT}$ output. As it is possible for $\overline{HINT}$ to be activated by a retry or fault on a host access, or by the host/EMU handshake protocol, $\overline{HINT}$ may be active when the INTOUT bit in HSTCTLL (and therefore in SHDHCTL) is inactive.

AI determines how the TMS34094 will increment HADDRH and HADDRL to follow the TMS34020s host address autoincrement mechanism. AI should be set to match the TMS34020s HPFW bit when autoincrement accesses are being performed. The AI bit is set to 0 at reset.

16M3–16M0 are individual $\overline{M16}$ enables for each base register. When an access occurs to a memory segment defined by a base register, BASEn, $\overline{M16}$ is asserted only if the corresponding bit, 16Mn, is set to 1 and the corresponding BEn bit is set to 1. 16M3–16M0 are cleared after reset, configuring memory maps as 8-bit peripherals.

SDD, when set to 1, disables direct VGA palette writes and reads of the local palette. SDD is set to 0 at reset which allows the local palette to respond to VGA palette writes.

RS, when set to 1 causes a reset of the TMS34094 and assertion of the $\overline{RESET}$ signal for at least 4 LCLK1 cycles. RS resets itself to 0.

BE3–BE0 are individual enable bits for the base registers. Setting BEn to 1 enables the decode functions of BASEn. The enables are superceded by IOE. When IOE is set to 1, the memory map functions are disabled regardless of BE3–BE0. At reset, BE2–BE0 are set to 0 and BE3 is set to reflect the BIOSEN pin.

MAP0E

Extended Map Address is utilized in extended mapping mode to form a 32-bit register in conjunction with MAP0. It thus provides a 28-bit address completely specifying a 16-bit word in TMS34020 local memory. The extended address is then used as the initial address for a block of data transfers using the autoincrement mode of the TMS34020. The extended map address is uninitialized after reset.

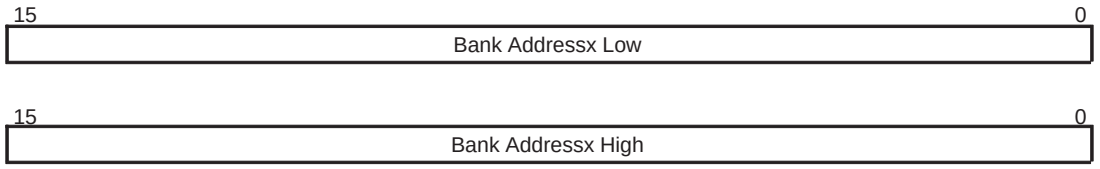
XD disables the extended mapping mode when set to 1. The value of XD after reset is 1, thus map extension is disabled by default.

Bits 3-1 of MAP0E are reserved and should be set to 0 when MAP0E is written.

BKPORT

This register is used to access the bank select address (BKADn) or bank select mask (BKMSKn) register indexed by BPNT3–BPNT0 in the BSCTL register. BPNT3–BPNT0 are autoincremented after every 16-bit access to BKPORT. This register is uninitialized after reset.

BKAD0L–BKAD3L
BKAD0H–BKAD3H

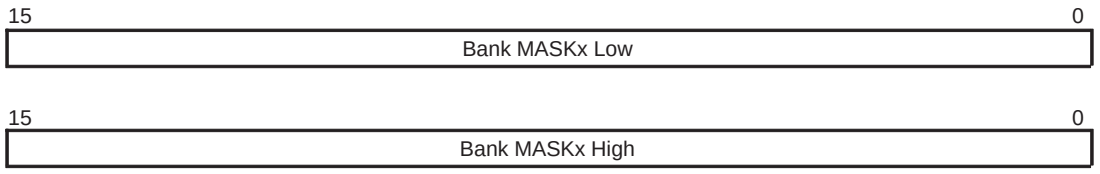


These registers are used to specify the four address compare values for the bank decode logic. Each set of 16-bit BKADxL and 16-bit BKADxH values is treated as a 32-bit BKADx value. Each 32-bit BKADx value is masked using the corresponding BKMSKx value, compared with the LAD bus address bits allowed by the corresponding BKMSKx value and conditioned based on LAD bus cycle type, to generate the corresponding BSELx output. BKCTL provides selective control over whether a BSELx output will or will not respond to DRAM refresh or VRAM special cycles (see *BKCTL*, page 10).

Each 32-bit BKADx register is accessed via the BKPORT register as two 16-bit halves, BKADxL and BKADxH. The BPNT3–BPNT0 bits of the BKCTL register select which bank select register is accessed during a read or write of BKPORT.

Host write accesses to BKAD0–BKAD3 may cause improper decode of ongoing TMS34020 local bus cycles. Do not write to any BKAD0–BKAD3 register when the TMS34020 is performing any operation which could be adversely affected by improper address decoding, including execution of code.

BKMSK0L–BKMSK3L
BKMSK0H–BKMSK3H



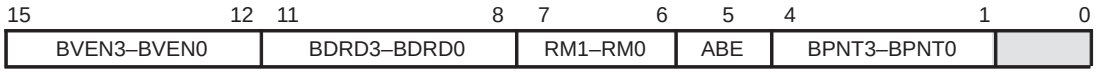
These registers are used to specify the four mask values for the bank decode logic. Each set of 16-bit BKMSKxL and 16-bit BKMSKxH values are treated as a 32-bit BKMSKx value. Each 32-bit BKMSKx value is used to mask the corresponding BKADx value and the LAD31–LAD0 values which are then compared to determine which BSELx output to activate for the given LAD bus cycle. BKCTL provides selective control over whether a BSELx output will or will not respond to DRAM refresh or VRAM special cycles (see *BKCTL*, page 10).

A BKMSKx bit set to 1 allows comparison of the corresponding BKADx bit with the corresponding LAD bus address bit. A BKMSKx bit set to zero causes the 34094 to disregard the corresponding BKADx and LAD bus address bit in the comparison.

Each 32-bit BKMSKx register is accessed via the BKPORT register as two 16-bit halves, BKMSKxL and BKMSKxH. The BPNT3–BPNT0 bits of the BKCTL register select which bank select register is accessed during a read or write of BKPORT.

Host write accesses to BKMSK0–BKMSK3 may cause improper decode of ongoing TMS34020 local bus cycles. Do not write to any BKMSK0–BKMSK3 register when the TMS34020 is performing any operation which could be adversely affected by improper address decoding, including execution of code, may cause improper decode of ongoing TMS34020 local bus cycles.

BKCTL



This register contains several bits which control how the TMS34094 decodes LAD bus cycles for bank select operations.

BVEN3–BVEN0 are individual VRAM selectors for each bank. If a memory bank contains VRAM, it should respond to write mask load or color register load cycles generated by the TMS34020. Setting BVENn to a 1 causes BSELn to be asserted whenever one of these special VRAM cycles occur. BVEN3–BVEN0 are cleared after reset.

BDRD3–BDRD0 are individual DRAM refresh deselectors for each bank. If a bank does not require refresh, the corresponding bit in BDRD3–BDRD0 should be set to 1. This will cause the corresponding bank select signal to ignore DRAM refresh cycles generated by the TMS34020. These bits are cleared after reset.

RM1–RM0 determines how the DRAM refresh cycles generated by the TMS34020 should affect the bank select signals as summarized in the table below. If the memory banks are to be refreshed alternately, the TMS34094 determines which bank is refreshed using the values on LAD16 and LAD17. RM1–RM0 are cleared after reset.

RM1	RM0	FUNCTION
0	0	Refresh all banks simultaneously
0	1	Refresh alternate pairs
1	0	Refresh one bank at a time
1	1	No refresh

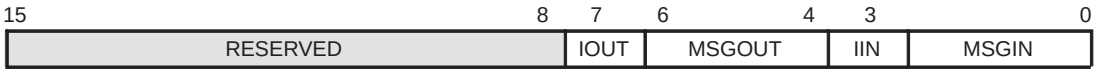
ABE enables all bank select operations. After reset, ABE is set to 0 causing $\overline{\text{BSEL3}}$ to be unconditionally low and all other bank select signals to be inactive (high) except for memory refresh. Setting ABE to 1 allows the bank select signals to decode local addresses from the TMS34020.

BPNT3–BPNT0 are used to index BKPORT to one of the bank select programming registers. BPNT3–BPNT0 will be incremented after each 16-bit access to BKPORT. BPNT3–BPNT0 are set to zero after reset. The registers indexed by BPNT3–BPNT0 are summarized below.

BPNT3–BPNT0	BANK SELECT PROGRAMMING REGISTER
0000b	Bank Address 0 Low (BKAD0L)
0000b	Bank Address 0 High (BKAD0H)
0010b	Bank Address 1 Low (BKAD1L)
0011b	Bank Address 1 High (BKAD1H)
0100b	Bank Address 2 Low (BKAD2L)
0101b	Bank Address 2 High (BKAD2H)
0110b	Bank Address 3 Low (BKAD3L)
0111b	Bank Address 3 High (BKAD3H)
1000b	Bank Select Mask 0 Low (BKMSK0L)
1001b	Bank Select Mask 0 High (BKMSK0H)
1010b	Bank Select Mask 1 Low (BKMSK1L)
1011b	Bank Select Mask 1 High (BKMSK1H)
1100b	Bank Select Mask 2 Low (BKMSK2L)
1101b	Bank Select Mask 2 High (BKMSK2H)
1110b	Bank Select Mask 3 Low (BKMSK3L)
1111b	Bank Select Mask 3 High (BKMSK3H)

Bit 0 of BKCTL is reserved. When writing to BKCTL, bit 0 must be set to 0.

SHDHCTL



This register shadows the least significant byte of the TMS34020s HSTCTLL register to allow the ISA host to poll interrupts and/or messages without having to perform a host access to the TMS34020. This allows handshaking without interrupting the TMS34020s operations. SHDHCTL cannot be written directly by the host; it is only altered by host or TMS34020 cycles to HSTCTLL. The TMS34094 protects the IIN, MSGIN, IOUT, and MSGOUT bits in much the same way as the TMS34020 protects the bits in HSTCTLL. Only the host writes of HSTCTLL may alter MSGIN. Only TMS34020 writes can alter MSGOUT. ISA host writes may only set IIN or clear IOUT. TMS34020 writes may only set IOUT and clear IIN.

SHDHCTL may not properly reflect the state of HSTCTLL if the TMS34020 is reset by setting the RST bit of HSTCTLH.

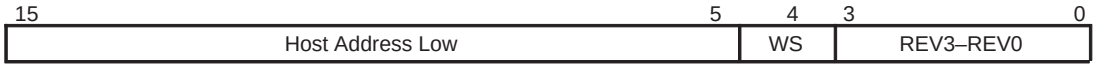
HDATA

In I/O mapped mode, this register is used to access the data transceiver for passing information between the ISA host and the TMS34020 local memory. It is accessed as a 16-bit register from the ISA bus. The WS bit in the HADDRL register determines whether the contents of the register is presented to the upper or lower half of the LAD bus. HDATA is uninitialized after reset. HDATA may be affected by memory mapped accesses when the IOE bit of MODECTL is set to 0.

HADDRH

In I/O mapped mode, the data stored in this register is used to generate HA31–HA16. In conjunction with HADDRL, it forms the address presented to the TMS34020 on HA31–HA5 at the falling edge of $\overline{\text{HCS}}$. This register is uninitialized after reset. HADDRH may be affected by memory mapped accesses when the IOE bit of MODECTL is set to 0.

HADDRL

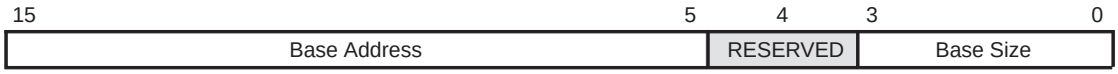


Host Address Low in the I/O mapped mode contains the data used to form HA15–HA5. In conjunction with HADDRH, it forms the address presented to the TMS34020 on HA31–HA5 at the falling edge of $\overline{\text{HCS}}$. It is uninitialized after reset. Host Address is incremented every time the WS bit is toggled from 1 to 0 due to an access to HDATA. HADDRH is incremented when an increment of HADDRL generates a carry out of bit 15. Autoincrement modes are discussed under I/O mapped interface to TMS34020 local memory on page 6. HADDRL may be affected by memory mapped accesses when the IOE bit of MODECTL is set to 0.

WS is used to determine which pair of HBS3–HBS0 signals to assert using HBS01 and HBS23. It is uninitialized after reset. WS is toggled after access to the most significant 8 bits of HDATA, as appropriate for the autoincrement mode defined by the AI bit in MODECTL.

REV3–REV0 are read only bits containing a TMS34094 revision control code.

BASE0–BASE3



Base Address is used in the memory mapped mode. Each register may contain a value which is compared against the address bits on the ISA bus. The address comparison is left aligned, the most significant ISA address (LA23) is compared against the most significant bit in Base Address and so on. When a match occurs, the corresponding memory map is selected, providing that it is enabled by the corresponding bit in BE3–BE0. The number of bits used for the actual comparison depends on the Base Size declared. Base Address 0, 1, and 2 are uninitialized at reset. Base Address 3 is set to 0C0h at reset so that BASE3 points to ISA bus physical address 0C0000h.

Base Size indicates the number of bits from Base Address that should be used to compare against incoming ISA addresses. Base Size 0, 1, and 2 are uninitialized at reset. Base Size 3 is set to 1h so that BASE3 represents a 16K-byte window.

BASE SIZE	SEGMENT SIZE	ISA ADDRESS BITS USED FOR COMPARISON	BASE ADDRESS BITS USED FOR COMPARISON	MAP ADDRESS BITS USED FOR TMS34020 LOCAL MEMORY ADDRESS
0000b	8 K	LA23–17, SA19–13	Base Address 10-0	Map Address 15-0
0001b	16 K	LA23–17, SA19–14	Base Address 10-1	Map Address 15-1
0010b	32 K	LA23–17, SA19–15	Base Address 10-2	Map Address 15-2
0011b	64 K	LA23–17, SA19–16	Base Address 10-3	Map Address 15-3
0100b	128 K	LA23–17, SA19–17	Base Address 10-4	Map Address 15-4
0101b	256 K	LA23–18, SA19–18	Base Address 10-5	Map Address 15-5
0110b	512 K	LA23–19, SA19	Base Address 10-6	Map Address 15-6
0111b	1 M	LA23–20	Base Address 10-7	Map Address 15-7
1000b	2 M	LA23–21	Base Address 10-8	Map Address 15-8
1001b	4 M	LA23–22	Base Address 10-9	Map Address 15-9
All others	Undefined	Undefined	Undefined	Undefined

Bit 4 of each BASEx register is reserved. When writing to these registers, write this bit as a zero.

MAP0–MAP3

Each MAPx register contains a 16-bit value which acts as a pointer into a segment of the TMS34020 local memory. The number of bits used as the most significant part of the host address presented to the TMS34020 is determined by the BASE SIZE field in the corresponding base address register. From 6 to 16 of the most significant bits of the Map Address value will be used, with the ISA address bits providing the lower order address bits. At reset, MAP0–MAP2 are uninitialized and MAP3 is set to 0F000h.

access decode

The IOSEL2–IOSEL0 pins on the TMS34094 are used to determine the base I/O location in ISA I/O space where the I/O registers appear.

IOSEL2–IOSEL0	I/O REGISTER LOCATIONS
000b	Reserved
001b	I/O register disabled
010b	02D0h - 02DFh and 06D0h - 06DFh
011b	02C0h - 02CFh and 06C0h - 06CFh
100b	02B0h - 02BFh and 06B0h - 06BFh
101b	02A0h - 02AFh and 06A0h - 06AFh
110b	0290h - 029Fh and 0690h - 069Fh
111b	0280h - 028Fh and 0680h - 068Fh

Setting the IOSEL2–IOSEL0 inputs to 000b is a reserved configuration and should be avoided in designs. Setting IOSEL2–IOSEL0 to 001b prevents the TMS34094 I/O registers from responding to any I/O accesses from the ISA host. However, the device would still respond to VGA palette accesses if VGASHD is enabled (see description of the MODECTL register).

All other settings of IOSEL2–IOSEL0 select 32 byte locations in ISA I/O space where the sixteen TMS34094 I/O registers will appear. Eight of these registers appear in ISA I/O space between 02x0h and 02xfh, the remaining eight appear in extended I/O space between 06x0h and 06xfh. Thus, only 16 bytes of the standard I/O space available to ISA peripheral devices are occupied.

ISA I/O LOCATION	TMS34094 REGISTER
02×0h – 02×1h	Memory Map Register 0 (MAP0)
02×2h – 02×3h	Memory Map Register 1 (MAP1)
02×4h – 02×5h	Memory Map Register 2 (MAP2)
02×6h – 02×7h	Memory Map Register 3 (MAP3)
02×8h – 02×9h	Base Memory Register 0 (BASE0)
02×Ah – 02×Bh	Base Memory Register 1 (BASE1)
02×Ch – 02×Dh	Base Memory Register 2 (BASE2)
02×Eh – 02×Fh	Base Memory Register 3 (BASE3)
06×0h – 06×1h	Host Address Low (HADDRL)
06×2h – 06×3h	Host Address High (HADDRH)
06×4h – 06×5h	Host Data (HDATA)
06×6h – 06×7h	Shadow HSTCTLL (SHDHCTL)
06×8h – 06×9h	Bank Select Control (BKCTL)
06×Ah – 06×Bh	Bank Select Data Port (BKPORT)
06×Ch – 06×Dh	Map Extension (MAP0E)
06×Eh – 06×Fh	Mode Control (MODECTL)
× = 8, 9, A, B, C, or D	

graphics system interface

The TMS34094 generates all the inputs required by the TMS34020 host interface to support normal and autoincrement accesses. Additionally, the graphics system interface indicates VGA palette accesses and VRAM split serial register transfers to the video back-end to further simply the design of a TMS34020 based graphics system.

data flow

The TMS34094 transfers data between the ISA bus and the TMS34020 local bus via its internal data transceivers. These transceivers implement a 32-bit wide data path and appropriate data steering to allow the TMS34094 to operate either as a 16-bit or 8-bit ISA peripheral.

The TMS34094 implements its 32-bit wide data transceiver as two separate 16-bit wide halves. This means that the TMS34094 will treat all host accesses as 16-bit accesses to either the even or the odd 16-bit word of the 32-bit long-word specified by the address presented on HA31–HA5. The TMS34094 provides two signals to specify which 16-bit half will be accessed. The TMS34094 asserts HBS01 high when accessing the even 16-bit word of data and asserts HBS23 when accessing the odd 16-bit word. HBS01 is connected to both HBS0 and HBS1 and indicates, when high, an access to the even 16-bit word. HBS23 is connected to both HBS2 and HBS3, and indicates an access to the odd word. When the TMS34020 local memory device responds as a 32-bit wide device, the even word corresponds to data on LAD15–LAD0 and the odd word corresponds to data on LAD31–LAD16.

When the TMS34094 is operating as a ISA 16-bit device, data steering between the 16-bit transceiver halves and the ISA bus is based on the TMS34020 address of the data to be accessed. In memory mapped mode when MAP0E is disabled, HBS23 (which follows SA1) determines which 16-bit half of the 32-bit data transceiver is to be accessed. In I/O mapped mode, the WS bit of HADDRL determines which half of the transceiver is to be accessed. In memory mapped mode with MAP0E enabled, the TMS34094 selects which 16-bit half is used based on the original value in MAP0E bit 4, and swaps 16-bit halves as appropriate for the setting of AI bit in MODECTL.

When the TMS34094 is operating as an 8-bit memory-mapped device or is installed in an 8-bit slot and operating in I/O mapped mode, the 16-bit half of the transceiver is selected in the same manner as shown above for operation as a 16-bit device. SA0 determines which portion of the selected 16-bit half of the data transceiver is to be accessed. The TMS34094 assumes that both the low byte and the high byte of the selected 16-bit half of the transceiver will be accessed, in that order. For host writes, the TMS34094 will not deassert $\overline{\text{HWRITE}}$ until the most significant 8-bits of the 16-bit half of the data transceiver have been written. For host reads, the ISA bus read of the least significant 8-bits will be wait-stated until the 32-bit long word which contains the requested data has been loaded into the data transceiver. The read of the most significant 8-bits of the requested 16-bit word will not be wait-stated.

Because the TMS34094 implements its 32-bit wide data transceiver as two separate 16-bit wide halves, software which accesses the TMS34094's interface to TMS34020 memory should only use instructions which access the entire 16-bit half of the transceiver. When the TMS34094 is operating as an 8-bit memory mapped device or is installed in an 8-bit ISA bus slot, the motherboard will serialize the 16-bit access into two 8-bit accesses. Since a serialized instruction must be completed before any other instruction is begun, there is no possibility that data could be orphaned in the data transceiver if a hardware interrupt occurred during the serialized cycle.

accessing I/O registers

The TMS34094 I/O registers can be accessed as 8 or 16 bit quantities. $\overline{\text{IO16}}$ is always asserted when the TMS34094 detects an access to one of its registers. However, $\overline{\text{SBHE}}$ from the host is used to determine the actual size of the communications channel.

VGA passthrough support

VGA passthrough refers to the display of VGA images from the palette which is otherwise used by the TMS34020 graphics system. To properly reproduce the VGA image, the TMS34020 system's palette must contain the same color look-up table information and read mask as the VGA's palette.This requires the host to be able to communicate with the TMS34020 system's palette as if it were a standard VGA palette via accesses to ISA locations 03C6h to 03C9h. Usually, the VGA display hardware, complete with its own palette, co-exists with the TMS34020 and its palette within the ISA host. Therefore, the host is allowed to write to both palettes during VGA passthrough but read only from the VGA palette. The palette in the TMS34020 system which mirrors the VGA palette setup during VGA passthrough is commonly known as the *shadow palette*.

The TMS34094 can detect read and/or write accesses to the VGA palette and initiate a host access. The standard VGA palette register control inputs, which select the register accessed within the VGA palette, will be available on the two most significant bits of local address. The VGASHD output is asserted prior to the host cycle generated by a VGA palette access and remains active during the cycle. $\overline{\text{BSEL3}}$–$\overline{\text{BSEL0}}$ remain inactive (high) during the host VGA passthrough cycle.

The TMS34020 indicates a host cycle in progress by presenting a status code 0010b on LAD3–LAD0 at the falling edge of $\overline{\text{ALTCH}}$. The palette control logic should detect VGASHD and the subsequent host cycle to identify a VGA palette access. The value on LAD31 and LAD30 at the falling edge of $\overline{\text{ALTCH}}$ determines the register accessed. Note: The value of LAD30 is copied to LAD29 to prevent the TMS34020s I/O registers from being accessed accidentally.

SA9–SA0	LAD31–LAD29	PALETTE REGISTER
03C6h	100b	Read Mask
03C7h	111b	Read Index
03C8h	000b	Write Index
03C9h	011b	Color Data

The SDD and SRE bits in MODECTL control VGA palette support. When SDD is set to 0 and SRE set to 1, both read and write access to the VGA palette registers will activate VGASHD and cause a host cycle. This allows a VGA to share the same palette as the TMS34020. If both SRE and SDD are set to 0, only write access to VGA palette registers will be allowed. This allows the palette to shadow the register contents of the VGA palette for VGA passthrough operations.

SDD	SRE	PALETTE ACCESS
0	0	Shadow VGA palette writes (VGA has separate palette)
0	1	Shadow all VGA palette access (VGA does not have its own palette)
1	X	VGASHD is disabled, no VGA shadowing

NOTE: Decoding of VGA passthrough cycles must not rely on any particular $\overline{\text{CASx}}$ strobe going active during the LAD bus host cycle. When the TMS34094 is operating in memory mapped mode (IOE[MODECTL] = 0), HBS23 follows SA1 and HBS01 follows the inverse of SA1. When the TMS34094 is in I/O mapped mode, (IOE[MODECTL] = 1), HBS01 and HBS23 retain their previous values. Since HBS01 and HBS23 will always be the inverse of each other, the LAD bus host cycle corresponding to the VGA passthrough request will execute either with both $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ active or with both $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$ active. VGA passthrough write data will be placed onto LAD7–LAD0, regardless of which $\overline{\text{CAS}}$ strobes are active. VGA passthrough read data is expected on LAD7–LAD0.

split serial register transfer support

The TMS34020 generates split serial register transfer cycles to VRAM when the SRT bit in the DPYCTL register is set. During horizontal blanking, a regular transfer cycle is generated to transfer the next row of pixel data into the serial register. This is immediately followed by a split serial register transfer cycle to replace the inactive half row of serial register data with new undisplayed data, rather than those most recently displayed.

Most VRAM require a shift clock pulse between the normal serial register transfer and the split register transfer to ensure that the tap point presented during the normal serial transfer is not overwritten by the tap point of the split shift register transfer. The TMS34094 provides an SSRT signal between the rising edge of $\overline{RAS}$ at the end of the normal transfer cycle and the next falling edge of LCLK2. This signal may be used to indicate to the TLC34075 (or other SCLK generating circuit) that a shift clock pulse must be generated.

local address decode

The TMS34094 provides four active low bank select signals. $\overline{BSEL0}$–$\overline{BSEL3}$ are typically gated externally with $\overline{RAS}$ to form four separate row-address strobes to four banks of memory devices.

Each bank select control mechanism is defined by the contents of five registers:

- Two 16-bit Bank Select Mask Registers. These registers form a 32-bit value to define which bits of the address output on LAD31–LAD0 are to be ignored when determining whether a bank has been selected. A bit set to 0 in a mask register corresponds to an address bit which is ignored.
- Two 16-bit Bank Select Address Registers. These registers form a 32-bit quantity which determines the value of the unmasked bits of the address output on LAD31–LAD0 that should select the bank.
- The values of BVEN3–BVEN0, BDRD3–BDRD0, and RM1–RM0 in the BKCTL register determine how the bank should be selected for VRAM write mask or color register load cycles, and DRAM refresh cycles.

To place a bank of RAM into TMS34020 memory space without aliasing, use the following formula to determine the BKMSK value:

BKMSKx = 0FFFFFFFFh – (bank size in bits) + 1

Therefore, the BKMSKx value for a 1MByte bank of RAM connected to $\overline{BSEL1}$ is:

BKMSK1 = 0FFFFFFFFh – 0800000h + 1 = 0FF800000h

For this setting, the bank select mechanism will only compare BKAD1 bits 31 through 23 with LAD bus address bits 31 through 23. BKAD1 bits 22 through 0 and LAD address bits 22 through 0 will be ignored.

$\overline{BSEL0}$–$\overline{BSEL3}$ are inactive during a VGA shadow palette access. A $\overline{BSELx}$ signal will only go active during VRAM write-mask-load cycles and color-register-load cycles if its corresponding BVEN bit is set. The value of the BPNT field in BKCTL is used as an index into the BKAD0–BKAD3 and BKMSK0–BKMSK3 registers. Data accesses to the indexed register are performed via the BKPORT register.

Bank 3 is unconditionally enabled for all accesses except VGA shadow reads/writes after reset. All other banks are disabled except for memory refresh when ABE is set to 0. Bank select control must be initialized by setting ABE in MODECTL to 1.

Host write accesses to BKAD3–BKAD0 or BKMSK3–BKMSK0 may cause improper decoding of ongoing TMS34020 local bus cycles. Do not write any BKAD3–BKAD0 or BKMSK3–BKMSK0 register while the TMS34020 is performing any operation which could be adversely affected by improper address decoding, including execution of code. When multiple banks are programmed to respond to the same LAD bus address, the TMS34094 will assert only the lowest-numbered $\overline{BSELn}$ output.

BIOS support

The TMS34094 provides the ability for a BIOS ROM in TMS34020 local memory to be mapped to ISA host memory at power-up and ROM scan. When the input to the BIOSEN pin is asserted high, the BASE3/MAP3 register pairs are initialized differently for BIOS ROM support.

The value of BASE3 is set to 0C01h after reset. This selects 0C000h as the ISA segment address with a 16 K segment size. The $\overline{\text{BSEL3}}$ output is unconditionally active for all host accesses other than VGA palette shadow reads or writes after reset. A BIOS ROM controlled by BASE3 therefore appears at ISA memory space 0C0000h to 0C3FFFh for ROM scan. The value for MAP3 is initialized to 0F000h so that the BIOS ROM may appear at 0F0000000h to 0F001FFFFh in local memory. After reset, the TMS34020 will be placed in Host Present Mode and remain halted until the host requests that the TMS34020 begin execution.

The segment size and the location of the BIOS ROM can be changed after reset by changing the values in BANK3, MAP3, BKAD3, and BKMSK3.

typical system interconnections

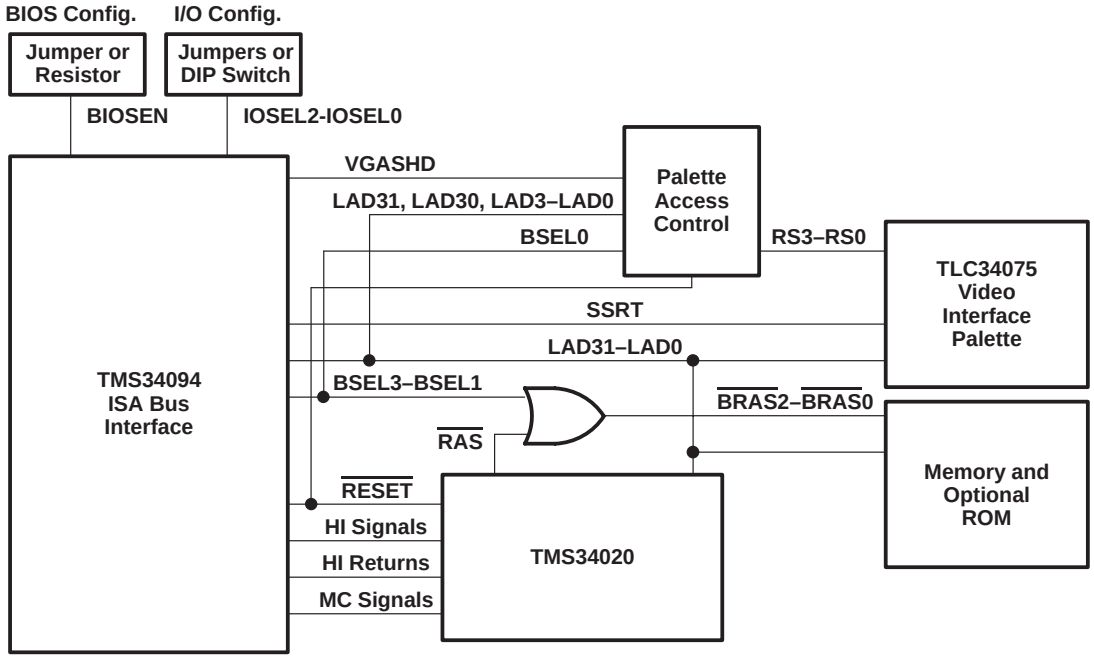


Figure 1. The TMS34094 Used in a Typical TMS34020 System.

Figure 1 is a high level block diagram showing a typical, highly integrated design using the TMS34094, a TMS34020, and a TLC34075. The HI signals are host interface inputs to the TMS34020: HA31–HA5, HBS01, HBS23, $\overline{\text{HCS}}$, $\overline{\text{HREAD}}$, $\overline{\text{HWRITE}}$. The HI returns are responses from the TMS34020: $\overline{\text{HINT}}$, $\overline{\text{HOE}}$, HDST, and HRDY. The MC signals are memory control signals from the TMS34020: $\overline{\text{ALTCH}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS2}}$, $\overline{\text{WE}}$, SF, LCLK1, and LCLK2.

Three of the four bank select control signals from the TMS34094 are used to control memory devices on the TMS34020 local bus. The optional BIOS ROM, if present, should be controlled by BSEL3. Otherwise, BSEL3 is available to control accesses to another bank of display or program memory. BSEL0 is used to decode TMS34020 access to the palette.

implementing a low chip count TMS34020 display system

The following sections will consider the implementation of a highly integrated display system with the following features:

— Variable display resolution (from 640 × 480 up to 1280 × 1024)

— Variable color depth support 1/2/4/8 bits per pixel at all resolutions, and a 24-bit true color plus 8-bit overlay at 640 × 480

— Memory mapped and I/O mapped interface

— Supports installation in an 8-bit or 16-bit ISA expansion slot

— VGA passthrough support

Since the feature set does not require the support of BIOS ROM, BIOSEN should be pulled down externally. IOSEL2–IOSEL0 will be connected to a set of jumpers or dip switches to allow the user to select the I/O base address for the system. Figure 2 illustrates the local memory map implemented in this discussion.

0FFFF FFFFh to 0FF80 0000h	DRAM Bank 0 (1M-Byte)
0FF7F FFFFh to 0C000 2200h	Unused
0C000 21FFh to 0C000 2000h	TLC34075 Registers
0C000 1FFFh to 0C000 0000h	TMS34020 I/O Registers
0BFFF FFFFh to 00200 0000h	Unused
001FF FFFFh to 00180 0000h	VRAM Bank 1 (1M-Byte)
0017F FFFFh to 00100 0000h	VRAM Bank 0 (1M-Byte)
00100 0000h to 00000 0000h	Unused

Figure 2. Sample Memory Map Implemented With a TMS34094

After reset, the device driver software should initialize the BKCTL and BKPORT registers in the TMS34094 to realize the memory map.

REGISTER VALUE	MEMORY SEGMENT
BKAD0L = 02000h BKAD0H = 0C000h BKMSK0L = 0FE00h BKMSK0H = 0FFFFh	TLC34075 Registers
BKAD1L = 00000h BKAD1H = 0FF80h BKMSK1L = 00000h BKMSK1H = 0FF80h	DRAM Bank 0
BKAD2L = 00000h BKAD2H = 00180h BKMSK2L = 00000h BKMSK2H = 0FF80h	VRAM Bank 1
BKAD3L = 00000h BKAD3H = 00100h BKMSK3L = 00000h BKMSK3H = 0FF80h	VRAM Bank 0

Driver software should set up the memory mapped interface. How the memory map should be set up depends on the system environment in the host. The following example shows the use of three map registers to map local memory organized as described in Figure 2 to a continuous block in ISA extended memory.

REGISTER VALUE	MAPPING FUNCTION
BASE0 = 0C007h MAP0 = 001000000h	Memory Map 0 is pointing at a 1 MB segment containing VRAM bank 0 and 1. They appear at extended ISA memory 0C00000h to 0CFFFFFh. MAP0E can be used to extend this register so that the host can transfer 2 MB of data continuously from 01000000h to 01FFFFFFh in local memory without having to modify the value in MAP0.
BASE1 = 0D007h MAP1 = 0FF800000h	Memory Map 1 is pointing at a 1 MB segment containing DRAM bank 0. They appear at extended ISA memory 0D00000h to 0DFFFFFh.
BASE2 = 0E000h MAP2 = 0C0000000h	Memory Map 3 is pointing at an 8 KB segment containing the TMS34020 and TLC34075 registers. They appear at extended ISA memory 0E00000h to 0E01FFFh.

NOTE: These register values place the memory windows outside the addrress space normally available to real mode applications.

If an I/O mapped interface is more appropriate due to constraints in the system environment, the driver software sets IOE in MODECTL.

The TMS34094 is configured for VGA passthrough support after reset. The driver software should set SDD in MODECTL to disable passthrough operations before allowing the TMS34020 to access the palette.

With split serial register transfer support in the TMS34094 and the TLC34075, variable display resolution and color depth requires only the appropriate oscillators and register settings within the TMS34020 and the TLC34075.

BIOS ROM support

For designs that require a BIOS ROM, BIOSEN should be pulled up and the ROM should be enabled by BSEL3. This utilizes the access control signal used for VRAM0 in the memory map in Figure 2. External logic to provide additional local decode may thus be necessary if more than two banks of memory are supported. As the BIOS is mapped to ISA memory location 0C0000h to 0C3FFFh it should not be used in a system which contains a VGA BIOS.

After ROM scan, the driver software may relocate the BIOS ROM in both host memory space and in TMS34020 local memory space by changing the values in BASE3, MAP3, BKAD3L, and BKAD3H.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.5 V to 7 V
Input voltage range, V_I . . . . . – 0.5 V to 7 V
Output voltage range, V_O . . . . . – 0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current , I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 20 mA
Continuous output current, (V_O = 0 to V_{CC}) . . . . . ± 25 mA
Operating free-air temperature range: . . . . . 0 °C to 55 °C
Storage temperature range . . . . . – 65 °C to 150 °C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage	$\overline{HOE}$	0.7 V_{CC}			V
		All other inputs	2			V
V_{IL}	Low-level input voltage	$\overline{HOE}$			0.2 V_{CC}	V
		All other inputs			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_A	Operating free-air temperature		0		55	°C

DC electrical characteristics over full ranges of recommended operating conditions

PARAMETER			MIN	MAX	UNIT
V_{OH}	High-level output voltage		3.7		V
V_{OL}	Low-level input voltage			0.5	V
I_I	Input current		– 1	1	µA
I_{OH}	High-level output current	D15–D0, PCINT		– 3	mA
		LAD31–LAD0		– 2	mA
		$\overline{BSEL3}$–$\overline{BSEL0}$ HA31–HA5, HBS01, HBS23, $\overline{HCS}$, $\overline{HWRITE}$, $\overline{HREAD}$, $\overline{RESET}$, SSRT, VGASHD		– 1	mA
I_{OL}	Low-level output current	D15–D0, $\overline{IO16}$, CHRDY, $\overline{M16}$, PCINT		24	mA
		LAD31–LAD0		4	mA
		$\overline{BSEL3}$–$\overline{BSEL0}$ HA31–HA5, HBS01, HBS23, $\overline{HCS}$, $\overline{HWRITE}$, $\overline{HREAD}$, $\overline{RESET}$, SSRT, VGASHD		1	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		200	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_I	Input capacitance			10		pF
C_O	Output capacitance			15		pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	t_{LCLKH}	Pulse width, LCLK1, LCLK2 high	$2t_Q - 7.5$		ns
2	t_{LCLKC}	Cycle time, LCLK1 and LCLK2	25		ns
3	t_{BCKC}	Cycle time, BCLK	120		ns
4	t_{BCKH}	Pulse width, BCLK high	55		ns
5	$t_{ALLLCK2L}$	Setup time, $\overline{\text{ALTCH}}$ low before LCLK2 low (see Note 2)	10		ns
6	t_{BCKL}	Pulse width, BCLK low	55		ns
7	t_{LCLKL}	Pulse width, LCLK1, LCLK2 low	$2t_Q - 7.5$		ns
8	t_{HIWD}	Delay time, D15–D0 valid after $\overline{\text{IOWC}}$ low (see Note 3)		0	ns
9	t_{MRLDNZ}	Delay time, D15–D0 driven after Memory read strobe low	5	45	ns
10	t_{IORLDV}	Delay time, $\overline{\text{IORC}}$ low to D15–D0 valid (see Note 4)	10	75	ns
11	$t_{IORLDNZ}$	Delay time, $\overline{\text{IORC}}$ low to D15–D0 driven	5	45	ns
12	t_{DSMS}	D15–D0 setup time to Memory write strobe high	5		ns
13	t_{DSIOWH}	Setup time, D15–D0 valid before $\overline{\text{IOWC}}$ high	5		ns
14	t_{LADOEA}	LAD31–LAD0 access time after $\overline{\text{HOE}}$ low	0	18	ns
15	$t_{LADSHDSTH}$	Setup time, LAD31–LAD0 valid before HDST rise	5		ns
16	$t_{LADSLCK2L}$	Setup time, LAD31–LAD0 valid before LCLK2 fall	5		ns
17	t_{DAP}	Data access time (see Note 9)	15	90	ns
18	t_{LCK2DV}	Delay time, LCLK2 fall to D15–D0 valid (see Note 5)		70	ns
19	$t_{LADHLCK2L}$	Hold time, LAD31–LAD0 valid after LCLK2 fall	5		ns
20	t_{HDSTDV}	Delay time, HDST high to D15–D0 valid (see Note 5)		70	ns
21	$t_{LADHHDSTH}$	Hold time, LAD31–LAD0 valid after HDST rise	5		ns
22	t_{LADZ}	LAD31–LAD0 disable time after $\overline{\text{HOE}}$ high	10	20	ns
23	t_{DHMS}	D15–D0 hold time after Memory write strobe high	5		ns
24	t_{DHIOWH}	Hold time, D15–D0 valid after $\overline{\text{IOWC}}$ high	5		ns
25	t_{MRHDZ}	D15–D0 disable time after Memory read strobe high	10	30	ns
26	t_{IORHDZ}	D15–D0 disable time after $\overline{\text{IORC}}$ high	10	30	ns
27	t_{MSLHSL}	Delay time, Memory strobe low to host strobe low	20	95	ns
28	$t_{IOSLHSL}$	Delay time, I/O strobe low to host strobe low	15	90	ns
29	t_{MSHHSH}	Delay time, Memory strobe high to host strobe high (see Note 6)	10	65	ns
30	$t_{IOWHHWH}$	Delay time, $\overline{\text{IOWC}}$ high to $\overline{\text{HWRITE}}$ high (see Note 6)	10	50	ns
31	$t_{IORHHRH}$	Delay time, $\overline{\text{IORC}}$ high to $\overline{\text{HREAD}}$ high (see Note 6)	10	50	ns
32	t_{MSLCRL}	Delay time, Memory strobe low to CHRDY low	0	25	ns
33	$t_{IOSLCRL}$	Delay, I/O strobe low to CHRDY low	0	20	ns
34	t_{HRHCRZ}	CHRDY disable time after HRDY high (see Note 7)	5	25	ns
35	t_{HEHCRZ}	CHRDY disable time after $\overline{\text{HOE}}$ high (see Note 8)	5	25	ns
36	$t_{PHRHCRZ}$	CHRDY disable time after HRDY high (see Note 9)	5	25	ns
37	$t_{HDSTHCRZ}$	CHRDY disable time after HDST high (see Note 5)	5	25	ns
38	t_{HIWHAV}	Delay time, $\overline{\text{IOWC}}$ low to HA31–HA5, HBS01, HBS23 valid (see Note 3)	15	$.5t_{BCKC} + 90$	ns

NOTES: 2. For LAD bus host cycles only.
3. For writes to HADDRL and HADDRH only.
4. Not valid for accesses to HDATA or shadow VGA registers.
5. For host read of non-prefetched data only.
6. When operating as an 8-bit device, this parameter is applicable only to the second byte transfer of the serialized access.
7. For host write when no previous host write is pending.
8. For host write when a previous host write is pending.
9. For host read of prefetched data only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) continued

NO.	PARAMETER		MIN	MAX	UNIT
39	t_{ISLCSH}	Delay time, I/O strobe low to $\overline{HCS}$ high (see Note 10)	5	50	ns
40	$t_{IOSLCSL}$	Delay time, I/O strobe low to $\overline{HCS}$ low	10	65	ns
41	t_{HSHHAV}	Delay time, Host strobe high to incremented HA31–HA5 valid	25	145	ns
42	t_{HSHHBV}	Delay time, Host strobe high to incremented HBS01, HBS23 valid	10	50	ns
43	t_{SAVHAV}	Delay time, SA19–SA0 valid to HA31–HA5, HBS01, HBS23 valid	20	95	ns
44	t_{MSLCSL}	Delay time, Memory strobe low to $\overline{HCS}$ low (see Note 11)	15	75	ns
45	t_{MSHCSH}	Delay time, Memory strobe high to $\overline{HCS}$ high (see Notes 6 and 12)	10	50	ns
46	$t_{SANVHANV}$	Delay, SA19–SA0 no longer valid to HBS01, HBS23, and HA31–HA5 no longer valid	5	40	ns
47	$t_{FMSLCSL}$	Delay, Memory strobe low to $\overline{HCS}$ low (see Note 13)		$.5t_{BCKC}$ + 60	ns
48	t_{MSLCSH}	Delay time, memory strobe low to $\overline{HCS}$ high (see Note 13)		45	ns
49	t_{LAS}	LA23–LA17 setup time to BALE falling edge	5		ns
50	$t_{LAVM16L}$	Delay time, LA23–LA17 valid to $\overline{M16}$ low	0	35	ns
51	$t_{AENLI16L}$	Delay time, AEN low to $\overline{IO16}$ low		30	ns
52	$t_{SAVI16L}$	Delay time, SA10–SA0 valid to $\overline{IO16}$ low	5	35	ns
53	t_{LAH}	LA23–LA17 hold time after BALE falling edge	10		ns
54	t_{M16Z}	$\overline{M16}$ disable time after LA23–LA17 no longer valid	5	25	ns
55	$t_{I16ZAEN}$	$\overline{IO16}$ disable time after AEN high		20	ns
56	t_{I16ZSA}	$\overline{IO16}$ disable time after SA10–SA0 invalid	0	20	ns
57	$t_{VISLHAV}$	Delay time, I/O strobe low to HA31–HA29 valid (see Note 14)	15	85	ns
58	$t_{VISLHCL}$	Delay time, I/O strobe low to $\overline{HCS}$ low (see Note 14)	10	$.5t_{BCKC}$ + 60	ns
59	$t_{VIOWLVSH}$	Delay time, $\overline{IOWC}$ low to VGASHAD high (see Note 15)	5	55	ns
60	$t_{VISLHSL}$	Delay time, I/O strobe low to host strobe low (see Note 14)	15	$.5t_{BCKC}$ + 75	ns
61	$t_{VIORLVSH}$	Delay time, $\overline{IORC}$ low to VGASHAD high (see Note 16)	5	55	ns
62	$t_{VHELVSH}$	Delay time, $\overline{HOE}$ low to VGASHAD high (see Note 17)	5	45	ns
63	$t_{VISHHANV}$	Delay time, I/O strobe high to HA31–HA5 no longer valid for shadowed VGA register access	10	55	ns
64	$t_{VISHCSH}$	Delay time, I/O strobe high to $\overline{HCS}$ high (see Notes 6 and 14)	5	45	ns
65	$t_{VIORHVSL}$	Delay, $\overline{IORC}$ high to VGASHAD low (see Note 16)	15	80	ns
66	$t_{VHELVSL}$	Delay time, $\overline{HOE}$ low to VGASHAD low	15	70	ns
67	$t_{HILPCIL}$	Delay time, $\overline{HINT}$ low to PCINT high	0	30	ns
68	$t_{HIHPCIH}$	Delay time, $\overline{HINT}$ high to PCINT low	5	35	ns
69	t_{RSDH}	Pulse width, RESDRV high	$9t_Q$		ns
70	$t_{RSDHRSTL}$	Delay, RESDRV high to $\overline{RESET}$ low	$5t_Q - 5$	$5t_Q$ + 75	ns
71	$t_{IOSHRSDH}$	Hold time, IOSEL2–IOSEL0 valid after RESDRV high	100		ns
72	t_{RSDHDZ}	D15–D0 disable time after RESDRV high		$5t_Q$	ns
73	$t_{RSDHSRTZ}$	SSRT disable time after RESDRV high	$5t_Q$	$5t_Q$ + 45	ns
74	$t_{RSDHCSZ}$	$\overline{HCS}$ disable time after RESDRV high	$5t_Q$	$5t_Q$ + 50	ns

NOTES: 6. When operating as an 8-bit device, this parameter is applicable only to the second byte transfer of the serialized access.
10. For accesses to HADDRL, HADDRH, or shadowed VGA registers only.
11. Parameter 7 applies when Note 13 does not apply.
12. HCS will not be forced high after a memory-mapped read when AI = 1, or after a memory mapped access to MAP0 when MAP0E is enabled.
13. For memory mapped access where current access is to a different MAP than the previous access and either the previous access was a read with AI = 1 or the last access was to MAP0 with MAP0E enabled.
14. Only valid for accesses to shadow VGA registers.
15. Only valid for write to shadow VGA register.
16. Only valid for read of shadow VGA register.
17. When a previous host write has not yet been completed.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) concluded

NO.	PARAMETER		MIN	MAX	UNIT
75	$t_{RSDHHWZ}$	HWRITE disable time after RESDRV high	$5t_Q$	$5t_Q + 50$	ns
76	$t_{RSDHHRZ}$	HREAD disable time after RESDRV high	$5t_Q$	$5t_Q + 50$	ns
77	$t_{RSDHHBZ}$	HBS01, HBS23 disable time after RESDRV high	$5t_Q$	$5t_Q + 50$	ns
78	$t_{RSDHVSZ}$	VGASHAD disable time after RESDRV high	$5t_Q$	$5t_Q + 45$	ns
79	$t_{RSDHBSZ}$	BSEL3–BSEL0 disable time after RESDRV high	$5t_Q$	$5t_Q + 40$	ns
80	$t_{RSDHHANV}$	Delay time, HA31–HA5 no longer valid after RESDRV high	$5t_Q$	$5t_Q + 50$	ns
81	$t_{RSDHCRZ}$	CHRDY disable time after RESDRV high		$5t_Q$	ns
82	$t_{RSDHIO16Z}$	IO16 disable time after RESDRV high		$5t_Q$	ns
83	$t_{RSDHM16Z}$	M16 disable time after RESDRV high		$5t_Q$	ns
84	$t_{IOSSRSDL}$	Setup time, IOSEL2–IOSEL0 valid before RESDRV low	100		ns
85	$t_{BIOSRSDL}$	Setup time, BIOSEN valid before RESDRV low	0		ns
86	$t_{RSDLRSTH}$	Delay time, RESDRV low to RESET high		50	ns
87	$t_{BIOHRSDL}$	Hold time, BIOSEN valid after RESDRV low	25		ns
88	$t_{RSDLSRTL}$	Delay time, RESDRV low to SSRT low		60	ns
89	$t_{RSDLCSH}$	Delay time, RESDRV low to HCS high		60	ns
90	$t_{RSDLHWH}$	Delay time, RESDRV low to HWRITE high		55	ns
91	$t_{RSDLHRH}$	Delay time, RESDRV low to HREAD high		55	ns
92	$t_{RSDLHBNZ}$	Delay time, RESDRV low to HBS01, HBS23 driven		90	ns
93	$t_{RSDLVSL}$	Delay time, RESDRV low to VGASHAD low		90	ns
94	$t_{RSDLBSNZ}$	Delay time, RESDRV low to BSEL3–BSEL0 driven		45	ns
95	$t_{LADSALL}$	Setup time, LAD31–LAD0 address and status valid before ALTCH low	5		ns
96	$t_{LADVBSV}$	Delay time, LAD31–LAD0 address and status valid to BSEL3–BSEL0 valid	0	25	ns
97	t_{ALHBSV}	Delay time, BSEL3–BSEL0 transparently decodes LAD31–LAD0 after the later of ALTCH high, RAS high		30	ns
98	$t_{LADHALL}$	Hold time, LAD31–LAD0 address and status valid after ALTCH low	5		ns
99	$t_{SFLLCK1L}$	Setup time, SF low before LCLK1 low	5		ns
100	$t_{CASSLCK1L}$	Setup time, CAS2 low before LCLK1 low	5		ns
101	$t_{LCK2LSRTH}$	Delay time, LCLK2 low to SSRT high	0	25	ns
102	$t_{LCK2LSRTL}$	Delay time, LCLK2 low to SSRT low	5	45	ns
103	$t_{AENVISL}$	Delay time, AEN valid to I/O strobe low	95		ns
104	t_{SBSISL}	Setup time, SBHE valid before I/O strobe low	85		ns
105	t_{SASISL}	Setup time, SA10–SA0 valid before I/O strobe low	85		ns
106	t_{SBSMSL}	Setup time, SBHE valid before MEM strobe low	22		ns
107	t_{SASMSL}	Setup time, SA19–SA0 valid before MEM strobe low	22		ns
108	$t_{AENVISH}$	Delay time, AEN valid after I/O stobe high	28		ns
109	t_{SBHISH}	Hold time, SBHE valid after I/O stobe high	30		ns
110	t_{SAHISH}	Hold time, SA10–SA0 valid after I/O strobe high	30		ns
111	t_{SBHMSH}	Hold time, SBHE valid after MEM stobe high	30		ns
112	t_{SAHMSH}	Hold time, SA19–SA0 valid after MEM strobe high	30		ns

PARAMETER MEASUREMENT INFORMATION

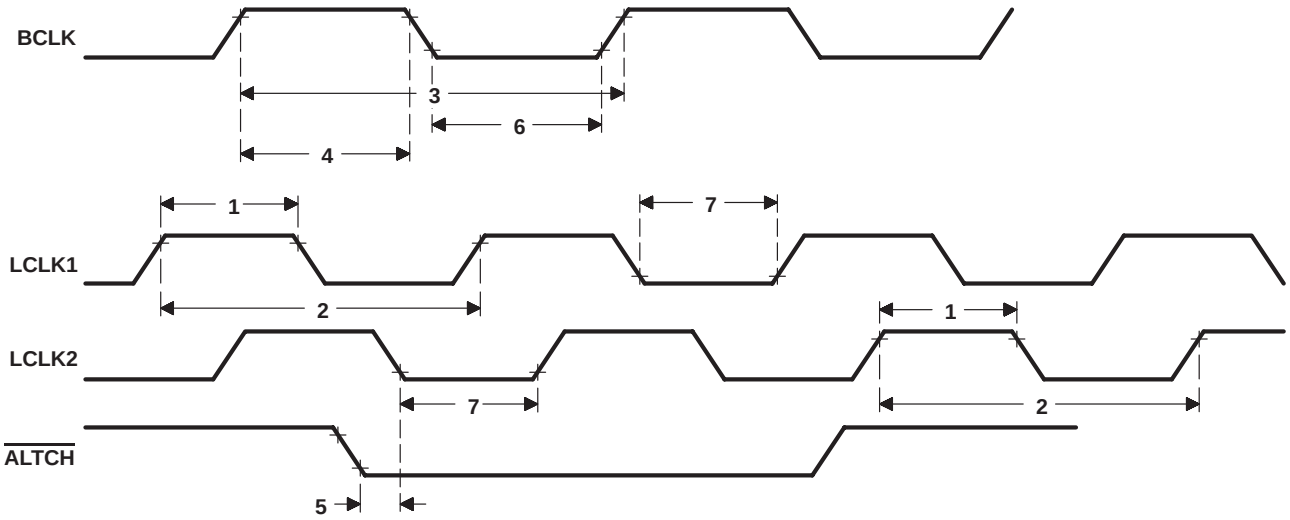
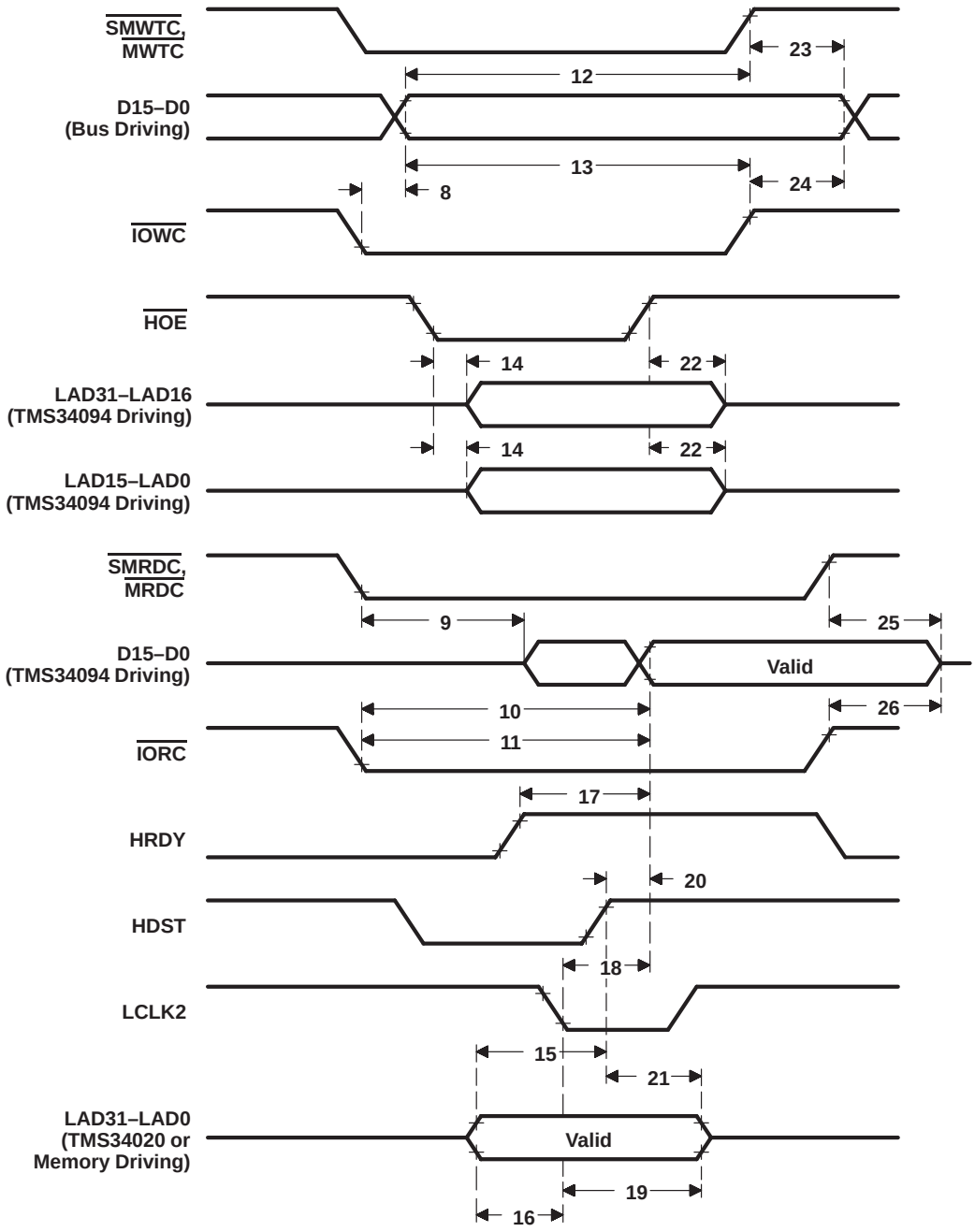


Figure 3. BCLK, LCLK1, and LCLK2

PARAMETER MEASUREMENT INFORMATION



NOTES: A. When operating as an 8-bit device, the TMS34094 will only drive D7–D0 during reads.
B. When operating as a 16-bit device, the TMS34094 will only drive D15–D0 when SBHE is active during reads.
C. When driving the LAD bus, the TMS34094 will always drive both halves of the bus.

Figure 4. D15–D0 and LAD31–LAD0 Data Timing

PARAMETER MEASUREMENT INFORMATION

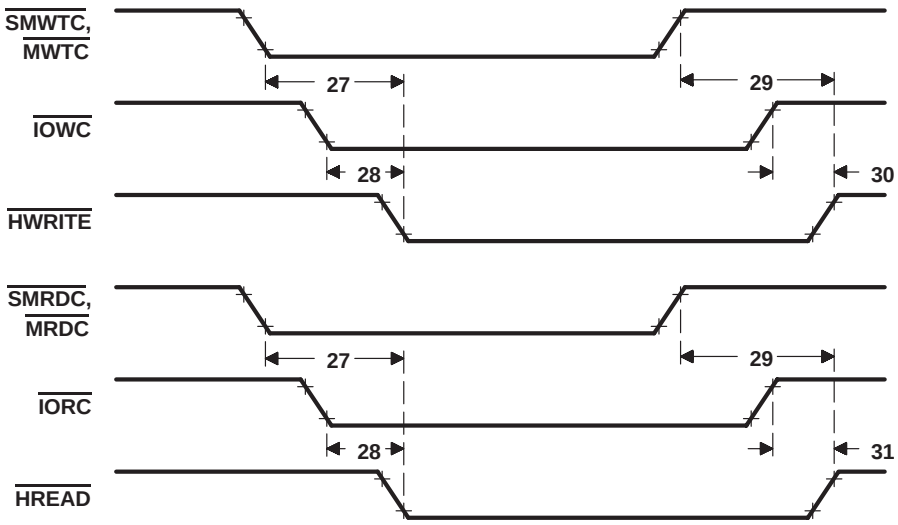
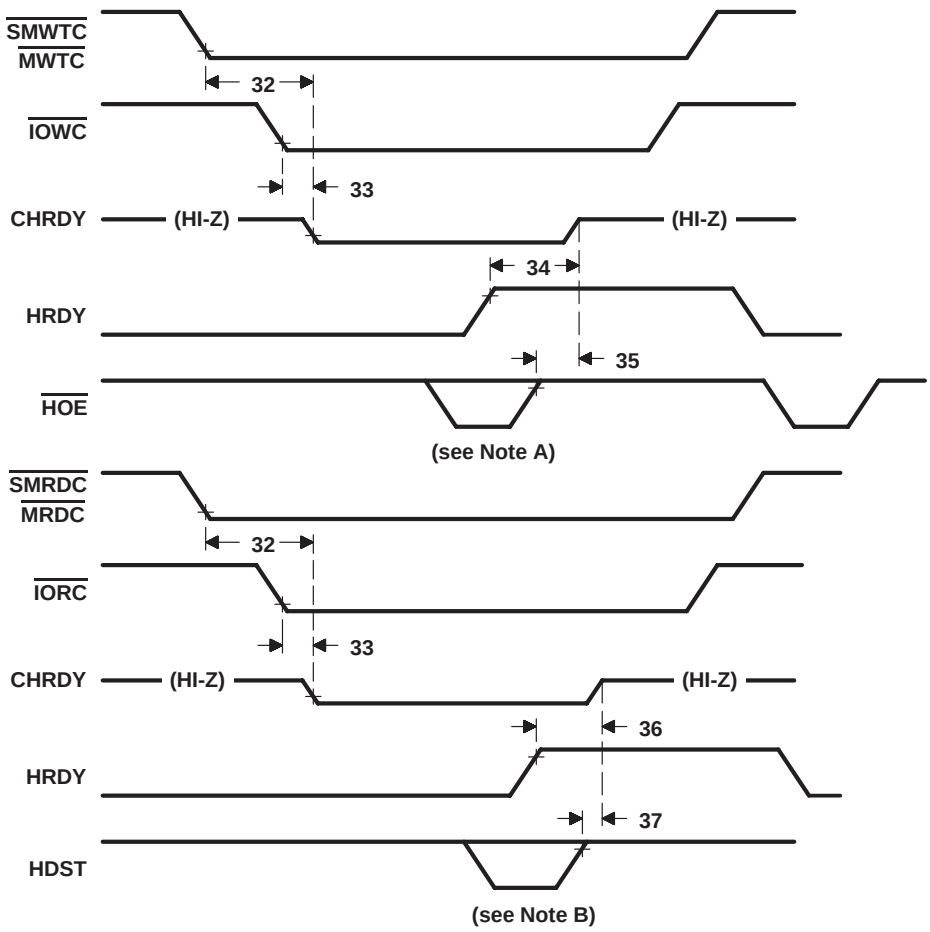


Figure 5. $\overline{\text{HWRITE}}$, $\overline{\text{HREAD}}$ Assertion

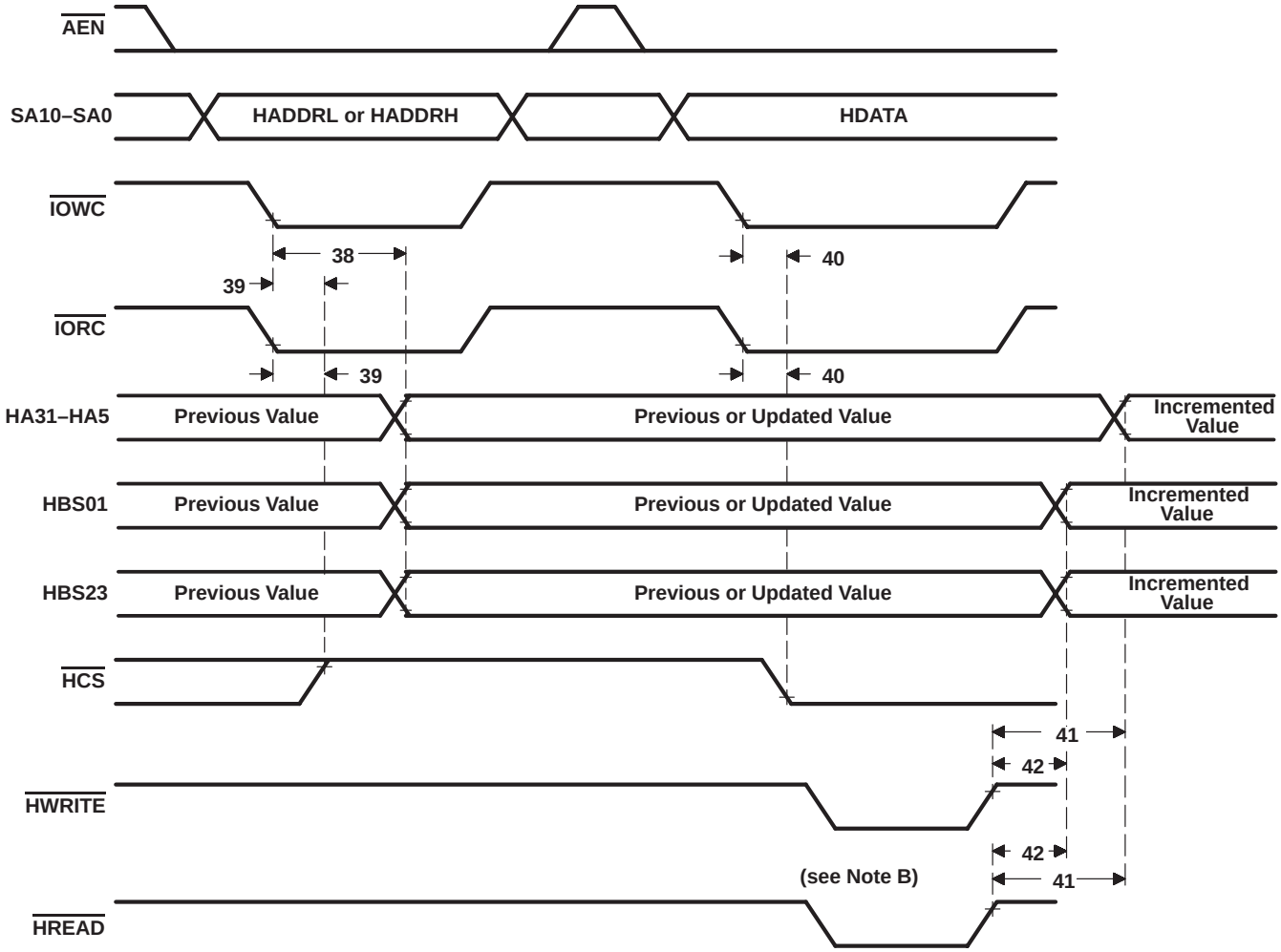
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Parameter 35 shows that CHRDY will not be floated until any previous host write to TMS34020 memory has completed.
B. When the requested read data is not currently in the TMS34094's data transceiver, the TMS34094 will not float CHRDY until the read data is latched into the TMS34094 by HDST rising.

Figure 6. CHRDY Assertion

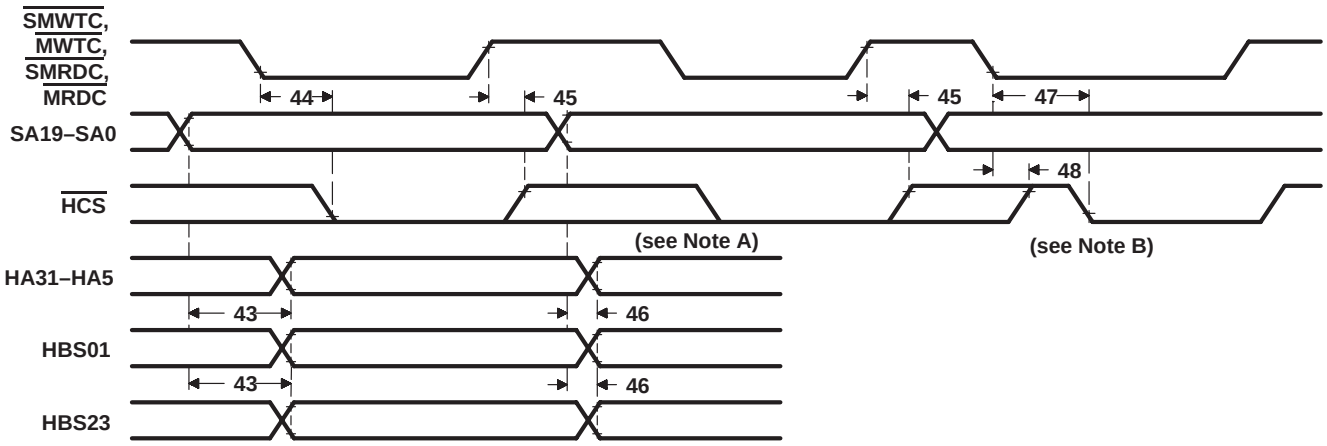
PARAMETER MEASUREMENT INFORMATION



NOTES: A. When in a 16-bit slot:
Writes to HADDRL only affect HA15–HA5, HBS01, and HBS23. Writes to HADDRH only affect HA31–HA16.
When in an 8-bit slot:
Writes to the low byte of HADDRL affect HBS01, HBS23, and HA5–HA7. Writes to the high byte of HADDRL affect HA8–HA15. Writes to the low byte of HADDRH affect HA16–HA23. Writes to the high byte of HADDRH affect HA24–HA31.
B. $\overline{\text{HWRITE}}$ and $\overline{\text{HREAD}}$ are shown active to show how $\overline{\text{HCS}}$ is asserted after HADDRL or HADDRH is written. $\overline{\text{HWRITE}}$ and $\overline{\text{HREAD}}$ will never be asserted at the same time.

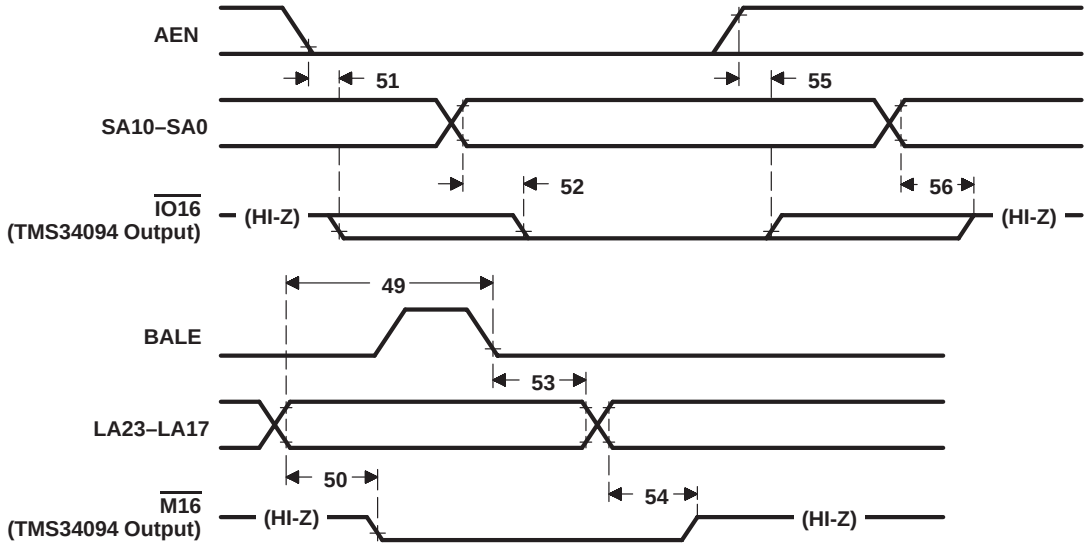
Figure 7. Access to HADDRL or HADDRH

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $\overline{\text{HCS}}$ is forced high at the end of memory-mapped accesses except:
When the access is a read and AI (MODECTL) = 1.
When the access is to MAP0 and MAP0E is enabled.
B. $\overline{\text{HCS}}$ is forced high at the beginning of a memory mapped access if it was previously low and the current access is to an address defined by a different BASEn register than the previous access.

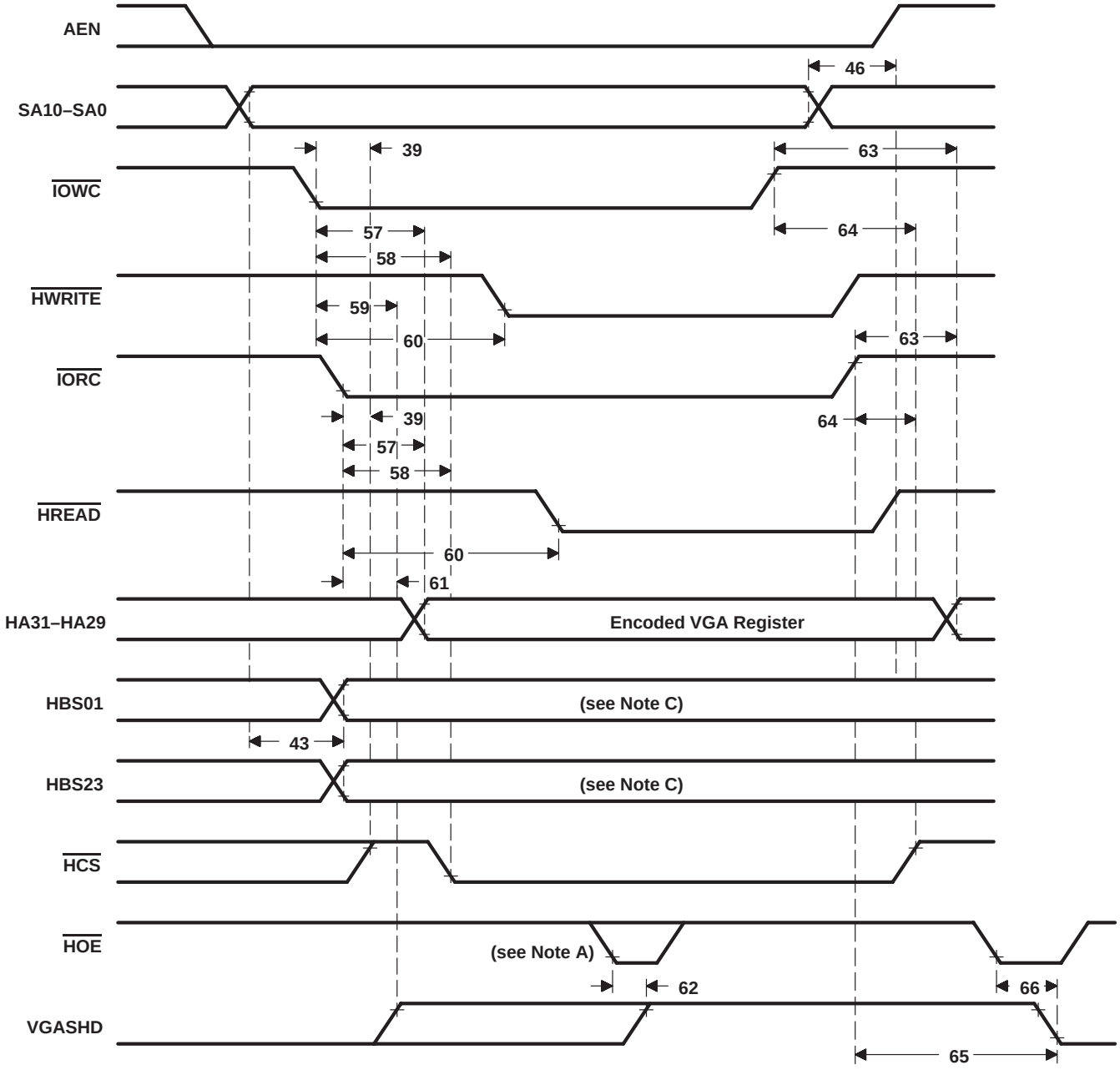
Figure 8. Host Address of Memory Mapped Access



NOTES: A. $\overline{\text{IO16}}$ is not pulled low for memory-mapped accesses or shadowed VGA LUT register accesses.
B. $\overline{\text{M16}}$ is not pulled low for I/O mapped accesses.

Figure 9. Assertion of $\overline{\text{IO16}}$ and $\overline{\text{M16}}$

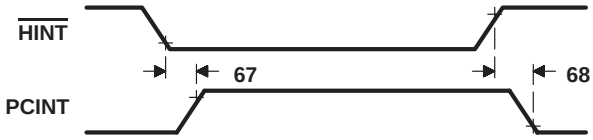
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Parameter 62 is applied whenever a previous host write has not yet been completed; in this case parameter 59 is ignored.
B. VGA LUT register accesses may be wait-stated by the TMS34020. CHRDY relationships shown in Figure 6 apply.
C. When IOE (MODECTL) is zero, then HBS23 follows SA1 and HBS01 follows the inverse of SA1, and parameters 44 and 47 apply. HBS01 and HBS23 will retain their previous states when IOE (MODECTL) is set to one, and parameters 44 and 47 do not apply.

Figure 10. Shadowed VGA Register Access

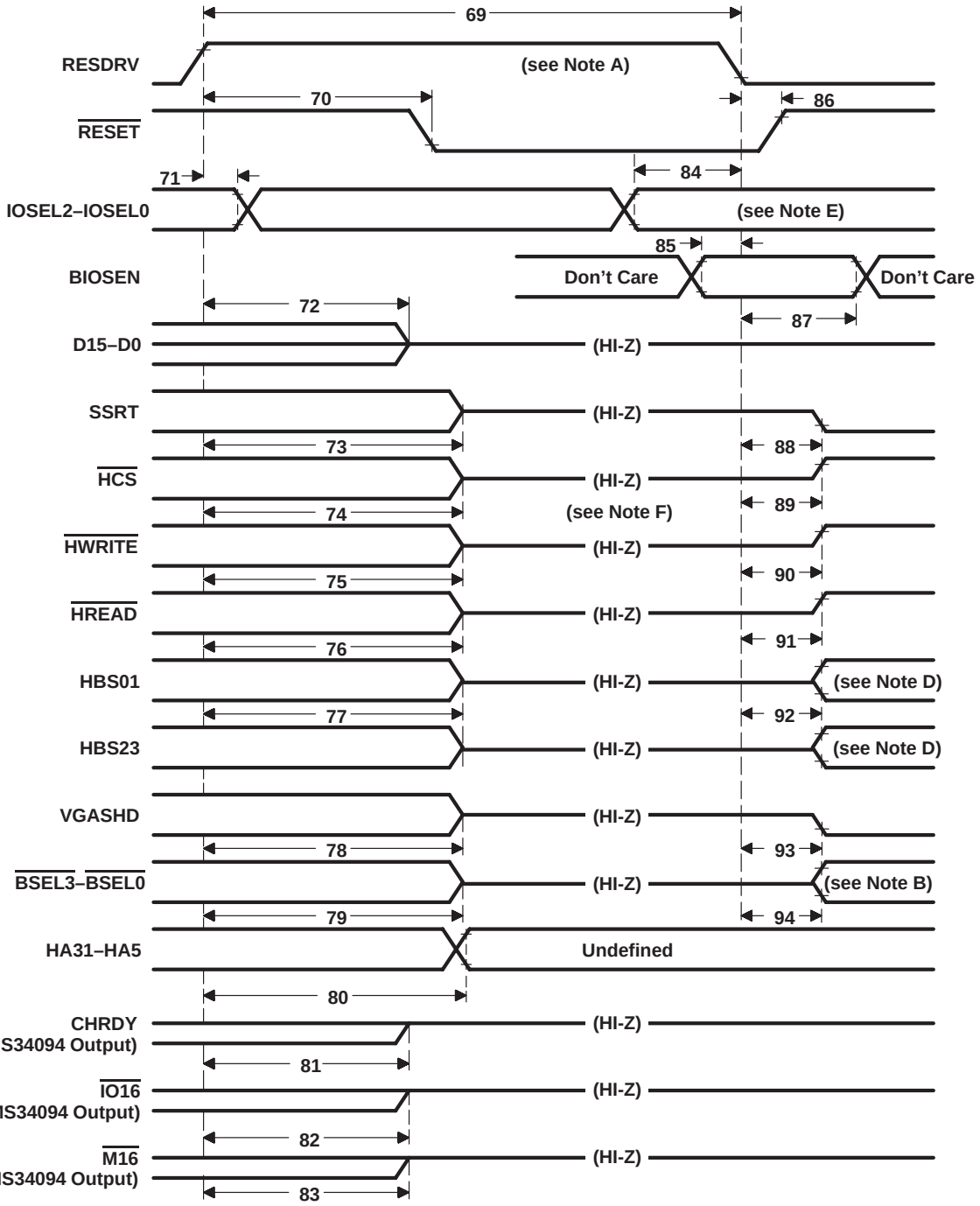
PARAMETER MEASUREMENT INFORMATION



NOTES: A. $\overline{\text{HINT}}$ is asserted when the GSP writes 1 to INTOUT (HSCTCLL) and is de-asserted when the GSP writes 0 to INTOUT (HSTCTLL).
B. The PCINT output of the TMS34094 is not intended to be used in level sensitive interrupt applications.

Figure 11. Assertion of $\overline{\text{PCINT}}$

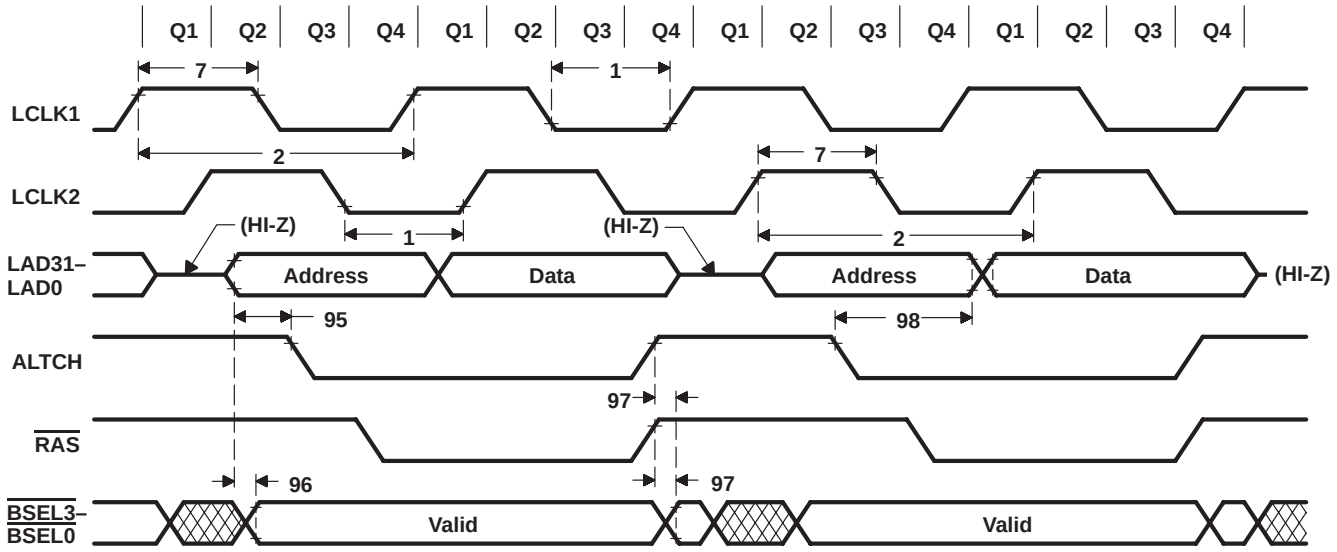
PARAMETER MEASUREMENT INFORMATION



NOTES: A. At power-up the TMS34020 requires a RESET pulse greater than 40 LCLK periods. The TMS34094 assumes that the input RESDRV signal will be active (high) long enough to satisfy this requirement.
B. BSEL2–BSEL0 will be disabled after RESET, except for DRAM refresh. BSEL3 will be held active after reset if BIOSEN is high, else it will be asserted only for DRAM refresh.
C. LAD31–LAD0 will be driven any time HOE is low. If HOE is low during RESET, the value on LAD31–LAD0 is undefined.
D. The state of HBS01 is not defined after reset. HBS23 will be driven to the opposite state.
E. IOSEL2–IOSEL0 must not change when RESDRV is not high.
F. A pull-up resistor is required on HCS to ensure that the TMS34020 will reset to Host Present mode.

Figure 12. Activity at Reset

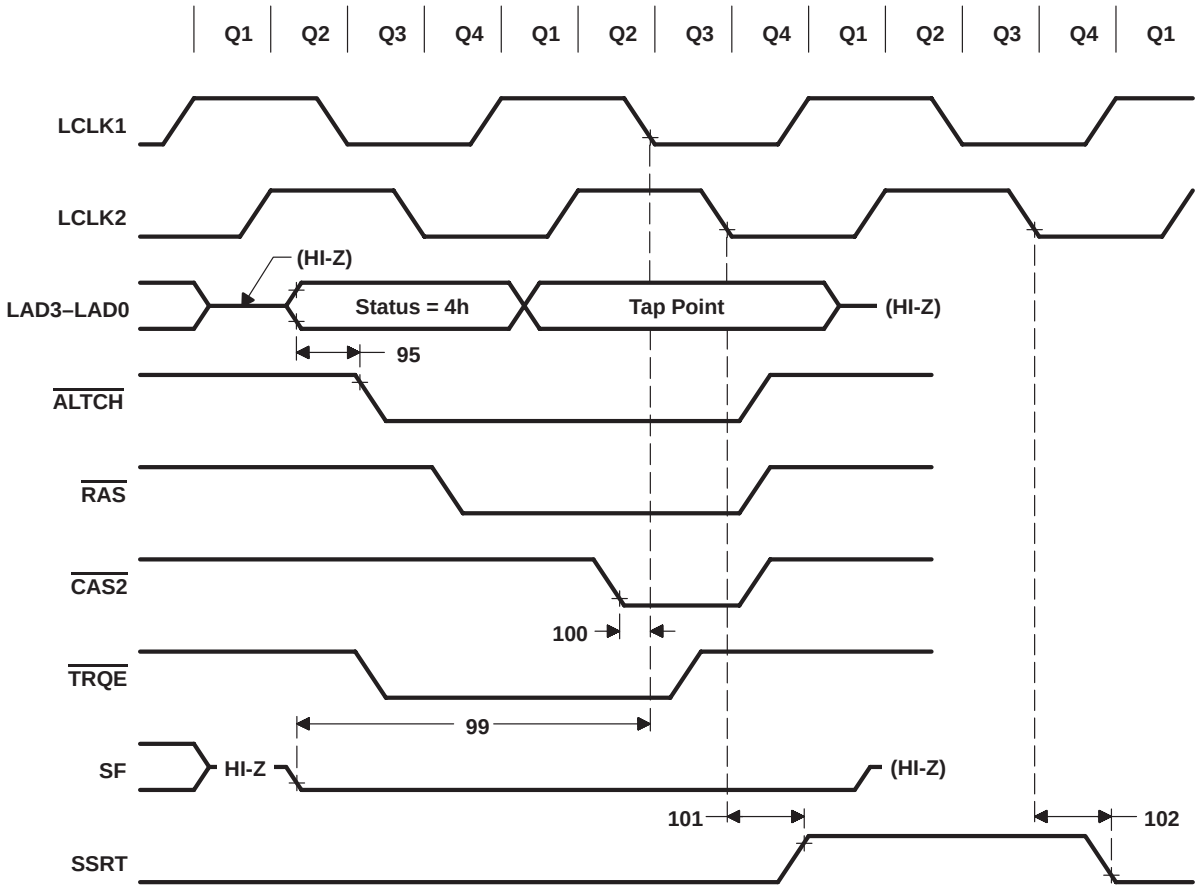
PARAMETER MEASUREMENT INFORMATION



NOTE A: Write accesses of BKADx and BKMSKx are asynchronous and may cause improper decoding of $\overline{\text{BSEL3}}$–$\overline{\text{BSEL0}}$. Do not modify these registers when the TMS34020 is executing code or at any time when $\overline{\text{BSEL3}}$–$\overline{\text{BSEL0}}$ should not decode improperly.

Figure 13. Assertion of $\overline{\text{BSEL3}}$–$\overline{\text{BSEL0}}$

PARAMETER MEASUREMENT INFORMATION



NOTE A: The SSRT output will not be asserted by a split shift register transfer.

Figure 14. Shift Register Transfer Decode

PARAMETER MEASUREMENT INFORMATION

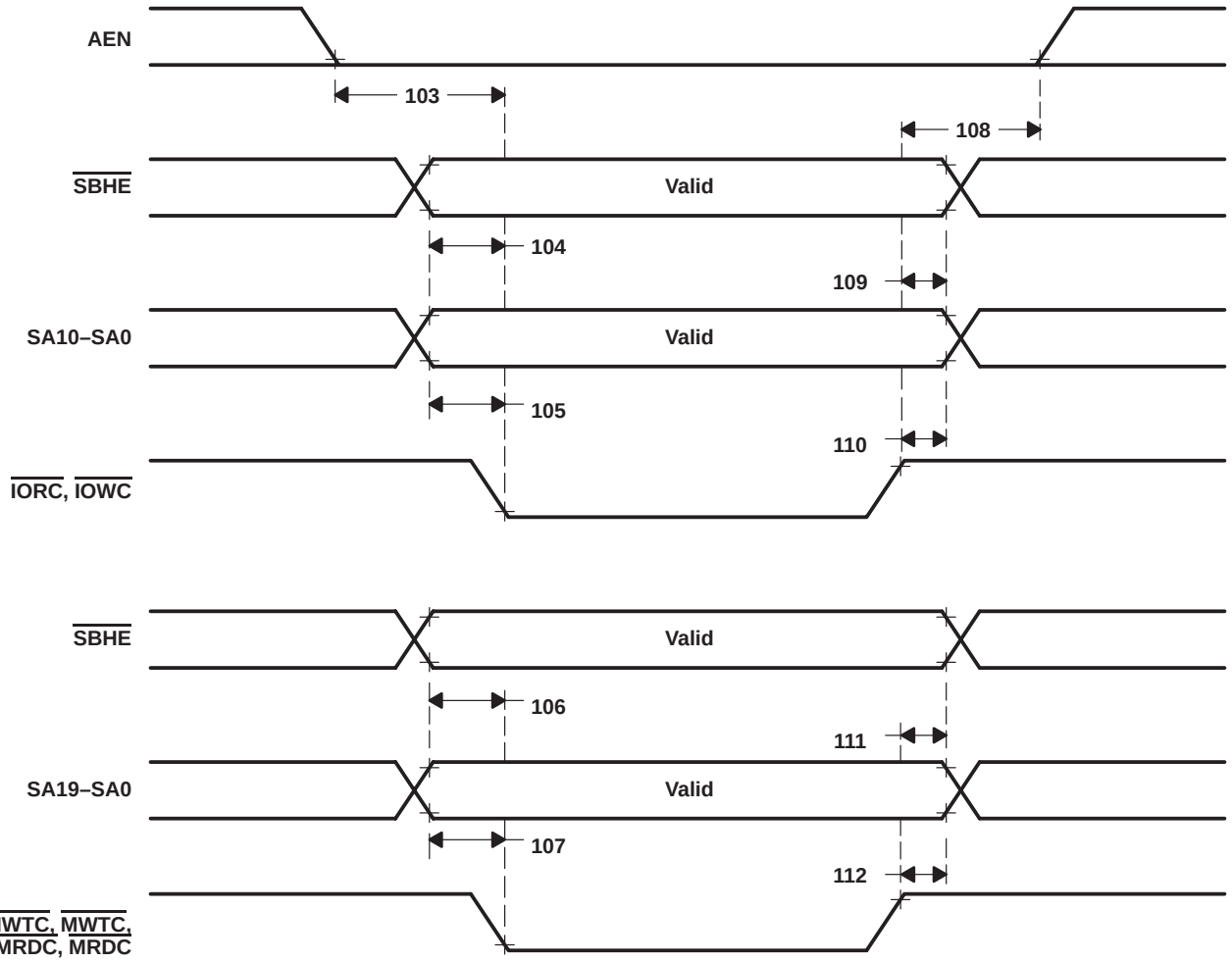
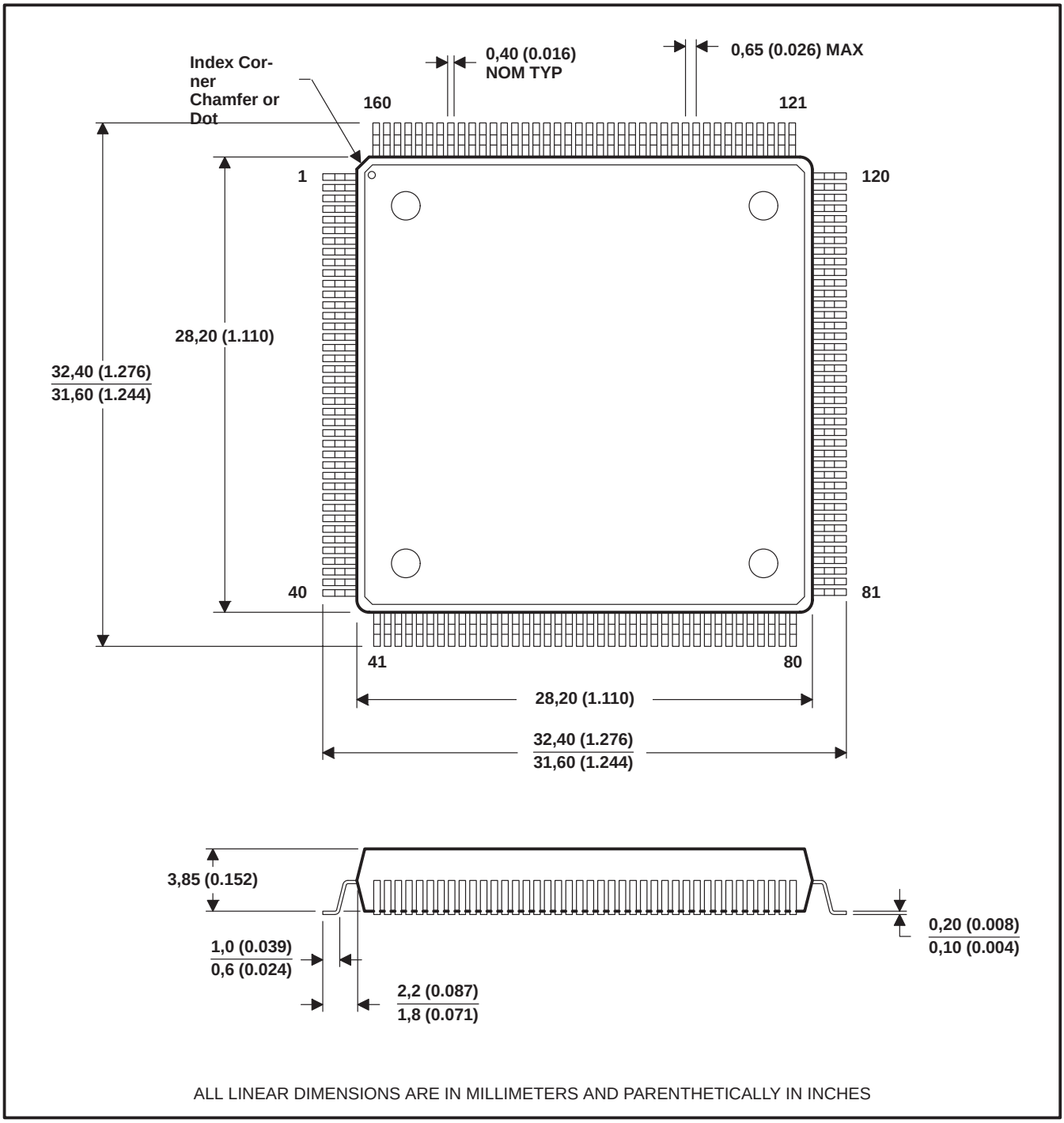


Figure 15. ISA Address Timing

MECHANICAL DATA

160-pin plastic quad-flat package (EIAJ)†



† All dimensions and notes for EIAJ QFP mechanical outline apply.

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