- **Integrated, Single-Chip, Ethernet™ Physical-Layer (PHY) Interface for Full-Duplex or Half-Duplex Connection to 10BASE-T, 100BASE-TX, and 100BASE-FX Networks**
- **Low-Power 3.3-V CMOS Design With Power-Down Capability for CardBus and Other Applications Requiring Low Power**
- **Integrated Transmit Filtering and Receive Equalization Provide for Minimal External Component Count to Reduce System Cost**
- **10BASE-T/100BASE-TX Connection Supported With Magnetics Package and RJ-45 Connector**
- **Electrostatic Discharge (ESD) Human Body Model (HBM) Protection 1.5 kV Per JEDEC JESD 22-A114-A**
- **Digital Signal Processor (DSP)-Based Digital Phase-Locked Loop (PLL) Technology Allows Data Recovery at 10 Mbit/s and 100 Mbit/s, Requiring One 20-MHz Clock Reference Source**
- **10BASE-T**
  - **Fully Compliant With IEEE Std 802.3**
  - **Smart Squelch for Improved Noise Immunity**
  - **Integrated Transmit Wave Shaping**
  - **Autopolarity (Reverse-Polarity Correction)**
  - **Transmit Jabber Detection**
- **100BASE-TX**
  - **Fully Compliant With ANSI Twisted-Pair Physical-Media-Dependent (TP-PMD) Standard and IEEE Std 802.3**
  - **Synthesized Rise-Time Control**
  - **Integrated Receiver With Adaptive Line Equalization (EQ) and Baseline Wander (BLW) Correction (DC Restoration)**
- **IEEE Std 802.3-Compliant Media-Independent Interface (MII) That Includes Management Interface**
- **IEEE Std 802.3-Compliant Autonegotiation (N-Way) With Next-Page Support**
- **IEEE Std 1149.1 (JTAG) Test Access Port (TAP)**
- **Packaged in 100-Terminal Plastic Quad Flatpack**

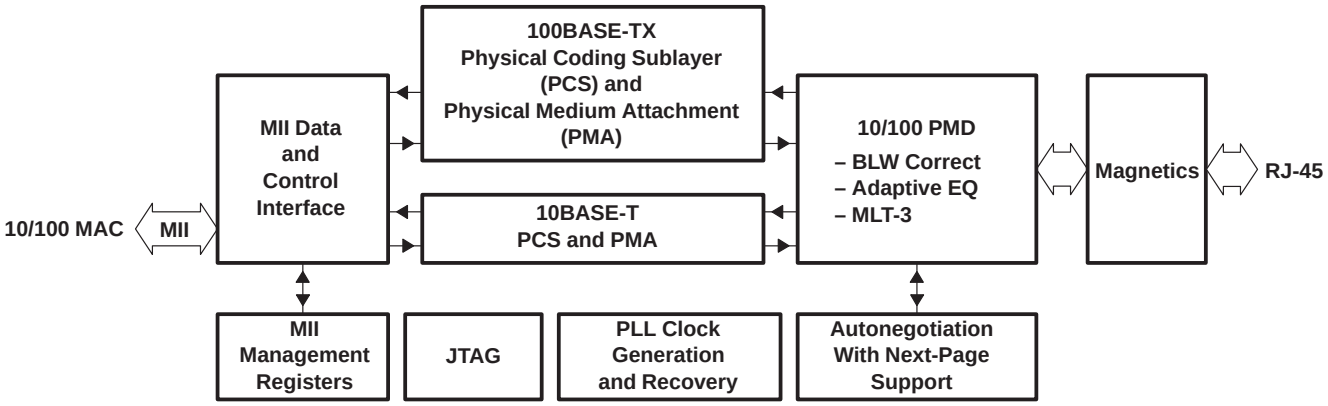

Figure 1. 10BASE-T/100BASE-TX PHY

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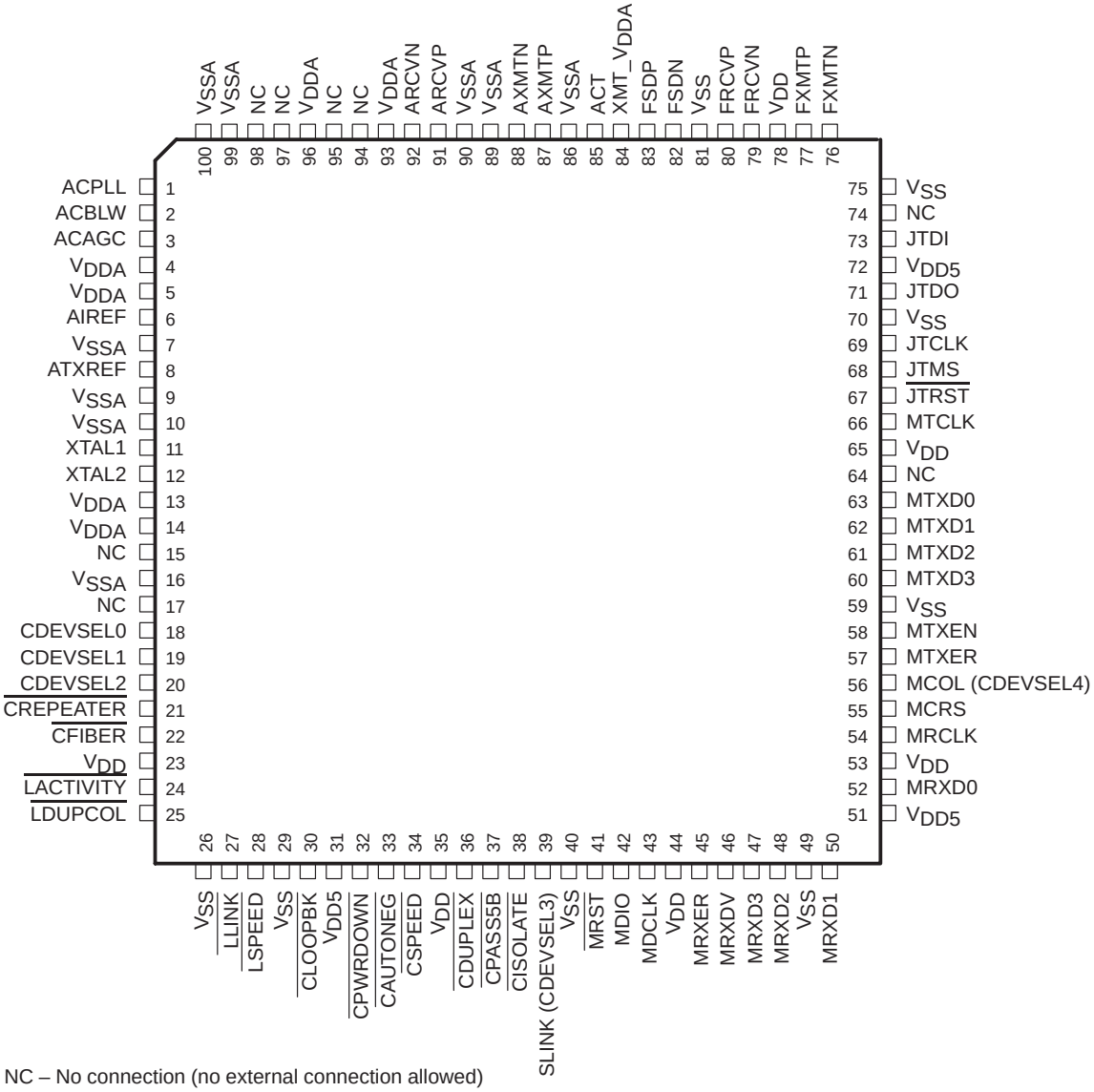
description

The TNETE2101 physical-layer (PHY) device from Texas Instruments (TI™) is a single-chip, high-performance solution for a range of 10BASE-T, 100BASE-TX, and 100BASE-FX networking systems (see Figure 1). The highly integrated TNETE2101 includes an on-board media-independent interface (MII) for simple connection to IEEE Std 802.3-compliant media-access controls (MACs). The device integrates all filtering and rise-time control functions for a cost-effective and space-saving PHY solution. Built-in autonegotiation allows automatic selection of half-/full-duplex 10BASE-T or 100BASE-TX, with an autopolarity-correction feature for immunity to receive-pair reversal.

PZ PACKAGE
(TOP VIEW)



NC – No connection (no external connection allowed)

Terminal Functions

analog function

TERMINAL NAME	TERMINAL NO.	TYPE†	I/O	DESCRIPTION
ACAGC	3	A	I	Automatic gain control (AGC) capacitor for the AGC loop
ACBLW	2	A	I	Baseline wander (BLW) capacitor for the BLW correction loop
ACPLL	1	A	I	PLL capacitor required for an internal PLL
AIREF	6	A	I	Analog current reference. An external resistor between AIREF and analog ground sets the bias current for internal analog circuits.
ATXREF	8	A	I	100BASE-TX transmit reference. An external resistor between ATXREF and analog ground sets the 100BASE-TX transmit amplitude.

† A = analog

configuration

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
$\overline{\text{CAUTONEG}}$	33	TTL	I	Autonegotiation enable. $\overline{\text{CAUTONEG}}$ enables (active high) or disables autonegotiation within the PHY. When $\overline{\text{CAUTONEG}}$ is low, the current values of $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ determine the speed and duplex of the PHY. On the rising edge of $\overline{\text{CAUTONEG}}$, the values of $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ set the advertised capabilities of the PHY for autonegotiate. This also occurs on power up or on the rising edge of $\overline{\text{MRST}}$ if $\overline{\text{CAUTONEG}}$ is high. When $\overline{\text{CAUTONEG}}$ is high, the autonegotiation process also can be controlled with the PHY register bit AUTOENB (register 0, bit 12). See *10BASE-T/100BASE-TX PHY operation* for details.
CDEVSEL2 CDEVSEL1 CDEVSEL0	20 19 18	TTL	I	MII device-select address. The values of CDEVSEL2–CDEVSEL0, SLINK (CDEVSEL3), and MCOL (CDEVSEL4) are latched into the MII on the rising edge of $\overline{\text{MRST}}$. This allows a unique address to be assigned to the PHY in applications in which multiple PHYs are in use.
$\overline{\text{CDUPLEX}}$	36	TTL	I/O	Duplex configuration. When $\overline{\text{CAUTONEG}}$ is low, $\overline{\text{CDUPLEX}}$ sets the PHY duplex to either half-duplex (low) or full-duplex (high). When $\overline{\text{CAUTONEG}}$ is high and autonegotiation is complete, $\overline{\text{CDUPLEX}}$ is driven low if half-duplex mode was selected, or set to the high-impedance state if full-duplex mode was selected. The PHY duplex also can be controlled and read at PHY register 0, bit 8, DUPLEX.
$\overline{\text{CFIBER}}$	22	TTL	I	100BASE-FX fiber-mode enable. In 100BASE-FX fiber mode, the fiber interface is enabled, and unshielded twisted pair (UTP) interface and autonegotiation are disabled. Selecting 10BASE-T mode with this mode enabled causes the PHY to power down. This function can be controlled by PHY register 0x11 bit 10, FIBER, if $\overline{\text{CFIBER}}$ is high.
$\overline{\text{CISOLATE}}$	38	TTL	I	MII-isolate enable. $\overline{\text{CISOLATE}}$ causes the PHY to raise all its MII outputs to a high-impedance state and ignore the MII inputs. In normal mode ($\overline{\text{CREPEATER}}$ is high), the PHY raises MTCLK, MRCLK, MRXD0–MRXD3, MRXDV, MRXER, MCRS, and MCOL to a high-impedance state and does not respond to MTXEN. In repeater mode, only MRCLK, MRXD0–MRXD3, MRXDV, and MRXER are raised to high impedance and, consequently, $\overline{\text{CISOLATE}}$ performs an active-high receive-enable function. This function can be controlled by PHY register 0, bit 10, ISOLATE, if $\overline{\text{CISOLATE}}$ is low.
$\overline{\text{CLOOPBK}}$	30	TTL	I	Loopback enable. When $\overline{\text{CLOOPBK}}$ is low, transmit is looped back to receive. This function can be controlled by PHY register 0, bit 14, LOOPBK, if $\overline{\text{CLOOPBK}}$ is high.
$\overline{\text{CPASS5B}}$	37	TTL	I	Pass-through mode enable. $\overline{\text{CPASS5B}}$ when set low, configures the PHY to bypass the internal 5B4B encoder and decoder. The 5B-encoded data is transmitted on MTXD0–MTXD3 and MTXER with the most significant data bit on MTXER. The 5B-encoded data is received on MRXD0–MRXD3 and MRXER, with the most significant bit on MRXER. This function can be controlled by PHY register 0x11, bit 8, NOENDEC, if $\overline{\text{CPASS5B}}$ is high.

Terminal Functions (Continued)

configuration (continued)

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
$\overline{\text{CPWRDOWN}}$	32	TTL	I	Power-down enable. When $\overline{\text{CPWRDOWN}}$ is low, the PHY is placed in a low power-consumption state. This function can be controlled by PHY register 0, bit 11, PDOWN, if $\overline{\text{CPWRDOWN}}$ is high.
$\overline{\text{CREPEATER}}$	21	TTL	I	Repeater-mode enable. When $\overline{\text{CREPEATER}}$ is low, the repeater mode is enabled and the PHY does not assert MCRS in response to transmit activity. This function can be controlled by PHY register 0x11, bit 5, REPEATER, if $\overline{\text{CREPEATER}}$ is high.
$\overline{\text{CSPEED}}$	34	TTL	I/O	Speed configuration. When $\overline{\text{CAUTONEG}}$ is low, $\overline{\text{CSPEED}}$ sets the PHY speed to either 10BASE-T (low) or 100BASE-TX (high). When $\overline{\text{CAUTONEG}}$ is high and autonegotiation is complete, $\overline{\text{CSPEED}}$ is driven low if 10BASE-T mode was selected, or set at high-impedance state if 100BASE-TX mode was selected. The PHY speed also can be controlled and read at PHY register 0, bit 13, SPEED.

fiber interface

TERMINAL NAME	TERMINAL NO.	TYPE†	I/O	DESCRIPTION
FRCVN FRCVP	79 80	PECL	I	100BASE-FX serial data input pair. Differential 3.3-V pseudo-emitter-coupled logic (PECL) 125-Mbit/s receive-data input for fiber mode.
FSDN FSDP	82 83	PECL	I	100BASE-FX serial data detect pair. Differential 3.3-V PECL 125-Mbit/s signal-detect input.
FXMTN FXMTP	76 77	PECL	O	100BASE-FX serial data output pair. Differential 3.3-V PECL 125-Mbit/s serialized transmit-data output for fiber mode.

† PECL = pseudo-emitter-coupled-logic

IEEE Std 1149.1 JTAG interface

TERMINAL NAME	TERMINAL NO.	TYPE‡	I/O	DESCRIPTION
JTCLK	69	5-V TTL	I	Test clock. JTCLK is used to clock state information and test data into and out of the device during operation of the test port.
JTDI	73	5-V TTL	I	Test data input. JTDI is used to serially shift test data and test instructions into the device during operation of the test port.
JTDO	71	5-V TTL	O	Test data output. JTDO is used to serially shift test data and test instructions out of the device during operation of the test port.
JTMS	68	5-V TTL	I	Test-mode select. JTMS is used to control the state of the test-port controller within the PHY.
$\overline{\text{JTRST}}$	67	5-V TTL	I	TAP reset. $\overline{\text{JTRST}}$ is used to reset the TAP controller (optional).

‡ 5-V TTL terminals are 5-V tolerant if V_{DD5} is connected to 5 V.

Terminal Functions (Continued)

LED status

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
$\overline{\text{LACTIVITY}}$	24	LED	O	Activity indicator. $\overline{\text{LACTIVITY}}$ lights an attached LED in response to receive and transmit activity within the PHY.
$\overline{\text{LDUPCOL}}$	25	LED	O	Duplex/collision indicator. $\overline{\text{LDUPCOL}}$ lights an attached LED in response to a network collision when the PHY is in half-duplex mode of operation. The LED is illuminated continuously when the PHY is in full-duplex mode.
$\overline{\text{LLINK}}$	27	LED	O	Link status indicator. $\overline{\text{LLINK}}$ lights an attached LED when the PHY has established a valid link with its partner. If autonegotiation is enabled, the driver flashes the LED during negotiation to indicate that it is attempting to establish a link. This is useful because a negotiation takes a minimum of 3 seconds (considerably longer if next-page information also is being exchanged), and the user may be tempted to remove the cable if the link light does not illuminate immediately. The user also is alerted to a network misconfiguration (where no common ability exists between the two link partners) by a continuously flashing LED.
$\overline{\text{LSPEED}}$	28	LED	O	Link speed indicator. $\overline{\text{LSPEED}}$ lights an attached LED when the PHY has established a valid 100BASE-TX link with its partner.

MII interface

TERMINAL NAME	TERMINAL NO.	TYPE†	I/O	DESCRIPTION
MCOL (CDEVSEL4)	56	5-V TTL	I/O	Collision detect. MCOL indicates that the PHY is receiving data while simultaneously transmitting. MCOL does not assert in full-duplex mode. The value of MCOL is latched on the rising edge of $\overline{\text{MRST}}$ for use as CDEVSEL4, bit 4, of the MII device-select address.
MDCLK	43	5-V TTL	I	Management data clock. MDCLK clocks serial management interface to the physical-media-dependent (PMD) chip.
MDIO	42	5-V TTL	I/O	Management data I/O. MDIO is serial management interface to the PMD chip. MDIO is synchronous to MDCLK.
MRCLK	54	5-V TTL	O	Receive clock. Receive clock source from the PHY. MRCLK is 2.5 MHz in 10BASE-T mode and 25 MHz in 100BASE-TX mode.
MCRS	55	5-V TTL	O	Carrier sense. MCRS asserts when the PHY initiates a frame reception.
$\overline{\text{MRST}}$	41	5-V TTL	I	MII reset. $\overline{\text{MRST}}$ is the reset signal to the PMD front end (active low).
MRXD3 MRXD2 MRXD1 MRXD0	47 48 50 52	5-V TTL	O	Receive data. MRXD3–MRXD0 are nibble receive data bits 3–0 from the PHY. Data is synchronous to MRCLK.
MRXDV	46	5-V TTL	O	Receive data valid. MRXDV indicates that data on MRXD0–MRXD3 is valid. MRXDV is synchronous to MRCLK.
MRXER	45	5-V TTL	O	Receive error. MRXER indicates reception of a coding error on received data. MRXER is synchronous to MRCLK.
MTCLK	66	5-V TTL	O	Transmit clock. MTCLK is the transmit clock source from the PHY. This clock is 2.5 MHz in 10BASE-T mode and 25 MHz in 100BASE-TX mode.
MTXD3 MTXD2 MTXD1 MTXD0	60 61 62 63	5-V TTL	I	Transmit data. MTXD3–MTXD0 are nibble transmit data bits 3–0 from the MAC. Data is synchronous to MTCLK.

† 5-V TTL terminals are 5-V tolerant if V_{DD5} is connected to 5 V.

Terminal Functions (Continued)

MII interface (continued)

TERMINAL NAME	TERMINAL NO.	TYPE†	I/O	DESCRIPTION
MTXEN	58	5-V TTL	I	Transmit enable. MTXEN indicates valid transmit data on MTXD0–MTXD3**.** MTXEN is synchronous to MTCLK.
MTXER	57	5-V TTL	I	Transmit error. MTXER allows coding errors to be propagated across the MII. MTXER is synchronous to MTCLK.

† 5-V TTL terminals are 5-V tolerant if V_{DD5} is connected to 5 V.

miscellaneous

TERMINAL NAME	TERMINAL NO.	TYPE‡	I/O	DESCRIPTION
SLINK (CDEVSEL3)	39	TTL	I/O	Link status. When asserted high, SLINK indicates that a good link has been established with the link partner. When autonegotiation is enabled, SLINK also indicates that the CSPEED and CDUPLEX terminals are being driven with the negotiated speed and duplex configuration. The value of SLINK is latched on the rising edge of MRST for use as CDEVSEL3, bit 3, of the MII device-select address.
XTAL1	11	A	I	Clock input. XTAL1 is the main 20-MHz reference clock input for the TNETE2101. A 20-MHz clock oscillator can be connected to XTAL1, or a crystal with a capacitor network can be connected across XTAL1 and XTAL2.
XTAL2	12	A	O	Output for external crystal circuit. See XTAL1.

‡ A = analog

network interface

TERMINAL NAME	TERMINAL NO.	TYPE‡	I/O	DESCRIPTION
ACT	85	A	O	Center tap. ACT is the connection to the primary center tap of the transmit transformer.
ARCVP ARCVN	91 92	A	I	Receive pair. ARCVP and ARCVN are the differential line inputs to the device from the transformer and termination components.
AXMTP AXMTN	87 88	A	O	Transmit pair. AXMTN and AXMTP are the differential line outputs from the device to the transformer and termination components.

‡ A = analog

no connection

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
NC	15, 17, 64, 74, 94, 95, 97, 98	No connection (no external connection allowed).

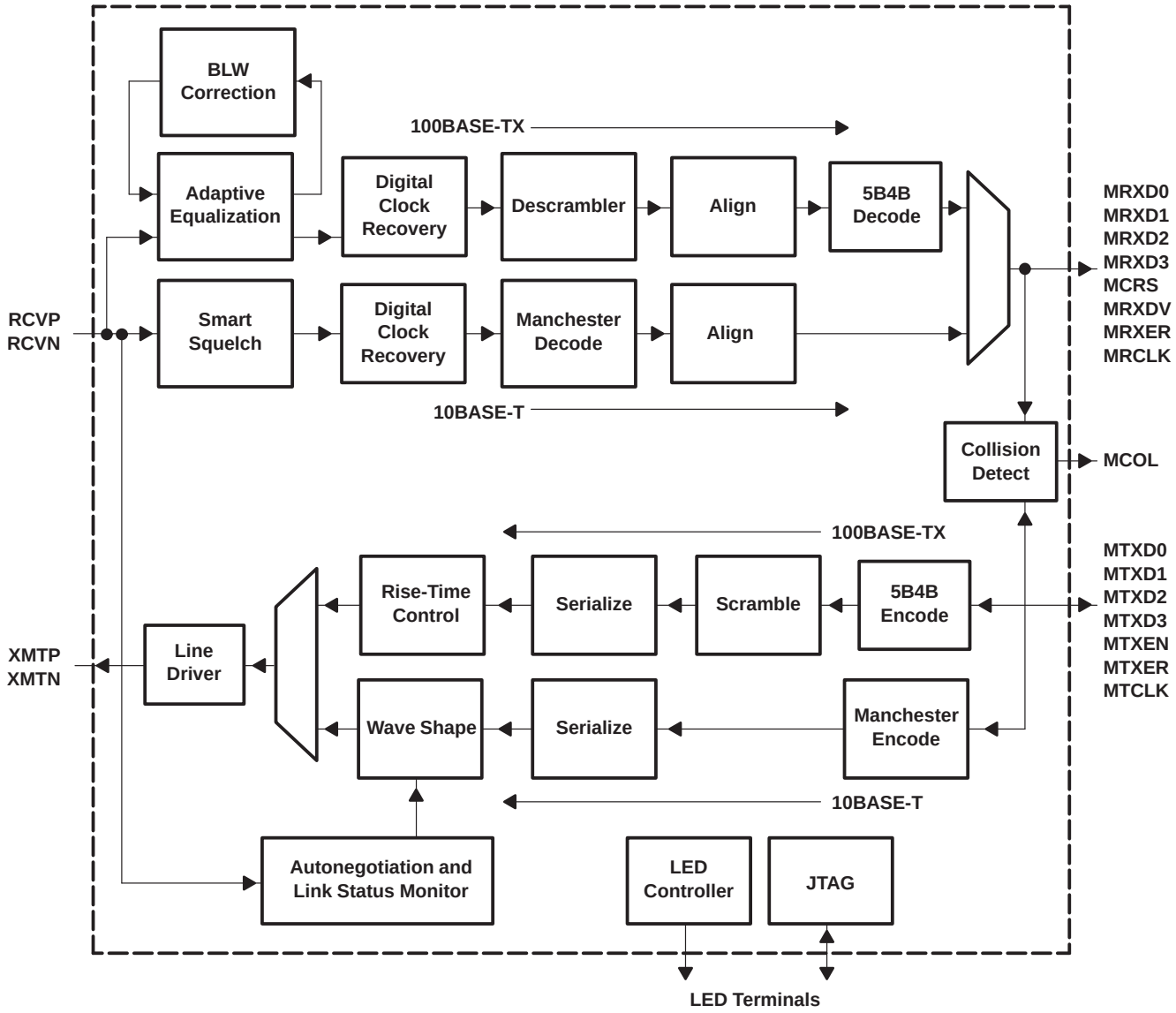
Terminal Functions (Continued)

power

TERMINAL NAME	TERMINAL NO.	POWER DOMAIN†	DESCRIPTION
V_{DDA}	5, 13, 14, 96	V_{DDA}	Power. Analog 3.3-V supply connection.
XMT_V_{DDA}	84	XMT_AV_{DD}	Power. Analog 3.3-V supply connection for transmit.
V_{DDA}	4, 93	V_{DDA}	Power. Analog 3.3-V supply connection for receive.
V_{DD5}	31, 51, 72	V_{DD} or V_{DD5}	Power. Power for digital I/O that connects to 3.3 V for 3.3-V I/O operations and to 5 V for 5-V I/O operations. Used for I/O on MII and JTAG interface.
V_{DD}	23, 35, 44, 53, 65, 78	V_{DDD}	Power. Digital 3.3-V supply connection for core logic and I/O.
V_{SSA}	7, 9, 10, 16, 86, 89, 90, 99, 100	GND	Ground. Analog ground connection.
V_{SS}	26, 29, 40, 49, 59, 70, 75, 81	GND	Ground. Digital ground connection.

† Denotes suggested power-plane connection for layout

functional block diagram for UTP interface



functional description

10BASE-T/100BASE-TX differential line transmitter function

The TNETE2101 differential line drivers are designed to drive at least 100 m of CAT5 cable in 100BASE-TX mode and in excess of 100 m of CAT3 (or CAT5) cable in 10BASE-T mode. Three transmitter-output terminals (including a center-tap connection) interface to a single transformer for both operating modes. This simplifies the external connection to a single RJ-45 socket connected directly to the transformer secondary winding (see Figure 2).

The TNETE2101 incorporates on-chip wave shaping for 10BASE-T transmission and rise-time control for 100BASE-TX transmission, which enables the device to interface directly to the magnetics without using external components, other than two termination resistors. The functional block diagram illustrates the TNETE2101 transmitter function for a single 10BASE-T/100BASE-TX PHY channel.

10BASE-T/100BASE-TX differential line receiver function

The two receiver-input terminals of the TNETE2101 must be connected to the physical-media interface (PMI) through an external isolation transformer. The receiver circuitry establishes its own common-mode input bias voltage, therefore, no external resistor divider-biasing network is required. A simple termination network consisting of two resistors and one capacitor is recommended (see Figure 2). Data received from the network is output on the MRXD data nibble of the MII and synchronized to the rising edge of the corresponding MRCLK signal. The MRCLK frequency automatically adjusts to 2.5 MHz in 10BASE-T mode or 25 MHz in 100BASE-TX mode.

A single receiver-input pair supports both speed modes, with all multiplexing functions performed internally to the device.

The 10BASE-T receiver smart-squelch function allows incoming data to pass only if the input amplitude is greater than a minimum signal threshold and a specific pulse sequence is received. This prevents input data being affected by impulse line noise that is mistaken for signal or link activity. The squelch circuits quickly deactivate if received pulses exceed the specifications; therefore, long pulses are not mistaken as link pulses.

The 100BASE-TX receiver decodes the MLT-3 waveform and provides a data nibble on MRXD0–MRXD3. After MLT-3 signal is received, the signal is immediately amplified and equalized. This allows reception over a minimum of 100 m of CAT5 cable. The low-frequency component of the MLT-3 signal, often referred to as BLW, is removed. BLW can be a consequence of long periods without data transitions in transformer-coupled circuits. The ideal MLT-3 then is internally converted to non-return-to-zero information (NRZI), then resynchronized to its own recovered clock using a digital phase-locked-loop (PLL) technique. The reclocked data then is deserialized into 5-bit code groups, descrambled, and 5B4B decoded. When a start-of-stream delimiter is detected in the 5B data stream, the next frame is output on the MII. The functional block diagram illustrates the TNETE2101 receiver function for a single 10BASE-T/100BASE-TX PHY channel.

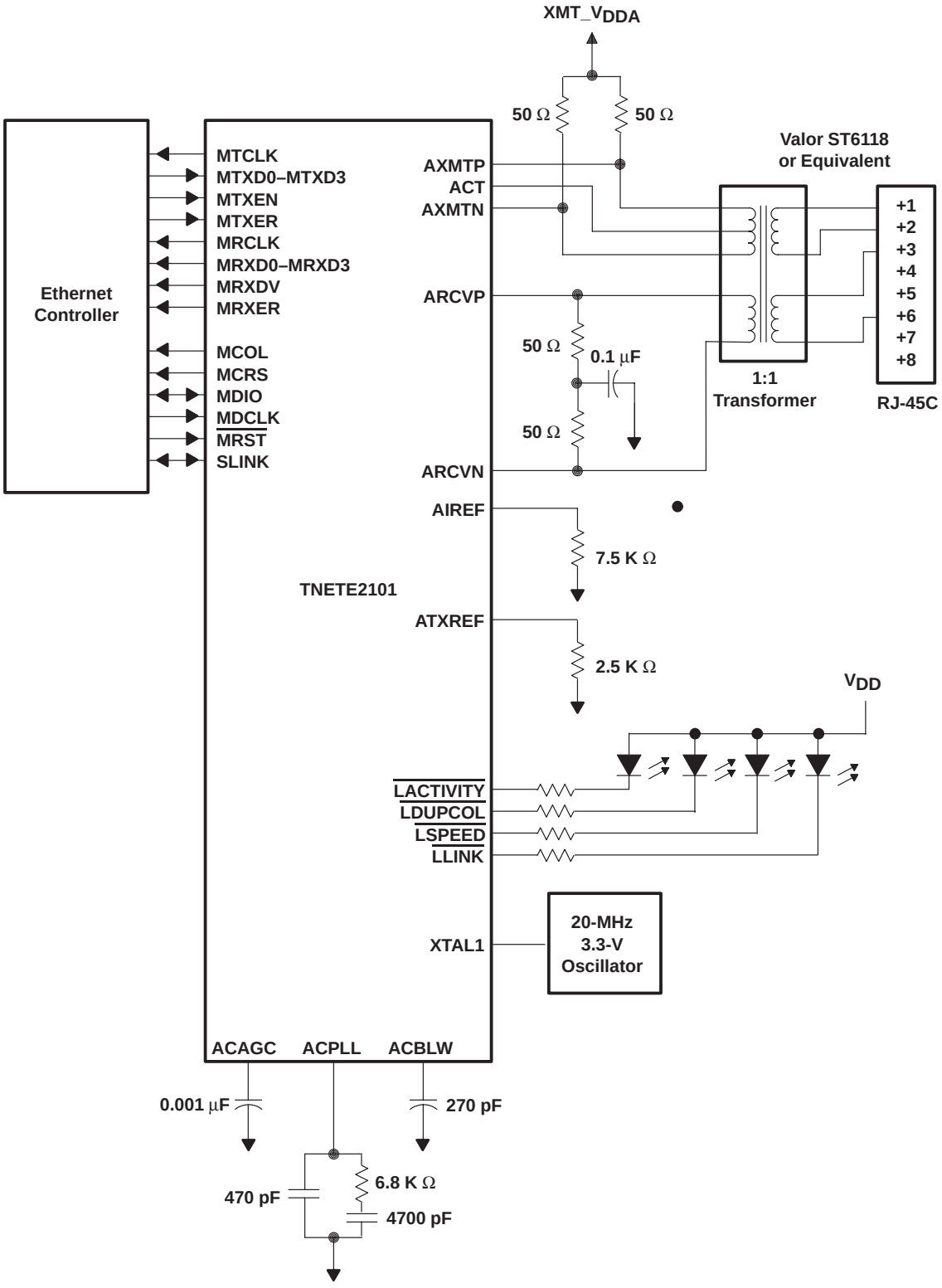


Figure 2. External Components for the TNETE2101

link-integrity test and reverse-polarity and correction

When autonegotiation is disabled and the TNETE2101 is configured for 10BASE-T only, the transmitter sends a normal link pulse through the data-out (DO) circuit every 16 ms.

The receiver looks for valid link pulses on the input pair. If a link pulse is not received within a given time interval, the device enters a link-fail state. In this state, link pulses continue to be generated, and the receiver continuously looks for the link pulse pattern. The device remains in this state until a valid receive packet or multiple legal-link test pulses are received.

Link pulses of the opposite polarity (received and qualified in the same manner as normal link pulses) are an indication that the receive-pair connections are reversed and that an automatic internal reconfiguration has occurred to correct this problem. Reverse-polarity correction is not required in 100BASE-TX mode, where the data is MLT-3-encoded.

autonegotiation

The TNETE2101 fully supports IEEE Std 802.3 autonegotiation, including next-page transfer. When enabled, this feature allows the TNETE2101 to negotiate with any other autonegotiation-capable PHYs on its link segment to establish their highest common protocol. Until a PHY has completed its negotiation, it cannot assert LINK.

More information on the link partner abilities can be obtained by reading the TNETE2101 registers.

loopback test mode

By asserting the $\overline{\text{CLOOPBK}}$ terminal on the device or by setting the LOOPBK bit in the GEN_ctl register, the transmit circuit of the PHY is looped back to the corresponding receive circuit located closest to the twisted-pair I/O terminals.

In 10BASE-T mode and loopback mode, all receive activities (other than link test pulses) are ignored. However, squelch information is still processed, allowing the link status to be maintained under momentary loopback self-test.

LED status indication

The TNETE2101 has four terminals that drive LEDs, indicating activity, duplex/collision, link, and speed. The circuitry contains an open-drain N-channel MOS (NMOS) device for the LED driver, and the LEDs should be connected to digital 3.3 V through a current-limiting resistor. The value of the resistor depends on the LED type.

In 10BASE-T mode, the link LED illuminates when the PHY has established a valid link. In 100BASE-TX mode, the link LED indicates that the descrambler has locked onto the data and the TNETE2101 is in a state to transmit and receive data. The link LED flashes during the autonegotiation process to indicate link activity to the user, since autonegotiation can take several seconds. During loopback test, the LED is not illuminated.

The activity LED illuminates when the PHY is transmitting or receiving data; it remains illuminated for a minimum of 20 ms for each activity. Its operation is the same in both speed modes. The activity LED illuminates on any attempt to transmit data, including those made in loopback mode and in link-fail state.

The duplex/collision LED illuminates continuously when the PHY is in full-duplex mode and for a minimum of 20 ms when collisions occur in half-duplex mode. If continuous or frequent collisions occur, it flashes at 10 Hz.

test access port (TAP)

To be compliant with IEEE Std 1149.1 and for boundary-scan testing, the TAP includes five terminals that are used to interface serially with the device and the board on which it is installed.

100BASE-FX differential PECL interface

The PHY provides three pairs of differential PECL terminals for connection to external fiber-optic transceivers. The data streams are 125-Mbit/s NRZI encoded, with the receive data stream routed to the digital PLL for data recovery. To maintain a reliable lock on the digital PLL, the receive data stream must be jitter free.

The FSDP/FSDN serial data-detect pair must be differentially positive to enable data recovery. While this pair is differentially negative, MRCLK is inactive, and no attempt is made to process any receive data appearing on FRCVP/FRCVN.

Differential PECL signals should be terminated with a standard emitter-coupled logic (ECL) load of 50 Ω to a voltage source of V_{DD} – 2 V (that is, 1.3 V) or to an equivalent circuit.

reset and power up timing

At initial power up, the PHY performs an internal reset. No external reset circuitry is required; however, operation of the TNETE2101 is not specified for 50 ms after power up (V_{DD} stable).

During operation, a full reset of the device can be performed by taking $\overline{\text{MRST}}$ low for not less than 50 μs. Correct operation of the device is not certain until 50 ms after $\overline{\text{MRST}}$ is deasserted high.

10BASE-T/100BASE-TX PHY operation

PHY link establishment

The PHY implements the full autonegotiation standard, including next-page capability. $\overline{\text{CAUTONEG}}$, $\overline{\text{CSPEED}}$, and $\overline{\text{CDUPLEX}}$ are used to directly configure the link speed or to set and report autonegotiated speeds.

When $\overline{\text{CAUTONEG}}$ is deasserted low, $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ determine the link configuration. $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ have weak pullups, giving a default configuration of full-duplex 100BASE-TX when not connected.

The rising edge of $\overline{\text{CAUTONEG}}$ latches the values of $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ into the autonegotiation advertisement (AN_adv) register as shown in Table 1. This advertises to the link partner during negotiation of the capabilities of PHY and the highest common link is determined. $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ then are driven with the negotiated speed and duplex.

Table 1. External-Link Configuration Speeds

$\overline{\text{CSPEED}}$	$\overline{\text{CDUPLEX}}$	AN_adv	ADVERTISED TECHNOLOGIES
0	0	0x0021	Half-duplex 10BASE-T
0	1	0x0061	Half-/full-duplex 10BASE-T
1	0	0x00A1	Half-duplex 10BASE-T Half-duplex 100BASE-TX
1	1	0x00E1	Half-/full-duplex 10BASE-T Half-/full-duplex 100BASE-TX

For external controlling and reading of $\overline{\text{CAUTONEG}}$, $\overline{\text{CSPEED}}$, and $\overline{\text{CDUPLEX}}$, timing to be considered is shown in Figure 3. $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ must not be driven externally for 1200 ms (maximum) after $\overline{\text{CAUTONEG}}$ is asserted high. The PHY begins negotiation when $\overline{\text{CAUTONEG}}$ is asserted. In the final 750 ms (minimum) of autonegotiation, the PHY drives $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$ to indicate the link configuration. The values of these two terminals can be latched on the rising edge of SLINK.

PHY link establishment (continued)

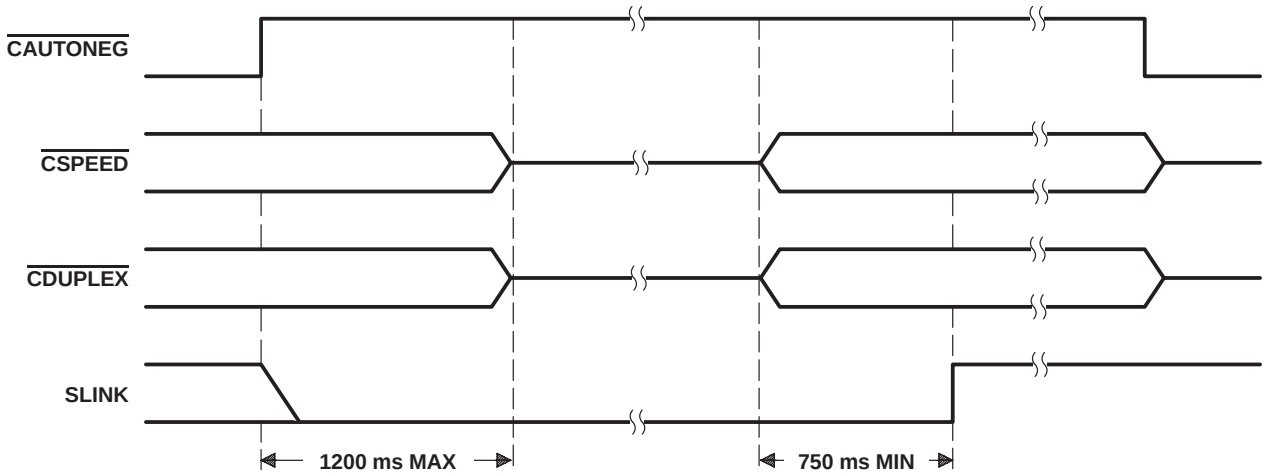


Figure 3. External Autonegotiation Configuration and Status

Autonegotiation, duplex, and speed also can be controlled through the PHY register 0, GEN_ctl. These bits, AUTOENB (bit 12), SPEED (bit 13), and DUPLEX (bit 8), are similar to and work with $\overline{\text{CAUTONEG}}$, $\overline{\text{CSPEED}}$, and $\overline{\text{CDUPLEX}}$, respectively. These bits can be written and read.

When $\overline{\text{CAUTONEG}}$ is low, the AUTOENB bit remains set to a 0 and cannot be set to a 1; therefore, autonegotiation cannot be enabled. In this case, the values read from SPEED and DUPLEX reflect the values driven on the terminals $\overline{\text{CSPEED}}$ and $\overline{\text{CDUPLEX}}$, respectively.

When $\overline{\text{CAUTONEG}}$ is high, AUTOENB can be set to a 1 (enabled) or a 0 (disabled). When AUTOENB is enabled, autonegotiation is started and the SPEED and DUPLEX bits are updated to reflect the negotiated values. When AUTOENB is disabled, autonegotiation is disabled and speed and duplex are forced to the values written in the SPEED and DUPLEX bits.

PHY configuration

The TNETE2101 can be configured externally through the terminals or internally through the PHY registers much like the autonegotiation terminals and register bits. Each external terminal has an equivalent PHY register bit. Table 2 correlates the terminal with the register bit.

Table 2. External Configuration Terminal/Register Bit Correlation

TERMINAL	PIN NO.	BIT	REGISTER	BIT NO.	FUNCTION
$\overline{\text{CISOLATE}}$	38	ISOLATE	0x0	10	Sets MII interface to high-impedance state
$\overline{\text{CPWRDOWN}}$	32	PDOWN	0x0	11	Places PHY in power-down state
$\overline{\text{CLOOPBK}}$	30	LOOPBK	0x0	14	Enables loopback
$\overline{\text{CREPEATER}}$	21	REPEATER	0x11	5	Enables repeater mode
$\overline{\text{CPASS5B}}$	37	NOENDEC	0x11	8	Disables 5B4B encoder/decoder
$\overline{\text{CFIBER}}$	22	FIBER	0x11	10	Enables fiber interface

All of the terminals are active low and the register bits are active when set to a 1. All the register bits can be written and read. The value read from the register bit reflects the internal configuration setting of the PHY and is derived from the external terminal setting and the internal register bit value.

PHY configuration (continued)

Table 3 shows the external configuration terminal, register value, and the result, except for the isolate function.

Table 3. Terminal and Register Values

TERMINAL VALUE (LOW = ACTIVE)	REGISTER VALUE WRITTEN	REGISTER VALUE READ	RESULT
Low	X	1	Enabled
High	0	0	Disabled
High	1	1	Enabled

Table 4 shows the operation for the isolate function and the resulting control of the isolate function.

Table 4. Isolate-Function Operation

TERMINAL VALUE (LOW = ACTIVE)	REGISTER VALUE WRITTEN	REGISTER VALUE READ	RESULT
Low	0	0	Disabled
Low	1	1	Enabled
High	X	0	Disabled

The terminal can be set to a value that disables control of the function through the internal PHY registers.

10BASE-T/100BASE-TX PHY registers

The IEEE Std 802.3 MII serial protocol allows for up to 32 different PMD devices, with up to 32 (16-bit-wide) internal registers in each device. The 10BASE-T/100BASE-TX PHY implements 11 internal registers, three of which are hardwired. Figure 4 shows the device register map. Most of the registers are the generic registers mandated by the MII specification. The three registers (TXPHY_X) in Figure 4 are TI-specific registers. All other registers are read as 0s.

REGISTER	ADDRESS	DESCRIPTION
GEN_ctl	0x00h	Generic control (see Figure 7 and Table 6)
GEN_sts	0x01h	Generic status (see Figure 8 and Table 7)
GEN_id_hi	0x02h	Generic identifier (high) hardwired (see Figure 9)
GEN_id_lo	0x03h	Generic identifier (low) hardwired (see Figure 10)
AN_adv	0x04h	Autonegotiation advertisement (see Figure 11 and Table 8)
AN_lpa	0x05h	Autonegotiation link partner ability (see Figure 12 and Table 9)
AN_exp	0x06h	Autonegotiation expansion (see Figure 15 and Table 13)
AN_np	0x07h	Autonegotiation next-page transmit (see Figure 16 and Table 14)
Reserved	0x08h	
Reserved	• • •	Reserved by IEEE Std 802.3
Reserved	0x0Fh	
TXPHY_id	0x10h	PHY identifier†
TXPHY_ctl	0x11h	PHY control (see Figure 17 and Table 15)
TXPHY_sts	0x12h	PHY status (see Figure 18 and Table 16)

† TI-specific register

Figure 4. Register Map

MII frame format

The default or IDLE state of the MII is a logic 1. All 3-state drivers are disabled and the PHY pullup resistor pulls the management data input/output (MDIO) line to a logic 1. Before initiating any other transaction, the station management entity sends a preamble sequence of contiguous logic-1 bits on MDIO with 32 corresponding cycles on MDCLK. This sequence provides the PHY a pattern to use to establish synchronization. A PHY observes the sequence of 32 contiguous 1 bits on MDIO with 32 corresponding cycles on MDCLK before responding to any other transactions. See Figures 5 and 6 for MII frame formats.

Start Delimiter	Operation Code	PHY Address	Register Address	Turnaround	Data
01	10	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

Figure 5. MII Read Frame Format

Start Delimiter	Operation Code	PHY Address	Register Address	Turnaround	Data
01	01	AAAAA	RRRRR	10	DDDD.DDDD.DDDD.DDDD

Figure 6. MII Write Frame Format

start delimiter

The start of a frame is indicated by a 01 pattern. This pattern specifies transitions from the default logic-1 line state to 0 and then back to 1.

operation code

The operation code for a read is 10, and the code for a write is 01.

PHY address

The PHY address is five bits, providing 32 unique PHY addresses. The first PHY address bit transmitted and received is the most significant bit of the address. The TNETE2101 address is set using CDEVSEL0–CDEVSEL2, CDEVSEL 3 (SLINK), and CDEVSEL4 (MCOL).

register address

The register address is 5 bits, providing 32 individual registers to be addressed within each PHY. See Figure 4 for the addresses of individual registers.

turnaround

An idle-bit time, during which no device actively drives the MDIO signal, is inserted between the register address field and the data field of a read frame to avoid contention. During a read frame, the PHY drives a 0 bit onto MDIO for the bit time that follows the idle bit and precedes the data field. During a write frame, this field consists of a 1 bit followed by a 0 bit.

data

The data field is 16 bits. The first data bit transmitted and received is the most significant bit of the data payload.

MII interrupt operation

The TNETE2101 can provide an interrupt based on certain PHY events through the MII MDIO signal. This allows software to receive an interrupt on events, such as a change in link, without periodically polling the device. Interrupt is indicated by driving the MDIO terminal low after the quiescent cycle and while MDCLK is high. The quiescent cycle is the cycle following the data transfer, during which neither the MACs nor the PHYs drive the MDIO.

The interrupt feature is controlled by register bits, MINT, INTEN, and TINT. MINT is the MII-interrupt bit (register 0x12, bit 15) and is set to a 1 when one or more interrupt events have occurred. INTEN is the interrupt-enable bit (register 0x11, bit 1) which allows MINT to generate an interrupt on the MDIO terminal. Additionally, to test interrupt operation (TINT), test interrupt (register 0x11, bit 0) can be set to a 1 which generates an interrupt, regardless of the value of MINT and INTEN.

Once an interrupt has occurred, MINT can be set to a 0 again by reading the register that contains the event status. Table 5 shows all the events that can cause MINT to be set and the register location.

Table 5. Interrupt Causes and Register Location

EVENT	CAUSE	REGISTER	BIT
JABBER	When set to a 1	0x01	1
LINK	Change in state or is different from either the last read value of current state of LINK	0x01	2
RFAULT	When set to a 1	0x01	4
AUTOCMPLT	When set to a 1	0x01	5
PAGERX	When set to a 1	0x06	1
FEFI	When set to a 1	0x12	10
SYNCLOSS	When set to a 1	0x12	11
TPENERGY	When set to a 1 and MANCONF is enabled	0x12	12
PLOK	Change in state and MANCONF is enabled	0x12	13
PHOK	When set to a 1	0x12	14

details of an interrupt on MDIO

- The first MII frame exchanged after power up on MDCLK/MDIO synchronizes the internal MII-state machine. (After the first MII frame, the TNETE2101 does not require the 32 contiguous 1s before the start of frame for synchronization.)
- A complete clock cycle (high and low) must occur after the last data bit. This clock cycle, or quiescent cycle, allows the device driving MDIO to set its output to a high-impedance state. After reaching the high-impedance state, MDIO goes high due to the required external pullup on the MDIO signal.
- Clock brought high again enables the interrupt to be driven on the MDIO line (MDIO = low). For as long as the clock is held high, if an interrupt occurs, MDIO is driven low. The interrupt occurring is not contingent on seeing another rising edge on the MDCLK, instead, it is clocked through, based on the internal PHY clock.
- On every rising edge thereafter, PHY samples the MDIO line to see if the management entity is outputing a low, signifying the start of frame. If the MDIO line is high, there is no start of frame and the PHY again drives the MDIO line low, if there is an interrupt. If start of frame is recognized, the PHY inhibits driving the interrupt onto the MDIO line until after the MII frame has completed.

PHY generic control register – GEN_ctl at 0x00

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
RESET	LOOPBK	SPEED	AUTOENB	PDOWN	ISOLATE	AUTORSRT	DUPLEX	COLTEST	Reserved						

Figure 7. PHY Generic Control Register

Table 6. PHY Generic Control Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
RESET	15	PHY reset. Writing a 1 to RESET causes the PHY to be reset and all registers (except GEN_ctl) to be reset to their default values. RESET is self-clearing–it returns a value of 1 when read, until the internal reset is complete (which takes no longer than 500 ms). Writing a 0 to RESET (default) has no effect. This operation can interrupt data communications.
LOOPBK	14	Loopback. LOOPBK enables or disables internal loopback within the PHY device. When LOOPBK is set to 1, data is wrapped internally within the PHY and does not appear on the network. When LOOPBK is cleared to 0 (default), data is transmitted to and received from the network. While the PHY is in loopback, all network lines are placed in a noncontentious state. If CLOOPBK is asserted low, loopback is enabled and this bit cannot be set to 0 but is read as 1.
SPEED	13	Speed select. Link speed is determined by way of either autonegotiation or manual setting. There are three methods by which the PHY speed can be determined: – Autonegotiation enabled. Speed determined by negotiation. – Autonegotiation disabled by CAUTONEG being low . Speed determined by CSPEED setting. – Autonegotiation disabled by register bit AUTOENB set to a 0. Speed determined by register bit SPEED setting. When SPEED is set to a 1 (default) the PHY speed is 100 Mbit/s and when set to a 0 the PHY speed is 10 Mbit/s. The value read from the SPEED bit always reflects the current PHY speed, regardless of which method is used to select the speed (as described previously).
AUTOENB	12	Autonegotiate enable. AUTOENB enables or disables the autonegotiation process if CAUTONEG is high. When AUTOENB is 0, the link is configured by way of the DUPLEX and SPEED bits, and the PHY implements the appropriate link-integrity test. When AUTOENB is set to 1 (default), autonegotiation is enabled and the PHY engages in the autonegotiation process when a LINK FAIL condition is detected or the AUTORSRT bit is set. The link must not be treated as valid until the AUTOCMPLT bit and LINK bit are set to 1. If CAUTONEG terminal is low, autonegotiation is disabled, and AUTOENB cannot be set to 1 but is read as 0.
PDOWN	11	Power down. When PDOWN is set to 1, the PHY is placed in a low power-consumption state. The time required for the PHY to power up after PDOWN is cleared can vary considerably. It is good practice to set RESET after this time to make certain that the PHY is in a valid state. If CPWRDOWN is asserted low, the PHY is powered down, and this bit cannot be set to 0 but is read as 1.
ISOLATE	10	Isolate. The function of ISOLATE depends on whether the PHY is in repeater mode or node mode (determined by the REPEATER bit in TXPHY_ctl). In node mode, when ISOLATE is set to 1 (default), the PHY electrically isolates its data paths from the MII. In this state, it does not respond to MTXD0–MTXD3, MTXEN, and MTXER inputs, but presents a high impedance on its MTCLK, MRCLK, MRXDV, MRXER, MRXD0–MRXD3, and MCOL outputs. It still responds to management frames on MDIO and MDCLK. In repeater mode, when ISOLATE is set to 1, the PHY presents a high impedance on its MRCLK, MRXDV, MRXER, and MRXD0–MRXD3 outputs only. If CISOLATE is deasserted high, the ISOLATE function is disabled, and this bit cannot be set to 1 but is read as 0.
AUTORSRT	9	Restart autonegotiation. If autonegotiation has been enabled by setting AUTOENB to 1, the autonegotiation process can be restarted by setting AUTORSRT to 1. AUTORSRT is self clearing, and the PHY returns a value of 1 in this bit until autonegotiation fast-link pulse (FLP) data-burst transmission has been initiated. When AUTOENB is cleared to 0, AUTORSRT is read as 0. The default value of AUTORSRT is 0.
DUPLEX	8	Duplex mode. Duplex mode is determined by way of either autonegotiation or normal setting. There are three ways the PHY speed can be determined: – Autonegotiation enabled. Duplex determined by negotiation. – Autonegotiation disabled by CAUTONEG being low. Duplex determined by CDUPLEX setting. – Autonegotiation disabled by register bit AUTOENB set to a 0. Duplex determined by register bit DUPLEX setting. When DUPLEX is set to 1 (default), the PHY is in full duplex. When DUPLEX is set to 0, the PHY is in half duplex. The value read from the DUPLEX bit always reflects the current PHY duplex, regardless of which is used to select the duplex, (as described previously).
COLTEST	7	Collision test mode. When COLTEST is set to 1 and LOOPBK is set to 1, the PHY asserts the collision-detect signal MCOL when transmit enable MTXEN is asserted. The default value of COLTEST is 0.
Reserved	6–0	Reserved. Read and write as 0.

PHY generic status register – GEN_sts at 0x01

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
0	1	1	1	1	Reserved				1	AUTOCMPLT	RFAULT	1	LINK	JABBER	1

Figure 8. PHY Generic Status Register

Table 7. PHY Generic Status Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
0	15	100BASE-T4 ability. Not supported.
1	14	100BASE-TX full-duplex ability. Supported by this PHY.
1	13	100BASE-TX half-duplex ability. Supported by this PHY.
1	12	10BASE-T full-duplex ability. Supported by this PHY.
1	11	10BASE-T half-duplex ability. Supported by this PHY.
Reserved	10–7	Reserved. Read and write as 0.
1	6	Management frame preamble suppression. This PHY accepts management frames with the preamble suppressed. Management frames sent over MDIO do not need to be preceded by the preamble pattern of 32 1s.
AUTOCMPLT	5	Autoconfiguration complete. When AUTOCMPLT is read as 1, it indicates that the autonegotiation process has completed and the values of registers AN_adv, AN_lpa, AN_exp, and AN_np are valid. If autonegotiation is in progress, or has been restarted and AUTORSRT is still set to 1, or has been disabled by clearing AUTOENB to 0, the AUTOCMPLT bit reads as 0.
RFAULT	4	Remote fault. The RFAULT bit is set to 1 during autonegotiation if an error in the protocol is detected and negotiation is restarted. If the negotiation involved the exchange of multiple next pages, this bit indicates that the first of those pages needs to be reloaded into AN_np due to the restart. RFAULT is latched as 1 until the register is read. The default value of RFAULT is 0.
1	3	Autonegotiation ability. Supported by this PHY.
LINK	2	Link status. In general, when LINK is set to 1, the PHY is reporting that a good link is available to the link partner for exchange of data. The value of LINK is latched until the register is read. The default value of LINK is 1. In 10BASE-T mode, LINK is set to 1 when the PHY has determined that a valid 10BASE-T link is established. LINK read as a 0 indicates that the link is not valid. The PHY implements the standard 10BASE-T link integrity test state machine. To maintain a good link, link pulses are expected every 8–24 ms. If no link pulses are seen for over 100 ms, the link invalid state is entered, and this bit is cleared. If AUTOENB is not set, then the bit is set again after seven consecutive, correctly timed link pulses are received. In 100BASE-TX mode, the LINK bit is set when the descrambler has locked onto the incoming data stream and has remained locked for a minimum of 330 μs. If AUTONEG is set, then the link is becoming invalid, which causes the autonegotiation process to restart.
JABBER	1	Jabber detect. The jabber function is not specified for 100BASE-TX PHYs, so JABBER always reads as 0 (default) when the PHY is operating in the 100-Mbit/s mode. When JABBER is read as 1, it indicates that a 10BASE-T jabber condition has been detected. JABBER is latched as 1 until the register is read or PHY is reset. The jabber condition occurs when a single packet transmission exceeds 20 ms. In the jabber condition, all transmit requests are ignored, MCOL is asserted high, and collision detection is disabled, as is the internal loopback of transmit data (when in half-duplex mode). The jabber condition persists for 576–628 ms after deassertion of MTXEN before packet transmission can restart.
1	0	Extended capability. This PHY implements an extended register set.

PHY generic identifier – GEN_id_hi/GEN_id_lo at 0x02/03

These two hardwired 16-bit registers contain an identifier code for the 10BASE-T/100BASE-TX PHY. GEN_id_hi contains 0x4000, and GEN_id_lo contains 0x503X.

The PHY ID is composed of bits 3–24 of the 25-bit organizationally unique identifier (OUI) assigned to TI by IEEE. Bit 3 of the OUI maps to bit 15 of GEN_id_hi, bit 4 of the OUI to bit 14 of the GEN_id_hi, and so on. Figures 9 and 10 show the bit layout of GEN_id_hi and GEN_id_lo.

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
OUI Bits 3–18															
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9. PHY Generic Identifier – GEN_id_hi at 0x02

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
OUI Bits 19–24						Manufacturer Model Number						Manufacturer Revision Number			
0	1	0	1	0	0	0	0	0	0	1	1	X	X	X	X

Figure 10. PHY Generic Identifier – GEN_id_lo at 0x03

autonegotiation advertisement register – an_adv at 0x04

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
NP	ACK	RF	Technology Ability Field								Selector Field				

Figure 11. Autonegotiation Advertisement Register

Table 8. Autonegotiation Advertisement Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
NP	15	Autonegotiation next page. When NP is set to 1, the autonegotiation process indicates to the link partner that the PHY wishes to exchange next pages. The capability of the link partner to exchange next pages can be determined by the value of the LPNPABLE bit in the AN_exp register. When the link partner is capable of next-page exchange, it requests an exchange by setting the LPNP bit to 1 in the AN_lpa register. Then, the autonegotiation process waits until the next page is written to the AN_np register, and the link partner has had its next page loaded. The link partner's next page then is received into the AN_lpa register. A consequence of this process is that the PHY fails to complete autonegotiation if the PHY and its link partner agree to exchange next pages, but the link partner never sends its next page. A software timeout, which forces renegotiation with NP cleared to 0, should be implemented to avoid this situation. The default value of NP is 0.
ACK	14	Acknowledge. Reserved for internal use of the autonegotiation process. Write as 0, ignore during read.
RF	13	Remote fault. When RF is set to 1, the PHY indicates a remote fault condition to its link partner. The type of fault, as well as the criteria and method of fault detection, is PHY specific. The default value of RF is 0.
Technology Ability Field	12,11	Autonegotiation advertised technology ability. Bits 12–5 represent an 8-bit value sent to the link partner to indicate the abilities of the PHY. Once negotiated, the values of the bits are reflected in bits 12–5 in register 0×05 of the link partner. Bits 11 and 12 are set to 0 by default. These bits are reserved for future use according to IEEE 802.3u. These bits can be changed and are sent to the link partner during autonegotiation.
	10	Pause operation of full duplex links. Defined for use at the MAC level and when set to a 1 signifies that the MAC is capable of performing the pause function. The pause capability is exchanged between the PHYs during the autonegotiation but does not change the PHY's mode of operation. The pause function is valid only during full-duplex operation regardless of the medium. The default value of this bit is 0.
	9	100BASE-T4. Default value is a 0 and should not be set to a 1 since the TNETE2101 does not support this medium.
	8	100BASE-TX full duplex. Set to 1 to advertise availability to the link partner.
	7	100BASE-TX half duplex. Set to 1 to advertise availability to the link partner.
	6	10BASE-T full duplex. Set to 1 to advertise availability to the link partner.
	5	10BASE-T half duplex. Set to 1 to advertise availability to the link partner.
Selector Field	4–0	Autonegotiation selector field code. This field has a default value of 0001, meaning that the PHY supports only IEEE Std 802.3 format link code words.

autonegotiation link partner ability register – an_lpa at 0x05

The link partner ability register, AN_lpa, has three different formats, depending on when the page is received. The first page received from the link partner always is in the base-page encoding and is used by the PHY for autoconfiguration. If the link partner supports next-page exchange, subsequently received pages can be in either message-page or unformatted-page encoding, as determined by the value of the LPNP bit (in AN_lpa).

The use of next pages is summarized as:

- Both the PHY and the link partner must indicate next-page ability before either can commence exchange of next pages.
- If both devices are next-page able, then both devices must send at least one next page.
- Next-page exchange continues until neither device on a link has more pages to transmit [as indicated by the LPNP bit (in AN_lpa) and the NP bit (in AN_adv)]. A message page with a null-message code field value is sent if the device has no other information to transmit.
- A message code can carry a specific message or information that defines how subsequent unformatted page(s) should be interpreted.
- If a message code references unformatted pages, the unformatted pages immediately follow the referencing message code in the order specified by the message code.
- Unformatted page users are responsible for controlling the format and sequencing of their unformatted pages.

base-page encoding

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
LPNP	ACK	LPRF	Link Partner Technology Ability Field								Link Partner Selector Field				

Figure 12. Autonegotiation Link Partner Ability Register

Table 9. Autonegotiation Link Partner Ability Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
LPNP	15	Link partner next page. When LPNP is set to 1, the link partner is indicating that it wishes to exchange a next page. See the description of NP in register AN_adv for more information on next-page exchange.
ACK	14	Acknowledge. Reserved for internal use of the autonegotiation process. Write as 0, ignore during read.
LPRF	13	Link partner remote fault. When LPRF is set to 1, the link partner is reporting a remote fault condition.
Link Partner Technology Ability Field	12, 11	Link partner technology ability field. Bits 12–5 are updated during autonegotiate with the 8-bit values received from the link partner's PHY advertisement register. Bits 9–5 are examined to determine the highest common-link capability between the two PHYs. Bit values for 12–11 are updated but to do so affects the PHY's mode of operation.
	10	Pause operation for full duplex links. Defined for use at the MAC level and when set to a 1 after autonegotiation, signifies that the link partner's MAC is capable of performing the pause function. The pause capability is exchanged between the PHYs during the autonegotiation but does not change the PHY's mode of operation. The pause function is only valid during full-duplex operation, regardless of the medium.
	9	100BASE-T4. Set to a 1 if link partner supports 100BASE-T4. The TNETE2101 does not support this capability.
	8	100BASE-TX full duplex. Set to 1 if supported by the link partner.
	7	100BASE-TX half duplex. Set to 1 if supported by the link partner.
	6	10BASE-T full duplex. Set to 1 if supported by the link partner.
	5	10BASE-T half duplex. Set to 1 if supported by the link partner.
Link Partner Selector Field	4–0	Link partner selector field. This 5-bit value encodes the format of this register. The PHY supports only IEEE Std 802.3 format fields (see description of bits 12–5), code 00001. (The only other currently specified IEEE value is 00010 for IEEE Std 802.9a multimedia frames).

message-page encoding (LPMP = 1)

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
LPNP	ACK	LPMP	ACK2	T	Message Code Field										

Figure 13. Message-Page-Encoding Register

Table 10. Message-Page-Encoding Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
LPNP	15	Link partner next page. When LPNP is set to 1, the link partner is ready to exchange an extra next page. See the description of NP in register AN_adv for more information on next-page exchange.
ACK	14	Acknowledge. Reserved for internal use of the autonegotiation process. Ignore during read.
LPMP	13	Link partner message page. When LPMP is set to 1, register AN_lpa contains a message page.
ACK2	12	Acknowledge 2. Reserved for internal use of the autonegotiation process. Ignore during read.
T	11	Toggle. Reserved for internal use of the autonegotiation process. Ignore during read.
Message Code Field	10–0	Message code. An 11-bit message code. See Table 11 for descriptions of the currently defined IEEE message codes.

message-code field values

Table 11 summarizes the message-code field values specified in IEEE Std 802.3. All message codes not specified are reserved for future IEEE use or allocation.

Table 11. Message-Code Field Values

MESSAGE CODE	BIT 10–0	MESSAGE-CODE DESCRIPTION
0	00000000000	Reserved for future autonegotiation use
1	00000000001	Null message. The null-message code is transmitted during next-page exchange when the local device has no further messages to transmit and the link partner is still transmitting valid next pages.
2	00000000010	Technology ability extension code 1 [one unformatted page (UP) with technology ability field to follow]. This message code is reserved for future expansion of the technology ability field and indicates that a defined user code with a specific technology ability field encoding follows.
3	00000000011	Technology ability extension code 2 (two UPs with technology ability fields to follow). This message code is reserved for future expansion of the technology ability field and indicates that two defined user codes with specific technology ability field encoding follow.
4	00000000100	Remote-fault number code (one UP with binary-coded remote fault follows). This message code is followed by a single user code whose encoding specifies the type of fault that has occurred. The following user codes are defined: 0 – RF test. Used to test remote-fault operation. 1 – Link loss 2 – Jabber 3 – Parallel detection fault. Sent to identify when PDFAULT (in AN_exp) is set.

Table 11. Message-Code Field Values (Continued)

<table>
<tr><th>MESSAGE CODE</th><th>BIT 10–0</th><th>MESSAGE CODE DESCRIPTION</th></tr>
<tr><td>5</td><td>00000000101</td><td>OUI-tagged message. The OUI-tagged message consists of a single message code of 0000.0000.0101, followed by four user codes defined in the following chart. The numbers indicate where each bit of the 24-bit OUI should be stored in the 11-bit user code. Bits 8–0 of the third user code and the fourth (and final) user code contain a user-defined user-code value that is specific to the OUI transmitted.
<table>
<tr><th></th><th>Bit 10</th><th colspan="9">User-Code Encoding of OUI</th><th>Bit 0</th></tr>
<tr><td>1st</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td></tr>
<tr><td>2nd</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td></tr>
<tr><td>3rd</td><td>1</td><td>0</td><td colspan="9">User-defined user code specific to OUI</td></tr>
<tr><td>4th</td><td colspan="11">User-defined user code specific to OUI</td></tr>
</table></td></tr>
<tr><td>6</td><td>00000000110</td><td>PHY identifier tag code. The PHY ID tag code message consists of a single message code of 0000.0000.0110 followed by four user codes defined in the following chart. The numbers indicate where each bit of the 32-bit PHY ID (stored in GEN_id_hi register 0x2:15–0 and GEN_id_lo register 0x3:15–0) should be stored in the 11-bit user code. Bit 0 of the third user code and the fourth (and final) user code contain a user-defined user-code value that is specific to the PHY ID transmitted.
<table>
<tr><th></th><th>Bit 10</th><th colspan="9">User-Code Encoding of PHY ID</th><th>Bit 0</th></tr>
<tr><td>1st</td><td>0x2 15</td><td>0x2 14</td><td>0x2 13</td><td>0x2 12</td><td>0x2 11</td><td>0x2 10</td><td>0x2 9</td><td>0x2 8</td><td>0x2 7</td><td>0x2 6</td><td>0x2 5</td></tr>
<tr><td>2nd</td><td>0x2 4</td><td>0x2 3</td><td>0x2 2</td><td>0x2 1</td><td>0x2 0</td><td>0x3 15</td><td>0x3 14</td><td>0x3 13</td><td>0x3 12</td><td>0x3 11</td><td>0x3 10</td></tr>
<tr><td>3rd</td><td>0x3 9</td><td>0x3 8</td><td>0x3 7</td><td>0x3 6</td><td>0x3 5</td><td>0x3 4</td><td>0x3 3</td><td>0x3 2</td><td>0x3 1</td><td>0x3 0</td><td>UD UC</td></tr>
<tr><td>4th</td><td colspan="11">User-defined user code specific to PHY ID</td></tr>
</table></td></tr>
<tr><td>2047</td><td>11111111111</td><td>Reserved for future autonegotiation use</td></tr>
</table>

unformatted-page encoding (LPMP = 0)

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
LPNP	ACK	LPMP	ACK2	T	Unformatted Code Field										

Figure 14. Unformatted-Page Encoding Register

Table 12. Unformatted-Page Encoding Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
LPNP	15	Link partner next page. When LPNP is set to 1, the link partner is indicating that it wishes to exchange an extra next page. Refer to the description of NP in register AN_adv for more information on next-page exchange.
ACK	14	Acknowledge. Reserved for internal use of the autonegotiation process. Ignore during read.
LPMP	13	Link partner message page. When LPMP is cleared to 0, register AN_lpa contains an unformatted page.
ACK2	12	Acknowledge 2. Reserved for internal use of the autonegotiation process. Ignore during read.
T	11	Toggle. Reserved for internal use of the autonegotiation process. Ignore during read.
Unformatted Code Field	10–0	Unformatted code. 11-bit user code. The format of this code is determined by the message code (see Table 11).

autonegotiation expansion register – AN_exp at 0x06

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
Reserved											PDFAULT	LPNPABLE	1	PAGERX	LPANABLE

Figure 15. Autonegotiation Expansion Register

Table 13. Autonegotiation Expansion-Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
Reserved	15–5	Reserved. Read and write as 0.
PDFAULT	4	Parallel detection fault. The PDFAULT bit is set to 1 during autonegotiation if the PHY detects a valid 10BASE-T or 100BASE-TX link that fails within 500–1000 ms or if both the 10BASE-T and 100BASE-TX link monitors report a good link. PDFAULT is latched until this register is read, then it is cleared to 0 (default).
LPNPABLE	3	Link-partner next-page able. When LPNPABLE is set to 1, the link partner is indicating that it is implementing the autonegotiation next-page ability. The default value of LPNPABLE is 0.
1	2	Next-page able. This PHY supports autonegotiation next-page exchange.
PAGERX	1	Page received. The PAGERX bit is set to 1 when a new link code word has been received and stored in the AN_lpa register. PAGERX is latched until this register is read, then it is cleared to 0 (default).
LPANABLE	0	Link-partner autonegotiation enable. When LPANABLE is set to 1, the PHY has received link code word(s) from the link partner during autonegotiation. The value of LPANABLE is retained after autonegotiation completes, and is re-evaluated only during a subsequent renegotiation (whether caused by a LINK FAIL condition or a forced restart) or PHY reset. The default value of LPANABLE is 0.

autonegotiation next-page transmit register – AN_np at 0x07

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
NP	ACK	MP	ACK2	T	Message or Unformatted Code Field										

Figure 16. Autonegotiation Next-Page Transmit Register

Table 14. Autonegotiation Next-Page Transmit-Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
NP	15	Next page. When a next page with NP set to 1 is transmitted, the link partner is informed that another next page is to be transmitted (see Table 11). The default value of NP is 0.
ACK	14	Acknowledge. Reserved for internal use of the autonegotiation process. Write as 0, ignore during read.
MP	13	Message page. When MP is set to 1, AN_np contains a message-page code field. When MP is cleared to 0, AN_np contains an unformatted-page code field (see Table 11). The default value of MP is 1.
ACK2	12	Acknowledge 2. Reserved for internal use of the autonegotiation process. Write as 0, ignore during read.
T	11	Toggle. Reserved for internal use of the autonegotiation process. Write as 0, ignore during read.
Message or Unformatted Code Field	10–0	Message or unformatted code field (see Table 11). The default value of the code field is 000.0000.0001, the null message code.

PHY identifier high/low – TXPHY_id at 0x10

This hardwired 16-bit register contains a TI-assigned identifier code for the PHY PMIs. An additional identifier is required to identify non-IEEE Std 802.3 PHY/PMIs, which are not otherwise supported by the IEEE Std 802.3 MII specification. The identifier code for the internal 10BASE-T/100BASE-TX PHY is 0x0003.

PHY control register – TXPHY_ctl at 0x11

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
IGLINK	SWAPOL	MANCONF	SQEEN	MTEST	FIBER	FEFEN	NOENDEC	NOALIGN	DUPONLY	REPEATER	RXRESET	NOLINKP	NFEW	INTEN	TINT

Figure 17. PHY Control Register

Table 15. PHY Control-Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
IGLINK	15	Ignore link. When IGLINK is cleared to 0 (default), the 10BASE-T PHY expects to receive link pulses from the link partner (hub, switch, and so on) and clears the LINK bit in the GEN_sts register to 0 if they are not present. When IGLINK is set to 1, the internal link-integrity-test state machine is forced to stay in the LINK GOOD state even when no link pulses are being received, and it also causes the LINK bit to stay set to 1.
SWAPOL	14	Swap polarity. Allows swapping the receive polarity when the MANCONF bit is set to 1. Writing a 1 to SWAPOL causes the PHY to use the reverse of the IEEE Std 802.3 standard polarity for the ARCVP/ARCVN 10BASE-T receiver-input pair. This is used to compensate for a cable in which the receive pair has been wired incorrectly. See the PLOK bit description in register 0×12 for a detailed explanation.

Table 15. PHY Control Register Bit Functions (Continued)

BIT NAME	BIT NO.	FUNCTION
MANCONF	13	Manual configuration. Writing a 1 to MANCONF enables manual configuration of the PHY polarity using the SWAPOL bit. The default value of this bit is 0 which enables automatic detection of polarity by monitoring link pulses for inversion. See the PLOK bit description in register 0×12 for a detailed explanation.
SQEEN	12	Signal quality error (SQE) enable. When SQEEN is set to 1, the 10BASE-T PHY (when selected) performs the SQE test function at the end-of-packet transmission. The default value of SQEEN is 1. The SQE test provides an internal simulated collision to test collision-detect circuit integrity after a transmission. In 10BASE-T mode, the SQE test asserts MCOL between 600–1600 ns after the last positive edge of a frame is transmitted, with the collision event lasting between 500–1500 ns.
MTEST	11	Manufacturing test. When MTEST is set to 1, the PHY is placed in manufacturing test mode. Manufacturing test mode is reserved for TI manufacturing test only. The default value of MTEST is 0. Operation of the PHY and MII registers is undefined when this bit is set.
FIBER	10	100BASE-FX mode. When FIBER is set to 1, PHY disables its cipher-stream scrambler and descrambler. The UTP interface terminals are placed in a nonfunctional low-power state and the differential PECL fiber-interface terminals are activated. The default value of FIBER is 0. If $\overline{\text{CFIBER}}$ is asserted low, the fiber interface is enabled and this bit cannot be set to 0 but is read as 1.
FEFEN	9	Far-end fault indication enable. When both FEFEN and FIBER are set to 1, the PHY transmits the far-end fault indication (FEFI) symbol stream (consisting of 84 1s and 0) when the 100BASE-FX signal detect is deasserted. Also, at this time the FEFI bit in TXPHY_sts is set to 1. The FEFI system is specified for use in 100BASE-FX fiber applications only. The default value of FEFEN is 0.
NOENDEC	8	No encode/decode. When NOENDEC is set to 1, the 100BASE-TX PHY bypasses its 5B4B encoder and decoder. Instead, it takes the 5-bit code presented on MTXD0–MTXD3 and MTXER (most significant bit) as transmit data, and presents the received 5B code groups on MRXD0–MRXD3 and MRXER (most significant bit). The default value of NOENDEC is 0. This mode of operation is provided for applications test purposes. If $\overline{\text{CPASS5B}}$ terminal is asserted low, the NOENDEC mode is enabled and this bit cannot be set to 0 but is read as 1.
NOALIGN	7	No symbol alignment. When NOALIGN is set to 1, the 100BASE-TX receive-symbol-alignment block is bypassed and the 5-bit descrambled receive symbols are passed directly to the 5B4B decoder.
DUPONLY	6	Duplex LED. When DUPONLY is set to 1, the $\overline{\text{LDUPCOL}}$ LED driver indicates the duplex mode in which the PHY is operating and does not indicate network collisions. The default value of DUPONLY is 0.
REPEATER	5	Repeater-mode enable. When REPEATER is set to 1, the PHY does not assert MCRS in response to transmit activity in 100BASE-TX mode. Also, the ISOLATE bit in the GEN_ctl register causes only MRCLK, MRXD0–MRXD3, MRXDV, and MRXER to resort to a high-impedance state. The default value of REPEATER is 0. If $\overline{\text{CREPEATER}}$ is asserted low, the repeater mode is enabled and this bit cannot be set to 0 but is read as 1.
RXRESET	4	100BASE-TX receive reset. Writing a 1 to this self-clearing bit allows the 100BASE-TX receive logic (descrambler, aligner, and 5B4B decoder) to be reset without affecting other parts of the PHY. The default value of RXRESET is 0.
NOLINKP	3	Disable link-pulse transmission. When NOLINKP is set to 1 and IGLINK is set to 1, the PHY does not transmit any form of link pulses. In 10BASE-T applications, the link partner does not detect a good link and does not transmit any data, unless it is not implementing the link-integrity test (for example, a PHY with IGLINK set to 1). Autonegotiation should be disabled by clearing AUTOENB to 0 when NOLINKP is set because no autonegotiation FLPs are transmitted to the link partner. NOLINKP has no effect on the PHY if IGLINK is cleared to 0. The default value of NOLINKP is 0. This mode of operation is provided for application-test purposes.
NFEW	2	Not far end wrap. NFEW has meaning only when the LOOPBK bit of GEN_ctl is set to 1. Writing a 1 to NFEW causes the PHY to wrap the MTXD input data to the MRXD output just after the MII interface. Writing a 0 to NFEW causes the PMI to wrap the TX data to the RX just before the network transceiver interface (either 10BASE-T or 100BASE-TX). When NFEW is set to 1, preamble is wrapped without degradation (in normal operation, the PHY may lose some preamble bits during initial clock-recovery synchronization). The default value of NFEW is 0.
INTEN	1	Interrupt enable. Writing a 1 to INTEN allows the PHY to generate interrupts on the MII when the MINT bit is set to 1. Writing a 0 to INTEN prevents the PHY from generating any MII interrupts. INTEN does not disable test interrupts. The default value of INTEN is 0.
TINT	0	Test interrupt. When TINT is set to 1, the PHY generates interrupts on the MII, regardless of the value of the MINT and INTEN bits. TINT is to be used for diagnostic test of the MII-interrupt function. The default value of TINT is 0.

PHY status register – TXPHY_sts at 0x12

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
MINT	PHOK	PLOK	TPENERGY	SYNCLOSS	FEFI	Reserved									

Figure 18. PHY Status Register

Table 16. PHY Status-Register Bit Functions

BIT NAME	BIT NO.	FUNCTION
MINT†	15	MII Interrupt. MINT indicates an MII-interrupt condition. The MII-interrupt request is activated and latched until this register is read. Writing to MINT has no effect. MINT is set to 1 when: – JABBER (register 0x0, bit 1) is set to 1. – LINK (register 0x0, bit 2) changes state or is different from either the last read value or the current state of the link. – RFAULT (register 0x1, bit 4) is set to 1. – AUTOCMPLT (register 0x1, bit 5) is set to 1. – PAGERX (register 0x6, bit 1) is set to 1. – FEFI (register 0x12, bit 10) is set to 1. – SYNCLOSS (register 0x12, bit 11) is set to 1. – PHOK (register 0x12, bit 14) is set to 1. Additional interrupt sources are active only when the MANCONF bit (register 0x11, bit 13) is set to 1. MINT is set to a 1 when: – TPENERGY (register 0x12, bit 12) is set to 1. – PLOK (register 0x12, bit 13) changes state.
PHOK	14	Power high OK. When PHOK is set to 1, it indicates that the oscillator circuit connected to XTAL1 has begun to oscillate (and perform around 75 cycles). PHY-sourced clocks (MRCLK and MTCLK) are not valid until PHOK is asserted. The clocks can take up to 50 ms to become stable and the PHY requires the RESET bit to be set to make certain it is in a valid state. When PHOK is 0, the PHY is not in a fully operational state.
PLOK	13	Polarity OK. PLOK set to a 1 (default) signifies that the 10BASE-T PHY is receiving valid (noninverted) link pulses. PLOK always is set to a 1 when MANCONF is set to a 0, since the PHY automatically corrects polarity. If MANCONF is set to a 1 for manual polarity configuration, PLOK is cleared to a 0 if a sequence of seven consecutive inverted link pulses is detected. PLOK can be set to a 1 again only if the SWAPOL bit is toggled and then 1 noninverted link pulse is received. If MANCONF is a 1 and then cleared to a 0 when PLOK is still a 0, PLOK is not set to a 1 until SWAPOL is toggled. This reenables the autopolarity detection and PLOK remains a 1. 10BASE-T polarity is determined strictly from link pulses and not from received data or TP idles.
TPENERGY	12	Twisted-pair energy detect. When TPENERGY is set to 1, it indicates that the PHY is receiving impulses on ARCVP/ARCVN.
SYNCLOSS	11	100BASE-TX receive descrambler synchronization loss. The 100BASE-TX descrambler expects to receive at least 12 consecutive IDLE symbols every 722 µs. If these are not seen, then SYNCLOSS is set to 1, and the descrambler attempts to resynchronize itself to the incoming scrambled data stream. The value of SYNCLOSS is latched high until this register is read.
FEFI	10	Far-end fault indication. When enabled via the FEFEN bit in TXPHY_ctl, this bit is set to 1 if the FEFI signaling sequence is being transmitted by the link partner. The value of FEFI is latched (held) high until this register is read.
Reserved	9–0	Reserved. Read and write as 0.

† Useful for switching applications (TI patented)

absolute maximum ratings†

Supply voltage range: V_{DD}, V_{DDA}, XMT_V_{DDA}, (see Notes 1 and 2)–0.5 V to 4.6 V
V_{DD5} (see Notes 1 and 2)–0.5 V to 5.5 V
Input voltage range: TTL, V_I–0.5 V to V_{DD} + 0.5 V
5-V tolerant TTL, V_I–0.5 V to V_{DD5} + 0.5 V
PECL, V_I(<4.6 V max) V_{DD} –2.02 V to V_{DD} + 0.5 V
Output voltage range: TTL, V_O–0.5 V to V_{DD} + 0.5 V
5-V tolerant TTL, V_O–0.5 V to V_{DD5} + 0.5 V
PECL, V_O(<4.6 V max) V_{DD} –2.02 V to V_{DD} + 0.5 V
Thermal impedance, junction-to-ambient package, $Z_{\theta JA}$: Airflow = 068.40°C/W
Airflow = 150 ft/min57.45°C/W
Thermal impedance, junction-to-case package, $Z_{\theta JC}$1.95°C/W
Operating case temperature range, T_C0°C to 95°C
Storage temperature range, T_{stg}–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. Turning power supplies on and off (cycling sequence) within a mixed 5-V/3.3-V system is an important consideration. The designer must observe a few rules to avoid damaging the TNETE2101. Check with the manufacturers of all components used in the 3.3-V to 5-V interface to ensure that no unique device characteristics exist that would lead to rules more restrictive than the TNETE2101 requires.
   - The optimum solution to power-supply sequencing in a mixed-voltage system is to ramp up the 3.3-V supply first. A power-on reset component operating from this supply forces all 5-V-tolerant outputs into the high-impedance state. Then, the 5-V supply is ramped up. On power down, the 5-V rail deenergizes first, followed by the 3.3-V rail.
   - The second-best solution is to ramp both the 3.3-V and the 5-V rails at the same time, making sure that no more than 3.6 V exists between these two rails during the ramp up or down. If the 3.3 V is derived from the 5 V, then the 3.3 V rises as the 5 V rises, so the 5-V rail never exceeds the 3.3-V rail by more than 3.6 V. Both the optimum and second-best algorithms for power up prevent device damage. If it is impractical to implement ramping, follow these rules:
     – When turning on the power supply, all 3.3-V and 5-V supplies should start ramping from 0 V and reach 95 percent of their end-point values within 25 ms. All bus contention between the device and external devices is eliminated by the end of 25 ms.
     – When turning off the power supply, 3.3-V and 5-V supplies should start ramping from steady-state values and reach 5 percent of their final values within 25 ms. All bus contention between devices and external devices is eliminated by the end of 25 ms. There is a 250-s lifetime maximum at greater than 3.6-V difference between the supply rails. Holding the ramp-up/ramp-down period to 25 ms per power-on/off cycle should not significantly contribute to mean-time-between-failure (MTBF) shifts during product lifetimes.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}, V_{DDA}, XMT_V_{DDA}	Supply voltage		3	3.3	3.6	V
V_{DD5}	Reference voltage		4.5	5	5.5	V
V_I	Input voltage	TTL	0		V_{DD}	V
		5-V TTL	0		5.5	
		PECL	V_{TTP}		V_{DD} – 0.5	
V_O	Output voltage	TTL, 5-V TTL	0		V_{DD}	V
		PECL	V_{TTP}		V_{DD} – 0.5	
		LED	0		V_{DD}	
V_{IH}	High-level input voltage	TTL	2		V_{DD}	V
		5-V TTL	2		5.5	
		PECL	V_{DD} – 1.35		V_{DD} – 0.70	
V_{IL}	Low-level input voltage	TTL, 5-V TTL	0		0.8	V
		PECL	V_{DD} – 2		V_{DD} – 1.55	
V_{TTP}	Termination voltage	PECL		V_{DD} – 2		V
R_t	Differential-termination resistance	PECL		50		Ω

electrical characteristics over recommended operating conditions

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	TTL, 5-V TTL	2.4			V
		50 Ω to V_{DD}–2	PECL	1.50		2.30	
V_{OL}	Low-level output voltage	V_{DD} = min, T_C = max	LEDs (see Note 3)			0.8	V
		50 Ω to V_{DD}–2	PECL	0.20		0.30	
		I_{OL} = 4 mA	TTL, 5-VTTL			0.4	
V_{ID}	Differential input voltage		PECL	1.20		2.10	V
I_{IL}	Low-level input current	$V_I = V_{IL(min)}$	TTL, 5-V TTL, PECL			20	μA
I_{IH}	High-level input current	$V_I = V_{IH(max)}$	TTL, PECL			–20	μA
I_{OZ}	High-impedance-state output current		TTL, LED, PECL			–20	μA
I_{DD}	Supply current, 3.3 V (see Note 4)	100BASE-TX,	Full duplex		200		mA
		Power down			20		
C_i	Capacitive input				6		pF
C_o	Capacitive output				6		pF

NOTES: 3. $\overline{\text{LACTIVITY}}$, $\overline{\text{LDUPCOL}}$, $\overline{\text{LLINK}}$, $\overline{\text{LSPEED}}$
4. Typical values measured at 25°C without LEDs connected

oscillator requirements

PARAMETERS	MIN	TYP	MAX	UNIT
Clock frequency		20		MHz
Clock frequency error	–50		50	ppm
Clock duty cycle	40		60	%
V_{OH}	2.85		V_{DD}	V
V_{OL}	–0.50		0.80	V
t_r, t_f (see Note 5)			5	ns

NOTE 5: Measured at 20%–80% transition low-to-high or high-to-low points

MDIO timing requirements (see Figure 19)

NO.	PARAMETERS		MIN	MAX	UNIT
1	$t_{su(MDIO)}$	Setup time, MDIO valid to MDCLK high (see Note 6)	10		ns
2	$t_{h(MDIO)}$	Hold time, MDCLK high to MDIO changing (see Note 6)	10		ns

NOTE 6: MDIO is a bidirectional signal that can be sourced by the TNETE2101 or the PMI/PHY. When the TNET2101 sources the MDIO signal, TNETE2101 asserts MDIO synchronous to the rising edge of MDCLK.

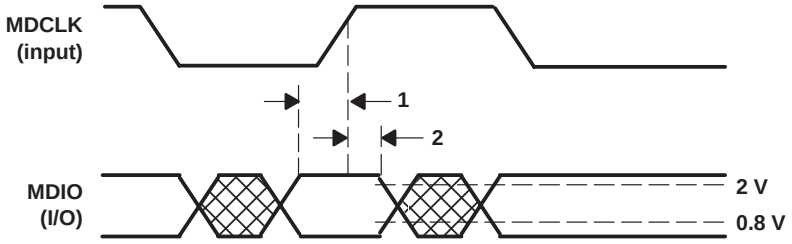


Figure 19. MDIO Sourced by External Controller

MDIO timing requirements (see Figure 20)

NO.			MIN	MAX	UNIT
1	$t_{a(MDIO)}$	Access time, MDIO valid to MDCLK high (see Note 7)	0	300	ns
2	$t_{c(MDCLK)}$	Cycle time		400	

NOTE 7: When the MDIO signal is sourced by the PMI/PHY, it is sampled by the TNETE2101 synchronous to the rising edge of MDCLK.

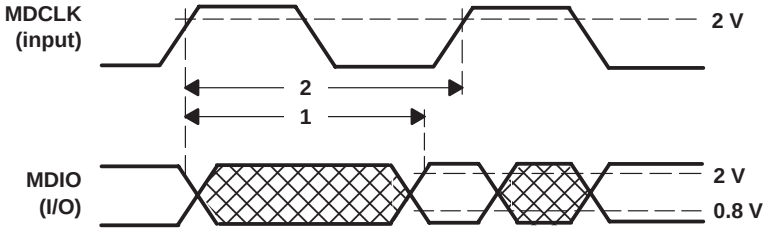


Figure 20. MDIO Sourced by the TNETE2101

MII transmit timing requirements (see Figure 21)

10BASE-T, 100BASE-TX, 100BASE-FX

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{su(MTXD3–MTXD0)}$	Setup time, MTXD3–MTXD0 valid to MTCLK↑	10			ns
1	$t_{su(MTXEN)}$	Setup time, MTXEN valid to MTCLK↑	10			ns
1	$t_{su(MTXER)}$	Setup time, MTXER valid to MTCLK↑	10			ns
2	$t_{h(MTXD3–MTXD0)}$	Hold time, MTCLK↑ to MTXD3–MTXD0 invalid	0			ns
2	$t_{h(MTXEN)}$	Hold time, MTCLK↑ to MTXEN↓	0			ns
2	$t_{h(MTXER)}$	Hold time, MTCLK↑ to MTXER↓	0			ns
3	$t_{c(MTCLK)}$	Cycle time, 10BASE-T		400		ns
3	$t_{c(MTCLK)}$	Cycle time, 100BASE-TX, 100BASE-FX		40		ns

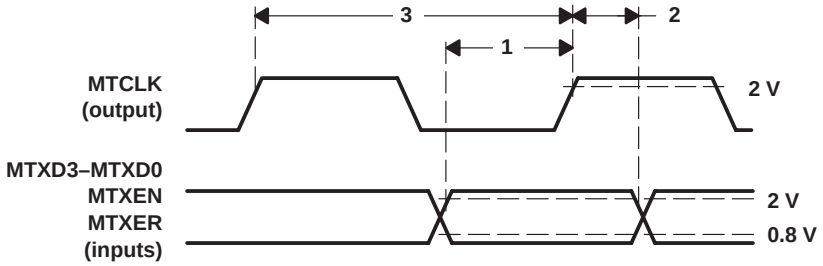


Figure 21. MII Transmit

MII receive timing requirements (see Figure 22)

10BASE-T, 100BASE-TX, 100BASE-FX

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{d(MRXD3–MRXD0)}$	Delay time, MRXD3–MRXD0 valid to MRCLK↑	10		20	ns
1	$t_{d(MRXDV)}$	Delay time, MRXDV valid to MRCLK↑	10		20	ns
1	$t_{d(MRXER)}$	Delay time, MRXER valid to MRCLK↑	10		20	ns
1	$t_{d(MCOL)}$	Delay time, MCOL valid to MRCLK↑	10		20	ns
2	$t_{c(MRCLK)}$	Cycle time, 10BASE-T		400		ns
2	$t_{c(MRCLK)}$	Cycle time, 100BASE-TX, 100BASE-FX		40		ns

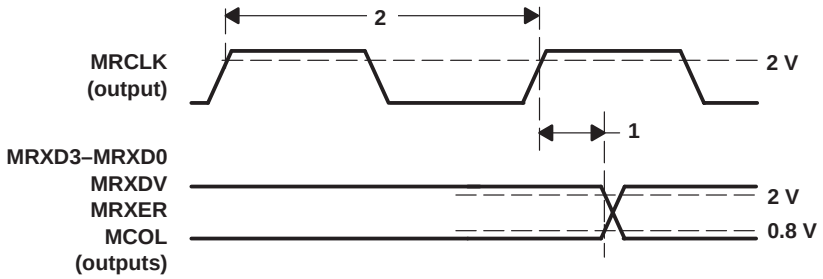


Figure 22. MII Receive

reset timing requirements (see Figure 23)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(XTALI)}$	Cycle time, XTAL1		50		ns
2	$t_{w(\overline{MRSTL})}$	Pulse duration	50			µs
3	$t_{su(\overline{MRSTL})}$	Setup time, MRST low before XTAL1↑	10			ns
4	$t_{h(\overline{MRSTL})}$	Hold time, MRST low after XTAL1↑	5			ns
5	$t_{d(XTALI)}$	Delay time, XTAL1 invalid to XTAL1 valid (stable)	25			ms

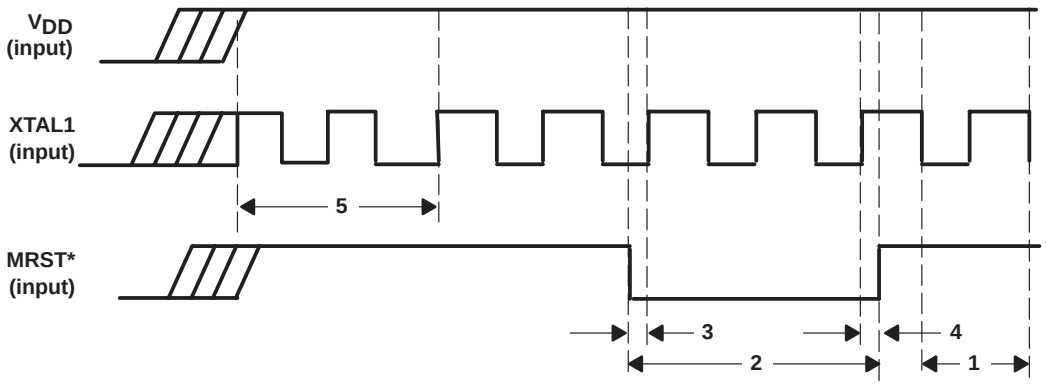


Figure 23. Reset

At initial power up, the TNETE2101 performs an internal reset. No external reset circuit is required, however, operation of the TNETE2101 is not specified for 50 ms after power up (V_{DD} is stable).

During operation, a full reset of the device can be performed by taking $\overline{MRST}$ terminal low for at least 50 µs. Correct operation of the devices is not assured for a duration of 50 ms after $\overline{MRST}$ terminal is deasserted high.

100BASE-TX parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{out+}	V_{out+} level on transmit waveform (see Figure 24)	0.95	1.05	V
$V_{out–}$	$V_{out–}$ level on transmit waveform (see Figure 24)	–1.05	–0.95	V
$V_{TX(sym)}$	$V_{out+}/V_{out–}$ symmetry (see Figure 24)	98	102	%
$V_{TX(os)}$	$V_{out+}/V_{out–}$ voltage overshoot (see Figure 24)	0	5	%
$t_{r1(TX)}$	Rise time, t_1 (0 –> V_{out+} transition) (see Figure 25)	3	5	ns
$t_{r2(TX)}$	Rise time, t_4 (0 –> $V_{out–}$ transition) (see Figure 25)	3	5	ns
$t_{f1(TX)}$	Fall time, t_2 (V_{out+} transition –> 0) (see Figure 25)	3	5	ns
$t_{f2(TX)}$	Fall time, t_3 ($V_{out–}$ transition –> 0) (see Figure 25)	3	5	ns
$t_{\Delta(TX)}$	Maximum $t_{r1(Tx)}$ – Minimum $t_{r1(Tx)}$, Maximum $t_{r2(Tx)}$ – Minimum $t_{r2(Tx)}$ (see Figure 25), Maximum $t_{f1(Tx)}$ – Minimum $t_{f1(Tx)}$, Maximum $t_{f2(Tx)}$ – Minimum $t_{f2(Tx)}$	0	0.5	ns
$t_{DCD(TX)}$	Duty-cycle distortion (see Figure 26)	0	0.5	ns

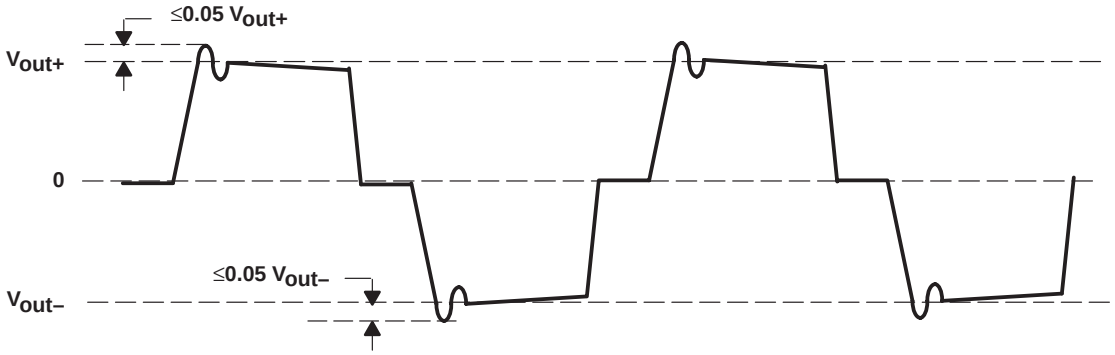
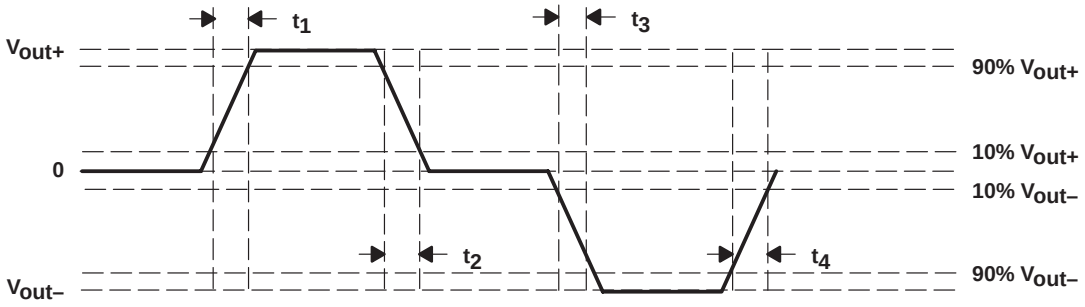


Figure 24. 100BASE-TX Transmit Amplitude



NOTES: A. t_1 occurs at 10% of V_{out+}.
B. t_2 occurs at 90% of V_{out+}.
C. t_3 occurs at 10% of $V_{out–}$.
D. t_4 occurs at 90% of $V_{out–}$.

Figure 25. 100BASE-TX Transmit Rise/Fall

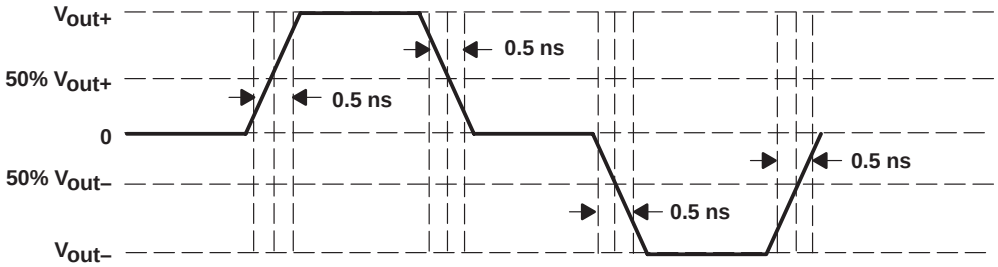


Figure 26. 100BASE-TX Transmit Duty-Cycle Distortion

receiver squelch parameters

10BASE-T

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{thp}	Positive-squelch receiver threshold voltage		250		mV
V_{thn}	Negative-squelch receiver threshold voltage		–250		mV
V_{thd}	Data receiver threshold voltage		75		mV

100BASE-TX

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{th}	Receiver differential voltage to maintain link		200		mV

PARAMETER MEASUREMENT INFORMATION

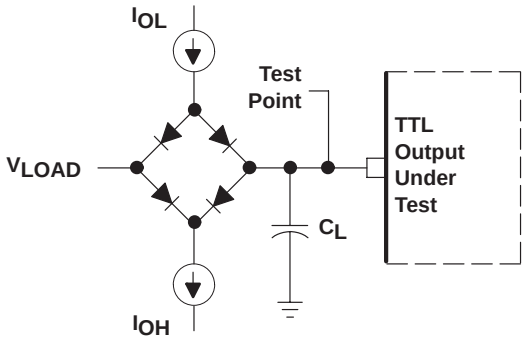
Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V.

Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is no longer said to be low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown in the following diagram.

The rise and fall times are not specified, but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

test measurement

The test and load circuit shown in Figure 27 represents the programmable load of the tester-terminal electronics used to verify timing parameters of the TNETE2101 output signals.



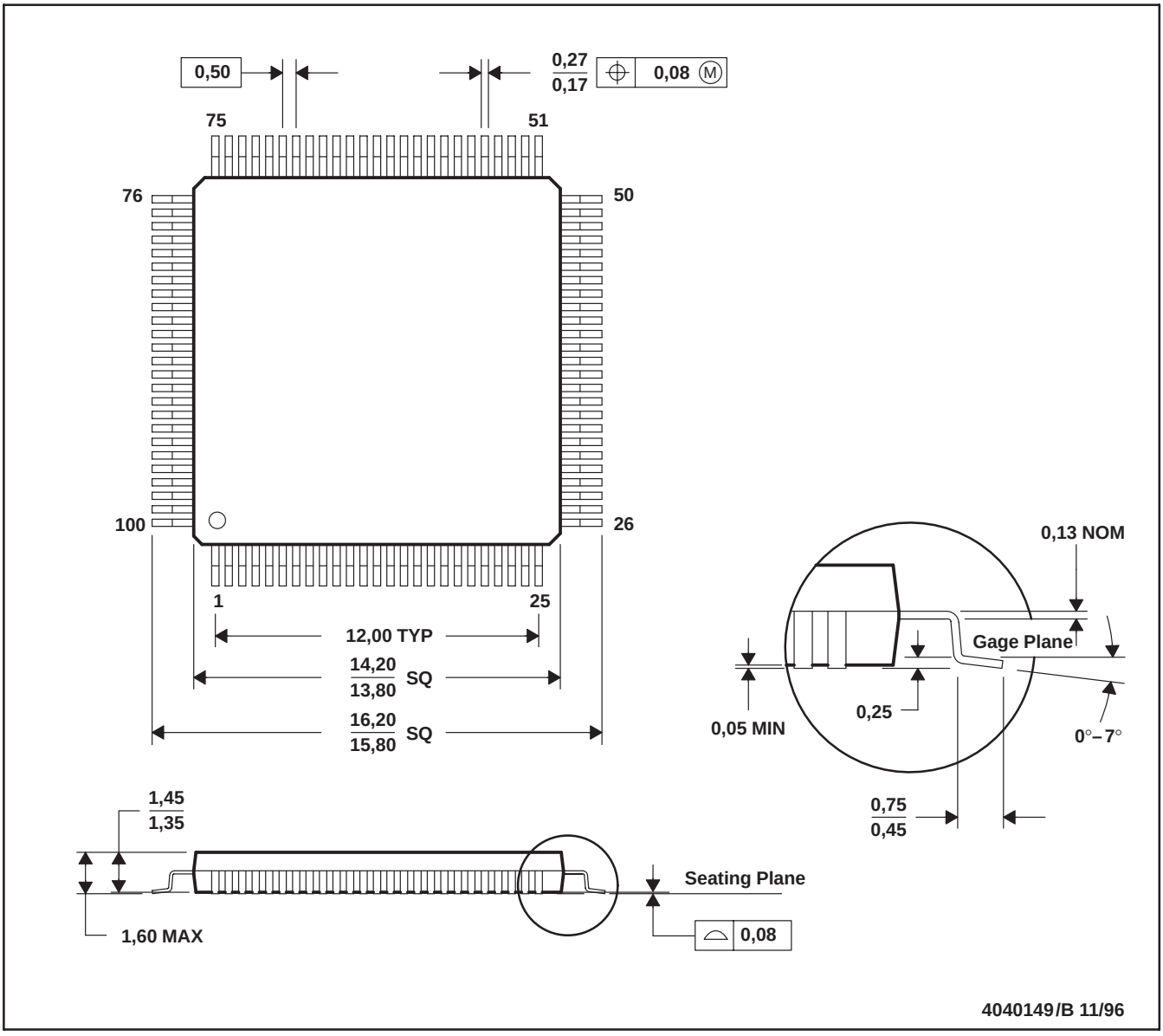
TTL OUTPUT TEST LOAD

Where: I_{OL} = Refer to I_{OL} in recommended operating conditions.
I_{OH} = Refer to I_{OH} in recommended operating conditions.
V_{LOAD} = 1.5 V, typical dc-level verification or 1.5 V, typical timing verification
C_L = 45 pF, typical load-circuit capacitance

Figure 27. Test and Load Circuit

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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